

Task 2: Memory Accesses

1. Venus setup for Scenario 1 showing Program parameters, Cache parameters etc

The program parameters and Cache parameters are shown below:

```
18 .data
19 array: .word 2048          # max array size specified in BYTES (DO NOT CHANGE)
20
21 .text
22 #####
23 # You MAY change the code below this section
24 main: li a0, 128          # array size in BYTES (power of 2 < array size)
25      li a1, 8             # step size (power of 2 > 0)
26      li a2, 4             # rep count (int > 0)
27      li a3, 0             # 0 - option 0, 1 - option 1
28 # You MAY change the code above this section
29 #####
30
```

Registers Memory Cache VDB	
Cache Levels	1
Block Size (Bytes)	8
Number of Blocks	4
Associativity	1
Cache Size (Bytes)	32
<input type="checkbox"/> Enable?	Enables current selected level of the cache.
Direct Mapped	
LRU	L1
Hit Count	0
Accesses	0
Hit Rate	???
0) EMPTY 1) EMPTY 2) EMPTY 3) EMPTY	
NOTE: This is a write through, write allocate cache.	
Seed	-8395975193662676403

Associativity: 1 (Venus won't let you change this with your placement policy, why?)

Since the cache is **Direct Mapped** the venus won't let us change the **associativity** it will remain 1 for the direct mapped cache, But if we change the placement policy to N-way set associativity then we can change the **associativity**.

Task

1. What combination of parameters is producing the hit rate you observe? Write your answer in the form “[parameter A], [parameter B]” where [parameter A] and [parameter B] complete the following response: "Because [parameter A] in bytes is exactly equal to [parameter B] in bytes." Note: Don't forget that 'cache size' is a valid parameter that you implicitly set by choosing the block size and the # of blocks.

[Parameter A] = Step Size

[Parameter B] = Cache Size

The hit rate is 0% because the **step size** is of **32B** which is equals to the **cache size** of **32B**. The number of access is 16 since the **rep count** was set to 4 and the array size was set to **128B (32 words)** in each rep count the number of access is **4** for **32 words** hence for 4 rep count the total number of access is **16**.

Hit Count	<input type="text" value="0"/>
Accesses	<input type="text" value="16"/>
Hit Rate	<input type="text" value="0"/>
0) MISS 1) EMPTY 2) EMPTY 3) EMPTY	
NOTE: This is a write through, write allocate cache.	
Seed	<input type="text" value="-8395975193662676403"/>

2. What is the hit rate if we increase Rep Count arbitrarily? Write your answer as a decimal (e.g. "1.0" if the HR is 100%).

The hit rate would not change if we increase the **rep count** arbitrarily the hit rate would remain **0**. Because the cache size and step size is same and on every **write** access it would be cache miss so it does not make sense to increase the rep count.

3. [PRACTICE] How could we modify one program parameter to get an increased hit rate? Write your answer in the form “[parameter], [value]” where [parameter] is the program parameter you want to change and [value] is the value you want to change it to. Note: We don't care if we access the same array of elements. Just give us a program parameter modification that would increase the hit rate. However, do make sure that your proposed value is valid.

[Parameter] = step size
[value] = 1

After changing the value of step size of 1 the hit rate obtained was **0.5 (50%)**. Because there are 4 blocks in the cache and each block is of 8B (2 words) when first time the write access occur the value is not present in the cache it would be a **cache miss** and due to spatial and temporal locality of cache the the next word in the array is also stored in the cache (Block 1) and next time when the write access occur the value is already present in the cache and it would be a **cache hit**, this would repeat for 32 times when the rep count is 1 out of which there would be 16 cache hits and 16 cache misses, since I have set the rep count to be 4 so there would be of total **128** access out of which there would be 64 cache hits and 64 cache misses and hence the hit rate obtained is 50%, as shown in the figure below

Registers Memory **Cache** VDB

Cache
Levels

1



Block Size
(Bytes)

8



Number of
Blocks

4



Associativity

1



Cache Size
(Bytes)

32

Enable?

Enables current selected level of the cache.

Direct Mapped



LRU



L1



Hit Count

64

Accesses

128

Hit Rate

0.5

0) HIT

1) HIT

2) HIT

3) HIT

NOTE: This is a write through, write allocate cache.

Seed

-8395975193662676403