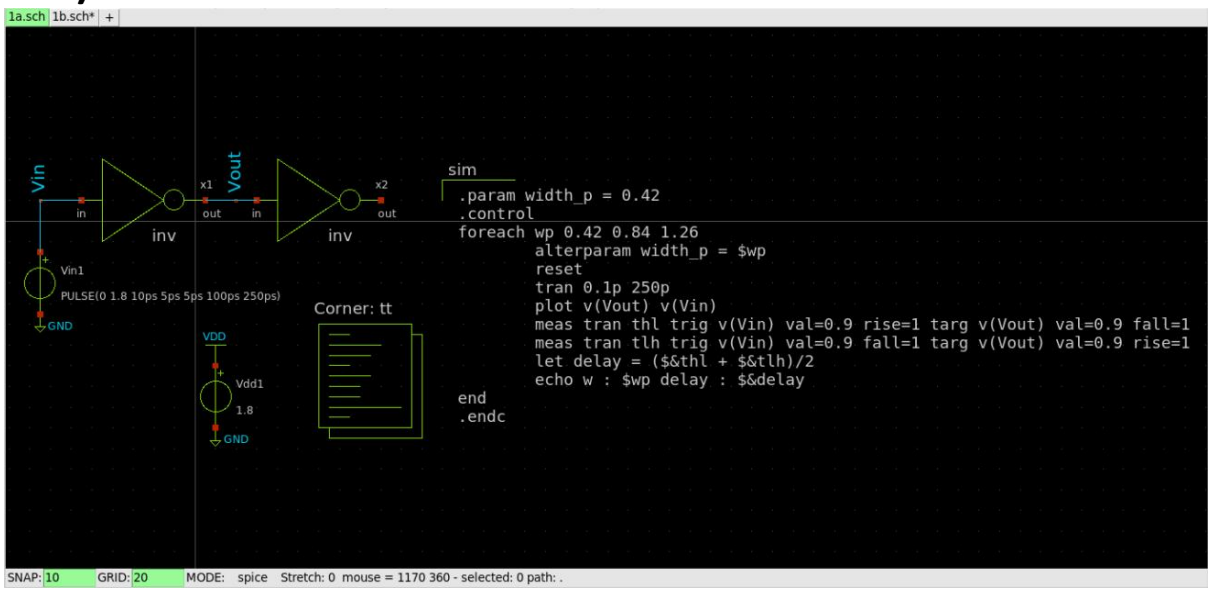
Tutorial 4 report
EE5311 (Digital IC design)

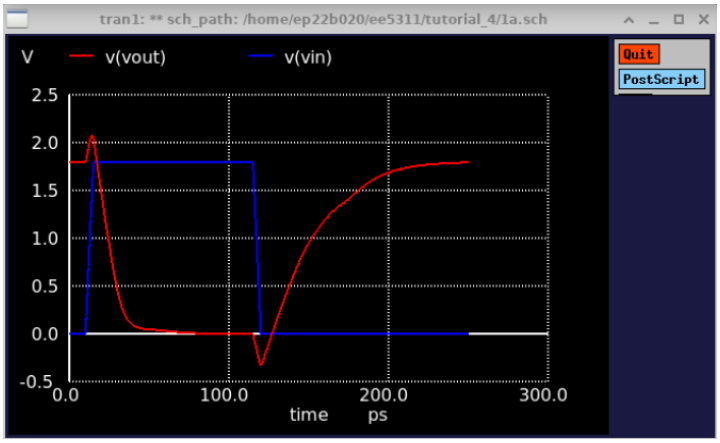
- Amogh G. Okade (EP22B020)

Question 1

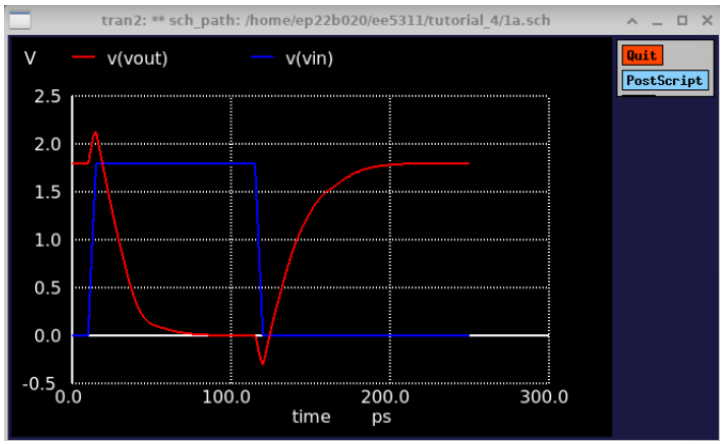
Part a)



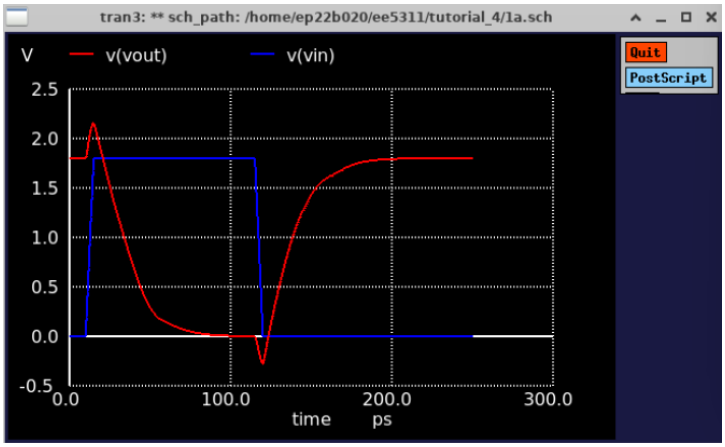
- Plot of the transient of the output voltage for an input pulse for –
  - W_p = 0.42µm



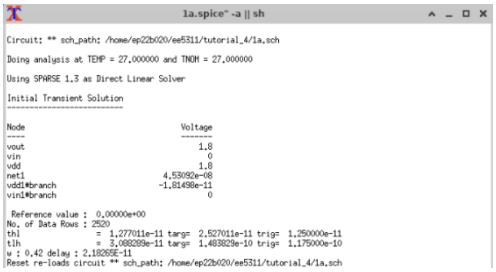
  - W_p = 0.84µm



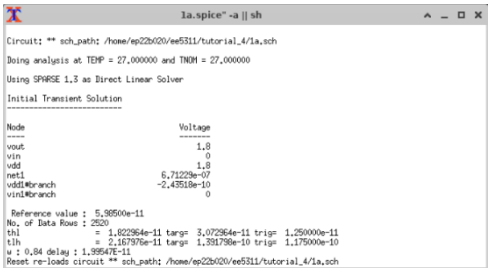
- W_p = 1.26µm



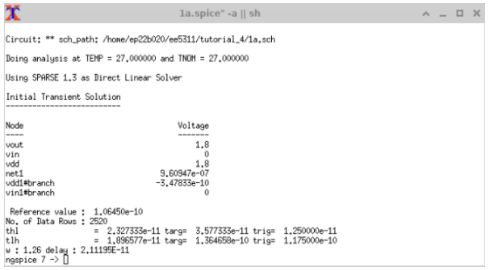
- The delay for –
  - W_p = 0.42µm is equal to 21.826ps. (thl = 12.77ps, tlh = 30.88ps)



  - W_p = 0.84µm is equal to 19.954ps. (thl = 18.23ps, tlh = 21.68ps)



  - W_p = 1.26µm is equal to 21.11 9ps. (thl = 23.27ps, tlh = 18.96ps)



Part b)

We know that

$$\text{Req, n } \alpha \frac{1}{\mu n \text{ Wn}},$$

$$\text{Req, p } \alpha \frac{1}{\mu p \text{ Wp}} \quad \text{and}$$

$$\text{Cint } \alpha \text{ (Wn + Wp)}$$

We know that the delay (which can be written as R C ln2),

$$\text{tp, inv } \alpha \text{ Req x Cint} = \left(\frac{\text{Req, n} + \text{Req, p}}{2}\right) \text{Cint}$$

$$\text{tp, inv } \alpha \left(\frac{1}{\mu n\, Wn} + \frac{1}{\mu p\, Wp}\right)(\text{Wn} + \text{Wp})$$

For the minimum delay,

$$\frac{\text{dtp, inv}}{\text{dWp}} = 0$$

$$-\frac{(\text{Wn} + \text{Wp})}{\mu p\, Wp^2} + \left(\frac{1}{\mu n\, Wn} + \frac{1}{\mu p\, Wp}\right) = 0$$

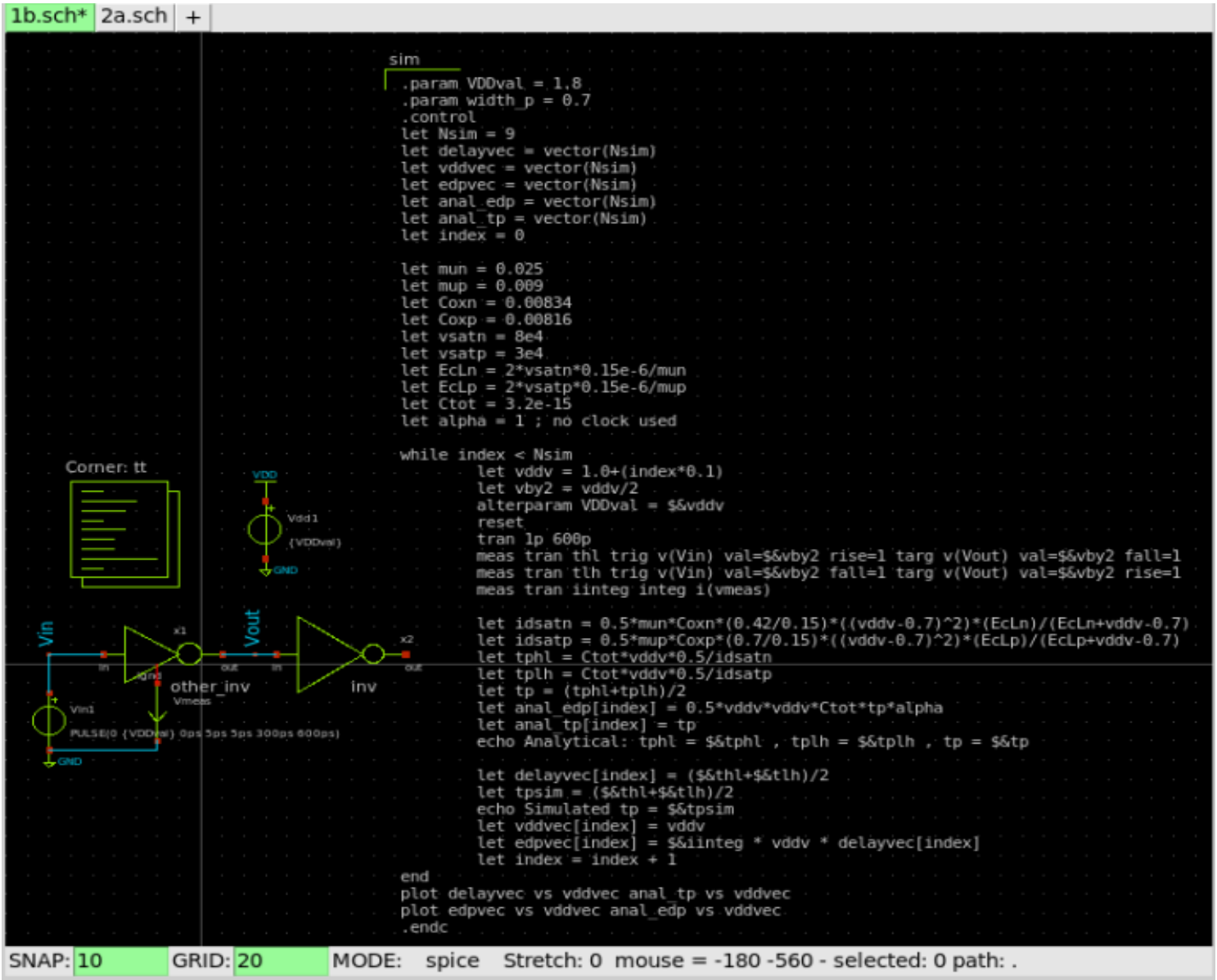
$$-\frac{\text{Wn}}{\mu p\, Wp^2} + \frac{1}{\mu n\, Wn} = 0$$

Or

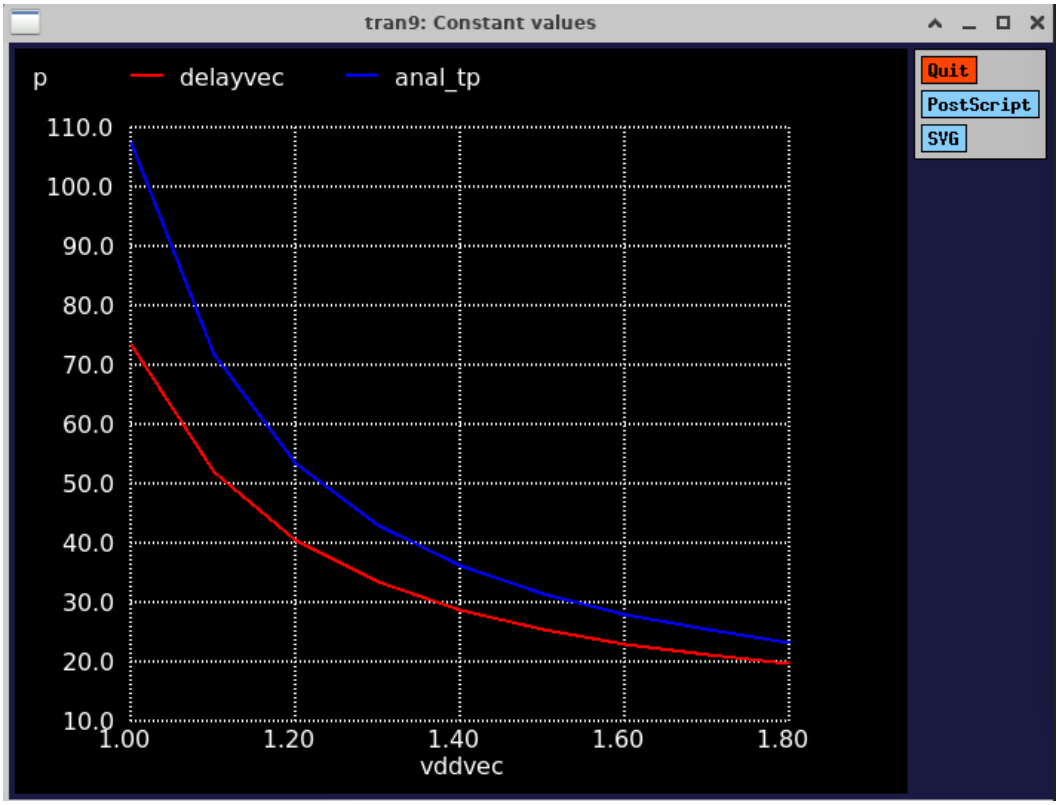
$$\text{Wp} = \sqrt{\frac{\mu n}{\mu p}}\ \text{x Wn}$$

Substituting (µn/µp) = (25/9) and Wn = 0.42µm, we get

Wp = 0.7µm for minimum delay



- Plot of the measured and analytical delay as a function of V_{DD} for V_{DD} = 1V to 1.8V –



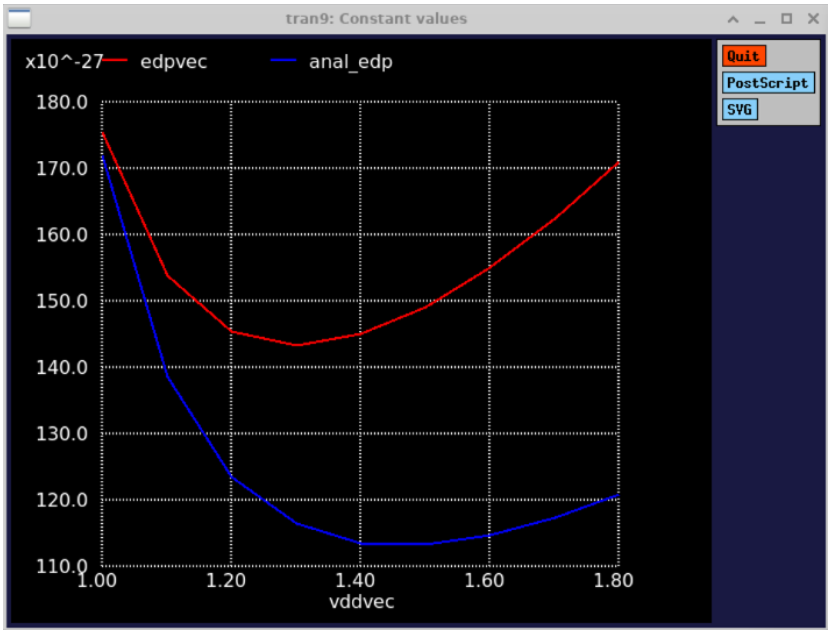
  - ➢ We note that the delay decreases as V_{DD} increases.
  - ➢ Although intuition dictates that the delay should be higher for a larger V_{DD}, (since the curve would take longer to come down from a larger V_{DD}), it is actually the increased current that is responsible for pulling the voltage down faster, at a higher V_{DD}.

- Comparison between measured and analytical values –

	Simulation			**Estimated**		
V_{DD} (volts)	**thl (ps)**	**tlh (ps)**	**tp (ps)**	**thl (ps)**	**tlh (ps)**	**tp (ps)**
1	53.53	93.67	73.60	79.94	134.87	107.40
1.1	37.69	66.32	52.00	53.38	89.87	71.63
1.2	29.80	51.10	40.45	40.14	67.23	53.62
1.3	25.20	41.65	33.42	32.16	53.95	43.05
1.4	22.20	35.32	28.76	27.08	45.35	36.21
1.5	21.10	30.86	25.48	23.55	39.39	31.47
1.6	18.57	27.60	23.08	20.98	35.04	28.01
1.7	17.38	25.14	21.26	19.02	31.75	25.38
1.8	16.44	23.26	19.85	17.50	29.17	23.33

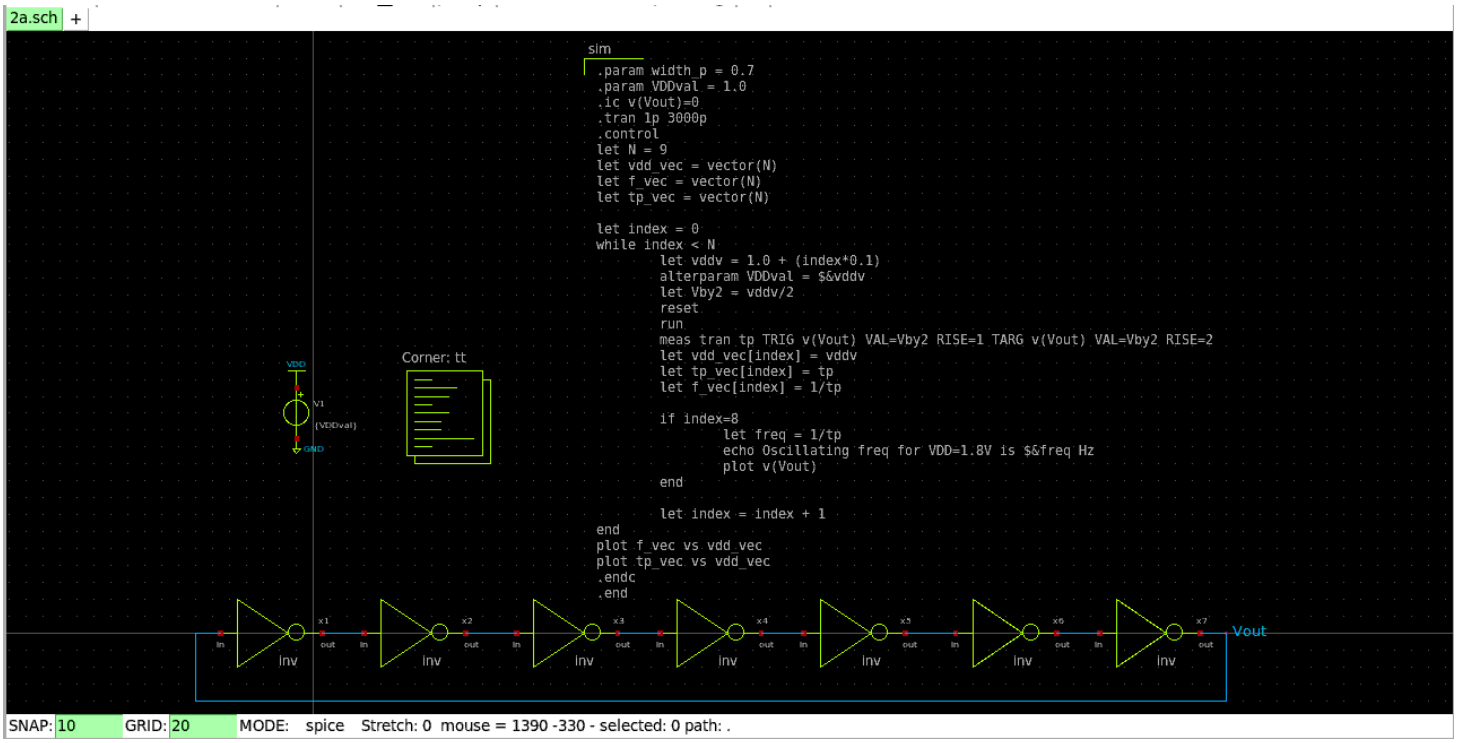
Part c)

- Plot of the measured and analytical energy-delay product as a function of V_{DD} for V_{DD} = 1V to 1.8V –



- The optimum VDD is observed to be 1.3V from the simulation, and 1.4V from the analytical estimate.

Question 2



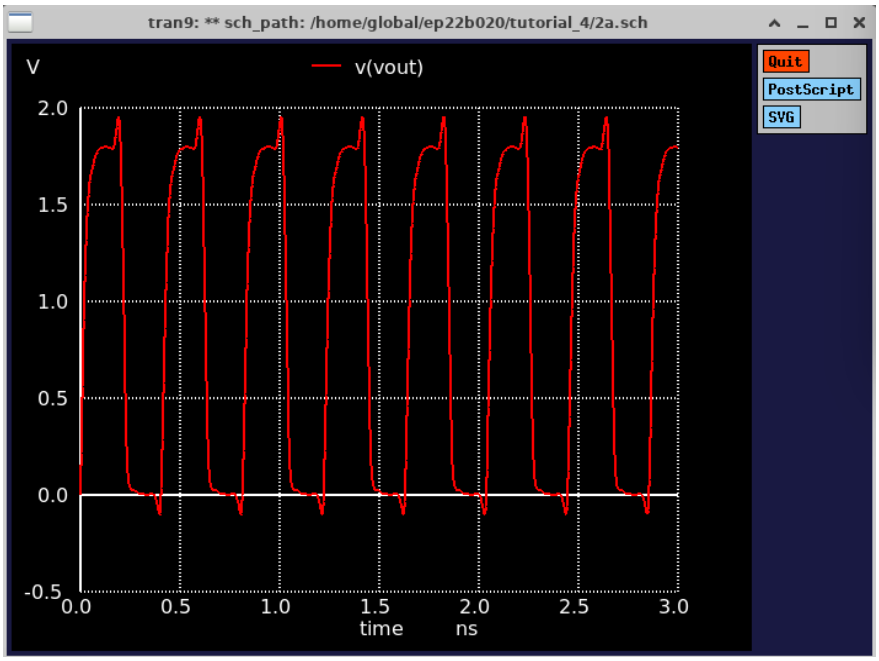
Part a)

For VDD=1.8V, the oscillating frequency is 2.45 GHz.

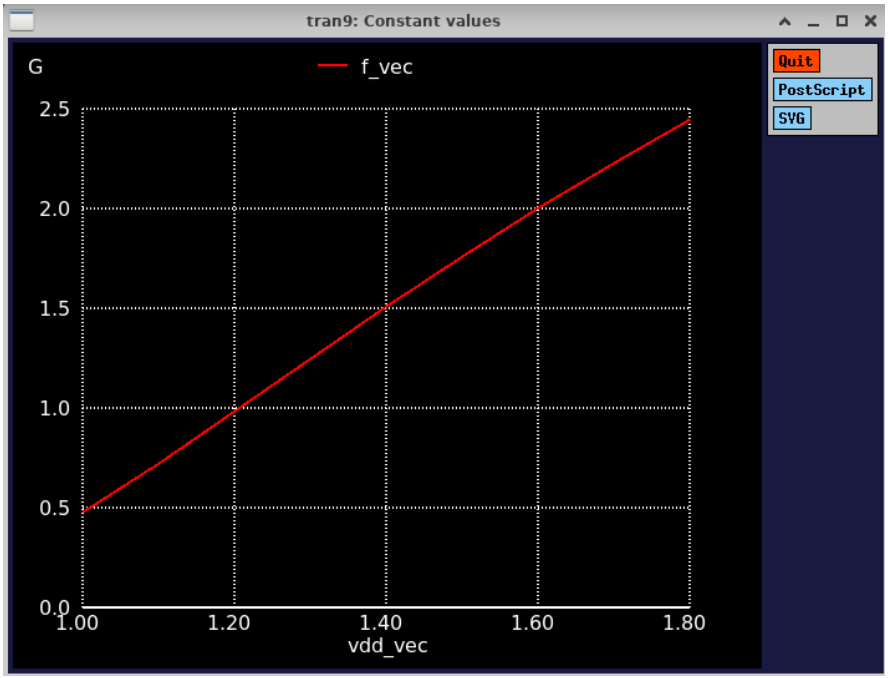
```
 Reference value :  2.49528e-09
No. of Data Rows : 3008
tp                 =  4.080253e-10 targ=  4.241690e-10 trig=  1.614375e-11
Oscillating freq for VDD=1.8V is 2.45083E+09 Hz
ngspice 8 ->
```

Part b)

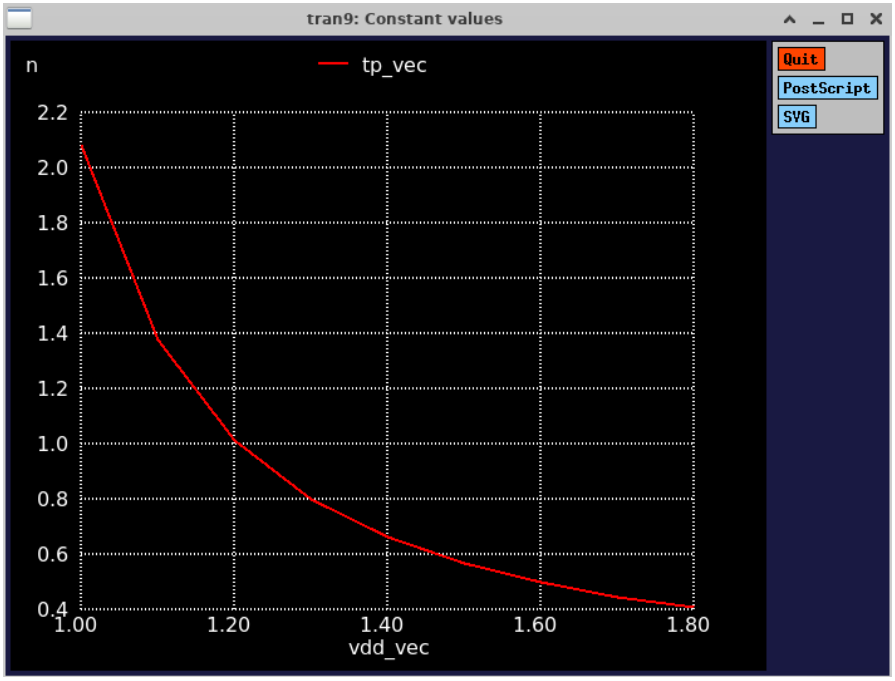
- Plot of the output voltage for V_{DD} = 1.8V –



- Plot of the oscillating frequency as a function of V_{DD} for V_{DD} = 1V to 1.8V –



- Plot of the time period as a function of V_{DD} for V_{DD} = 1V to 1.8V –

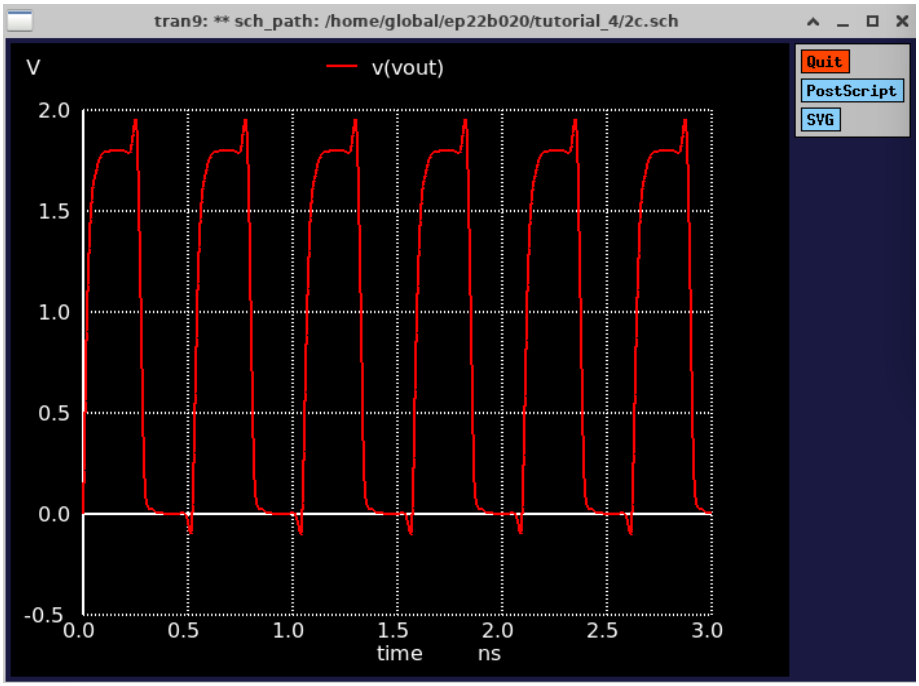


Part c)

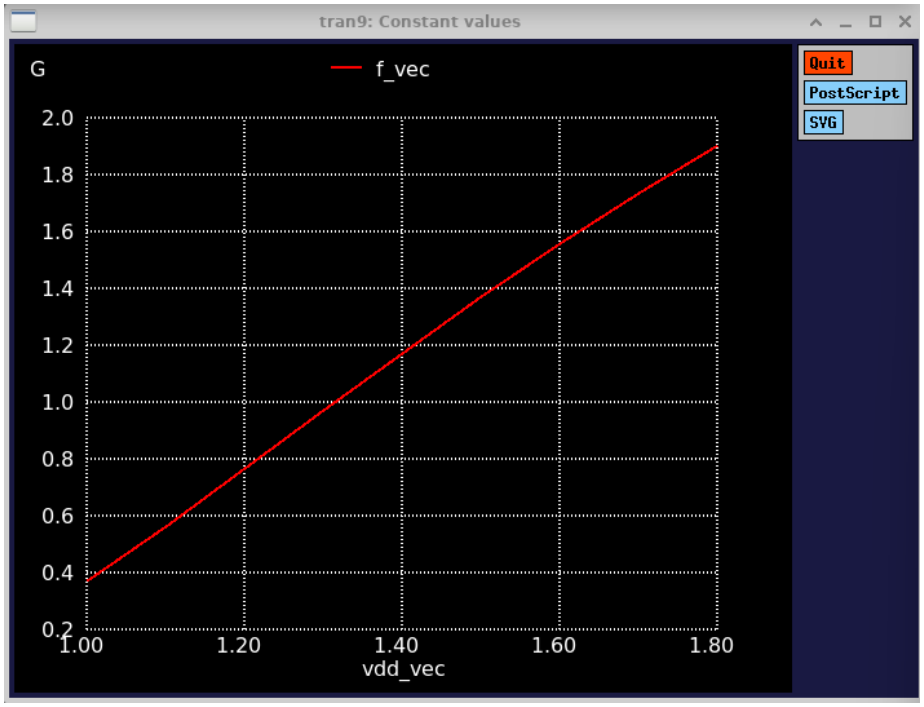
For VDD=1.8V, the oscillating frequency is 1.91 GHz.

```
 Reference value :  1.63128e-09
No. of Data Rows : 3008
tp                 =  5.246637e-10 targ=  5.408074e-10 trig=  1.614374e-11
Oscillating freq for VDD=1.8V is 1.90598E+09 Hz
ngspice 8 -> 
```

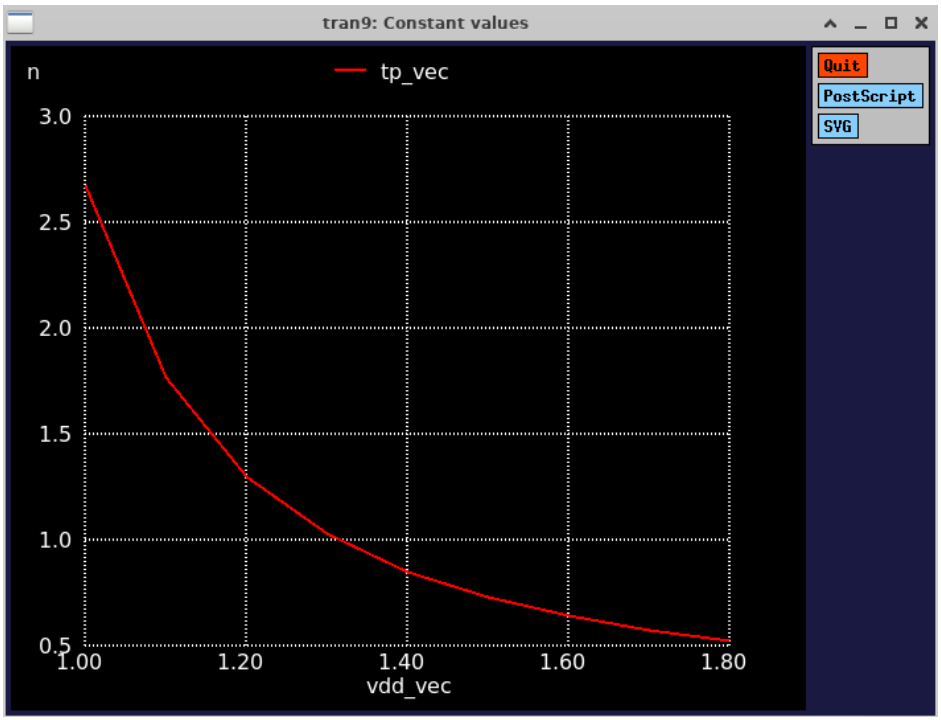
- Plot of the output voltage for V_{DD} = 1.8V –



- Plot of the oscillating frequency as a function of V_{DD} for V_{DD} = 1V to 1.8V –



- Plot of the time period as a function of V_{DD} for V_{DD} = 1V to 1.8V –



- We notice that the frequency of the oscillator with 7 inverters is higher, since there is lesser delay due to the reduced number of inveters.