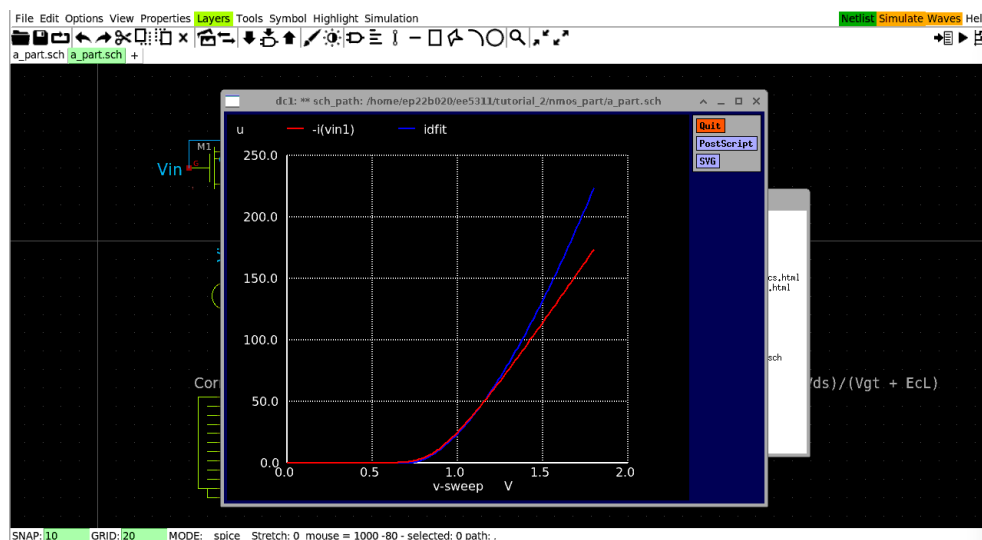# Tutorial 2 report
EE 5311 (Digital IC design)

- Amogh G. Okade (EP22B020)

Link to all the mean percentage error calculations using google sheets
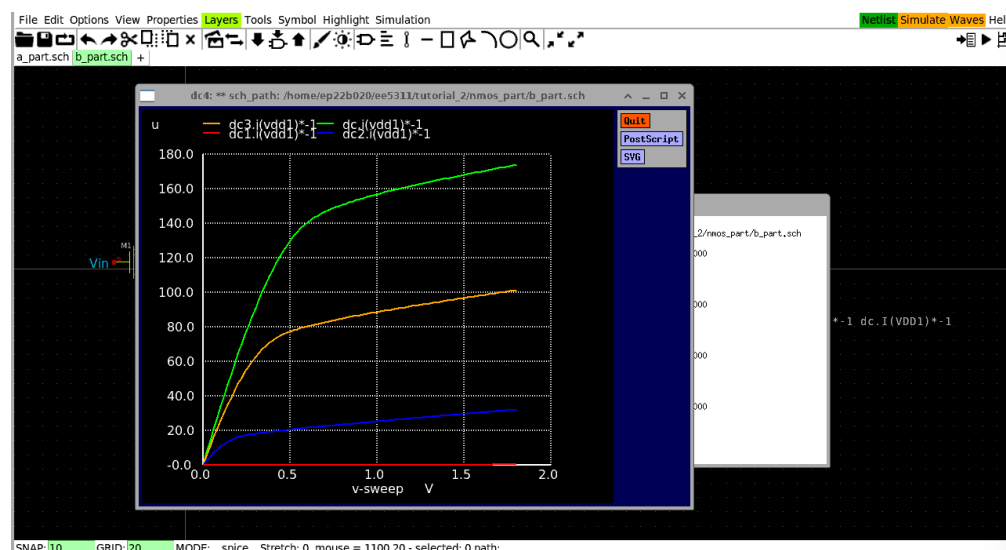
Question 1

Part a)

- The nMOS is in saturation.
  Since $V_G = V_D$ and $V_{Tn} > 0$, $V_{DS} > V_{GS} - V_{Tn}$
  Therefore, the nMOS is in saturation.
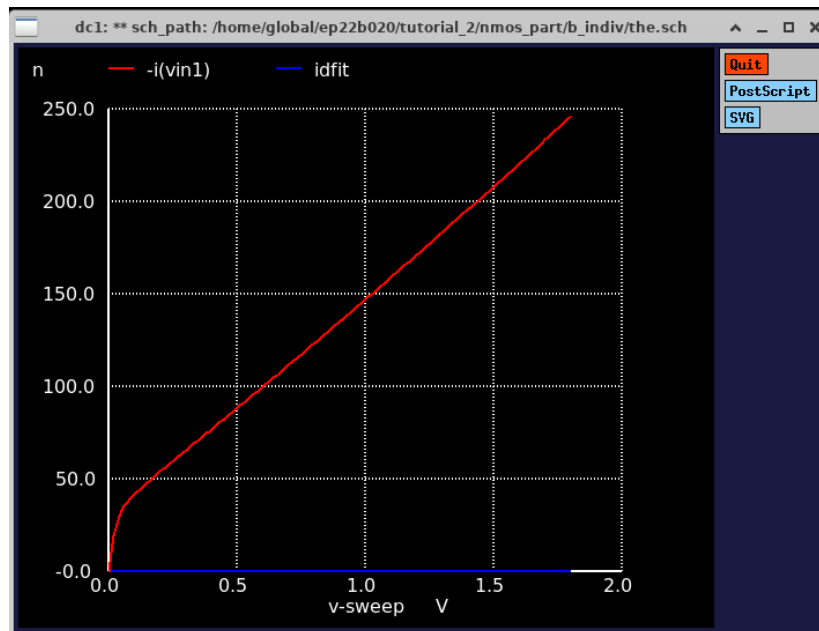- Plot of I_{DS} vs V_{GS} for L = 0.15μm and W = 0.42μm:-
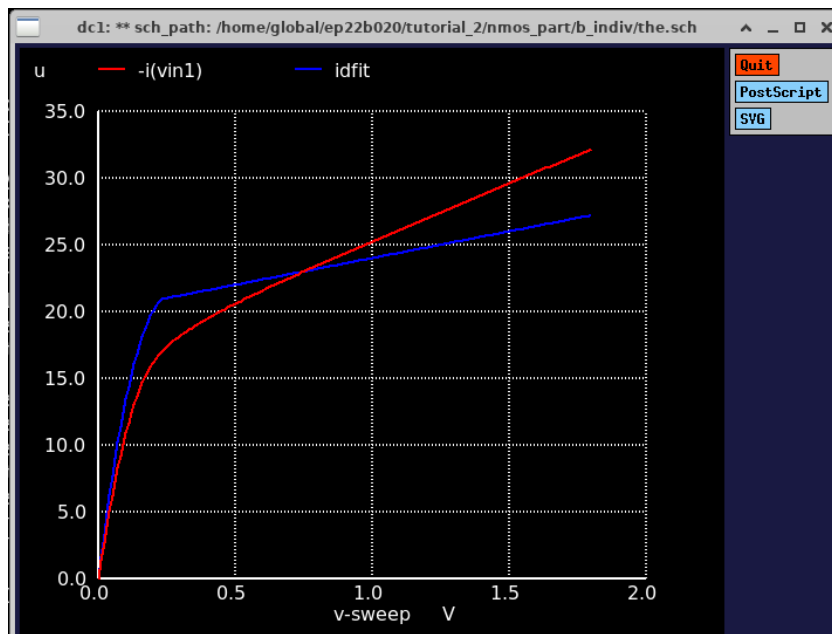

- Mean percentage error = 49.19%

Part b)

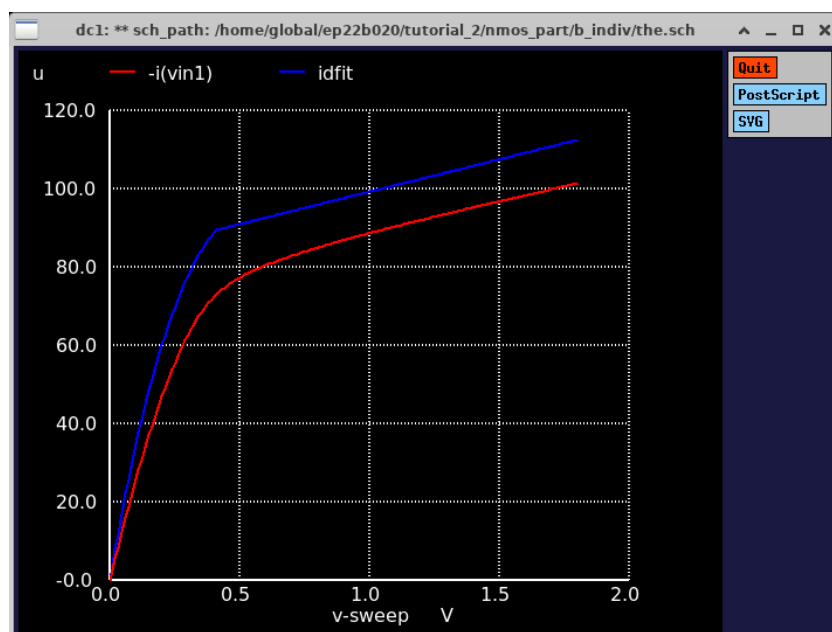- Plot of the output characteristics (I_{DS} vs V_{DS}) for different gate-source voltages (V_{GS} = 0.6V, 1V, 1.4V, 1.8V):-

- For Vgs = 0.6V, mean percentage error = 100%

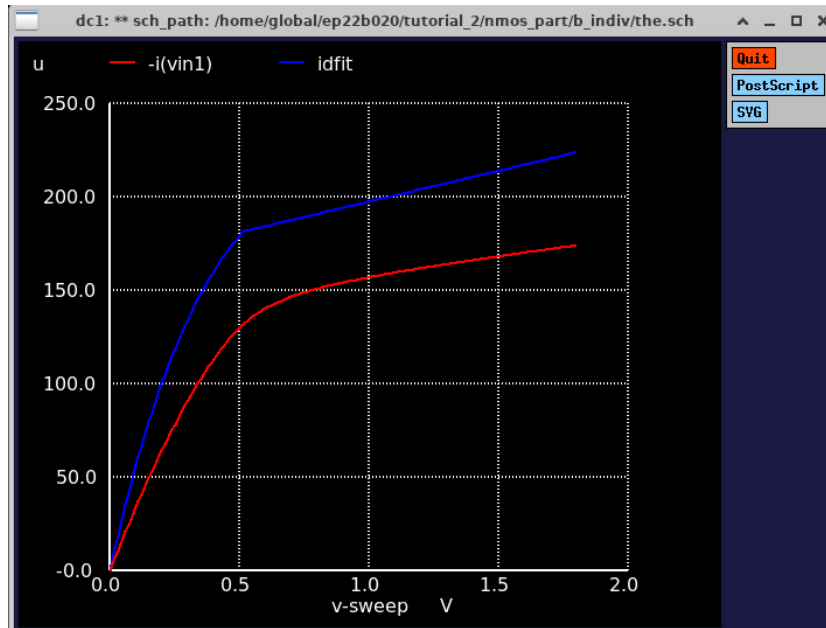- For Vgs = 1V, mean percentage error = 10.54%

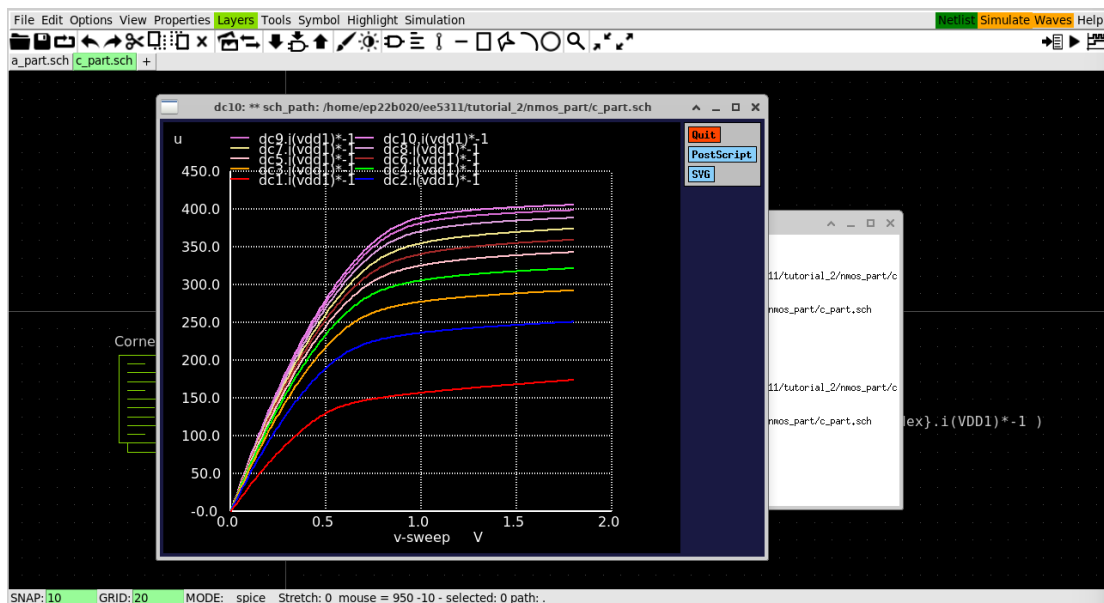- For Vgs = 1.4V, mean percentage error = 16.41%

- For Vgs = 1.8V, mean percentage error = 34.66%

Part c)

- Plot of I_{DS} vs V_{DS} for nMOSs of different sizes, keeping the W/L ratio constant (W/L = 0.42/0.15):-
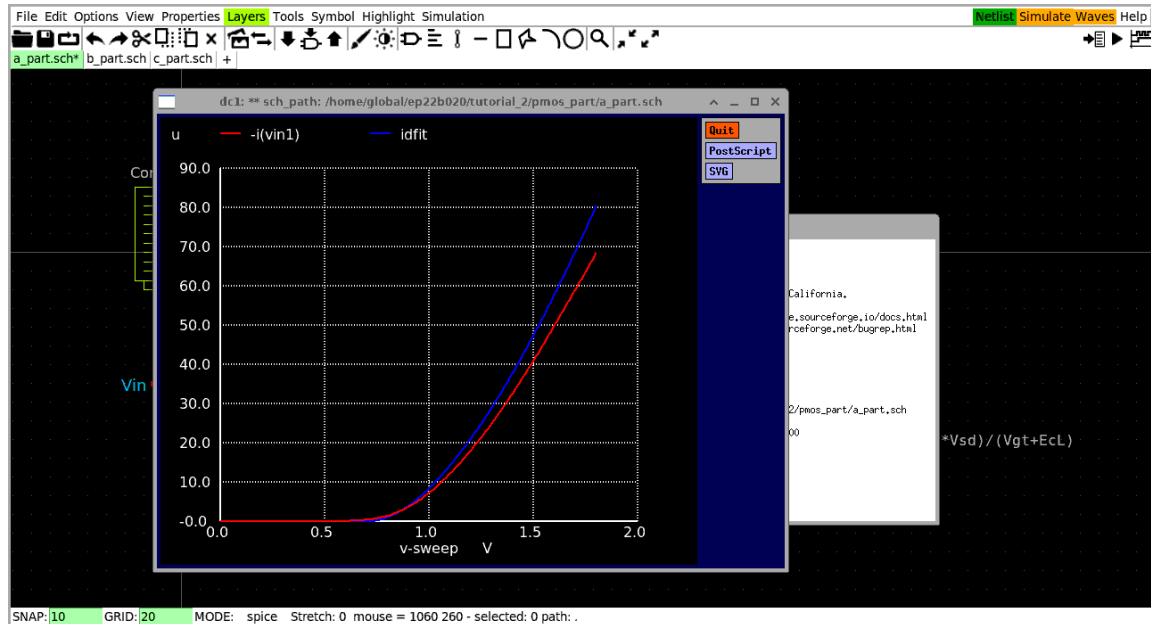

- We can clearly notice the velocity saturation effect decreasing, as the overall length increases.

Question 2

Part a)

- The pMOS is in saturation.
  Since $V_G = V_D$ and $|V_{Tp}| > 0$, $V_{SD} > V_{SG} - |V_{Tp}|$
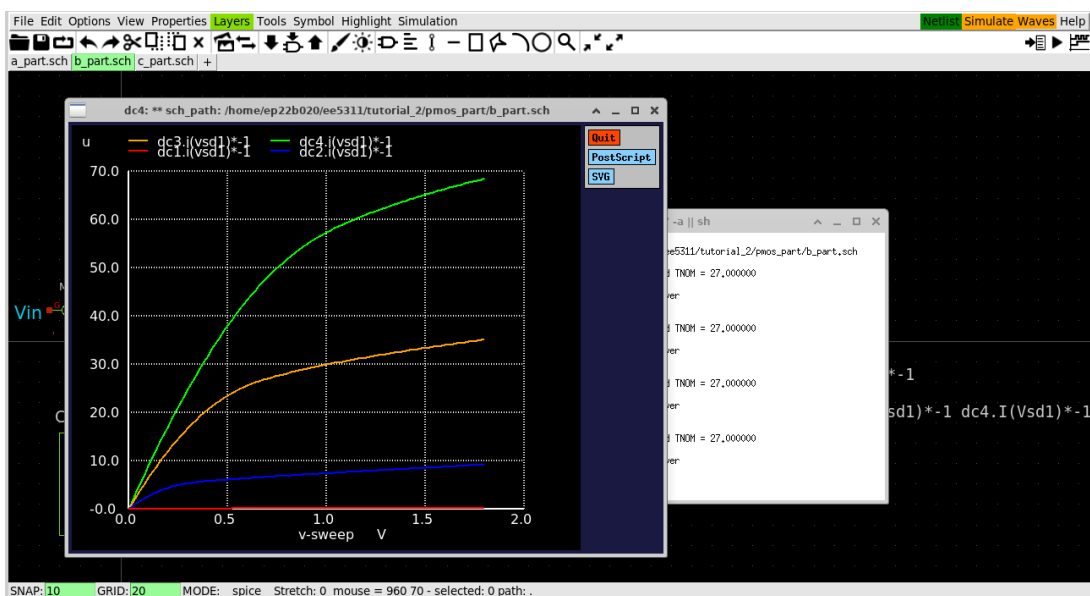 Therefore, the pMOS is in saturation.

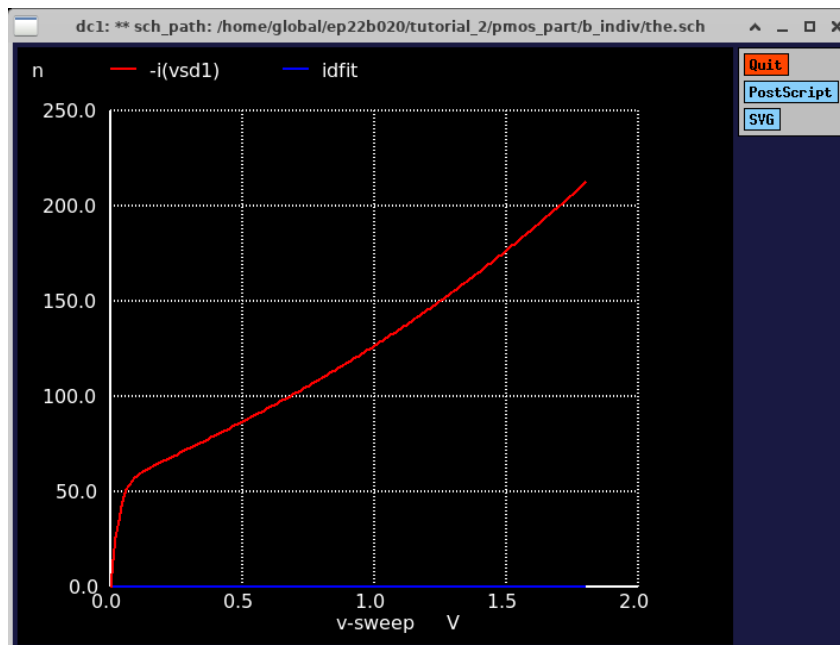- Plot of I_{SD} vs V_{SG} for L = 0.15µm and W = 0.42µm:-

- Mean percentage error = 50.71%

Part b)
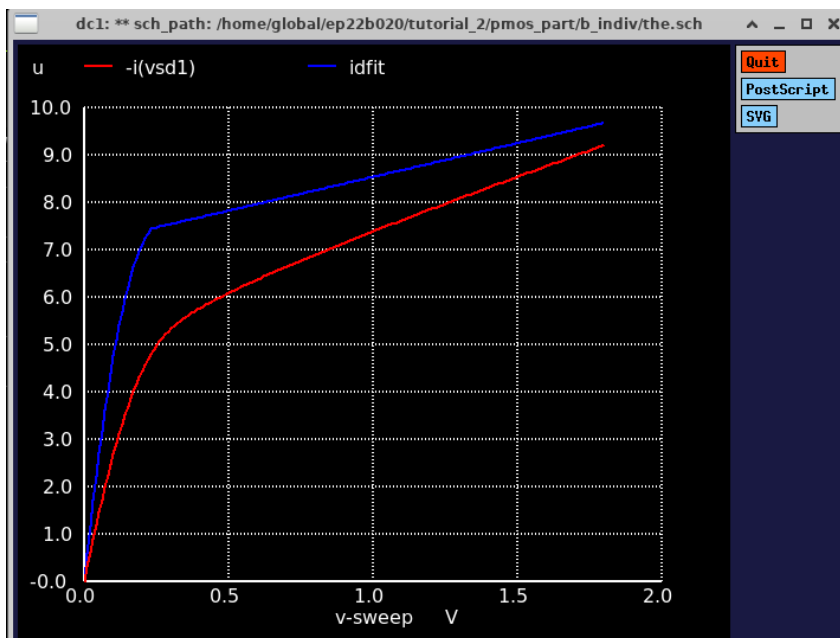
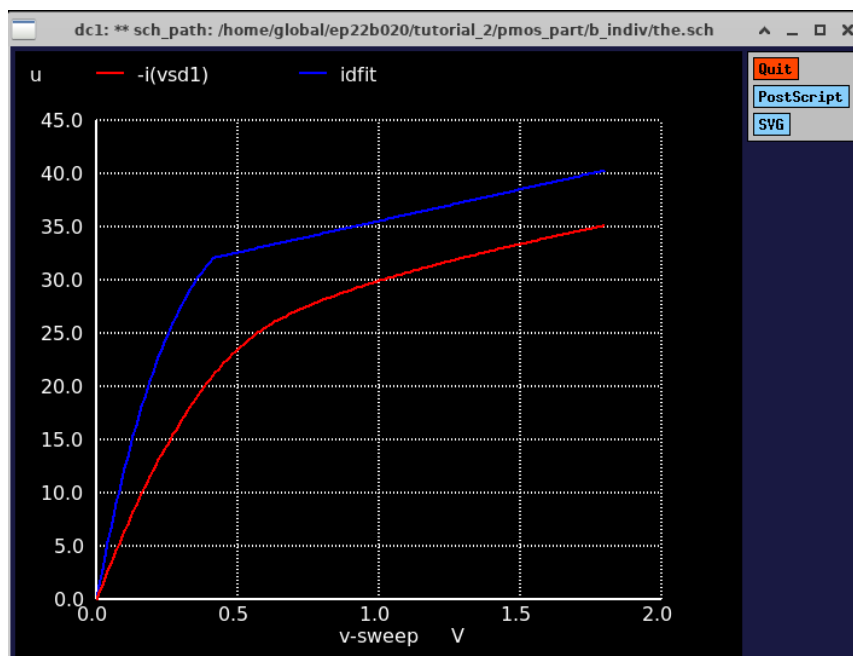- Plot of the output characteristics (I_{SD} vs V_{SD}) for different gate-source voltages (V_{SG} = 0.6V, 1V, 1.4V, 1.8V):-
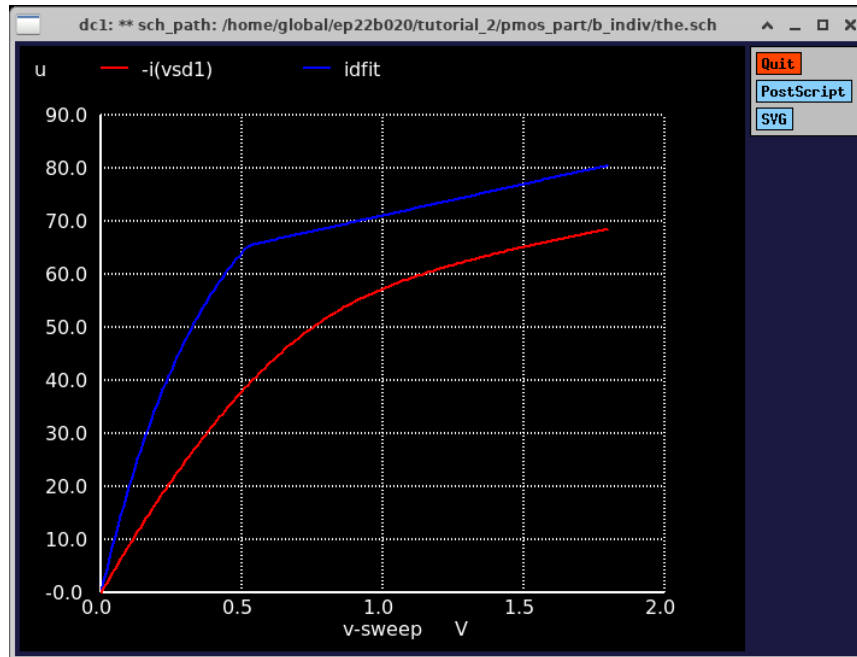

- For Vsg = 0.6V, mean percentage error = 100%

- For Vsg = 1V, mean percentage error = 25%
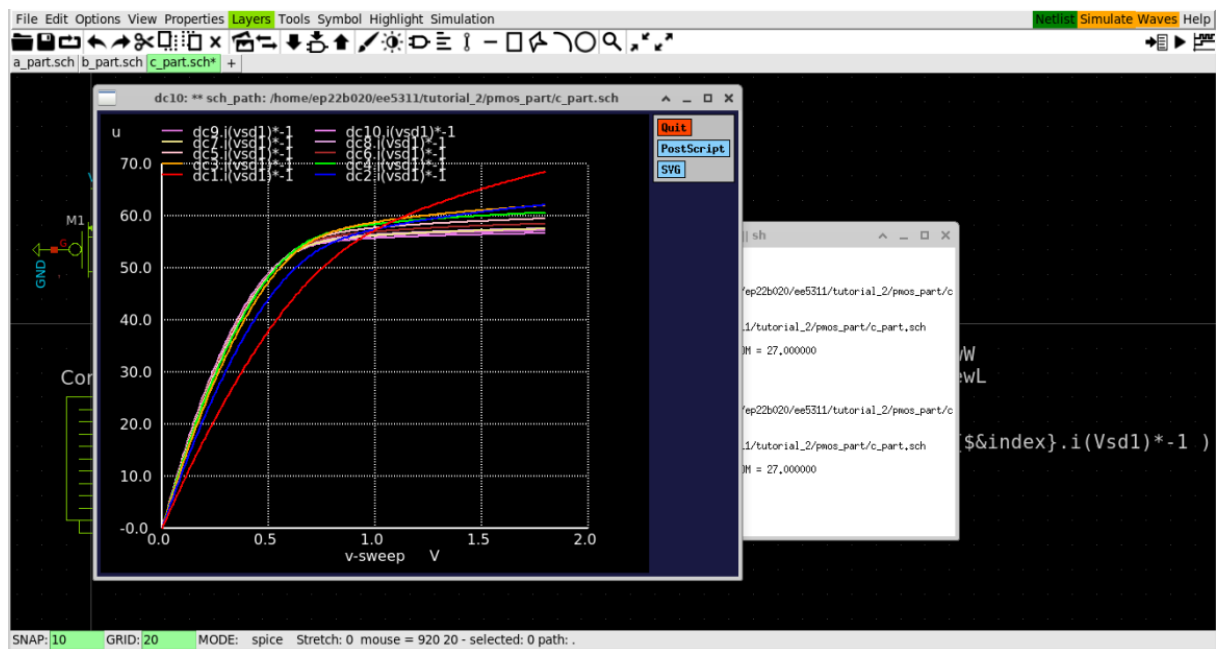

- For Vsg = 1.4V, mean percentage error = 33.68%

- For Vsg = 1.8V, mean percentage error = 47.43%

Part c)

- Plot of I_{DS} vs V_{DS} for nMOSs of different sizes, keeping the W/L ratio constant (W/L = 0.42/0.15):-

- We can clearly notice the velocity saturation effect decreasing, as the overall length increases.