Tutorial 5 report
EE5311 (Digital IC design)

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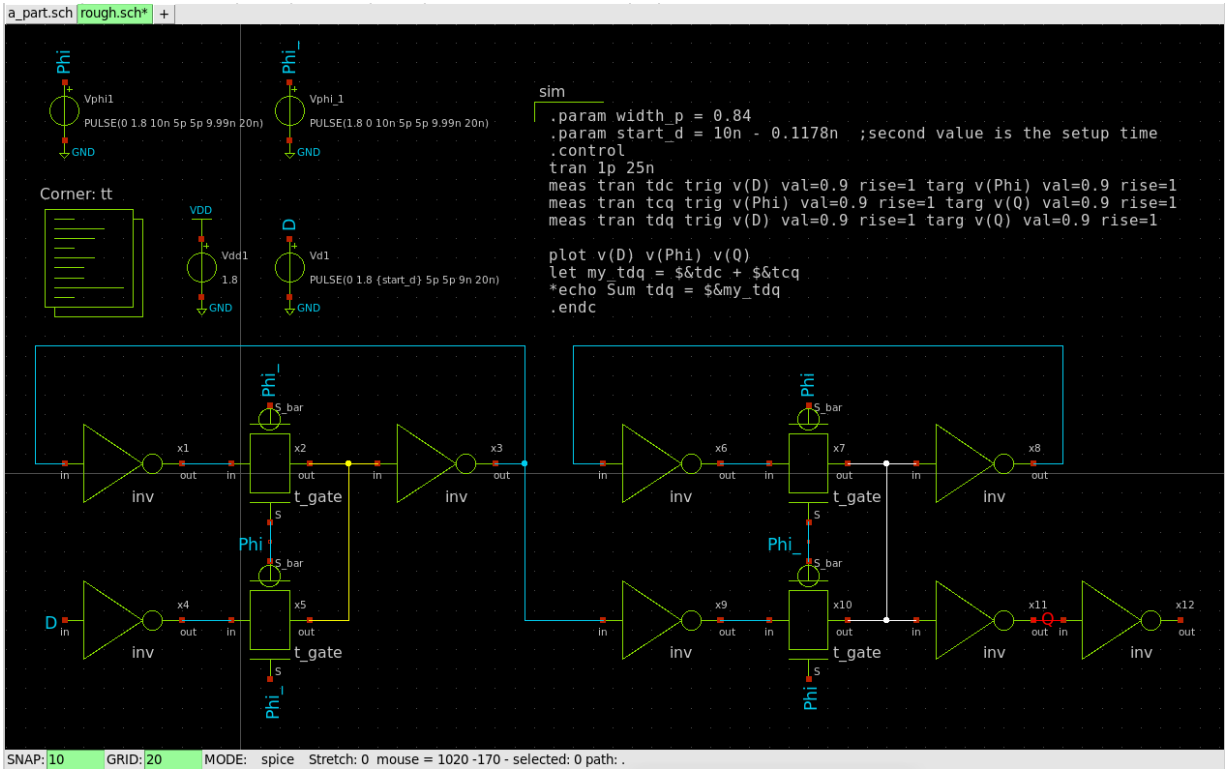
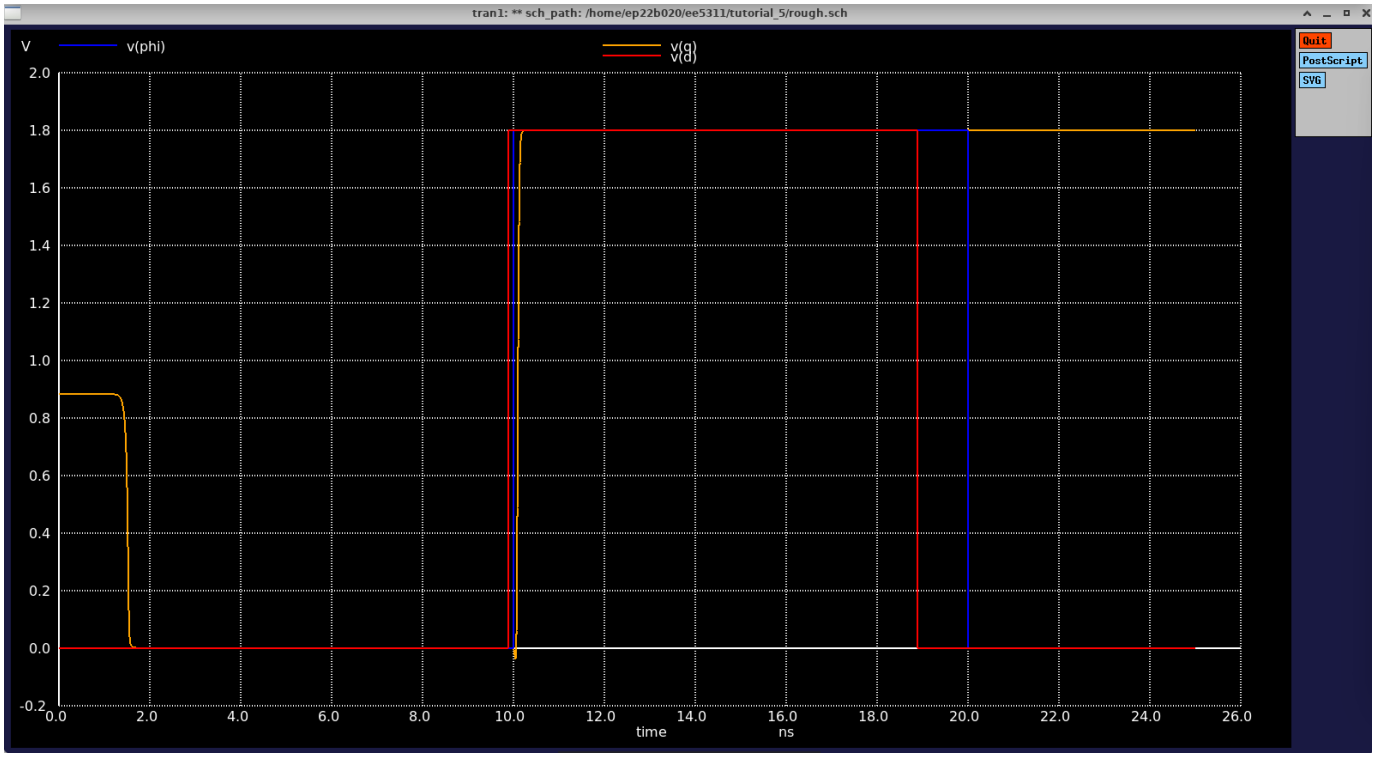
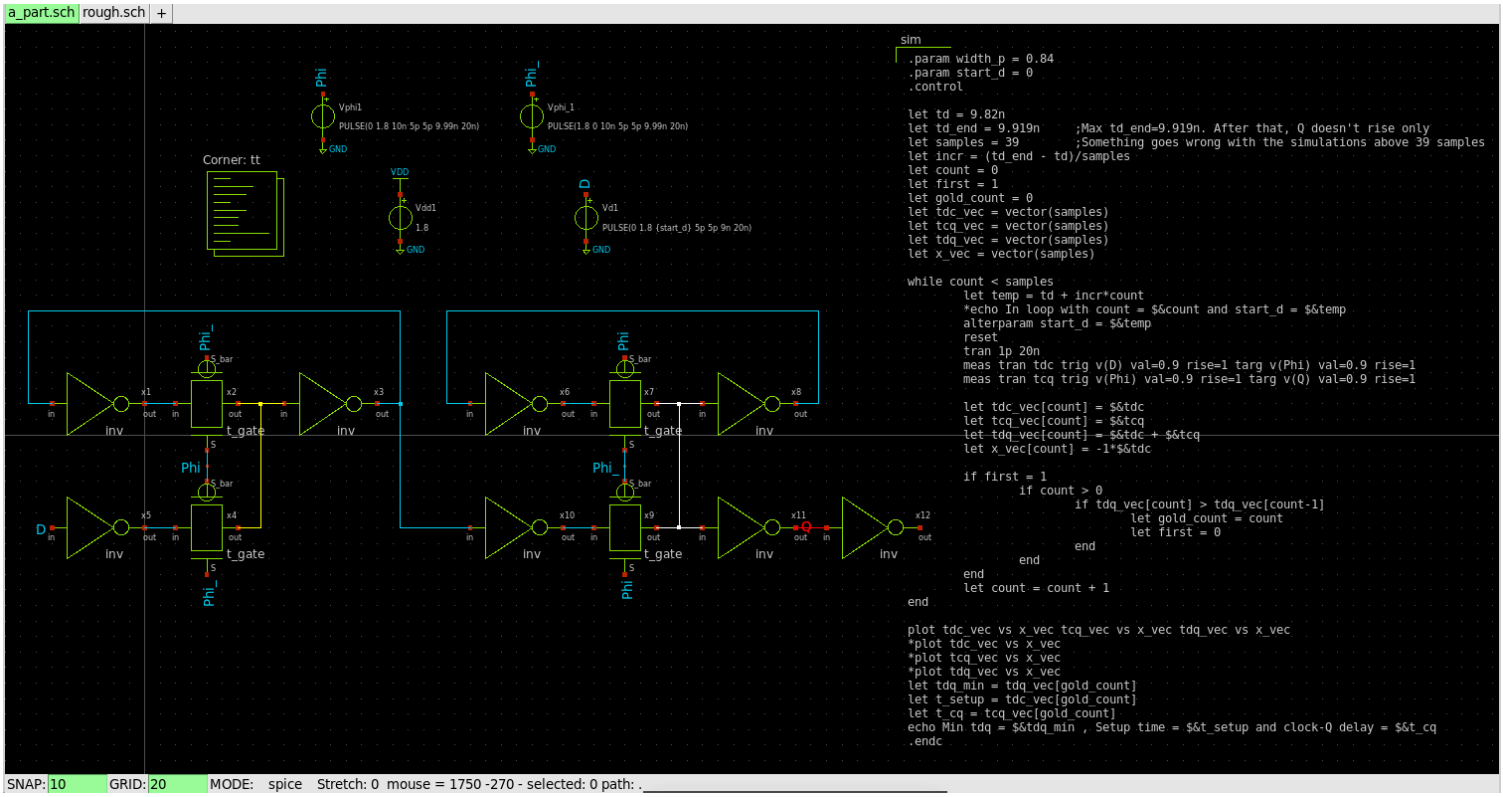
Question 1

Part a – Rising transition at D (and Q)

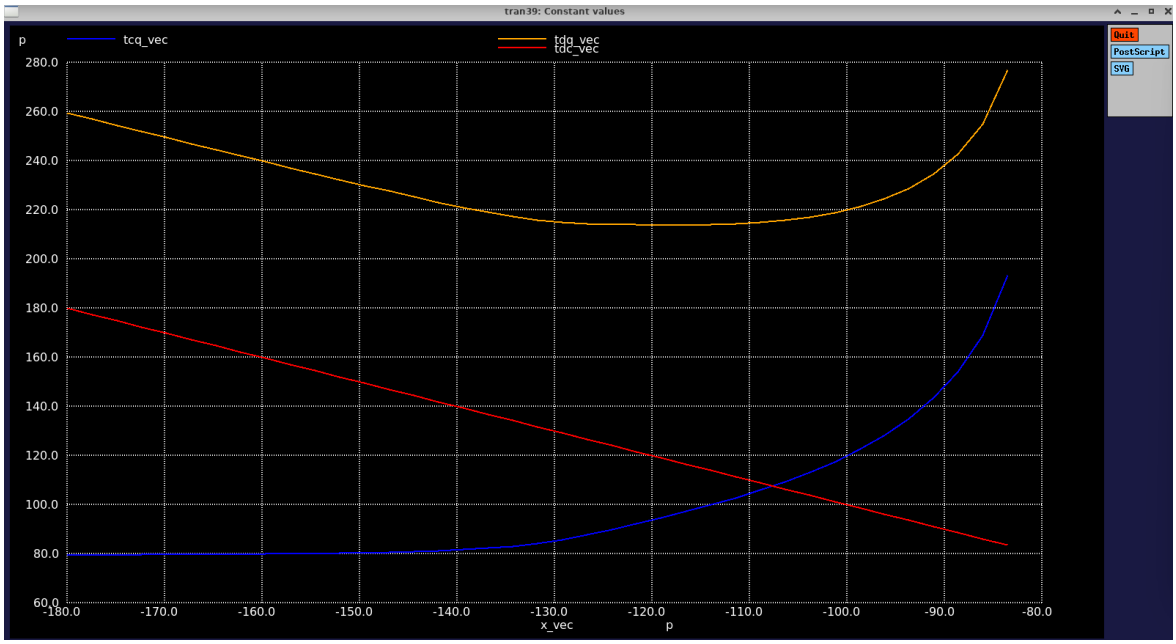


- Plot of the input (D) vs output (Q) when t_{DC} is the setup time –





- Plot showing the variation of t_{DC}, t_{CQ} and t_{DQ} for different values of t_{DC} –



- Values (from simulation)

```
Min tdq = 2.13836E-10 , Setup time = 1.1654E-10 and clock-Q delay = 9.72958E-11
ngspice 9 ->
```

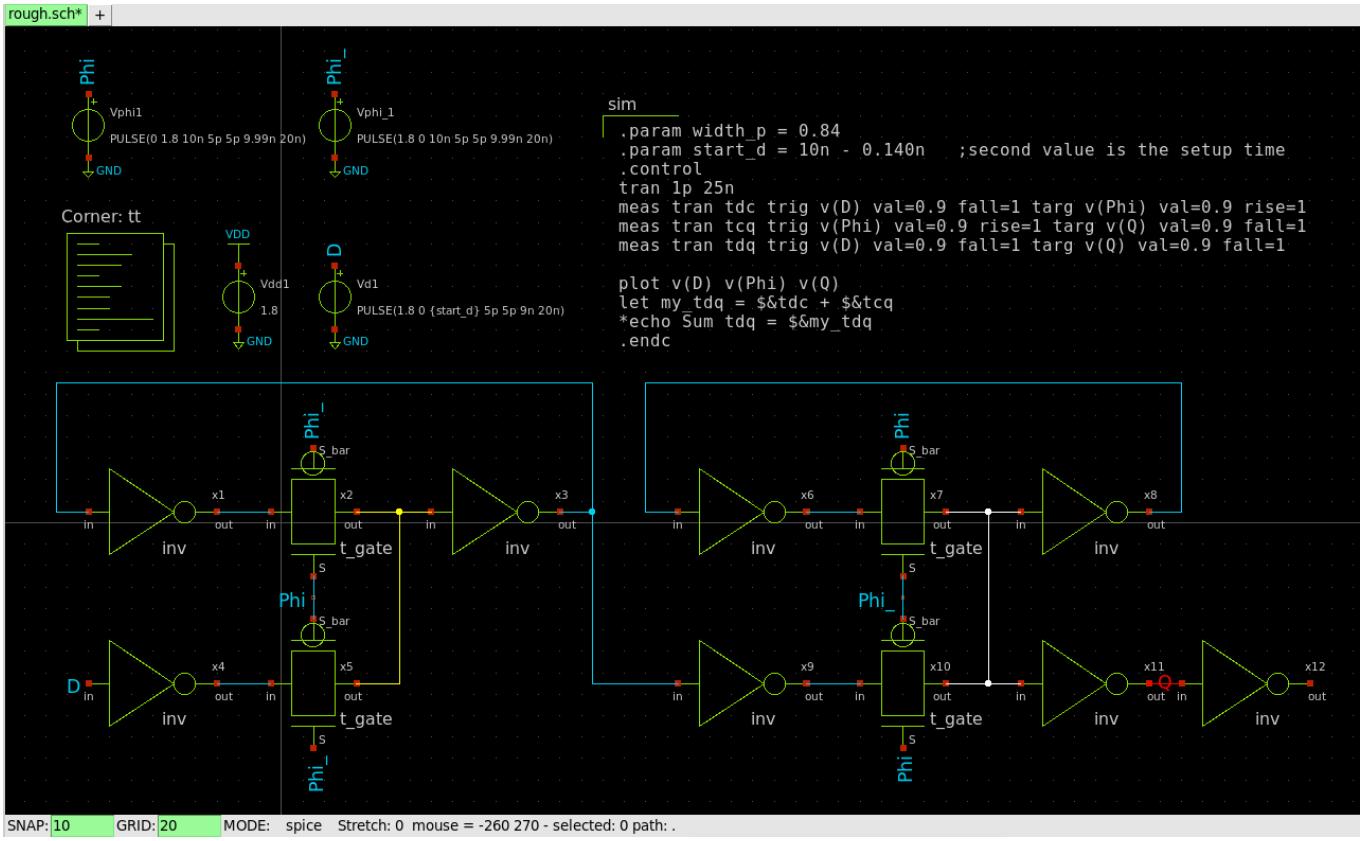
  - Minimum t_{DQ} = 0.213836 ns
  - Setup time = 0.11654 ns
  - Clock-Q delay = 97.2958 ps

- Accurate values (from probing around the simulated t_{setup})

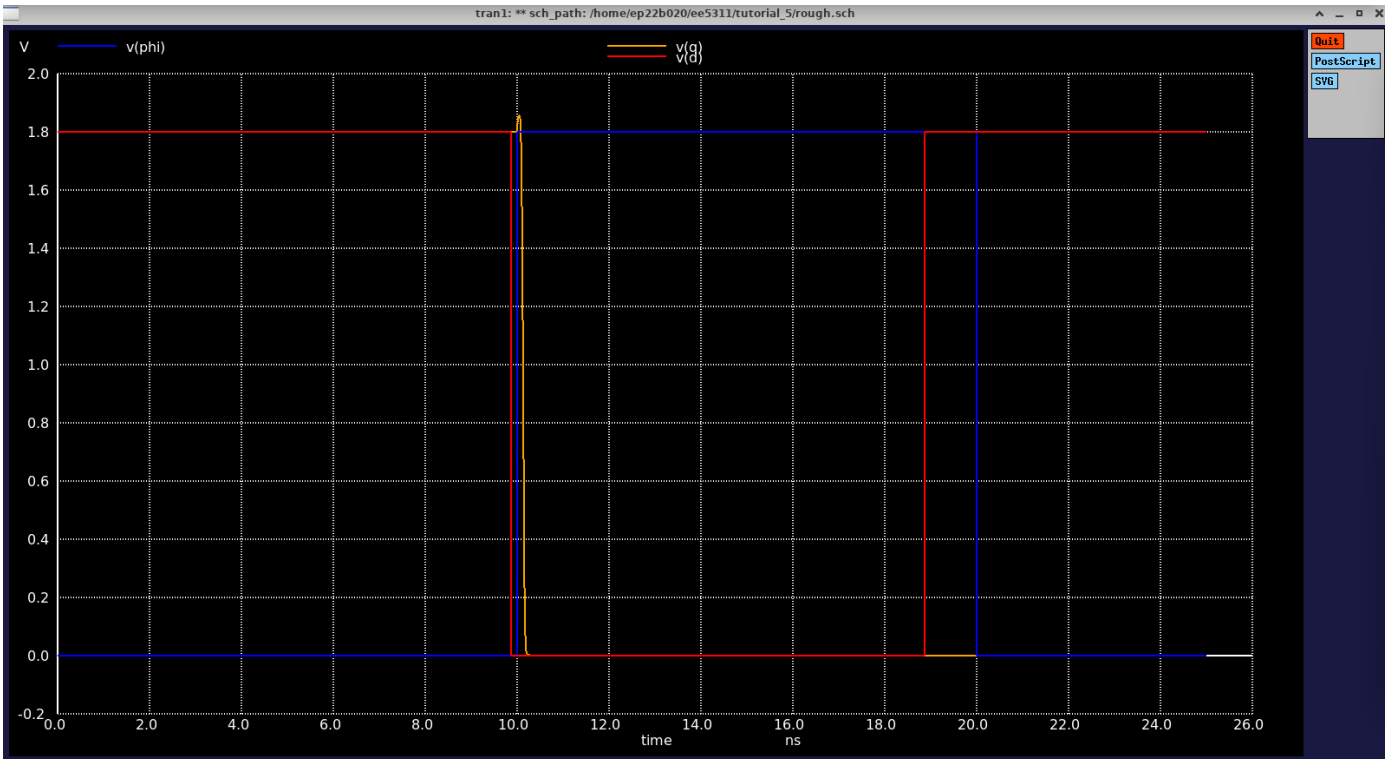
```
tdc                =  1.178000e-10 targ=  1.000250e-08 trig=  9.884700e-09
tcq                =  9.601704e-11 targ=  1.009852e-08 trig=  1.000250e-08
tdq                =  2.138170e-10 targ=  1.009852e-08 trig=  9.884700e-09
ngspice 9 ->
```

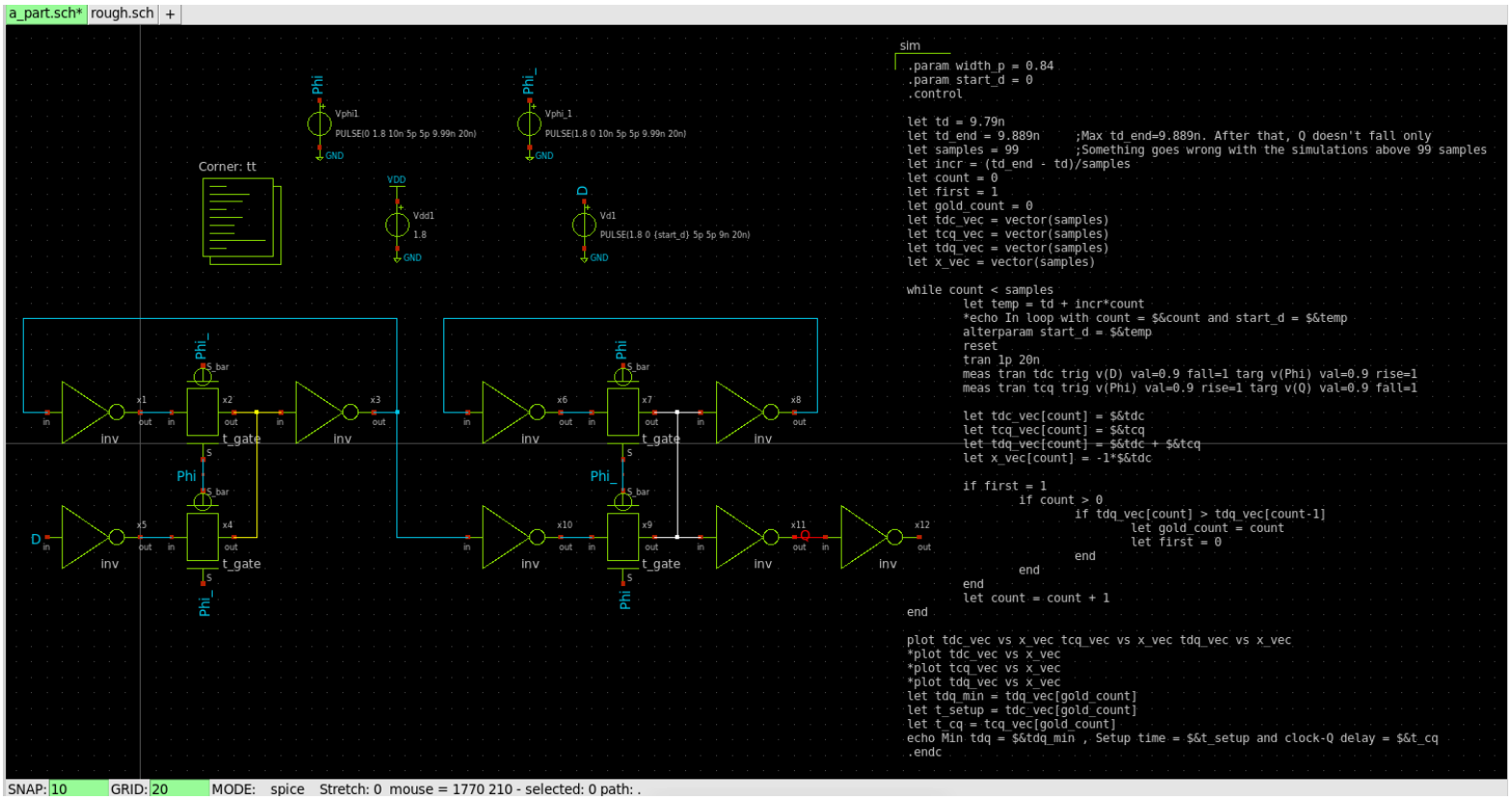
  - Minimum t_{DQ} = 0.213817 ns
  - Setup time = 0.1178 ns
  - Clock-Q delay = 96.01704 ps

Part b – Falling transition at D (and Q)

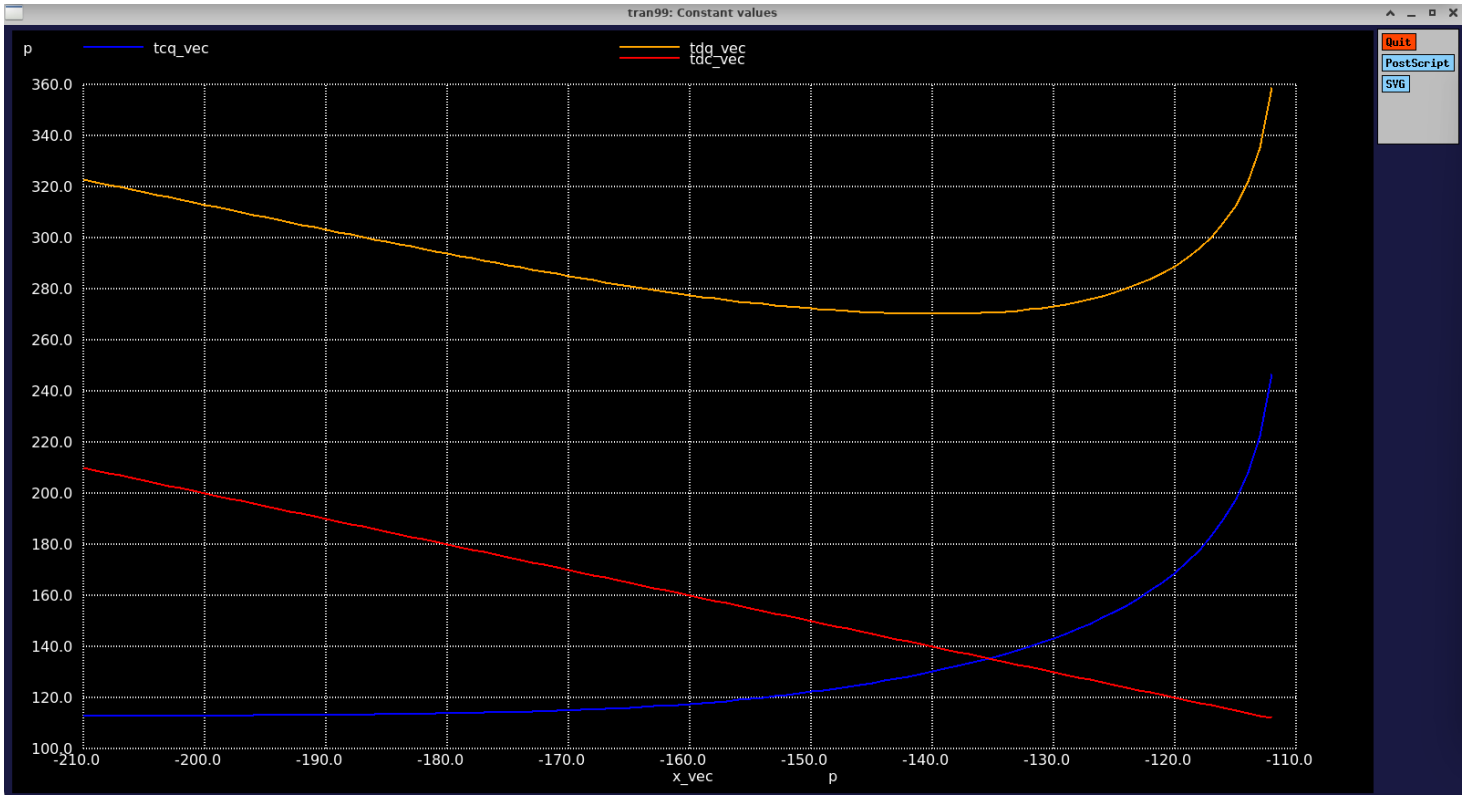


- Plot of the input (D) vs output (Q) when t_{DC} is the setup time –





- Plot showing the variation of t_{DC}, t_{CQ} and t_{DQ} for different values of t_{DC} –



- Values (from simulation)

```
tcq                =  2.486330E-10 targ=  1.024334E-08 trig=  1.000230E-08
Min tdq = 2.70318E-10 , Setup time = 1.39E-10 and clock-Q delay = 1.31318E-10
ngspice 11 ->
```

  - Minimum t_{DQ} = 0.270318 ns
  - Setup time = 0.1390 ns
  - Clock-Q delay = 0.131318 ns

- Accurate values (from probing around the simulated t_{setup})

```
No. of Data Rows : 25032
tdc                =  1.400000e-10 targ=  1.000250e-08 trig=  9.862500e-09
tcq                =  1.302994e-10 targ=  1.013280e-08 trig=  1.000250e-08
tdq                =  2.702994e-10 targ=  1.013280e-08 trig=  9.862500e-09
ngspice 11 -> 
```

  - Minimum t_{DQ} = 0.270299 ns
  - Setup time = 0.1400 ns
  - Clock-Q delay = 0.130299 ns