

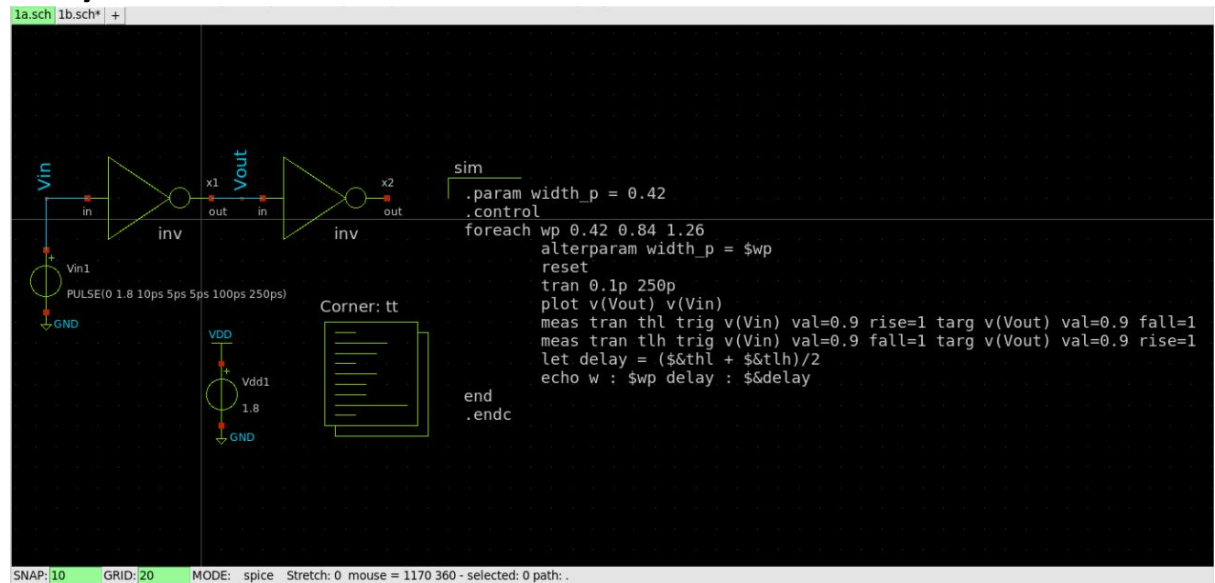
# Tutorial 4 report

## EE5311 (Digital IC design)

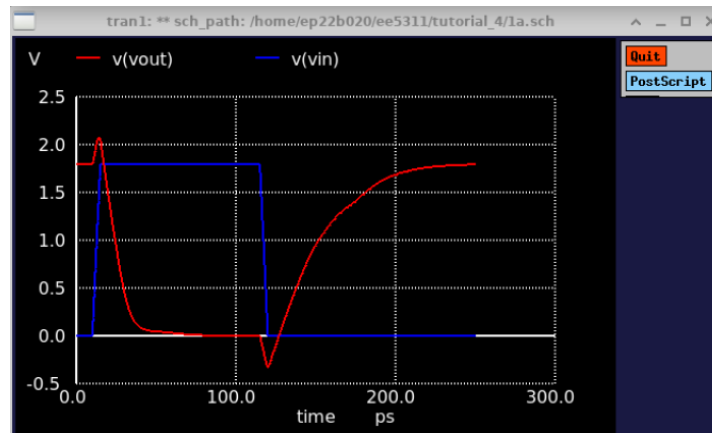
- Amogh G. Okade (EP22B020)

### Question 1

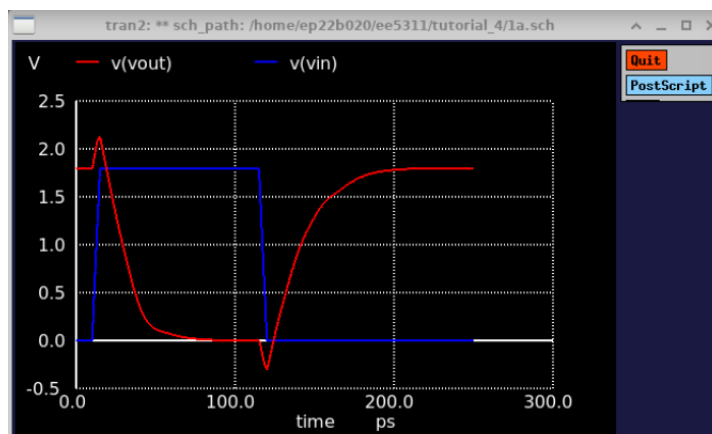
#### Part a)



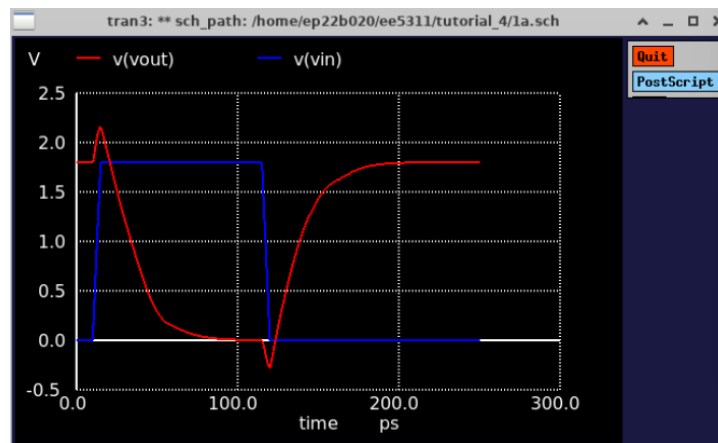
- Plot of the transient of the output voltage for an input pulse for –  
➤  $W_p = 0.42\mu\text{m}$



- $W_p = 0.84\mu\text{m}$



- $W_p = 1.26\mu\text{m}$



- The delay for –

- $W_p = 0.42\mu\text{m}$  is equal to 21.826ps. (thl = 12.77ps, tih = 30.88ps)

```

la.spice -a || sh
Circuit: ** sch_path: /home/ep22b020/ee5311/tutorial_4/1a.sch
Doing analysis at TEXP = 27.000000 and TNOH = 27.000000
Using SPWSE 1.3 as Direct Linear Solver
Initial Transient Solution
Node      Voltage
----
vout      1.8
vin        0
vdd        1.8
net1      4.59050e-08
vddI#branch -1.51498e-11
vini#branch 0
Reference value : 0.00000e+00
No. of Data Rows : 2520
thl      = 1.277011e-11 targ= 2.527011e-11 trigs 1.250000e-11
tjh      = 3.080209e-11 targ= 1.403829e-10 trigs 1.175000e-10
w : 0.42 delay : 2.18265E-11
Reset re-loads circuit ** sch_path: /home/ep22b020/ee5311/tutorial_4/1a.sch

```

- $W_p = 0.84\mu\text{m}$  is equal to 19.954ps. (thl = 18.23ps, tih = 21.68ps)

```

la.spice -a || sh
Circuit: ** sch_path: /home/ep22b020/ee5311/tutorial_4/1a.sch
Doing analysis at TEXP = 27.000000 and TNOH = 27.000000
Using SPWSE 1.3 as Direct Linear Solver
Initial Transient Solution
Node      Voltage
----
vout      1.8
vin        0
vdd        1.8
net1      6.712229e-07
vddI#branch -2.43518e-10
vini#branch 0
Reference value : 5.90500e-11
No. of Data Rows : 2520
thl      = 1.622364e-11 targ= 3.072364e-11 trigs 1.250000e-11
tjh      = 2.167370e-11 targ= 1.331730e-10 trigs 1.175000e-10
w : 0.84 delay : 1.99547E-11
Reset re-loads circuit ** sch_path: /home/ep22b020/ee5311/tutorial_4/1a.sch

```

- $W_p = 1.26\mu\text{m}$  is equal to 21.119ps. (thl = 23.27ps, tih = 18.96ps)

```

la.spice -a || sh
Circuit: ** sch_path: /home/ep22b020/ee5311/tutorial_4/1a.sch
Doing analysis at TEXP = 27.000000 and TNOH = 27.000000
Using SPWSE 1.3 as Direct Linear Solver
Initial Transient Solution
Node      Voltage
----
vout      1.8
vin        0
vdd        1.8
net1      9.60947e-07
vddI#branch -3.47833e-10
vini#branch 0
Reference value : 1.06450e-10
No. of Data Rows : 2520
thl      = 2.327333e-11 targ= 3.577333e-11 trigs 1.250000e-11
tjh      = 1.896577e-11 targ= 1.364858e-10 trigs 1.175000e-10
w : 1.26 delay : 2.11195E-11
ngspice 7 -> []

```

## Part b)

We know that

$$R_{eq, n} \propto \frac{1}{\mu_n W_n},$$

$$R_{eq, p} \propto \frac{1}{\mu_p W_p} \quad \text{and}$$

$$C_{int} \propto (W_n + W_p)$$

We know that the delay (which can be written as  $R C \ln 2$ ),

$$t_{p, inv} \propto R_{eq} \times C_{int} = \left( \frac{R_{eq, n} + R_{eq, p}}{2} \right) C_{int}$$

$$t_{p,inv} \propto \left( \frac{1}{\mu_n W_n} + \frac{1}{\mu_p W_p} \right) (W_n + W_p)$$

For the minimum delay,

$$\frac{d t_{p,inv}}{d W_p} = 0$$

$$-\frac{(W_n + W_p)}{\mu_p W_p^2} + \left( \frac{1}{\mu_n W_n} + \frac{1}{\mu_p W_p} \right) = 0$$

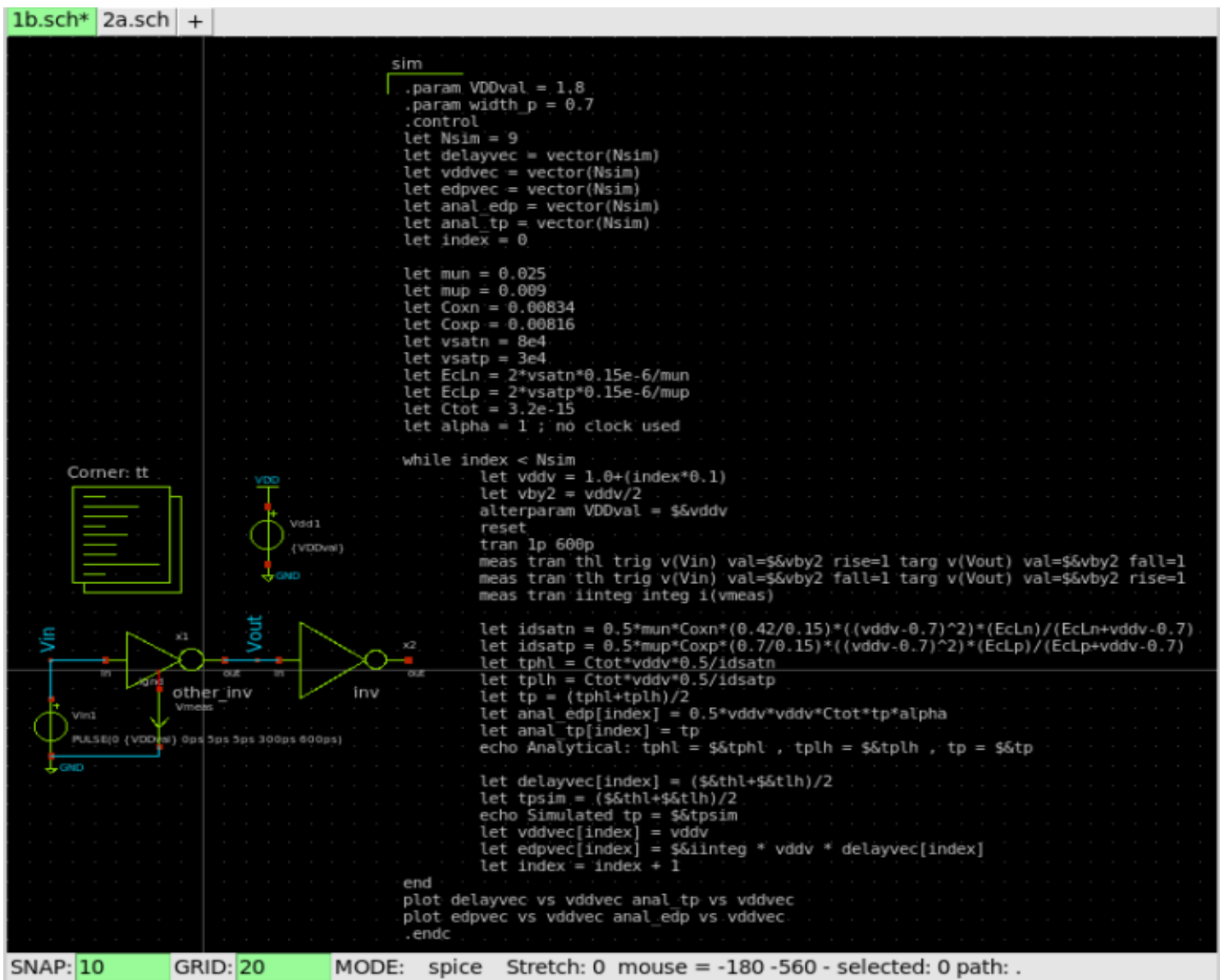
$$-\frac{W_n}{\mu_p W_p^2} + \frac{1}{\mu_n W_n} = 0$$

Or

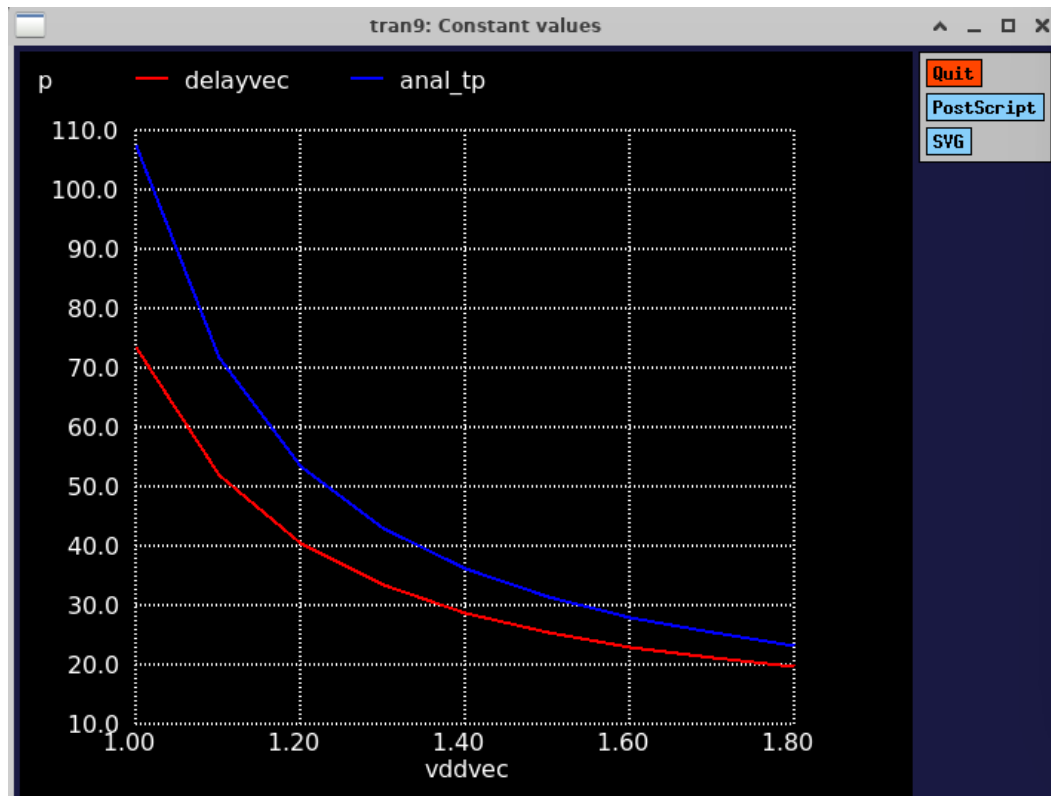
$$W_p = \sqrt{\frac{\mu_n}{\mu_p}} \times W_n$$

Substituting  $(\mu_n/\mu_p) = (25/9)$  and  $W_n = 0.42\mu\text{m}$ , we get

$W_p = 0.7\mu\text{m}$  for minimum delay



- Plot of the measured and analytical delay as a function of  $V_{DD}$  for  $V_{DD} = 1V$  to  $1.8V$  –

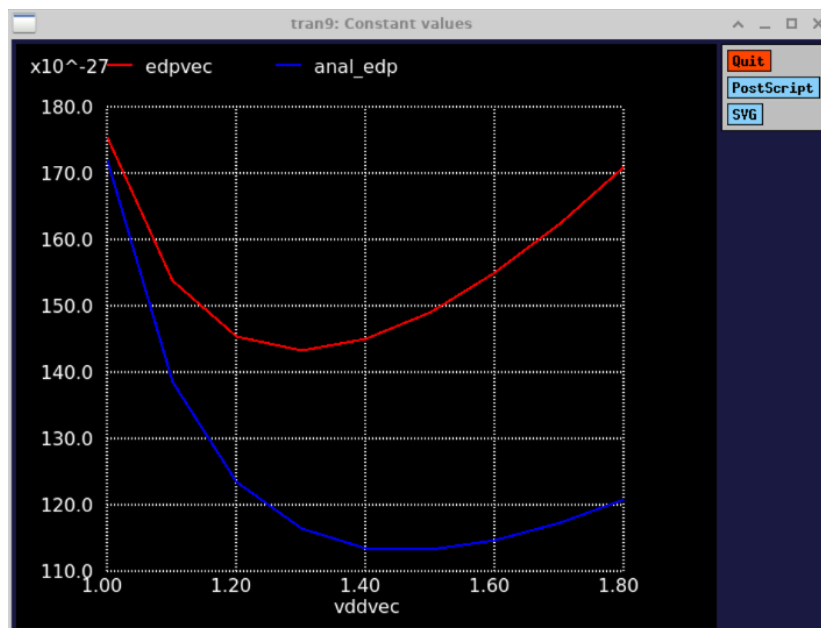


- We note that the delay decreases as  $V_{DD}$  increases.
- Although intuition dictates that the delay should be higher for a larger  $V_{DD}$ , (since the curve would take longer to come down from a larger  $V_{DD}$ ), it is actually the increased current that is responsible for pulling the voltage down faster, at a higher  $V_{DD}$ .
- Comparison between measured and analytical values –

	Simulation			Estimated		
$V_{DD}$ (volts)	thl (ps)	tlh (ps)	tp (ps)	thl (ps)	tlh (ps)	tp (ps)
1	53.53	93.67	73.60	79.94	134.87	107.40
1.1	37.69	66.32	52.00	53.38	89.87	71.63
1.2	29.80	51.10	40.45	40.14	67.23	53.62
1.3	25.20	41.65	33.42	32.16	53.95	43.05
1.4	22.20	35.32	28.76	27.08	45.35	36.21
1.5	21.10	30.86	25.48	23.55	39.39	31.47
1.6	18.57	27.60	23.08	20.98	35.04	28.01
1.7	17.38	25.14	21.26	19.02	31.75	25.38
1.8	16.44	23.26	19.85	17.50	29.17	23.33

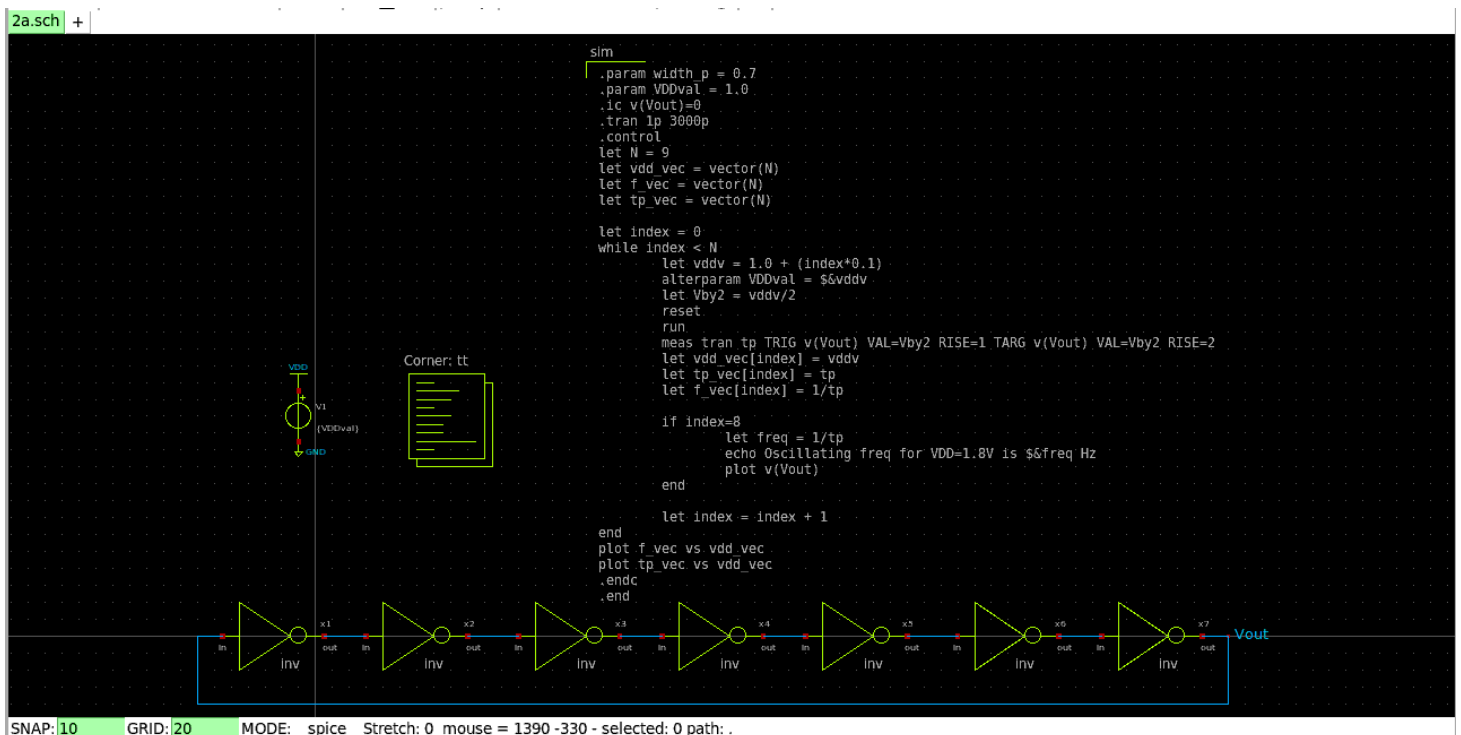
## Part c)

- Plot of the measured and analytical energy-delay product as a function of  $V_{DD}$  for  $V_{DD} = 1V$  to  $1.8V$  –



- The optimum VDD is observed to be 1.3V from the simulation, and 1.4V from the analytical estimate.

## Question 2



## Part a)

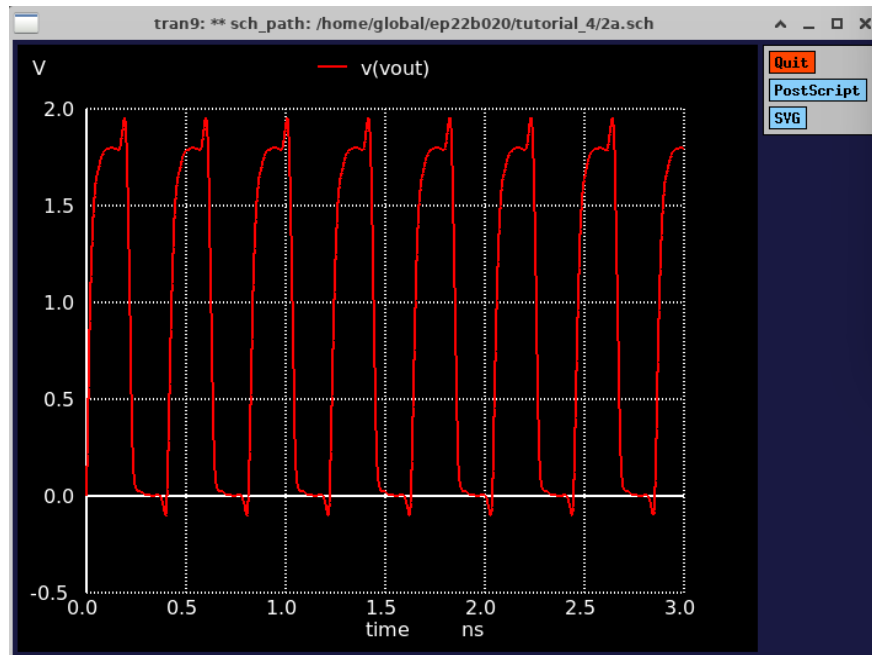
For  $V_{DD}=1.8V$ , the oscillating frequency is 2.45 GHz.

```

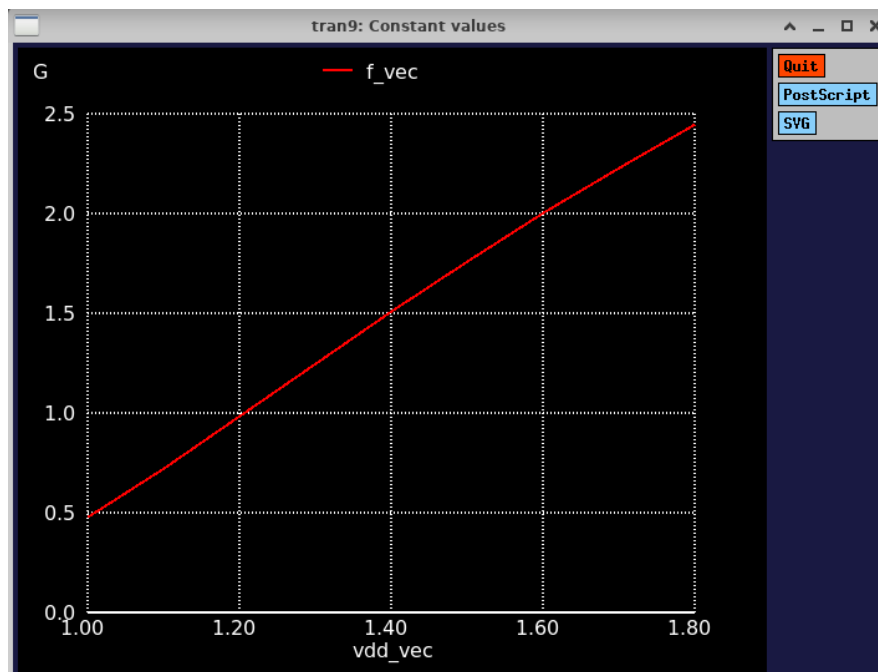
Reference value : 2.49528e-09
No. of Data Rows : 3008
tp                = 4.080253e-10 targ= 4.241690e-10 trig= 1.614375e-11
Oscillating freq for VDD=1.8V is 2.45083E+09 Hz
ngspice 8 -> █
  
```

## Part b)

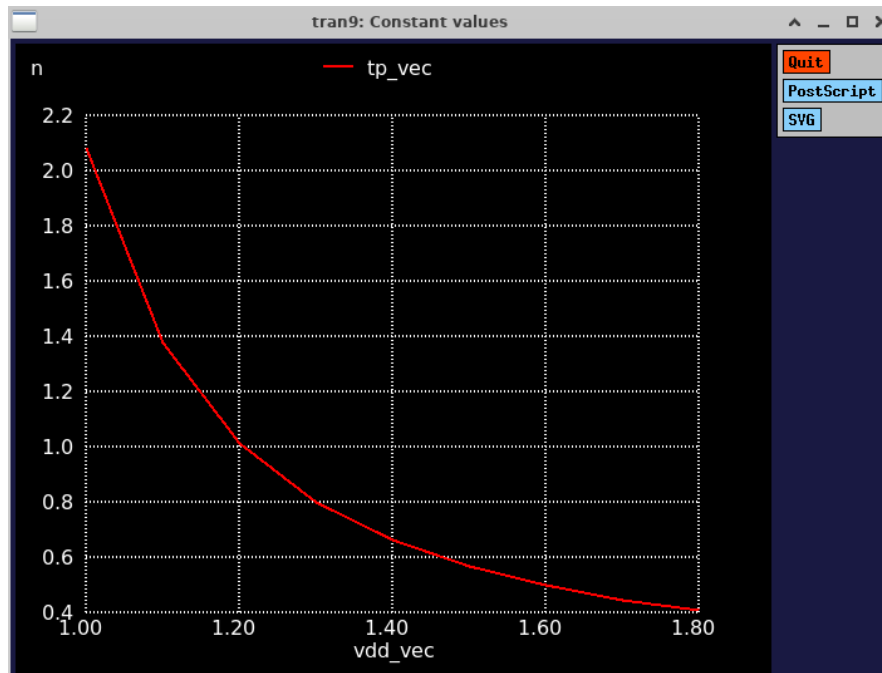
- Plot of the output voltage for  $V_{DD} = 1.8V$  –



- Plot of the oscillating frequency as a function of  $V_{DD}$  for  $V_{DD} = 1V$  to  $1.8V$  –



- Plot of the time period as a function of  $V_{DD}$  for  $V_{DD} = 1V$  to  $1.8V$  –

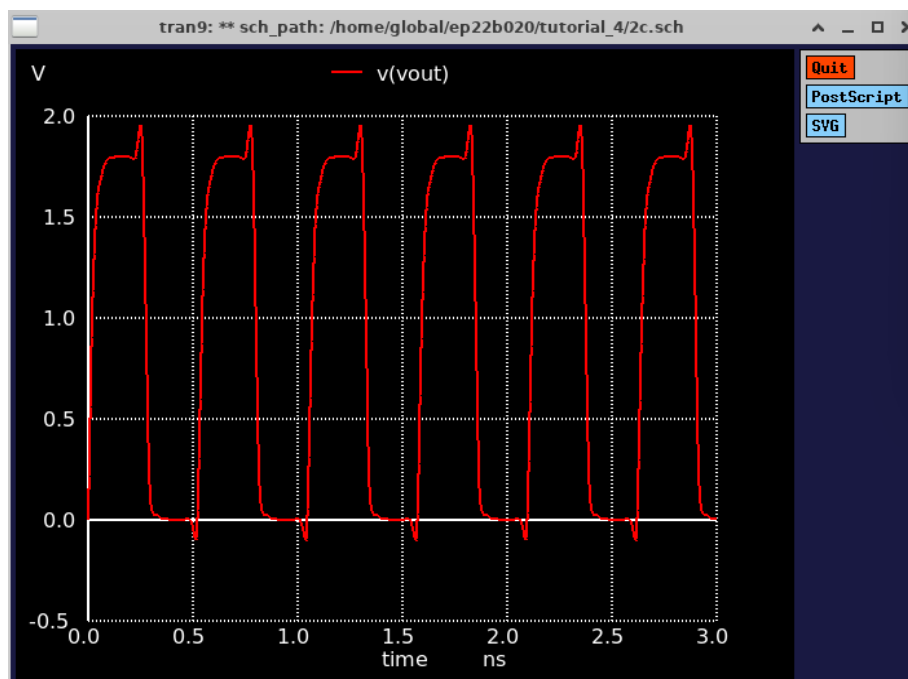


## Part c)

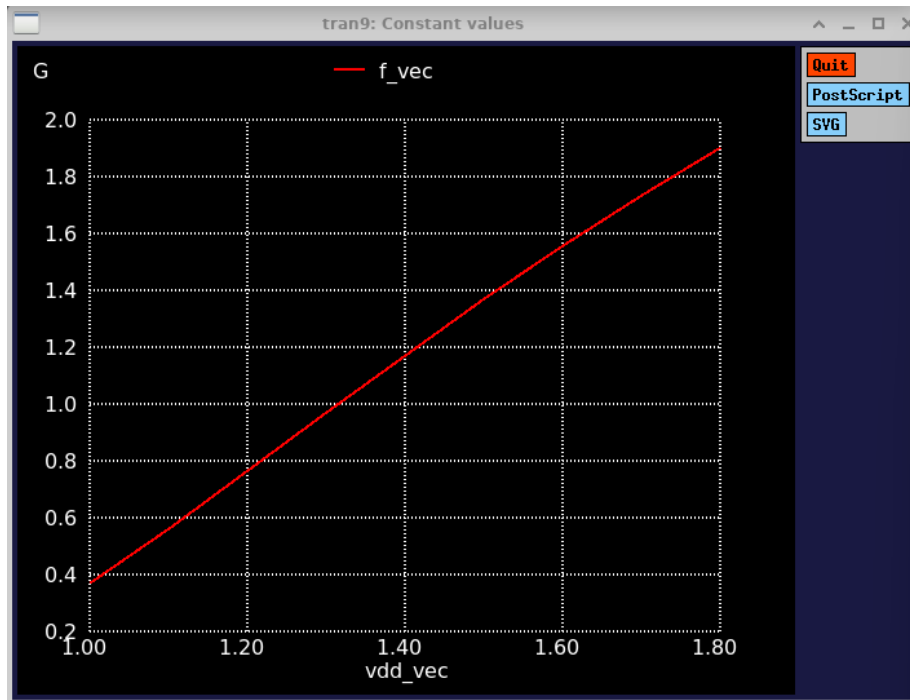
For  $V_{DD}=1.8V$ , the oscillating frequency is 1.91 GHz.

```
Reference value : 1.63128e-09
No. of Data Rows : 3008
tp = 5.246637e-10 targ= 5.408074e-10 trig= 1.614374e-11
Oscillating freq for VDD=1.8V is 1.90598E+09 Hz
ngspice 8 -> █
```

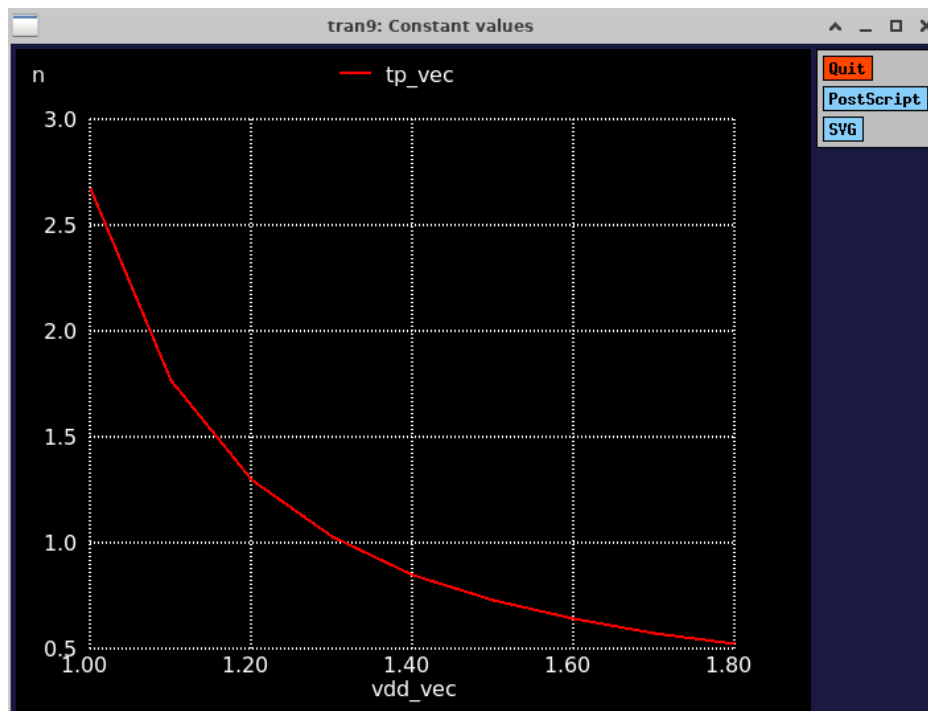
- Plot of the output voltage for  $V_{DD} = 1.8V$  –



- Plot of the oscillating frequency as a function of  $V_{DD}$  for  $V_{DD} = 1V$  to  $1.8V$  –



- Plot of the time period as a function of  $V_{DD}$  for  $V_{DD} = 1V$  to  $1.8V$  –



- We notice that the frequency of the oscillator with 7 inverters is higher, since there is lesser delay due to the reduced number of inverters.