

Tutorial 5 report

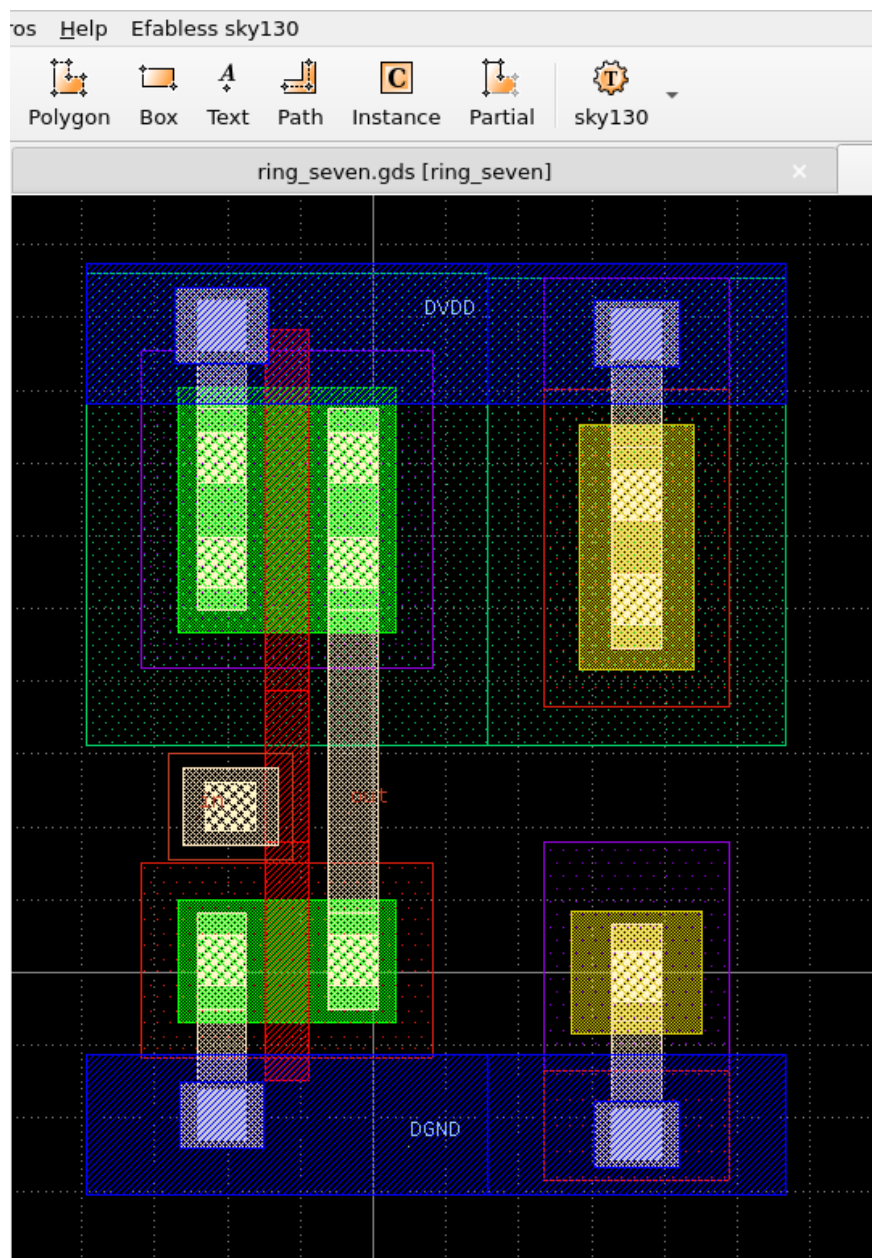
EE5311 (Digital IC design)

- Amogh G. Okade (EP22B020)

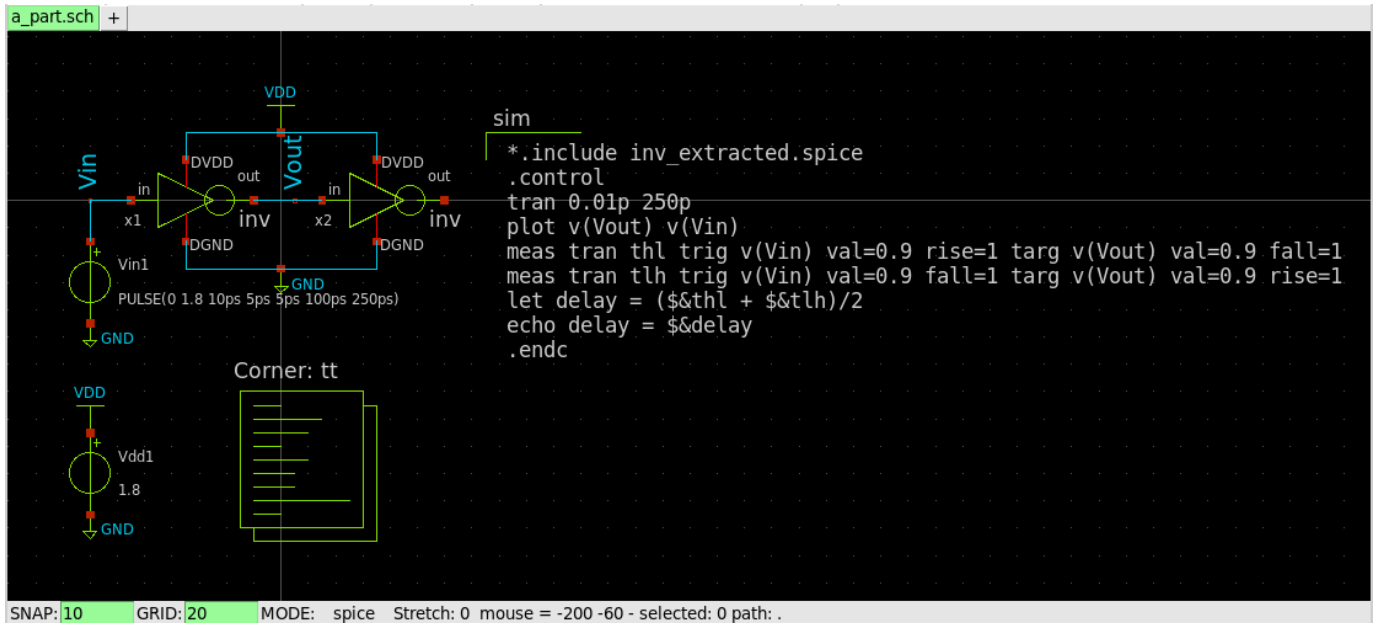
Question 1

Part a)

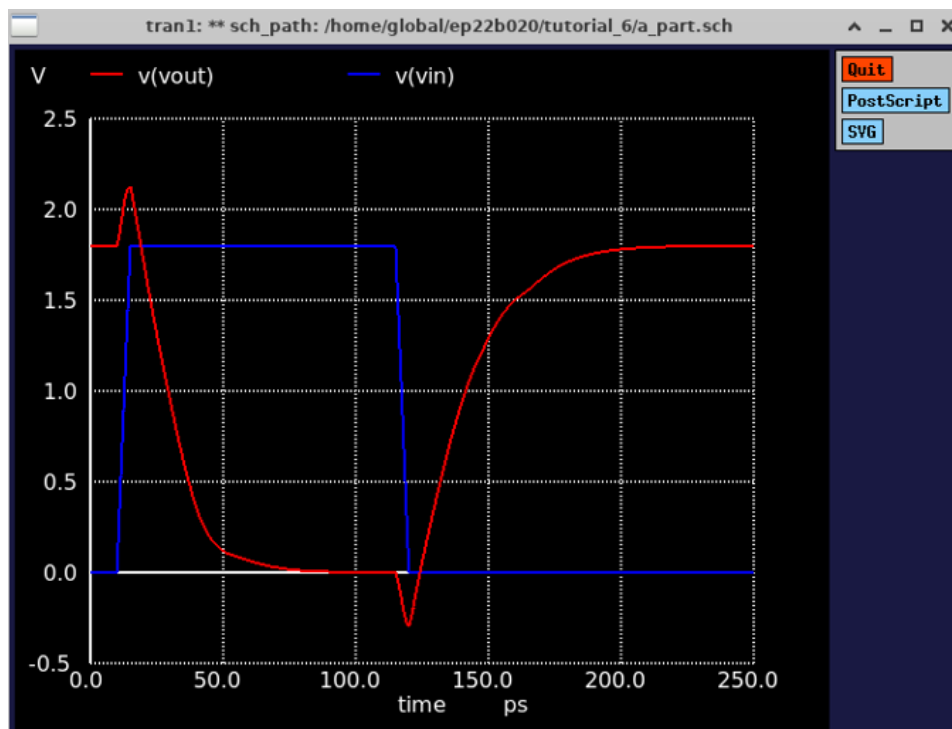
- Layout used for the reference CMOS reference inverter –



- xschem code and schematic used –



- Input vs output voltage waveforms –



- The delay without extracting the parasitic values from the layout = 19.95ps

```
Reference value : 2.30295e-10
No. of Data Rows : 25020
thl = 1.822969e-11 targ= 3.072969e-11 trig= 1.250000e-11
tlh = 2.167988e-11 targ= 1.391799e-10 trig= 1.175000e-10
delay = 1.99548E-11
ngspice 14 -> []
```

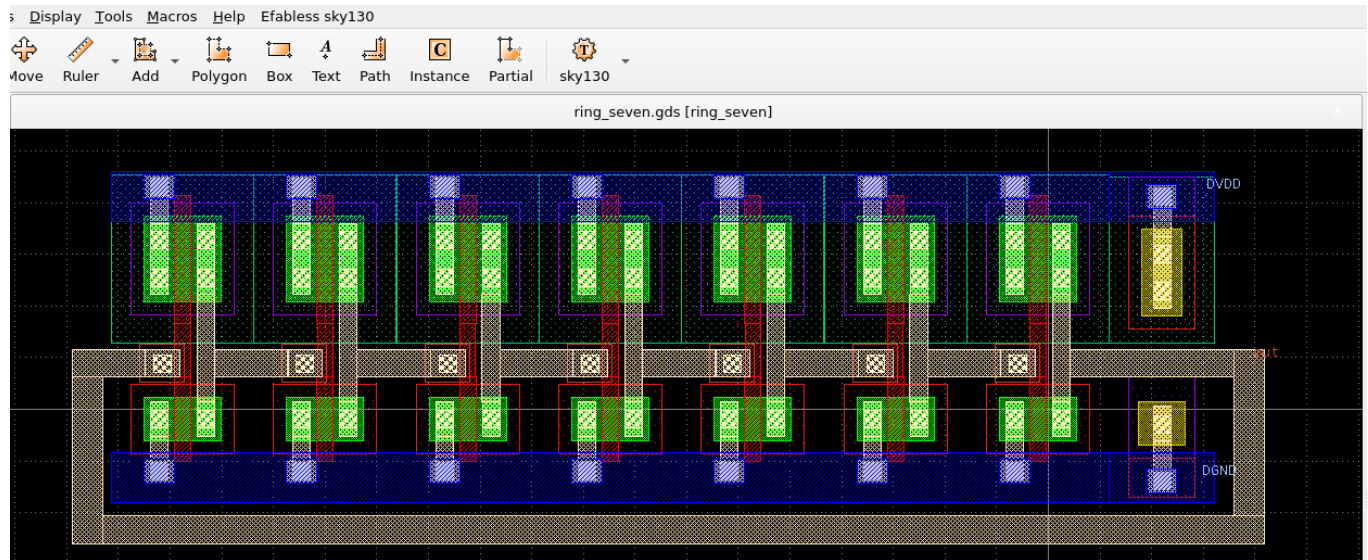
- The delay after the parasitics were extracted from the layout = 24.98ps

```
Reference value : 2.27145e-10
No. of Data Rows : 25020
thl = 2.247232e-11 targ= 3.497232e-11 trig= 1.250000e-11
tlh = 2.749761e-11 targ= 1.449976e-10 trig= 1.175000e-10
delay = 2.4985E-11
ngspice 14 -> []
```

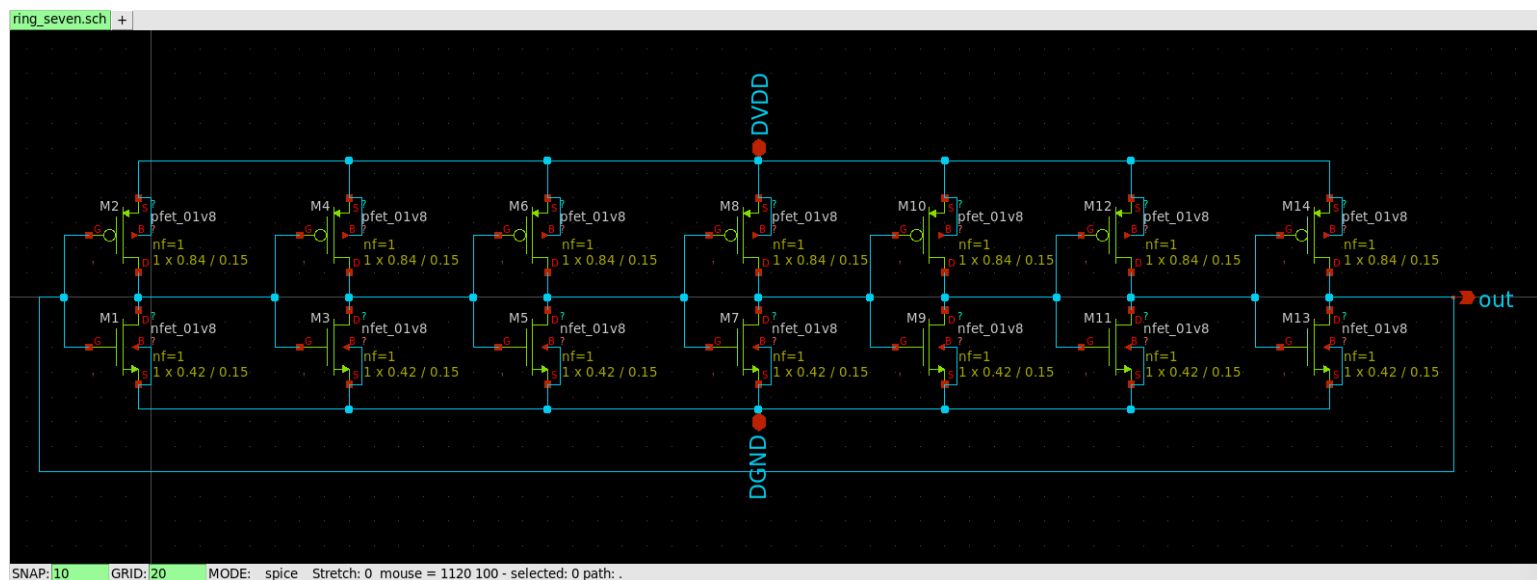
- The delay with the parasitics is higher, since it takes more time to charge the additional capacitors that arise as a virtue of the layout.

Question 2

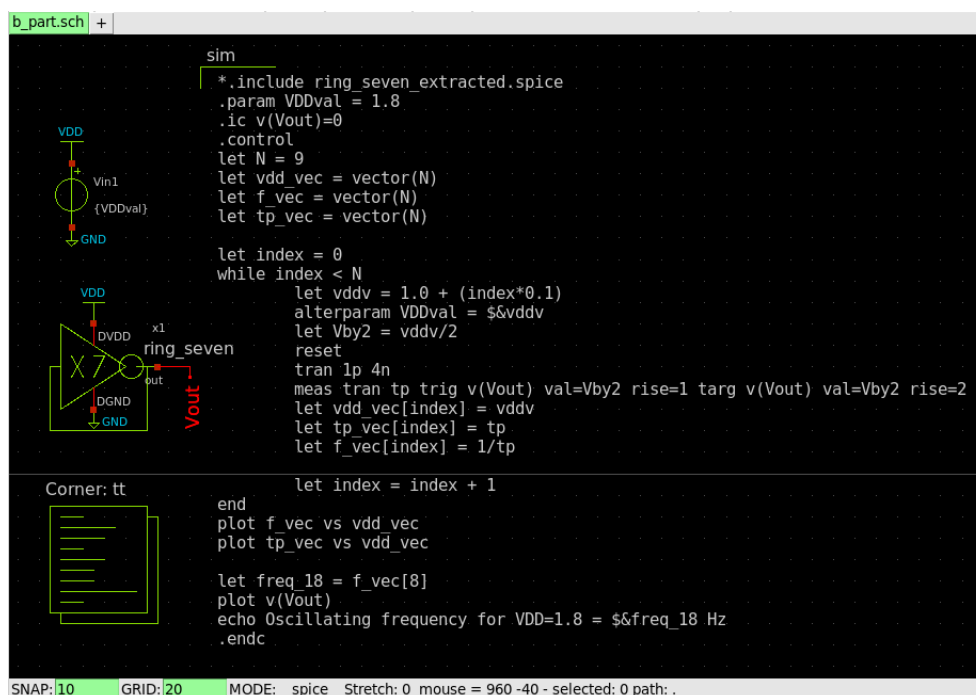
- Layout used for the seven stage ring oscillator –



- xschem symbol for the seven stage ring oscillator –



- xschem code and schematic used –



Part a)

- With the layout parasitics, the oscillating frequency for $V_{DD} = 1.8V$ is 1.75 GHz.

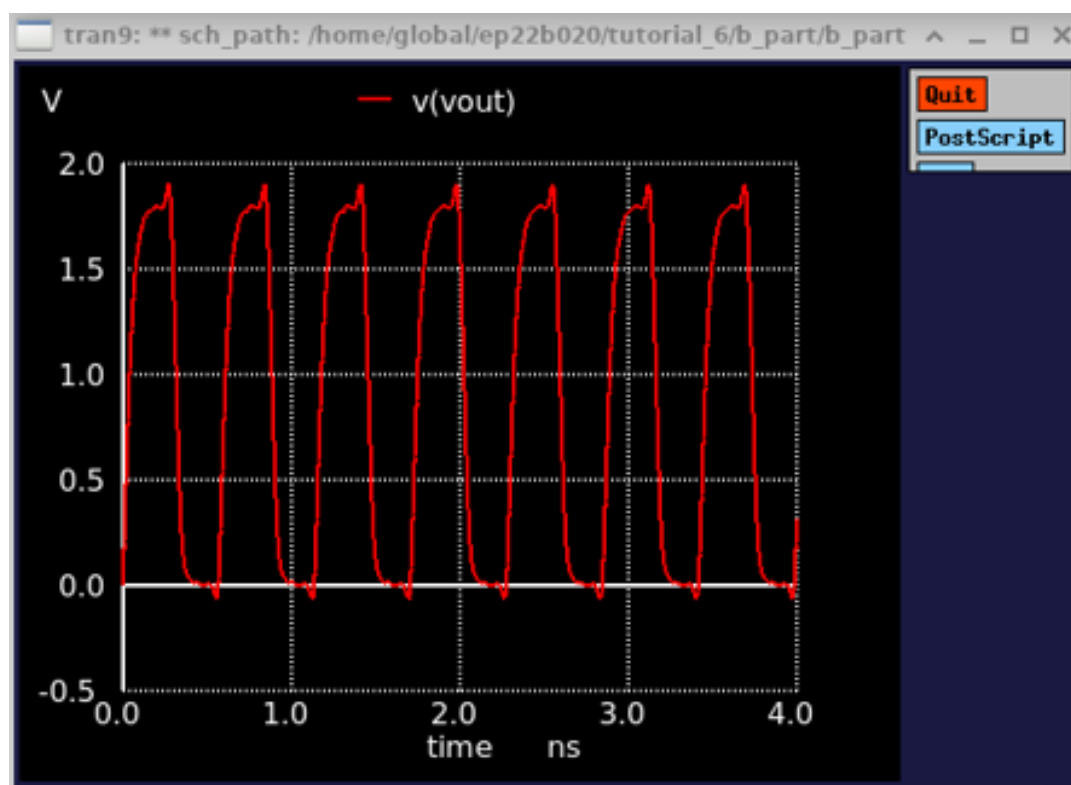
```
Reference value : 3.56228e-09  
No. of Data Rows : 4008  
tp          = 5.698879e-10 targ= 6.031605e-10 trig= 3.327264e-11  
Oscillating frequency for VDD=1.8 = 1.75473E+09 Hz  
ngspice 14 -> []
```

- With the layout parasitics, the oscillating frequency for $V_{DD} = 1.8V$ is 2.44 GHz.

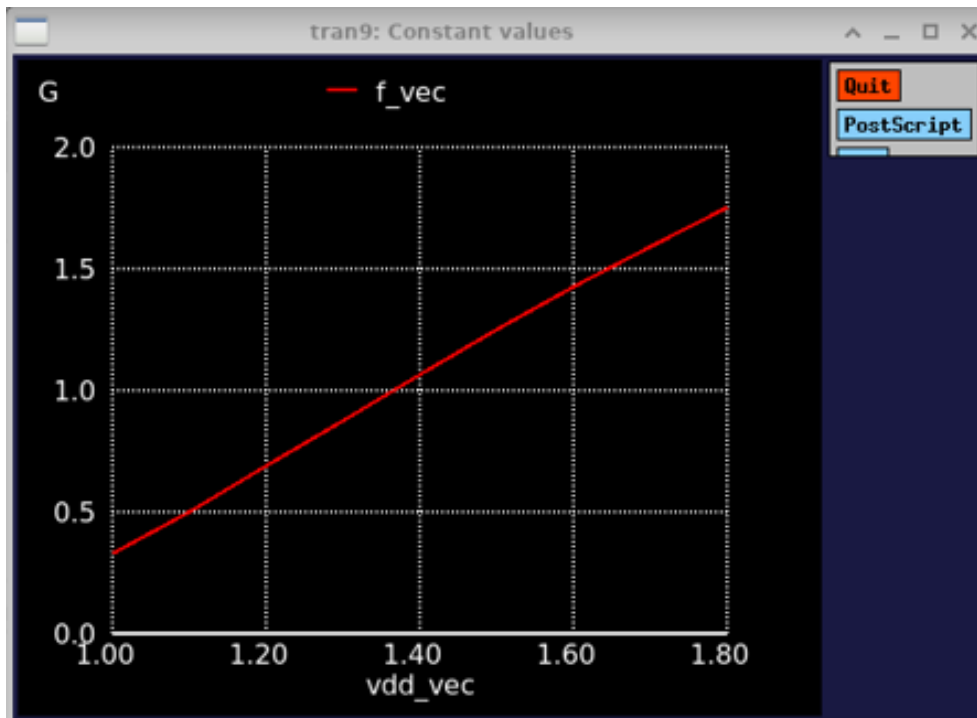
```
Reference value : 3.44328e-09  
No. of Data Rows : 4008  
tp          = 4.090127e-10 targ= 4.240400e-10 trig= 1.502726e-11  
Oscillating frequency for VDD=1.8 = 2.44491E+09 Hz  
ngspice 14 -> []
```

Part b)

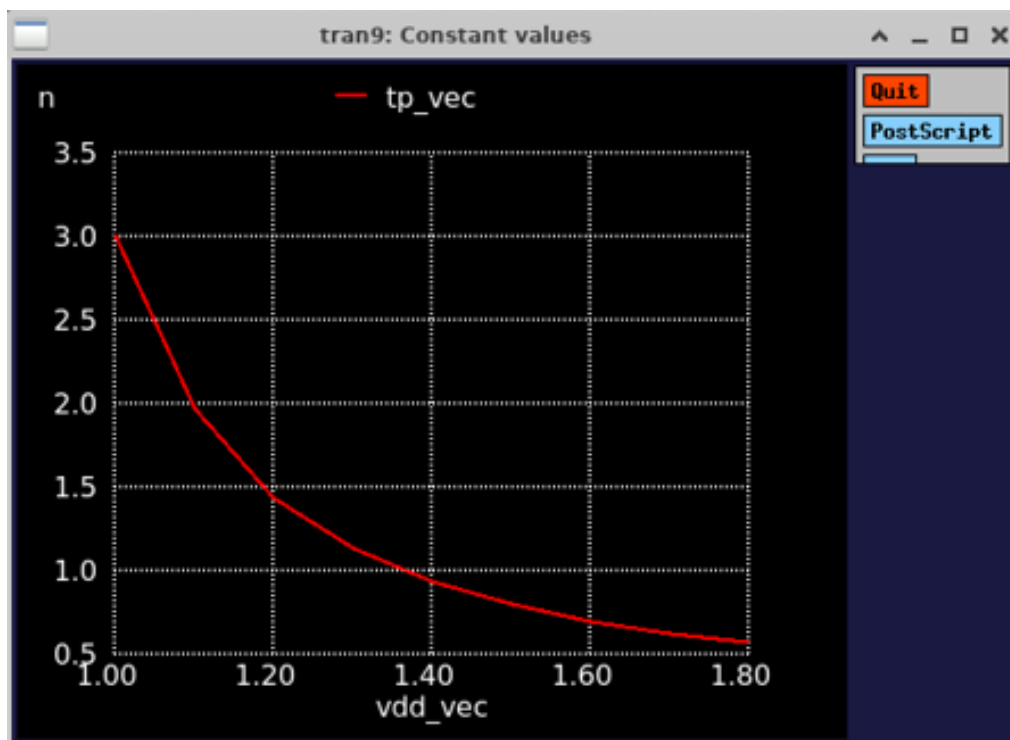
- Waveform at the output terminal –



- Plot of the oscillating frequency as a function of V_{DD} for $V_{DD} = 1V$ to $1.8V$ in steps of $0.1V$ –

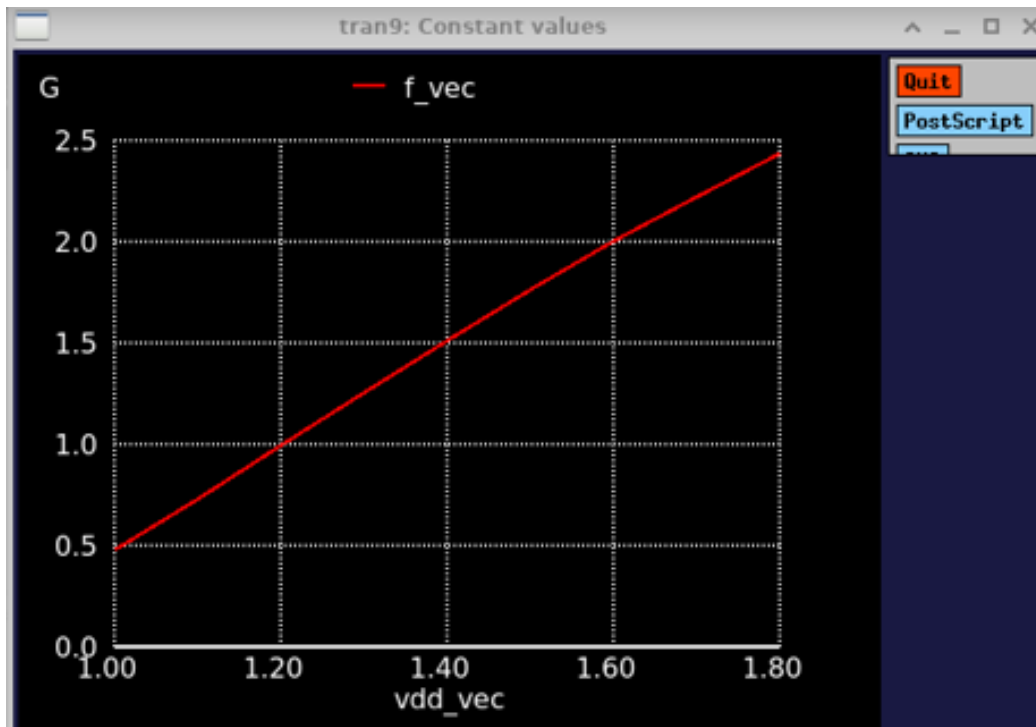


- Plot of the time period as a function of V_{DD} for $V_{DD} = 1V$ to $1.8V$ in steps of $0.1V$ –



Part c)

- Without the parasitics –



- We observe that the frequencies, for a given V_{DD} , are lesser when the parasitics are considered. This is a result of the increased delay caused by the extra capacitances that arise as part of the layout.