Tutorial 3 report
EE5311 (Digital IC design)

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Question 1

- In saturation, the PMOS current, $I_p = ½\ k_p\ cox_p\ (W/L)_p\ (V_{DD} - V_{in} - V_{tp})^2$
- In saturation, the NMOS current, $I_n = ½\ k_n\ cox_n\ (W/L)_n\ (V_{in} - V_{tn})^2$
- If the threshold voltage of the inverter, $V_{th} = V_{DD}/2$, then, at $V_{in} = V_{DD}/2$, $V_{out} = V_{DD}/2$ and the PMOS and NMOS will have equal saturation currents.
- Thus,

$$\frac{1}{2}\ \mathrm{kp}\ \left(\frac{\mathrm{VDD}}{2} - \mathrm{Vtp}\right) = \frac{1}{2}\ \mathrm{kn}\ \left(\frac{\mathrm{VDD}}{2} - \mathrm{Vtp}\right)$$

Therefore,

$$\mathrm{kp} = \mathrm{kn}$$

$$\mu_p\ \mathrm{cox}_p\ (\frac{W}{L})_p = \mu_n\ \mathrm{cox}_n\ (\frac{W}{L})_n$$

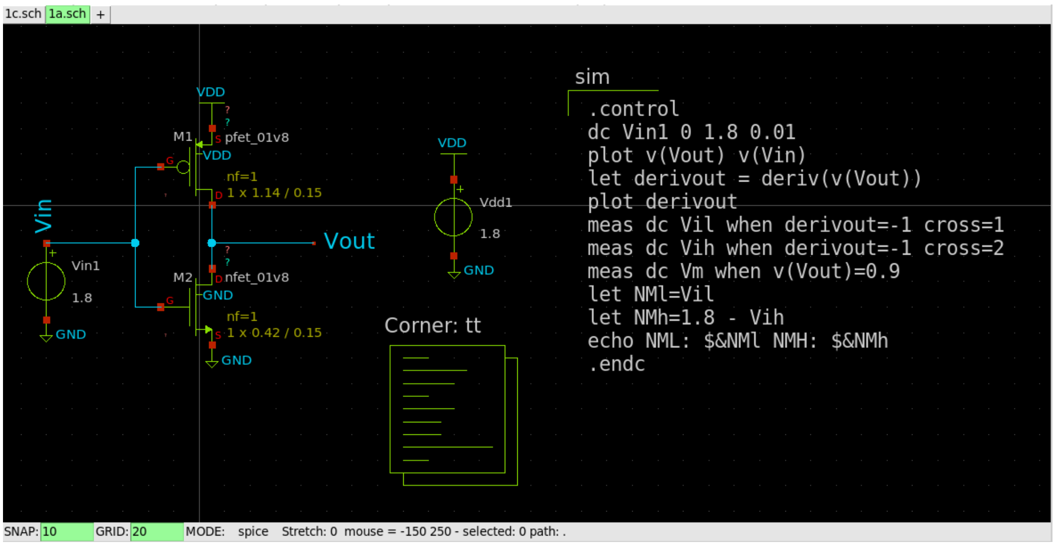
Setting $(W/L)_n = (0.42/0.15)$ and substituting the other known constants, we get

$$0.009 \text{ x } 8.16 \text{ x } (\frac{W}{L})_p = \frac{0.025 \text{ x } 8.34 \text{ x } 0.42}{0.15}$$

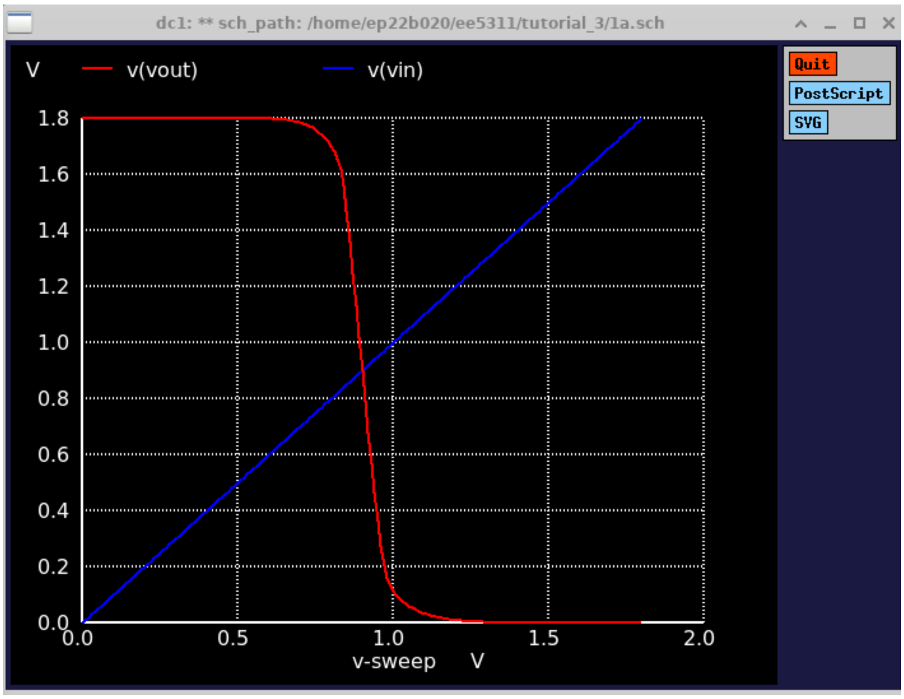
Solving, we get

$$(\frac{W}{L})_p = \frac{1.19}{0.15}$$

However, for simulating with values around the calculated one, we may find that $(W/L)_p = (1.14/0.15)$ yields more accurate results for $V_{DD} = 1.8V$.

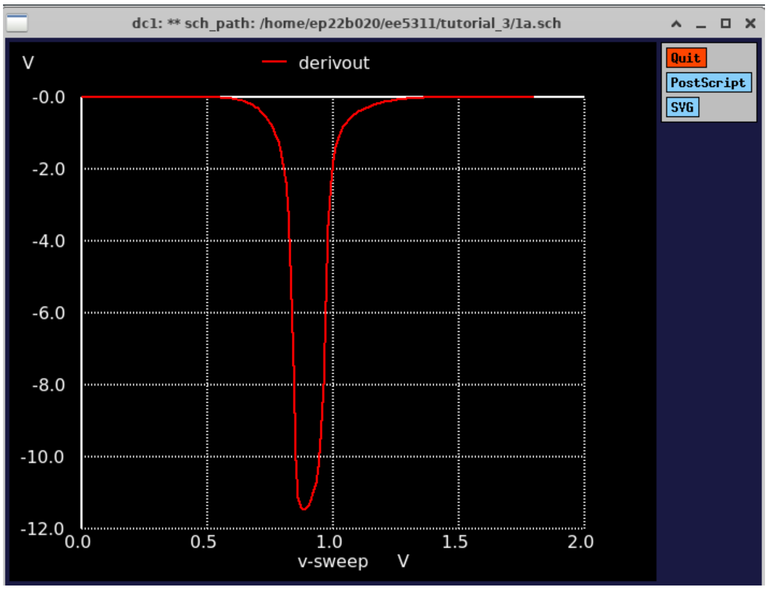


- Plot of the DC transfer charactersitics (Vout vs Vin):-



Part a)

- Plot of the derivative of the output voltage vs Vin –



- Noise margins –
  NML = 0.768, NMH = 0.773

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Using SPARSE 1.3 as Direct Linear Solver
 Reference value :  0.00000e+00
No. of Data Rows : 181
vil                 =  7.680573e-01
vih                 =  1.026838e+00
vm                  =  9.002006e-01
NML: 0.768057 NMH: 0.773162
ngspice 6 -> []
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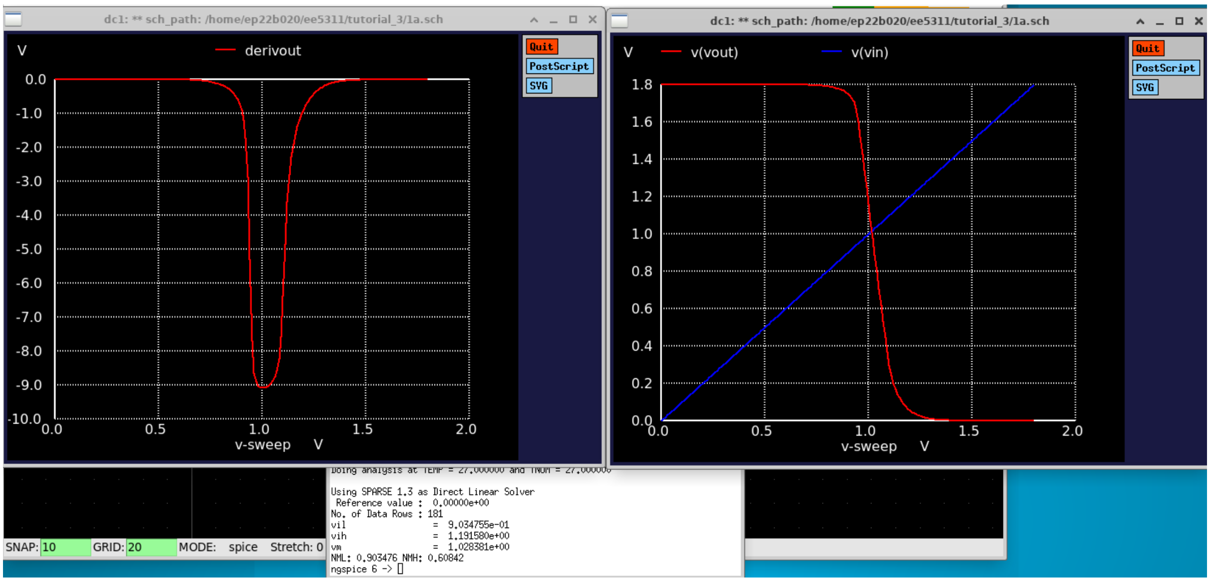
Part b)

- From the equation balancing the saturation currents at $V_{in} = V_{th}$

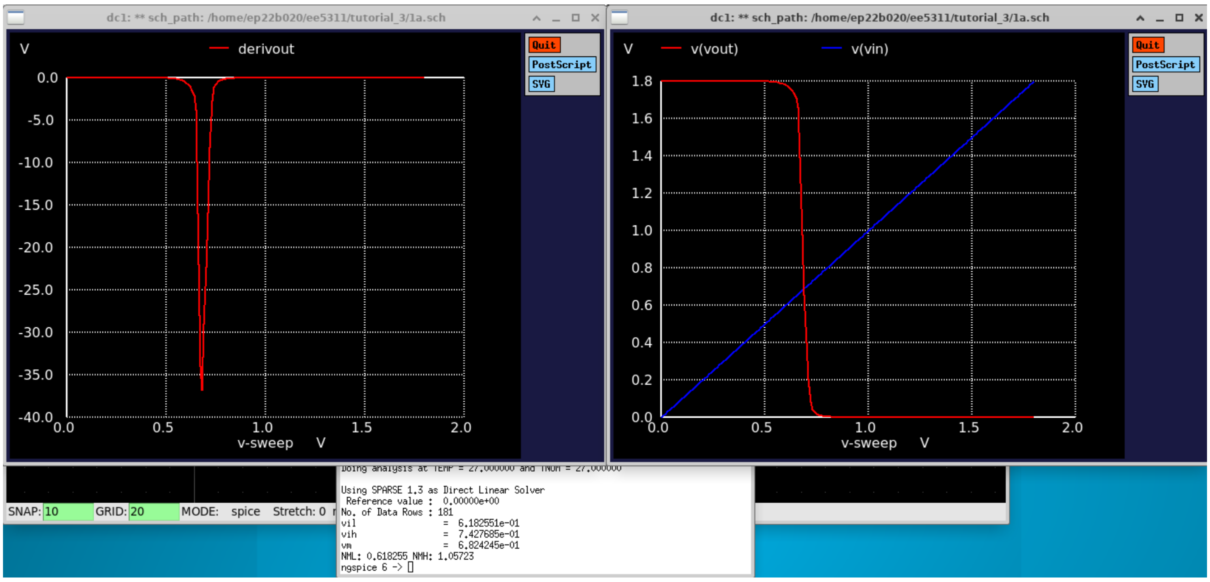
$$\mathrm{kp} = \mathrm{kn}\,\frac{(\mathrm{Vth} - \mathrm{Vtp})}{(\mathrm{VDD} - \mathrm{Vth} - \mathrm{Vtp})}$$

  we can clearly see that if $(W/L)_p$ is increased (k_p is increased), the inverter threshold V_{th} also increases, and vice-versa for when $(W/L)_p$ is decreased.
- When $(W/L)_p$ is increased, we also notice that NML increases, while NMH decreases. The converse can be said for the case where $(W/L)_p$ is decreased.

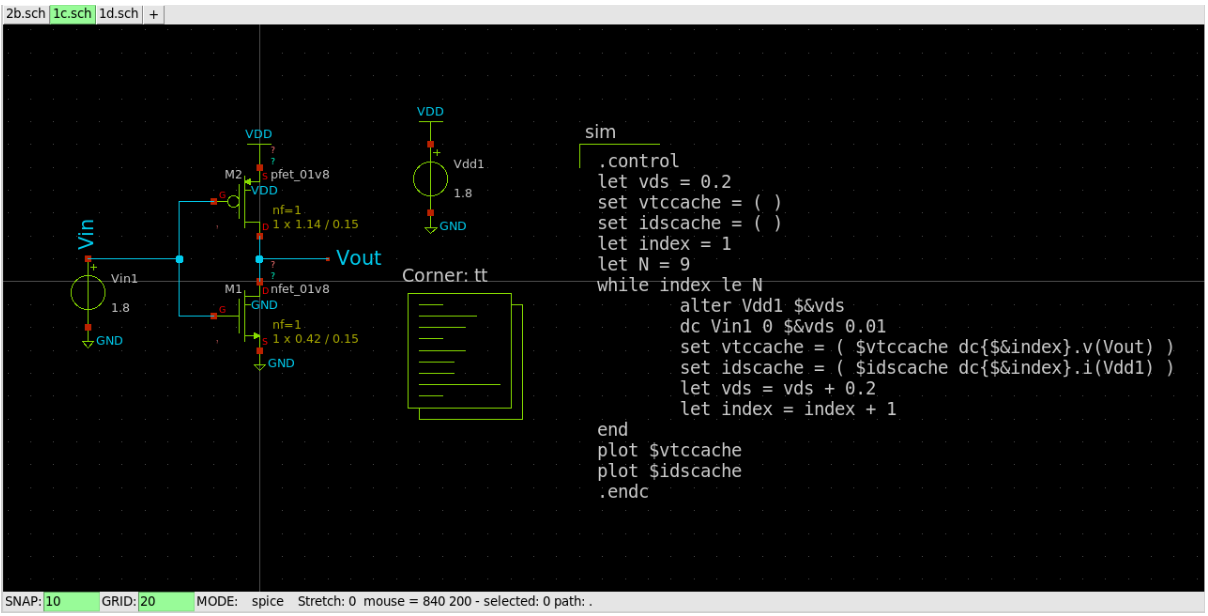
- Plot of the derivative of Vout and plot of Vout vs Vin when $(W/L)_p$ is increased by a factor of 10 (that is, $(W/L)_p = (11.4/0.15)$) –



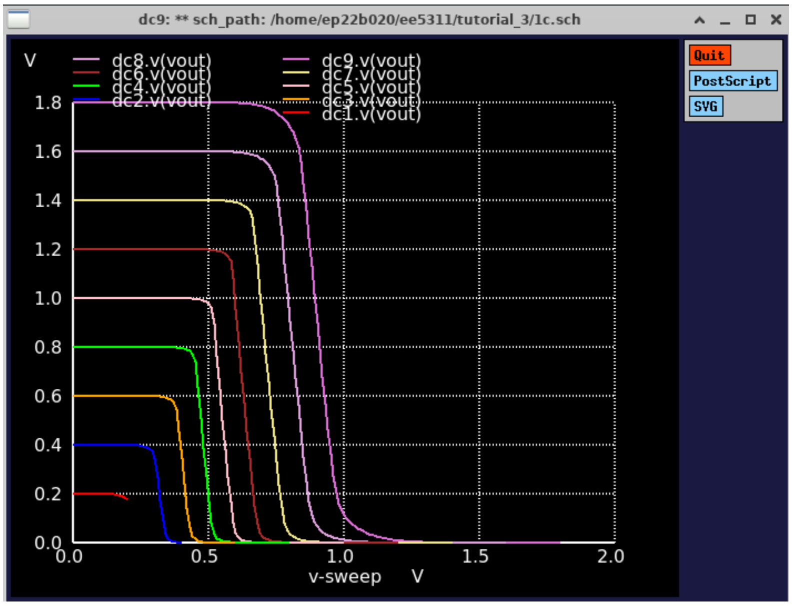
- Plot of the derivative of Vout and plot of Vout vs Vin when $(W/L)_p$ is decreased by a factor of 10 (that is, $(W/L)_p = (1.14/1.5)$) –



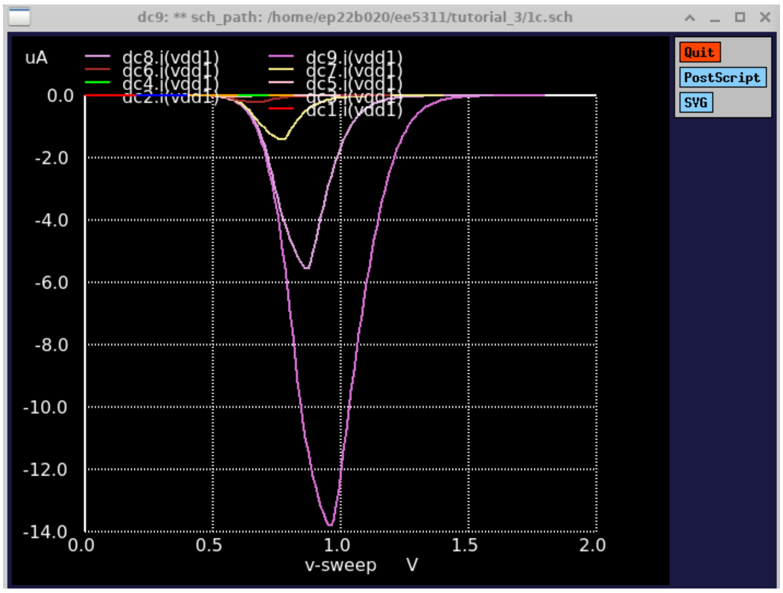
Part c)



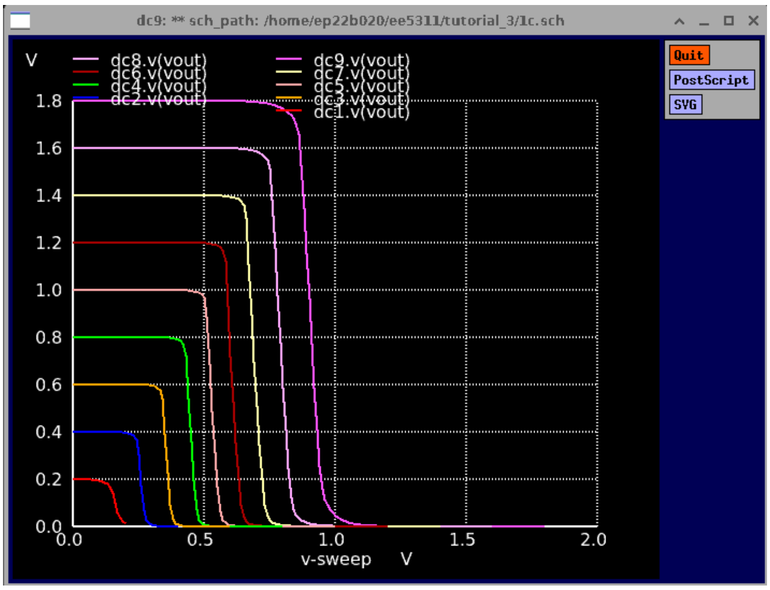
- Plot of the DC transfer characteristics (Vout vs Vin) for V_{DD} ranging from 0.2V to 1.8V –



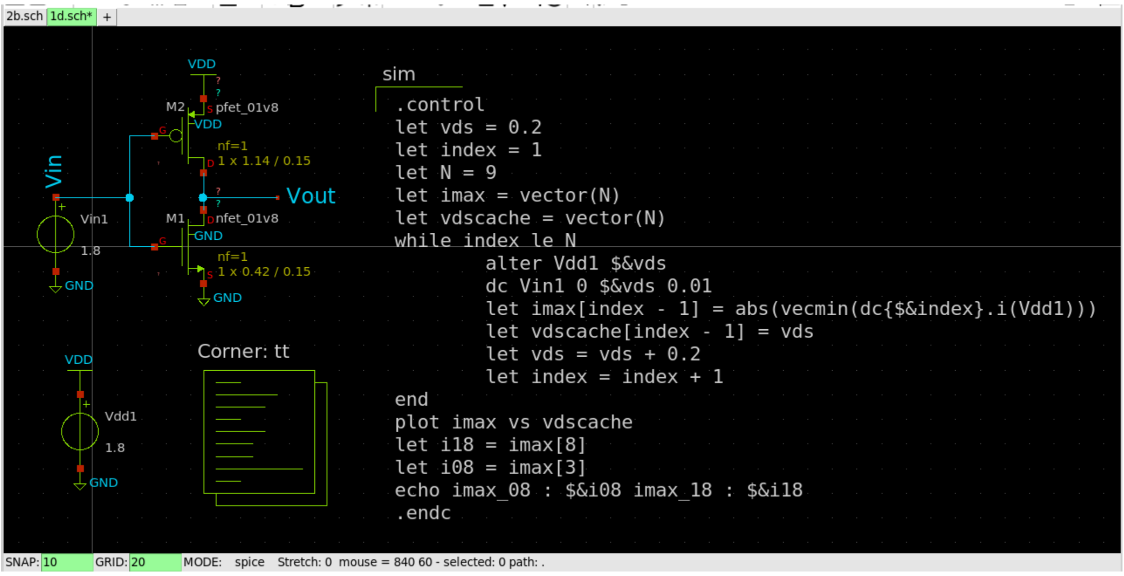
- Plot of I_{DS} vs V_{in} for V_{DD} ranging from 0.2V to 1.8V –



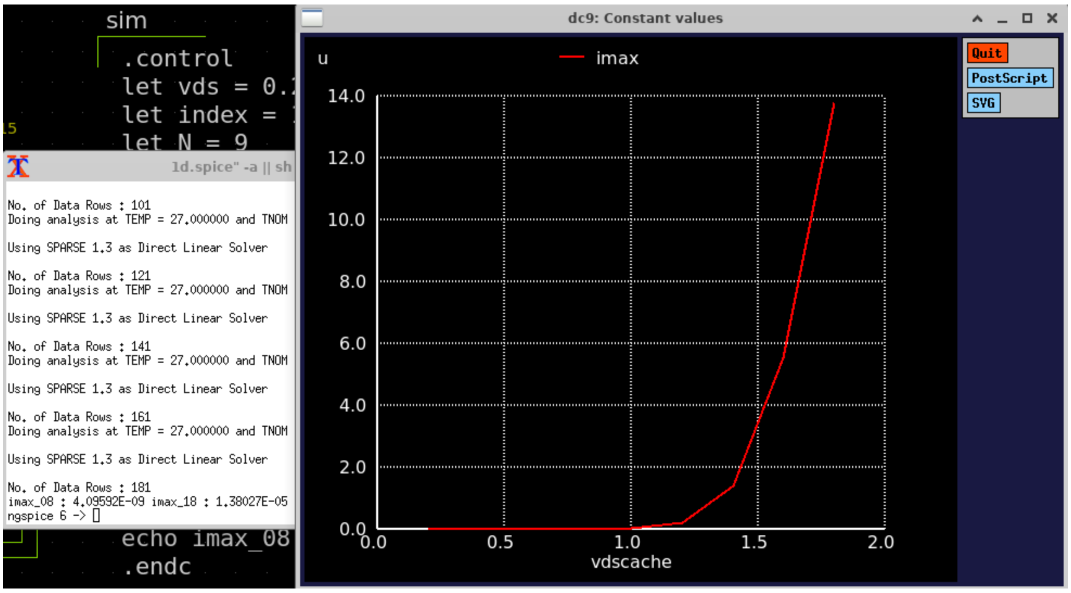
- For V_{DD} = 0.2V, it can't be used as an inverter.
  The PMOS length can be increased slightly (and the width fine-tuned) to turn it into an inverter. For $(W/L)_p = (5/0.18)$, we get –



Part d)



- Plot of the peak I_{DS} for different values of V_{DD} –



- From the plot, peak I_{DS} = 4.09nA for V_{DD} = 0.8V and 13.8uA for V_{DD} = 1.8V.
- The analytical values are-

  For VDD = 0.8V, peak I_{DS} = 0, since both MOSFETs are cutoff at all times.

  For VDD = 1.8V, assuming that the peak I_{DS} occurs at V_{in} = V_{out} = V_{th}, we get (from the NMOS saturation current equation)

$$\text{Ids, peak} = \frac{1}{2}\text{ kn }(0.9 - 0.7)^2(1 + 0.2 \text{ x } 0.9) = 13.778\text{uA}$$

Question 2

- At V_{in} = V_{DD}, V_{out} = V_{OL}
- For these conditions (and assuming V_{OL} = 0.1V), we find that the PMOS is in triode and the NMOS is in saturation.
- Balancing the currents for the above conditions, we get

$$\frac{1}{2}\text{ kp }(\text{VDD} - \text{Vtp})^2 = \text{kn}\left(\text{VDD} - \text{Vtn} - \frac{\text{VOL}}{2}\right)\text{ VOL}$$

On solving further, we get

$$kn \text{ x } VOL^2 - VOL \text{ x } 2kn\,(VDD - Vtn) + kp \text{ x } (VDD - Vtp)^2 = 0$$

$$VOL = VDD - Vtn - \sqrt{(VDD - Vtn)^2 - \frac{kp}{kn}(VDD - Vtp)^2}$$

For V_{OL} = 0.1V, V_{DD} = 1.8V and $V_{tn} = V_{tp}$ = 0.7V, we get

$$\frac{kp}{kn} = \frac{0.21}{1.21}$$

$$\frac{\mu_p\, cox_p\, (\frac{W}{L})_p}{\mu_n\, cox_n\, (\frac{W}{L})_n} = \frac{0.21}{1.21}$$

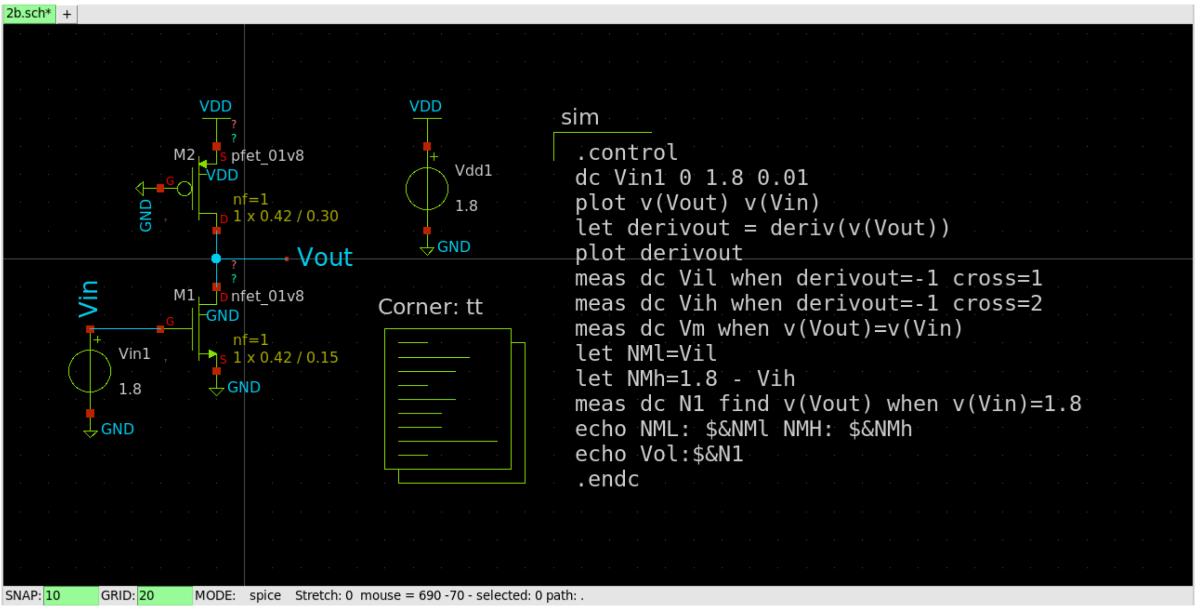
Substituting for the known constants, we get

$$\frac{0.009 \text{ x } 8.16\,\left(\frac{W}{L}\right)_p}{0.025 \text{ x } 8.34\,\left(\frac{W}{L}\right)_n} = \frac{0.21}{1.21}$$

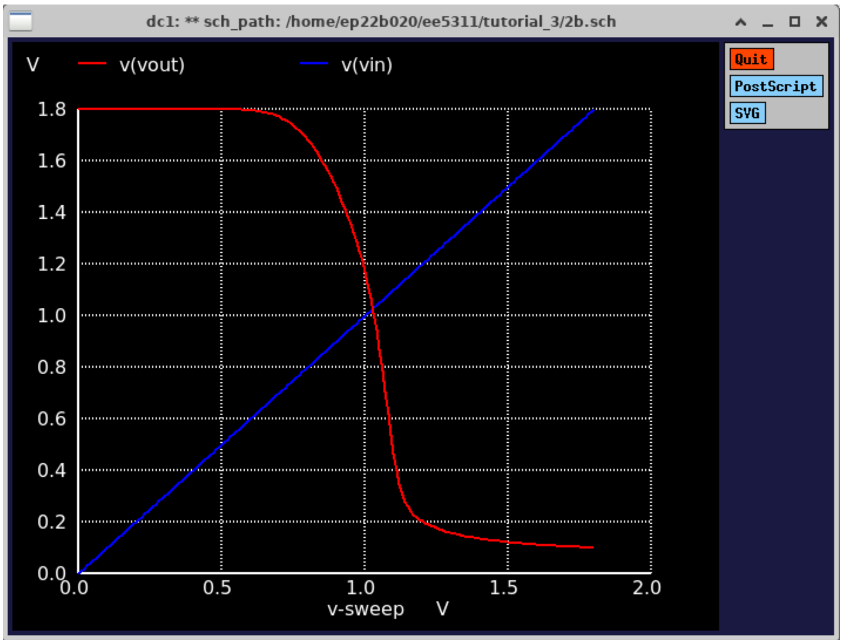
$$(\frac{W}{L})_p = 0.4927 \text{ x } (\frac{W}{L})_n$$

For $(W/L)_n$ = (0.42/0.15), we get

$$(\frac{W}{L})_p = \frac{0.42}{0.3044}$$



- Plot of the DC transfer characteristics (Vout vs Vin) –



Part a)

- We see that the inverter threshold is 1.03V.

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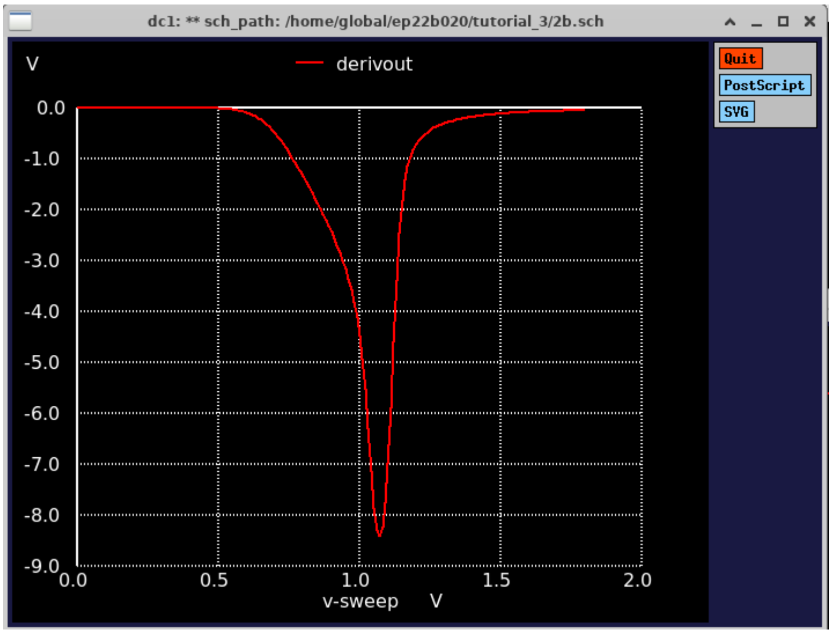
Using SPARSE 1.3 as Direct Linear Solver
 Reference value :  0.00000e+00
No. of Data Rows : 181
vil                 =  7.635257e-01
vih                 =  1.177218e+00
vm                  =  1.027268e+00
n1                  =  1.001355e-01
NML: 0.763526 NMH: 0.622782
Vol:0.100136
ngspice 6 ->
```

Part b)

- Plot of the derivative of Vout vs Vin –



- Note that the value of Vout when Vin = 1.8V is 0.100136V, which is almost the desired 0.1V for the value of V_{OL}.
- NML = 0.763V, NMH = 0.623V.
- Analytically,

$$\mathrm{NML = VIL = Vtn + \frac{kp}{kn}\,(Vout - Vtp)}$$

Approximately,

$$\mathrm{NML} = 0.7 + \frac{0.21}{1.21}\,(1.8 - 0.7) = 0.891\mathrm{V}$$

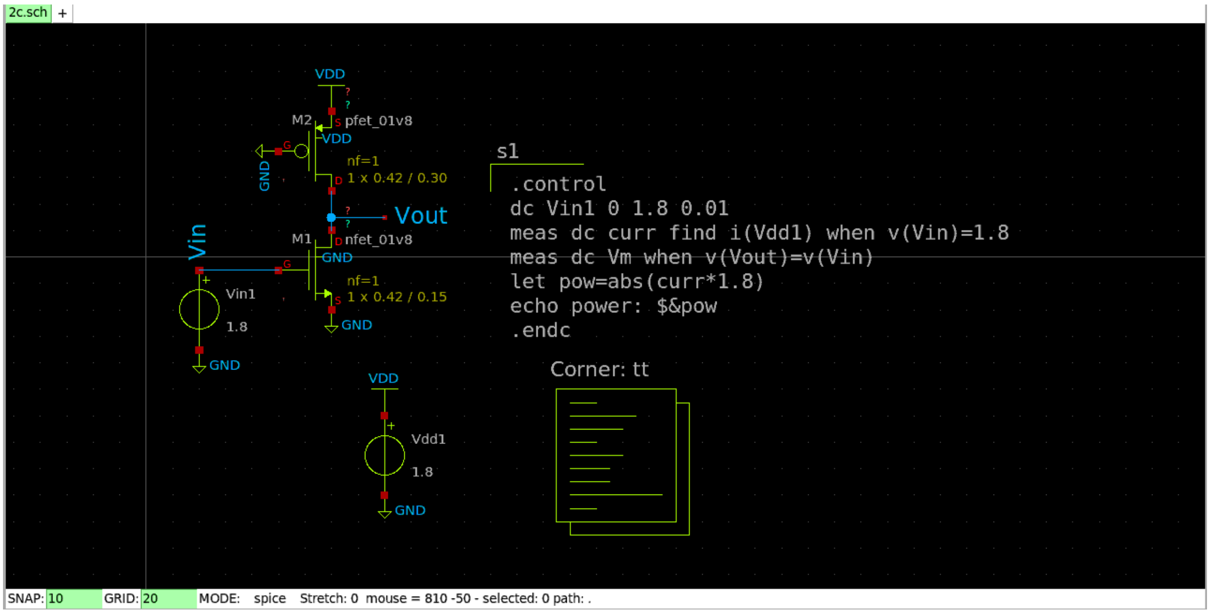
Also,

$$\mathrm{NMH = VDD - \ VIH = VDD - Vtn - \frac{2}{\sqrt{3}}\sqrt{\frac{kp}{kn}}\,(VDD - Vtp)}$$

Which approximately gives

$$\mathrm{NMH} = 1.8 - \ 0.7 - \frac{2}{\sqrt{3}}\sqrt{\frac{0.21}{1.21}}\,(1.8 - 0.7) = 0.571\mathrm{V}$$

Part c)




```
Using SPARSE 1.3 as Direct Linear Solver
 Reference value :  0.00000e+00
No. of Data Rows : 181
curr                 =  -3.420985e-05
vm                   =  1.027268e+00
power: 6.15777E-05
ngspice 6 ->
```

- The simulated value of the power dissipated is 61.578uW.
- Analytically, considering the triode current through the NMOS, we get

$$\mathrm{Ids = kn\left(VDD - Vtn - \frac{Vds}{2}\right)Vds\,(1 + \lambda\,Vds) = 64.05uA \quad (for\ Vds = Vol = 0.1V)}$$

Thus, the power will be I_{ds} x 1.8 = 115.29uW (analytical).