RAMAIAH SKILL ACADEMY

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VLSI-SoC Design

Title

Design and Implementation of RTL to Netlist and Logical equivalence Check for Booth Multiplier

Abstract

This project focuses on designing an optimized Booth Multiplier, widely used in DSP and arithmetic computing applications. The implementation follows a structured flow, including RTL design, functional verification using Synopsys VCS, linting and static analysis with Spyglass, synthesis using Design Compiler, timing verification using PrimeTime, and formal verification using Formality. The design aims to achieve high-speed multiplication with reduced power and area, making it efficient for FPGA and ASIC applications. DFT (Design for Testability) features are incorporated using Synopsys DFT Compiler to enhance manufacturability and test coverage. The Booth multiplication algorithm is chosen due to its ability to reduce the number of partial product additions, significantly improving performance for large operand multiplications. The design is optimized for low-power operation and minimal delay, making it ideal for high-speed DSP applications. The project also includes power-aware synthesis and advanced pipelining techniques to improve the multiplier's efficiency. The verification phase ensures correctness using formal verification and functional simulations, guaranteeing that the final synthesized netlist meets design specifications and industry standards.

Booth Multiplication Algorithm

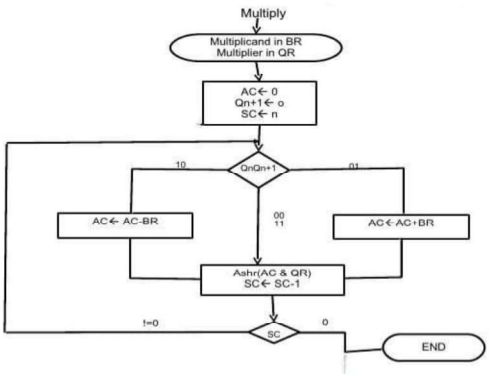

Fig 1: Flow Chart

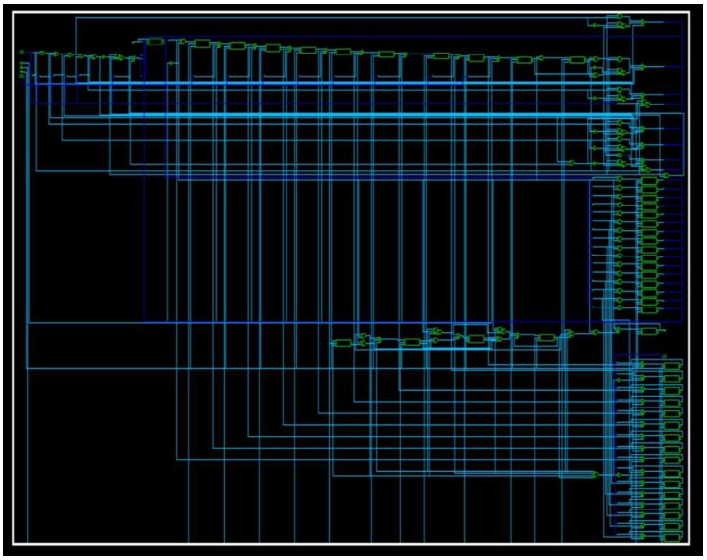

Fig 2: Netlist View

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