



## Amol Pagare

Fourth-Year Dual Degree Student  
Electronic Systems Specialization  
Electrical Engineering Department  
Indian Institute Of Technology, Bombay

+91-9834448080

22b3971@iitb.ac.in

amolpagare035@gmail.com

GitHub Profile

LinkedIn Profile

## INTERNSHIPS

---

### Data Analysis | Thermax Foundation

Analyzed and interpreted data to extract valuable insights and consolidated databases

[Jun '23]

- Database management using SQL and Dashboarding with Tableau

- Implemented **SQL** queries for data refinement and aggregation, ensuring integrity through duplicate elimination.
- Skillfully curated **Tableau**-based data visualization learning modules, showcasing a comprehensive **dashboard** and adeptly transforming diverse datasets into actionable intelligence crucial for informed decision-making processes.

## HACKATHONS

---

### IBM Quantum Challenge'24

IBM Quantum Learning

[May '24 - Jul '24]

- Achieved the IBM Quantum Challenge 2024 certification by successfully completing 5 labs within a timed environment.
- Built quantum circuits and used Qiskit StatevectorSampler for result sampling.
- Developed custom pass managers and scheduling passes for Dynamical Decoupling, and optimized circuits using both traditional and AI-powered methods, comparing performance metrics.
- Designed a Variational Quantum Classifier (VQC), simulated noise impact, and tested on IBM Quantum hardware with error suppression techniques.

### Indian Case Challenge | IIT Kharagpur's Annual Techno-Management Fest

[Jan '24]

India's Premier Business Strategy Case Study competition | Hosted in association with IIT KGP Business Club

- Proposed market strategies for dominance of GPT Builder and GPT Store through structured models and features.
- Developed a revenue model for the GPT Store, emphasizing financial visibility and differentiation from competitors.
- Crafted methods to counter oversaturation and promoted sustainable growth of the GPT Store, ensuring quality and specialization in GPTs by incorporating measures like user ratings, cost-based visibility, and plagiarism checks.
- Conducted feasibility analysis for onboarding an AI chip company, evaluating economic and market synergies, goals, and other metrics.

### Algoswarm | Quanhive

[May '23]

Advanced to round two of the Algorithmic Trading contest during a 24-hour virtual hackathon

- Formulated an appropriate **modeling technique** based on the problem statement involving **Machine Learning**.
- Methodically refined and systematically optimized the selected model, harnessing the insights and patterns within the training dataset to enhance performance and accuracy
- **Backtested** on historical market data with the developed model, successfully yielding an impressive **50% profit** on the initial investment through the trained Alpha

### Bona Consilia Challenge | StrategyCo. Global

[Oct '23]

Participated in a Nationwide Case study Competition, demonstrating problem solving abilities by addressing real-world challenges alongside top-tier talent

- Analyzed and addressed a real-life case problem, meticulously crafting and presenting comprehensive solutions in response to the presented problem statement.

## KEY PROJECTS

---

### EE 451: Supervised Research Exposition | Research Project

[Autumn '25]

Guide: Prof. Laxmeesha Somappa, Department of Electrical Engineering, IIT Bombay

- Implemented a full **RISC-V SoC** around the **KianV (RV32IMA)** core, integrating UART, GPIO, SDRAM, SPI NOR flash, and CLINT timer peripherals with a validated **memory map** and interconnect architecture.
- Implemented the multicycle **FSM-based CPU**, full **RISC-V privileged modes**, and **SV32** virtual memory for Linux support and built the FPGA top-level design and generated/deployed the **bitstream** on the target board.
- Brought up the boot flow involving **OpenSBI** and **U-Boot / Linux kernel**, enabling full system initialization.
- Successfully **booted Linux kernel on FPGA**, demonstrating timer-driven scheduling, and peripheral I/O functionality.

## EE 669: VLSI Technology | Coursework

[Autumn '25]

Guide: Prof. Anil Kottantharayil, Department of Electrical Engineering, IIT Bombay

- Conducted and analyzed silicon oxidation, diffusion, and implantation workflows by simulating process steps with **Sentaurus Process**, NanoHUB, and PV Lighthouse to evaluate device-level impacts.
- Analyzed **Deal–Grove/Massoud models**, dopant diffusion trends, and junction behavior across process conditions.
- Optimized **lithography** by simulating **standing-wave and proximity** effects, refining **PEB** and **ARC** parameters.
- Investigated **CMOS** process integration including trench oxidation, gate-stack formation, and shallow-junction design.
- Evaluated **SRIM/TRIM** implantation profiles and Sentaurus decks for tilt, rotation, PAI, and channeling suppression.
- Analyzed semiconductor fabrication steps up to **3nm node**, including **FinFET** and **GAAFET** device technologies.

## EE 709: Testing and Verification of VLSI Circuits | Coursework

[Autumn '25]

Guide: Prof. Madhav Desai, Department of Electrical Engineering, IIT Bombay

- Modeled Boolean functions and FSMs using **cmu bdd** for equivalence checking and functional analysis and verification.
- Implemented **Mealy-machine** encodings and optimized **next-state/output** logic using **don't-care** conditions.
- Analyzed invertibility and impossible output vectors for multi-bit Boolean maps using structured **ROBDD** exploration.
- Performed **ATPG** using **minisat** to generate distinguishing vectors via CNF formulations of good and faulty circuit.
- Executed **deductive fault simulation** to identify **stuck-at faults**, propagation paths, and output detectability.

## EE 748: Advanced Topics in Computer Architecture | Coursework

[Autumn '25]

Guide: Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay

- Analyzed **SPEC 2006** workloads on **gem5** and classified them using MPKI, APKI, LLC sensitivity, and IPC trends.
- Designed/Evaluated custom **LLC replacement policies** (LRU\_slow, LRU\_6) modifying promotion/insertion rules.
- Implemented **guided branch prediction** with **RVCF**-style leading/trailing-core hints to reduce mispredictions.
- Proposed **GPU** optimization combining **NL-DWF**, **register prefetching** reducing RF conflicts improving SIMD utilization.

## EE 789: Algorithmic Design of Digital Systems | Coursework

[Spring '25]

Guide: Prof. Madhav Desai, Department of Electrical Engineering, IIT Bombay

- Developed **matrix multiplication** (unrolled dot-product, block-based, etc) using **Algorithmic Assembly** Language.
- Designed **VHDL** shift/add multipliers, parallel multipliers, dividers, and sqrt units—with full **testbench** validation.
- Implemented a  $4 \times 4$  output-queued switch with fair arbitration, structured queuing, and control/data-path separation.
- Applied **Aa-to-hardware** compilation concepts including elastic pipelines, guarded statements, and deterministic virtual circuits.
- Translated **Aa** descriptions into synthesizable VHDL using **AHIR libraries** ensuring cycle-accurate behavior.

## EE 705: VLSI Design Lab | Course Project

[Spring '25]

Guide: Prof. Laxmeesha Somappa, Department of Electrical Engineering, IIT Bombay

- Designed and verified a **32-bit Brent–Kung adder**, 16-bit Dadda multiplier, and 8-bit barrel shifter using **Verilog**.
- Integrated controllers, BRAM interfaces, and VIO to build functional arithmetic subsystems on **PYNQ FPGA**.
- Developed ALU\_DECODE logic for **RISC-V 32IM** including arithmetic ops, shifts, multipliers, and decode circuitry.
- Implemented **ICACHE/DCACHE** modules and validated correctness in a full RISC-V pipeline and built a complete **RISCV SoC** integrating ALU, decode, LSU, CSR, AXI, UART, and GPIO with post-implementation verification.

## EE 739: Processor Design | Course Project

[Spring '25]

Guide: Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay

- Implemented a pipelined **OoO superscalar processor** with ALU/LSU pipelines, ROB, and Reservation Stations.
- Designed fetch, decode, issue, execute, and writeback stages with **hazard detection**, stall/flush logic, forwarding.
- Developed **ARF/RRF**-based physical register management and integrated **in-order commit** via a complete ROB.
- Built and verified instruction scheduling and dispatch using reservation stations and load buffers and constructed an **in-order superscalar** processor in **VHDL** using scoreboard-based hazard tracking and parallel execution units.

## EE 344: Electronic Design Lab | Course Project

[Spring '25]

Guide: Prof. Siddharth Tallur, Department of Electrical Engineering, IIT Bombay

- Developed **EcoSync 8X**, a dsPIC33A-based ultrasonic SHM system with an 8-channel configurable Tx/Rx interface.
- Implemented 100 kHz **excitation and sensing** using Hanning-windowed pulses and instrumentation-grade amplification.
- Programmed and integrated **dsPIC33** and **ESP32** modules for command control, data capture, wireless communication.
- Designed the system **PCB in KiCAD** and fabricated a custom laser-cut enclosure for complete hardware integration.

## **EE 671: VLSI Design | Course Project**

[Autumn '24]

*Guide: Prof. Lakshmeesha Somappa, Department of Electrical Engineering, IIT Bombay*

- Created the **gds-II** file for Laplacian filter in Verilog for **edge detection** on 16x16 grayscale images using 3x3 kernel.
- Developed Image Matrix-Operation, **Kogge-Stone adder**, multiplexers blocks for edge handling, and pixel clipping.
- Synthesized design to obtain **RTL** logic and performed **physical design** using OpenLane open-source IC design flow.
- Executed synthesis, floorplan, placement, CTS, routing, STA, Magic DRC, LVS, antenna check, and SPICE export.
- Created the GDS-2 layout, extracted **liberty** and **LEF** files, and matched **pre-synthesis** and **post-routing** results.

## **EE 677: VLSI CAD | Course Project**

[Autumn '24]

*Guide: Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*

- Synthesized algorithm for reversible logic circuits using **PPRM** expansions and **Toffoli gate** networks for optimization
- Utilized priority-based **search trees** and heuristics to explore and refine solutions, reducing terms in PPRM expansions.
- Validated scalable designs ensuring high-performance circuit synthesis with minimal **control bits**, optimizing efficiency.
- Designed a **circuit simulator** to process a **Verilog/EDIF** netlist and input vector, generating output values.

## **EE 678: Wavelets and multirate-Digital Signal Processing | Course Project**

[Autumn '24]

*Guide: Prof. Vikram Gadre, Department of Electrical Engineering, IIT Bombay*

- Developed **segmentation** approach integrating **DWT** into **U-Net** to preserve high-freq details in multi-class segmentation.
- Replaced downsampling/upsampling with **DWT/IDWT**, boosting feature retention through DWT-based skip connections.
- Experimented with DWT configurations and wavelet types, optimizing the architecture under computational constraints.
- Achieved superior **DICE** scores and **precision** with dual DWT-IDWT mechanism at Block 4, validating the effectiveness.

## **EE 309: CISC and RISC Processor Design | Course Project**

[Spring '24]

*Guide: Prof. Virendra Singh, Department of Electrical Engineering, IIT Bombay*

- Designed and implemented a 16-bit **RISC pipelined** microprocessor in VHDL, incorporating complete hazard mitigation techniques such as pipeline stalling, data forwarding and branch prediction techniques.
- Executed 26 instructions across **six pipeline stages**, categorized into different instruction sets.
- Designed decoders, including the instruction decoder, to generate **control signals** for various hardware components, and developed a **hazard detector** to identify execution hazards during multiple instruction processing.
- Utilized the **Intel Max-10** board for comprehensive FPGA-based demonstration and testing of the microprocessor.

## **DH 607: Introduction to Computational-MultiOmnics | Course Project**

[Autumn '25]

*Guide: Prof. Saket Choudhary, Koita Centre for Digital Health, IIT Bombay*

- Applied **probability**, Bayesian inference, and stochastic models, and implemented core algorithms including **BWT**, **Needleman–Wunsch**, suffix structures for biological sequence analysis.
- Built multi-omics pipelines integrating **genomic variants miRNA networks** to study dysregulation in *M. tuberculosis*.
- Modeled structural impacts of drug-resistance mutations using **Boltz docking** to assess altered binding mechanisms.

## **8051 Microprocessor Coding | Course Project**

[Spring '24]

*Guide: Prof. Nikhil Karamchandani, Department of Electrical Engineering, IIT Bombay*

- Implemented ATM functionality using a keyboard connected to a **PT-51 Board**, communicating via **UART**.
- Implemented musical notes ("sa-re-ga") on a PT-51 board using **timers and interrupts** for varied frequencies.
- Implemented a low-pass filter on the PT-51 board for DSP, simulated with Flip software, and interfaced with keypad.

## **Analog Circuit Design | Course Project**

[Spring '24]

*Guide: Prof. Anil Kottanharayil, Department of Electrical Engineering, IIT Bombay*

- Utilized **TL084 opamps**, **MC14007 MOSFETs**, and BJTs to design filters, oscillators, and current mirrors. Calculated critical frequencies and Q factors for an active band-pass filter for optimal performance.
- Simulated a complete logarithmic amplifier on **LTS spice** and designed all the above circuits virtually in **XCircuit**.

## **Implementation of Electrocardiogram | Course Project**

[Spring '24]

*Guide: Prof. Anil Kottanharayil, Department of Electrical Engineering, IIT Bombay*

- Designed and built an **ECG** front-end amplifier to capture electrical signals from the heart.
- Implemented low-pass filtering to remove high-frequency noise and 50 Hz **notch filter** to reduce noise interference.
- Successfully captured the ECG signal using provided probes and the constructed amplifier.

## **Option Pricing Models and their Accuracy**

[Jun'24]

*Finsearch | Finance Club, IIT Bombay*

- Studied options markets and pricing models, exploring the **Binomial Model**, Black-Scholes Model, and Monte Carlo Simulations for options pricing, while delving into the fundamental mathematics using Martingales and Ito's Lemma.

- Explored the Binomial Model, Black-Scholes Model, and Monte Carlo Simulations for options pricing.
- Delved deep into the fundamentals of the models using Martingales and Ito's Lemma.
- Implemented the **Black-Scholes Model** in Python to calculate option prices with given parameters.
- Conducted **Monte Carlo Simulations** to forecast option prices and backtested the models in different markets.

### Implementation of Snake Game and Chess Engine

[May'24]

*Summer of Code'24 | Web and Coding Club, IIT Bombay*

- Explored N-armed bandits, **Markov Decision Processes** (MDPs), and Dynamic Programming for RL.
- Developed the **Monte Carlo ES algorithm** for an MDP and solved Tic Tac Toe using minimax and an RL algorithm.
- Implemented the **Double Deep Q-Network** (DDQN) algorithm, drawing on techniques from Grokking's textbook.
- Implemented a research paper to develop a Chess Engine using advanced Deep Reinforcement Learning techniques.

### Quantum Computing, Information and Technologies

[May'24]

*Summer of Science'24 | Maths and Physics Club, IIT Bombay*

- Explored the **CSHS game**, teleportation, and superdense coding, with a focus on variational algorithm design.
- Mastered the **Query Model**, learned the Deutsch, Deutsch-Jozsa, and **Bernstein-Vazirani** algorithms.
- Studied **advanced algorithms** including Simon's, Shor's, and **Grover's**, mastering efficient strategies for each.
- Explored **Variation Algorithms** such as Variational Quantum Eigensolver (VQE), Subspace Search VQE (SSVQE), Variational Quantum Deflation (VQD), and Quantum Sampling Regression (QSR).

## POSITIONS OF RESPONSIBILITY

---

### Media Secretary | Electrical Engineering Students' Association

[Jun '23 - Apr '24]

*EESA, Department of Electrical Engineering, IIT Bombay*

- Played an instrumental role in strategizing, **coordinating**, and executing EESA events and collaborated as a key member of a 12-person team driving department-wide event planning and implementation
- Grew a social media account with **18k+ followers** and designed thematic posters for all EESA events
- Actively engaged in organizing events for the 2-day Electrical Department Fest 'Impulse,' including Alumni Networking, Workshops, Media Work, Formals Night, and Holi Night.
- Curated social media content, significantly increasing publicity by multiple folds in the Institute.

## TECHNICAL SKILLS

---

Programming	Verilog, VHDL, SQL, Python, Assembly, Embedded C, C/C++, Algorithmic Assembly (Aa)
Software	Vivado, Sentaurus Process, Synopsys, TRIM/SRIM, Gem5 Simulator, CMUBDD, Minisat, R Studio, MPLAB, MATLAB, Git, Arduino, Quartus, Atmel Flip, Keil $\mu$ Vision 5, Tableau, AutoDesk Fusion 360, MySQL Workbench, LTSpice, RealTerm
Machine Learning	TensorFlow, Keras, PyTorch, Scikit-Learn
Python Libraries	NumPy, Pandas, Matplotlib, Seaborn, SciPy, OpenCV, Gym
Miscellaneous	LAT $\mathrm{\acute{E}}\mathrm{X}$ , Qiskit, DaVinci Resolve, Google Colab, Miro, Figma

## KEY COURSES UNDERTAKEN

---

Electrical Engineering	VLSI Technology, Testing and Verification of VLSI Circuits, Advanced Topics in Computer Architecture, VLSI Design, VLSI CAD, Algorithmic Design of Digital Systems, Processor Design, Computer Architecture for Performance and Security, VLSI Design Lab, Wavelets, Analog Circuits, Digital Systems, Digital Systems Lab, Signals and Systems, Electronic Design Lab, Communications System-I, Artificial Intelligence and Data Science,
Mathematics	Calculus, Linear Algebra, Differential Equations, Probability and Random Processes

## EXTRACURRICULARS

---

- Attained **9th place** in the **All India Britannica Conquest Olympiad**, showcasing strong General Knowledge.
- Secured **2nd place** in an Inter School Animation competition held in Pune, showcasing proficiency in **Scratch**.
- Ranked **3rd** in 'Auction Wars', a game theory-based **asset management** competition by **Consult Club, IITB**.
- Earned the '**Basics of Quantum Information**' Badge issued by **IBM Quantum Learning**.
- Achieved '**IBM Quantum Challenge 2024 Achievement**' by completing all 5 labs within the allotted time.
- Advanced to the **Second round** of an Algorithmic Trading Competition hosted by **Quanthive**.