EE DEPARTMENT, IIT BOMBAY

20TH FEB 2025

TUE - 08

MILESTONE - 2

STRUCTURAL HEALTH MONITORING SYSTEM USING DSPIC33A

TABLE OF CONTENT

REVIEW OF MILESTONE - 1

- Efficient work distribution of components for better understanding and deeper analysis, schematic making etc.
- Do extensive testing for each components and then use.
- Power amplifier could not amplify to 100Vpp at 150MHz(our operating frequency) hence we need to change it.
- SMPS was not isolated power supply(AC side and DC side should be separated) hence we need to also change it.
- For Pulse C setting we required a Clipping circuit to reject the unwanted forthcoming high voltage signal(basically our sent signal) to burn our ADC

OVERVIEW OF PROJECT PLAN MANAGMENT

- PCB - Plan of Action
  - 1. Component Allocation
  - 2. Reading of Datasheets
  - 3. Simulation and Obtaining Peripheral Values
  - 4. Knowledge Transfer
  - 5. Designed Schematic

- ComSol Simulation - Plan of Action
  - 1. Attachment of PZT Sensor
  - 2. Generation of Hanning Pulse
  - 3. Excitation of PZT in Shear Mode
  - 4. Plotted Results for Ideal Aluminum Plating

OVERVIEW OF PROJECT PLAN MANAGMENT

- Testing Plan of Action:
  - Reading the datasheet for DsPIC and the testing components, and them writing Embedded C code for testing components.
  - Components tested include ADC, DAC, and INA.

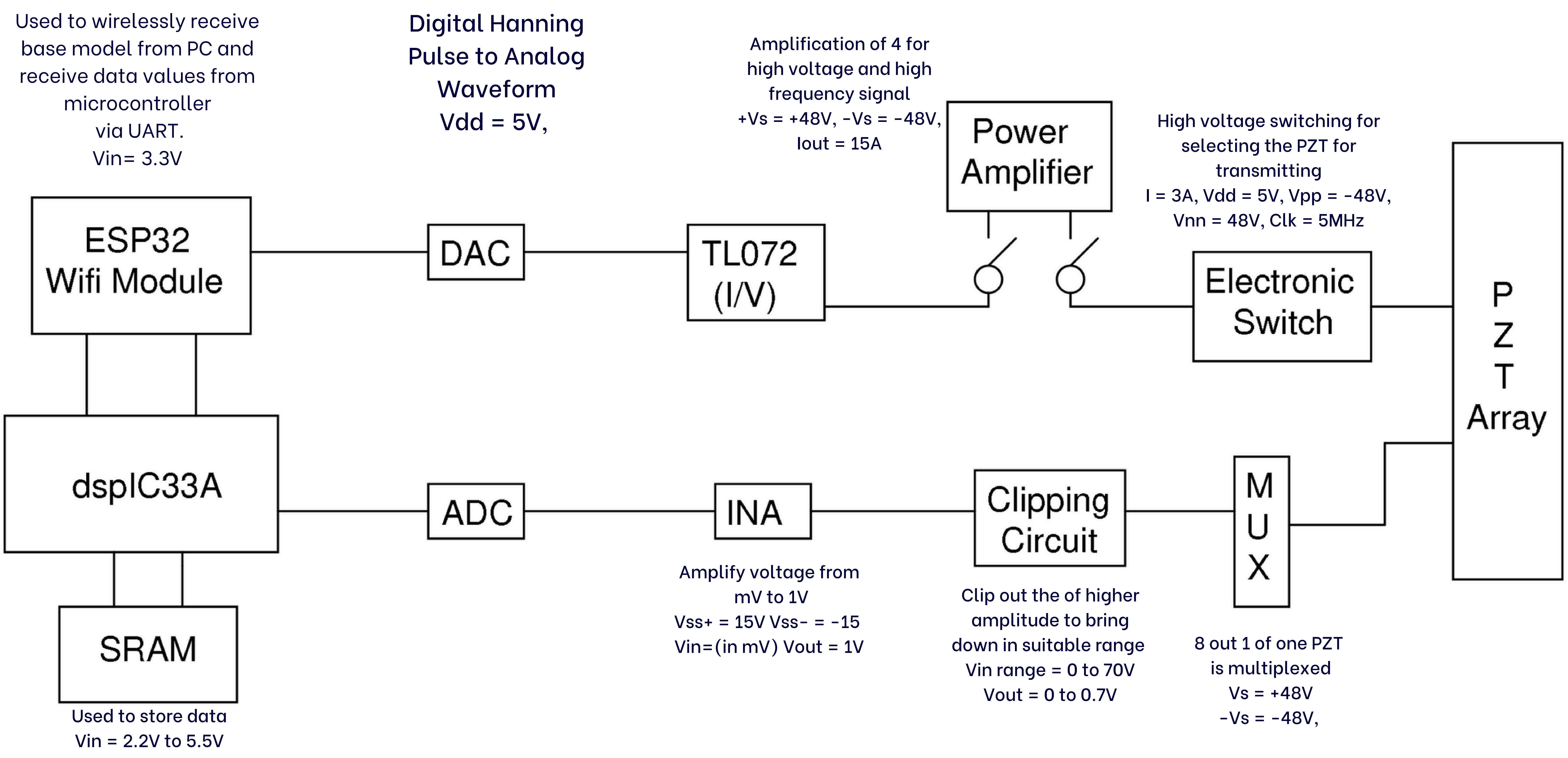
DOCUMENTATION

- For the clipping circuit, we initially used operational amplifiers (op-amps) to generate a voltage of less than 2V, as confirmed by our simulation results.
- This voltage level was safer for the ADC.
- However, after consulting with Sheetal Mam, we were advised to simplify the design by using diodes instead.
- Consequently, we created a diode-based clipping circuit, with one diode placed before the instrumentation amplifier (INA) and another placed after it.
- Our simulations confirmed that this setup also worked effectively.

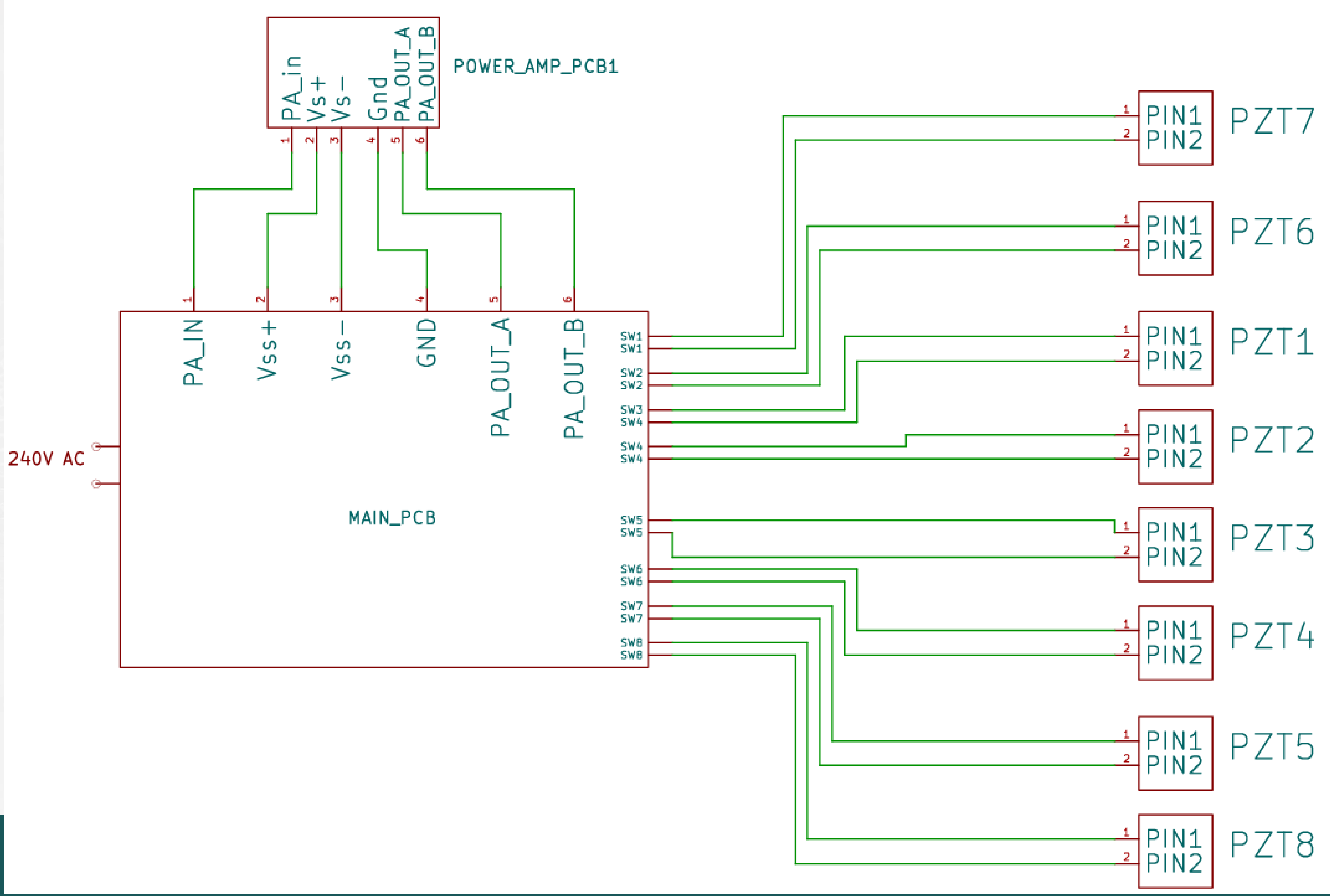
DOCUMENTATION

- Earlier, we were using LM741 to generate the Hanning pulse, which has a very low slew rate of 0.
- After a review, we were advised to use an operational amplifier (op-amp) with a high slew rate of approximately 20 V/µs.
- As a result, we switched to TL072CP, which has a slew rate of 20 V/µs.
- All other PCB-related simulations and COMSOL tasks were successfully completed, which will be covered in the upcoming slides.

BLOCK DIAGRAM

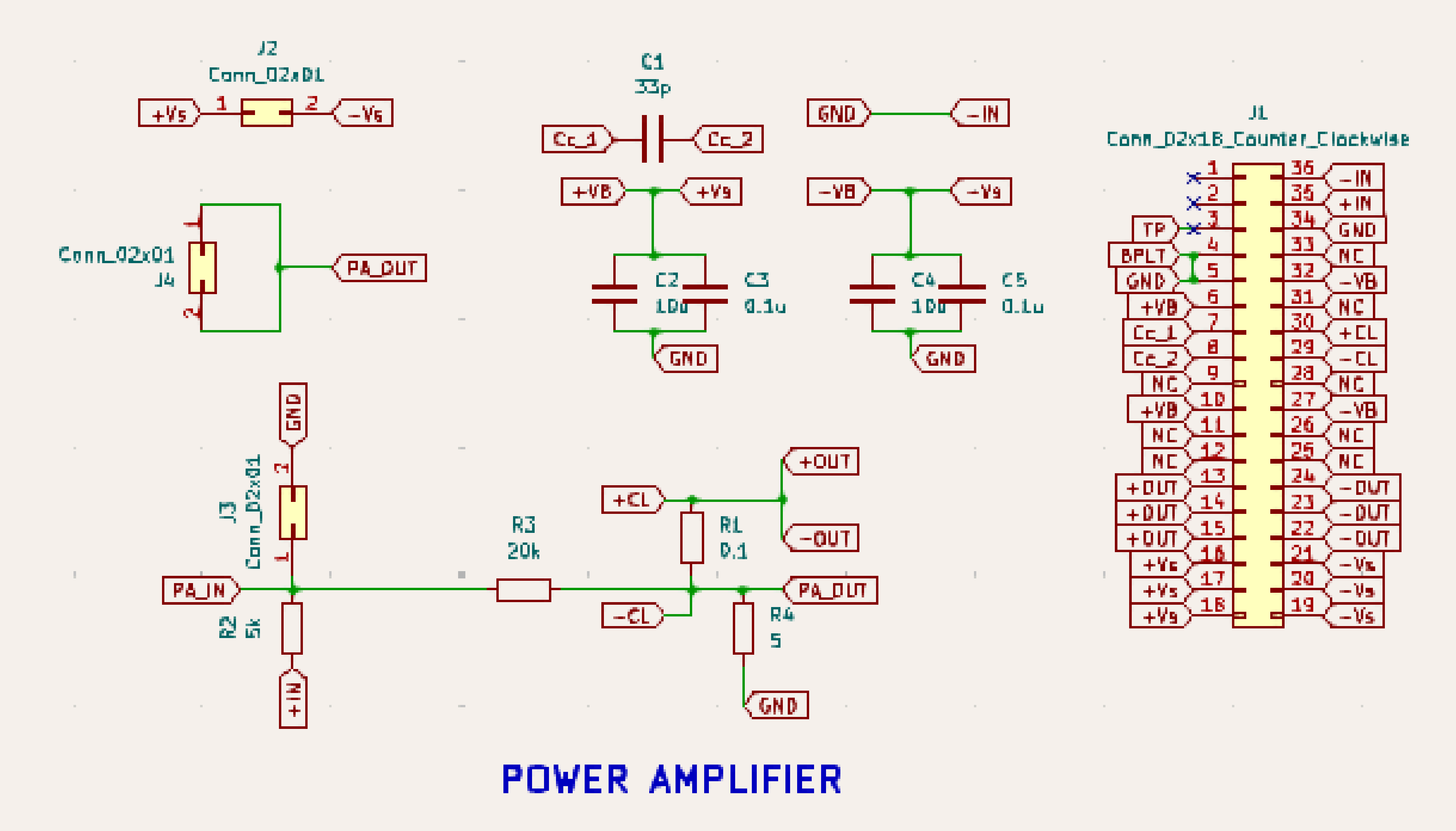


WIRING DIAGRAM

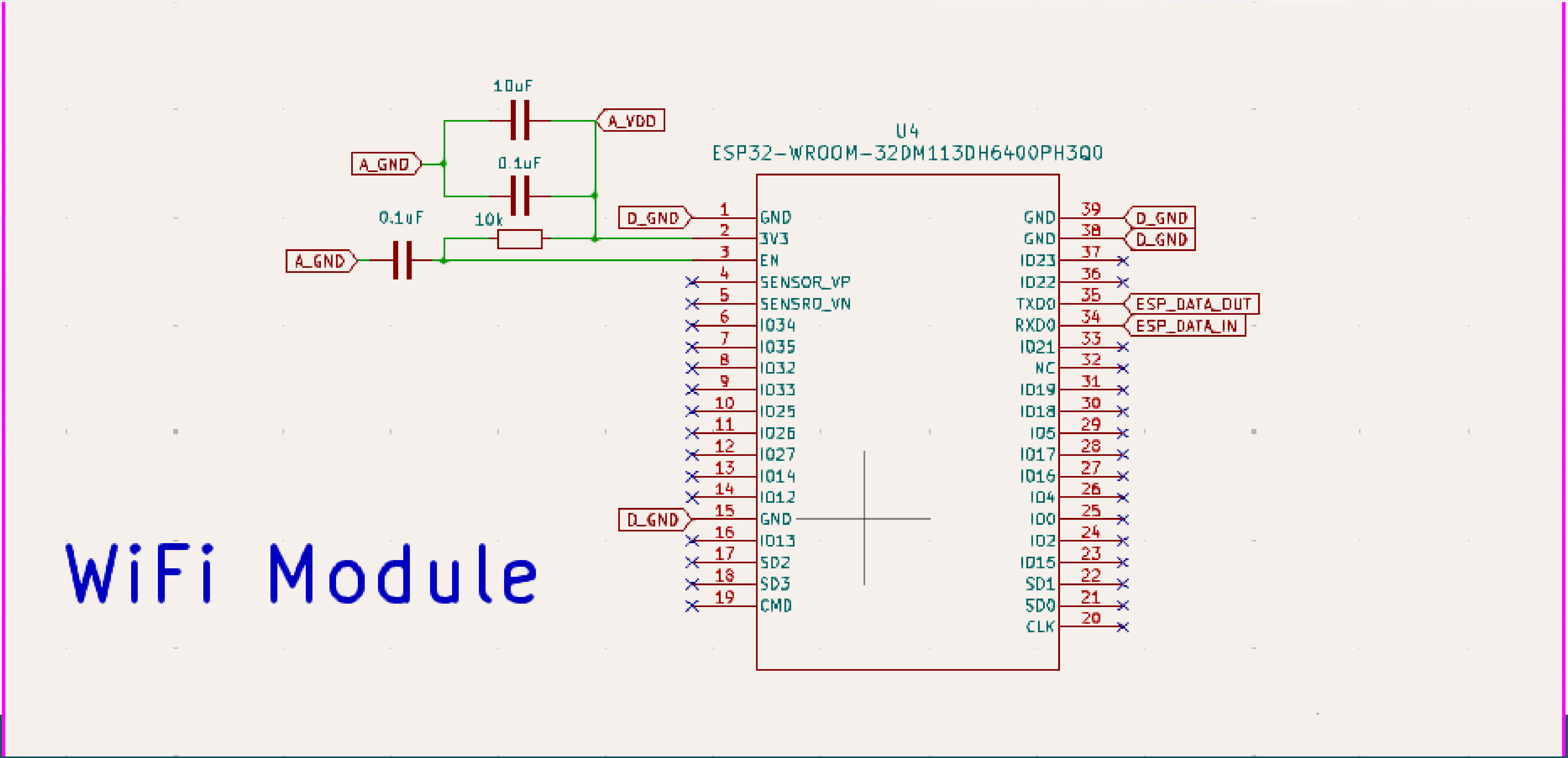


SCHEMATIC MODULES

POWER AMPLIFIER

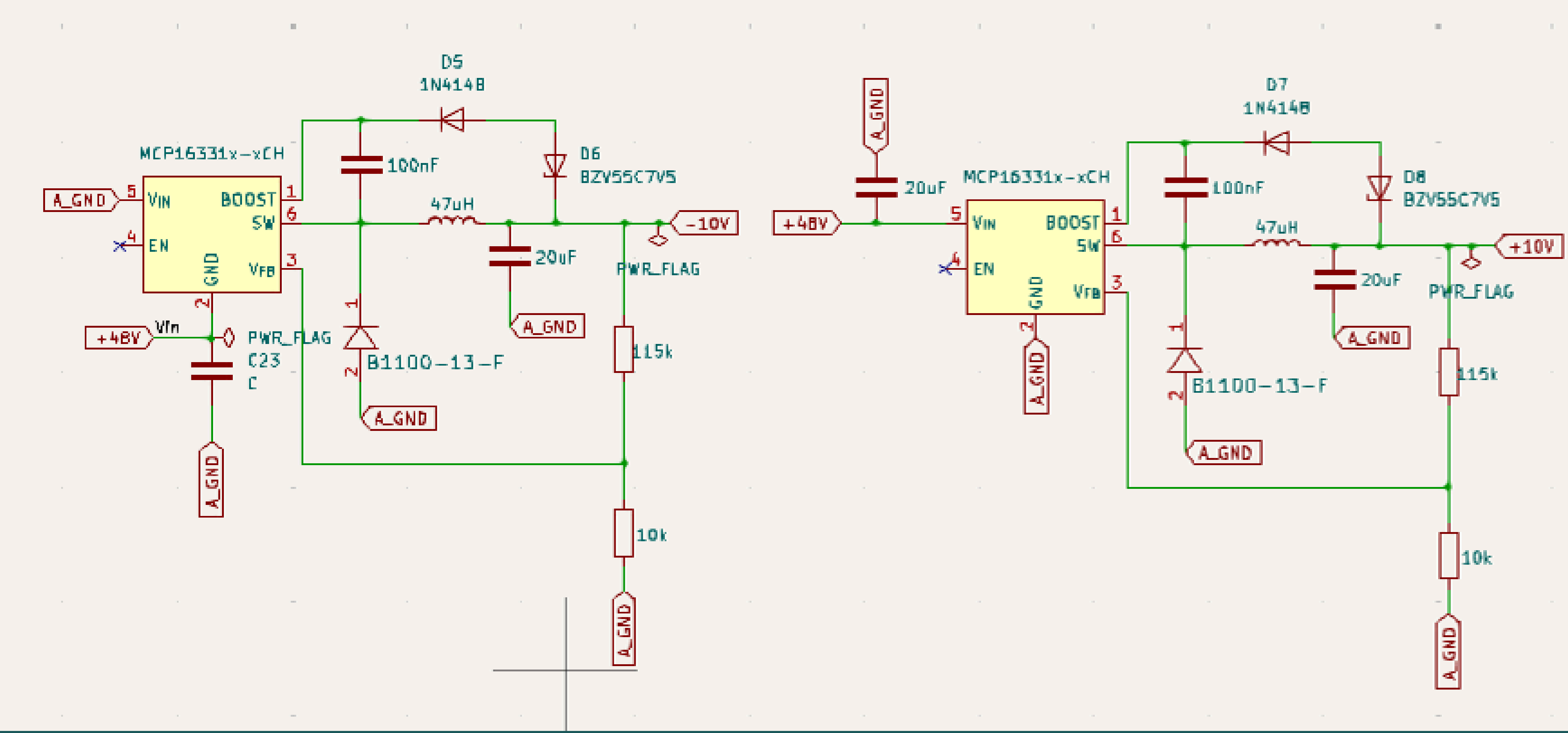


WIFI MODULE

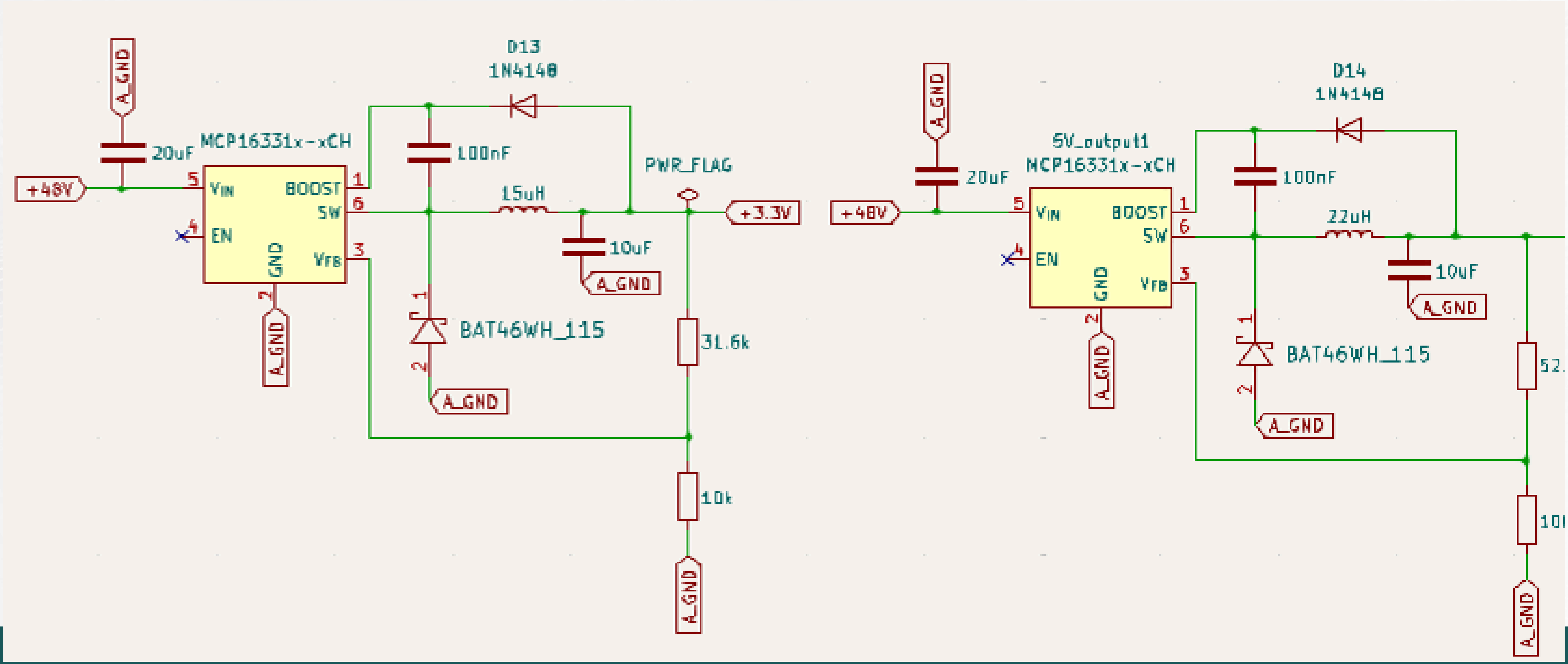


10uF
A_VDD
A_GND
0.1uF
0.1uF
10k
A_GND
U4
ESP32-WROOM-32DM113DH6400PH3Q0
D_GND
D_GND
1 GND
2 3V3
3 EN
4 SENSOR_VP
5 SENSRO_VN
6 IO34
7 IO35
8 IO32
9 IO33
10 IO25
11 IO26
12 IO27
13 IO14
14 IO12
15 GND
16 IO13
17 SD2
18 SD3
19 CMD
GND 39
GND 38
IO23 37
IO22 36
TXD0 35
RXD0 34
IO21 33
NC 32
IO19 31
IO18 30
IO5 29
IO17 28
IO16 27
IO4 26
IO0 25
IO2 24
IO15 23
SD1 22
SD0 21
CLK 20
D_GND
D_GND
ESP_DATA_OUT
ESP_DATA_IN
WiFi Module

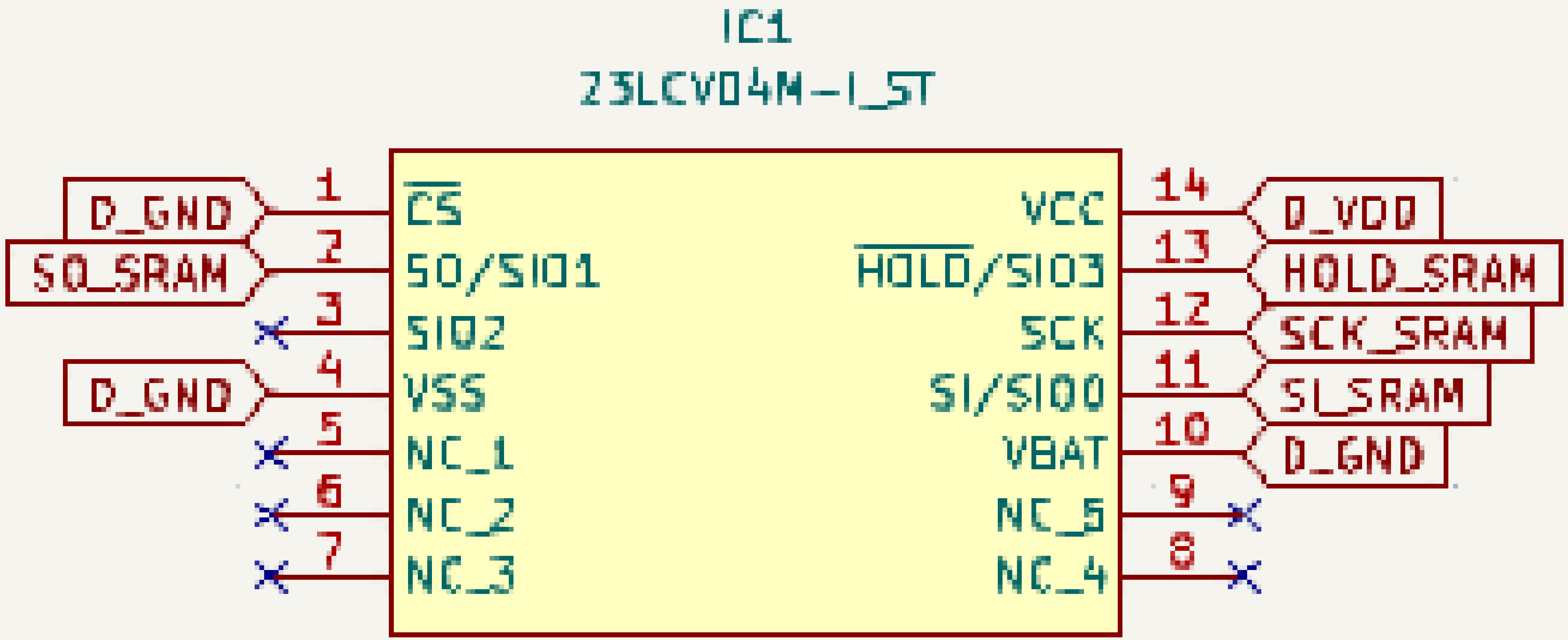
POWER SUPPLY - 1



POWER SUPPLY - 2

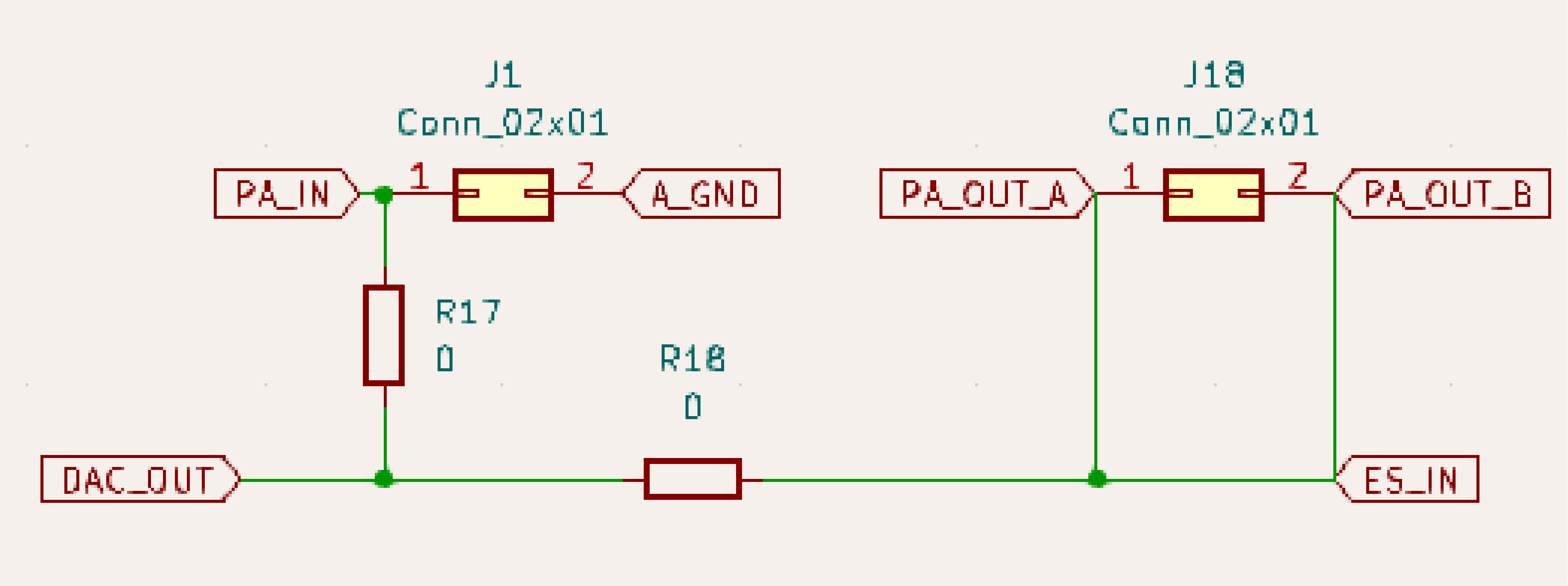


MEMORY (SRAM)

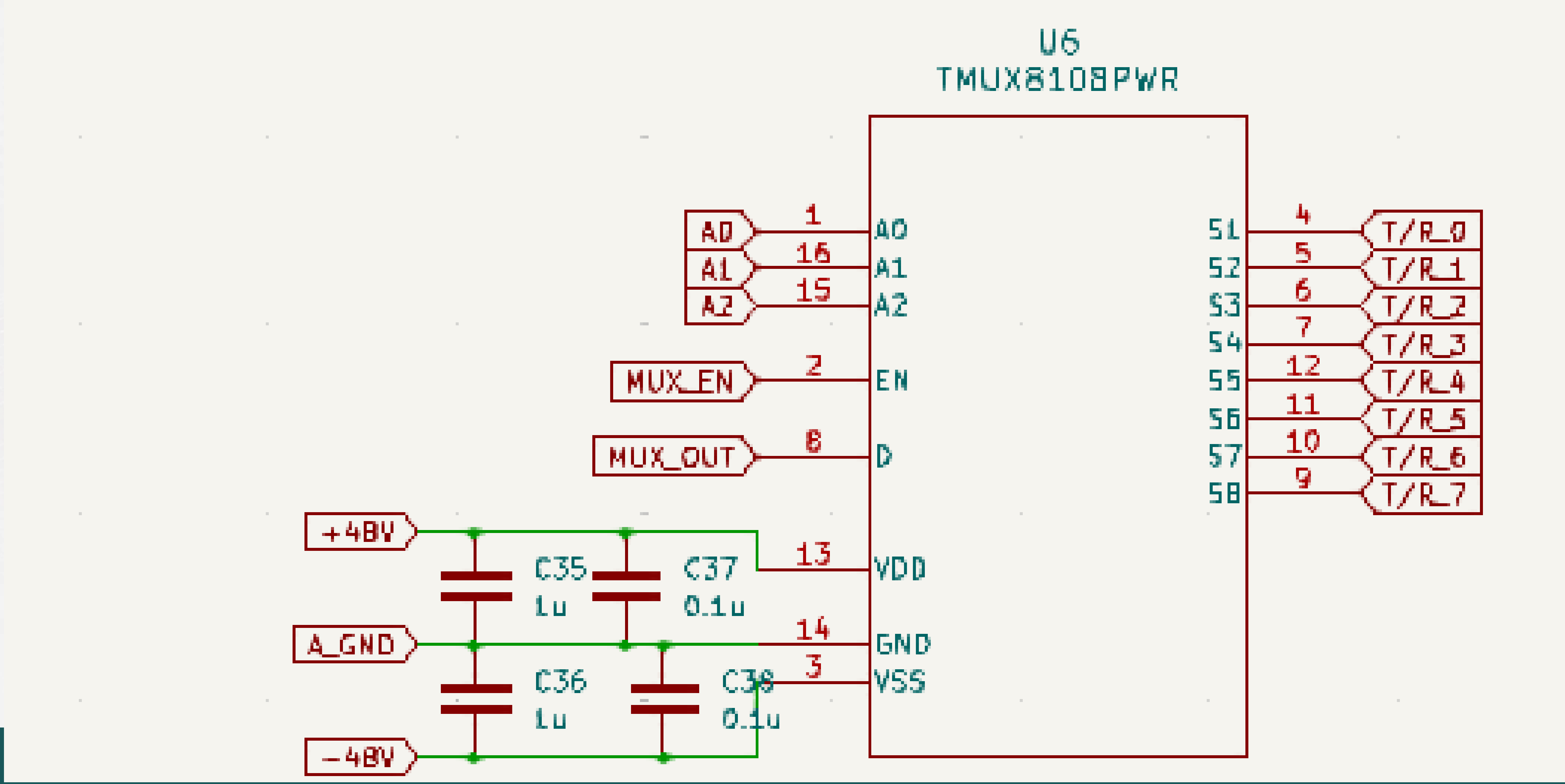


IC1
23LCV04M-I_ST
D_GND
SO_SRAM
D_GND
1
2
3
4
5
6
7
CS
SO/SIO1
SIO2
VSS
NC_1
NC_2
NC_3
VCC
HOLD/SIO3
SCK
SI/SIO0
VBAT
NC_5
NC_4
14
13
12
11
10
9
8
D_VDD
HOLD_SRAM
SCK_SRAM
SI_SRAM
D_GND

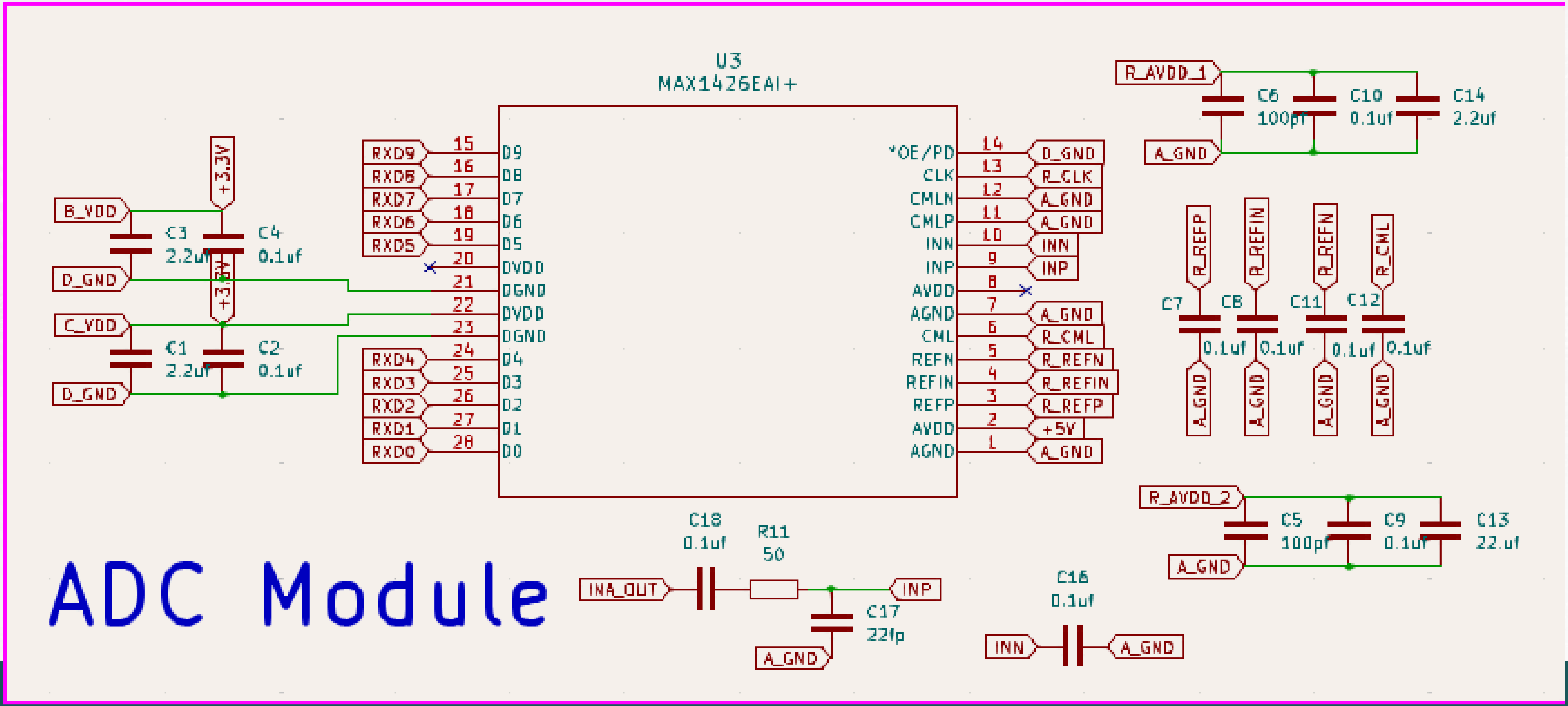
POWER AMPLIFIER SELECT SWITCH



MULTIPLEXER

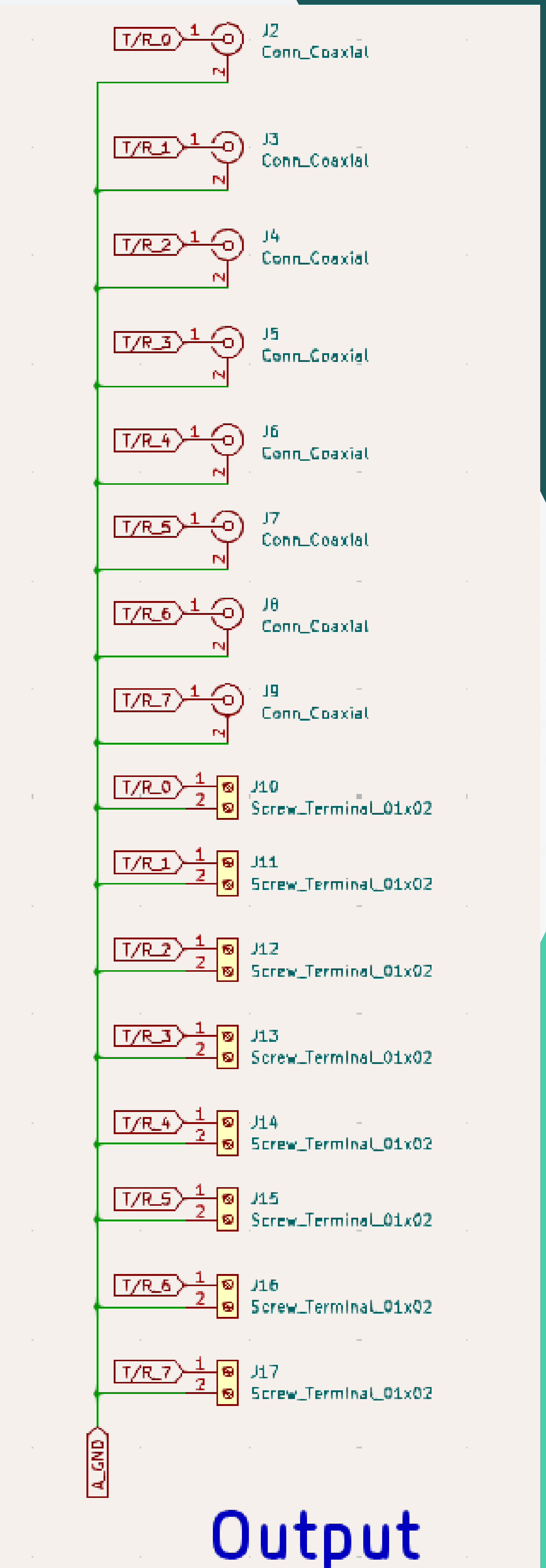


ADC MODULE

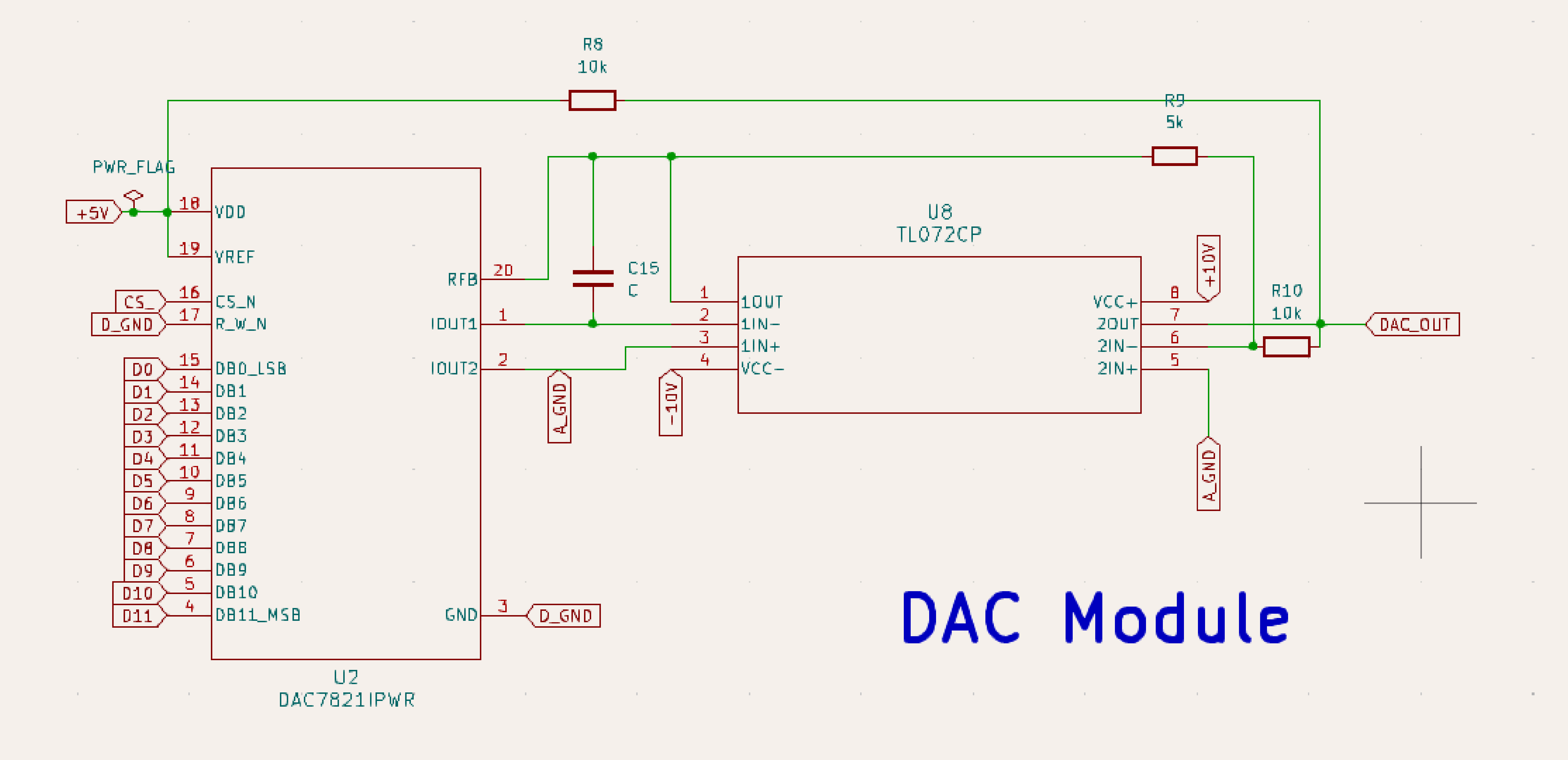


U3
MAX1426EAI+
RXD9
RXD8
RXD7
RXD6
RXD5
RXD4
RXD3
RXD2
RXD1
RXD0
D9
D8
D7
D6
D5
DVDD
DGND
DVDD
DGND
D4
D3
D2
D1
D0
*OE/PD
CLK
CMLN
CMLP
INN
INP
AVDD
AGND
CML
REFN
REFIN
REFP
AVDD
AGND
D_GND
R_CLK
A_GND
INN
INP
R_CML
R_REFN
R_REFIN
R_REFP
+5V
B_VDD
C_VDD
+3.3V
C3
2.2uf
C4
0.1uf
C1
2.2uf
C2
0.1uf
R_AVDD_1
C6
100pf
C10
0.1uf
C14
2.2uf
R_REFP
R_REFIN
R_REFN
R_CML
C7
C8
C11
C12
0.1uf
R_AVDD_2
C5
100pf
C9
0.1uf
C13
22.uf
ADC Module
INA_OUT
C18
0.1uf
R11
50
C17
22fp
C16
0.1uf

OUTPUT
BNC AND SCREW



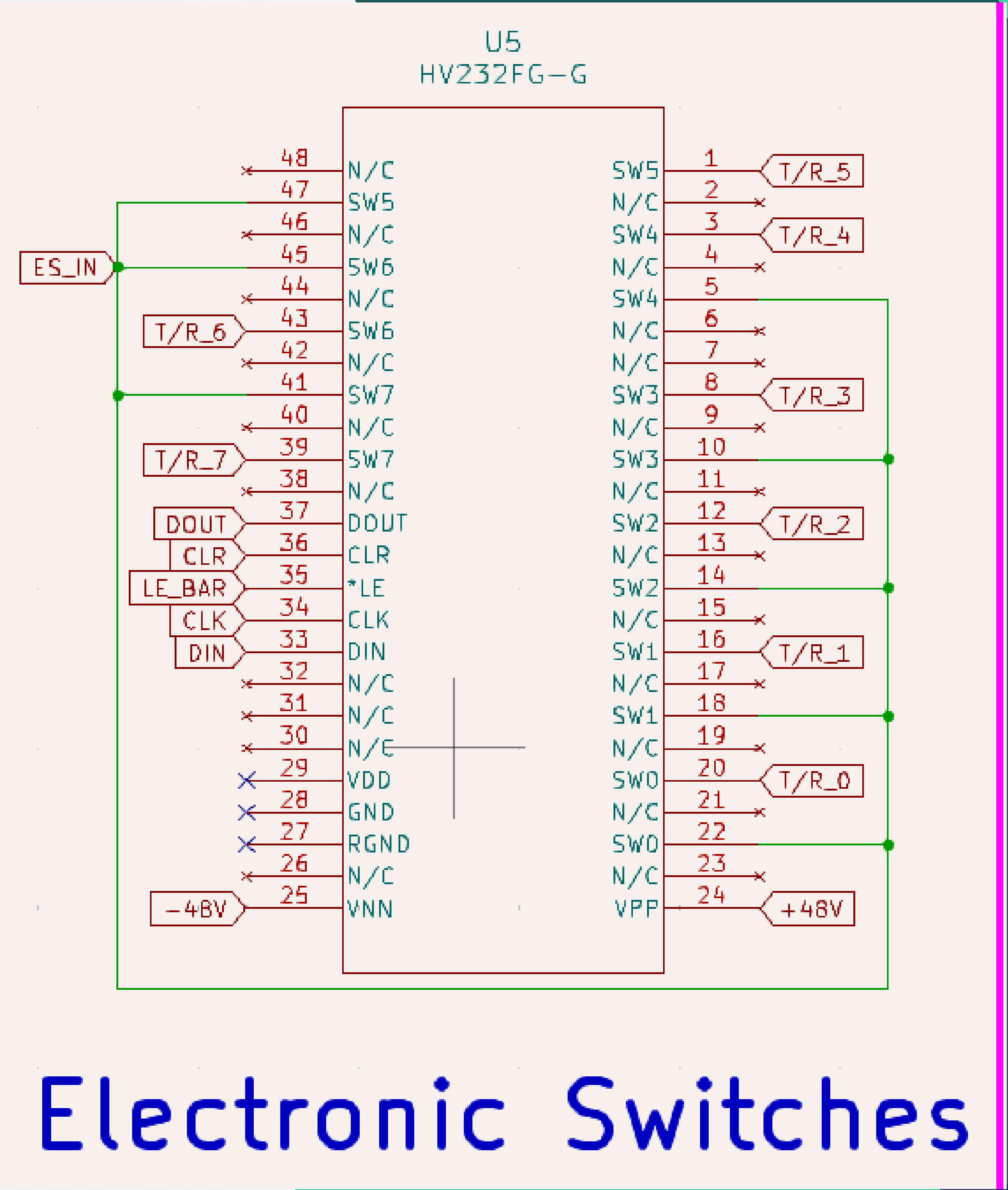
DAC MODULE



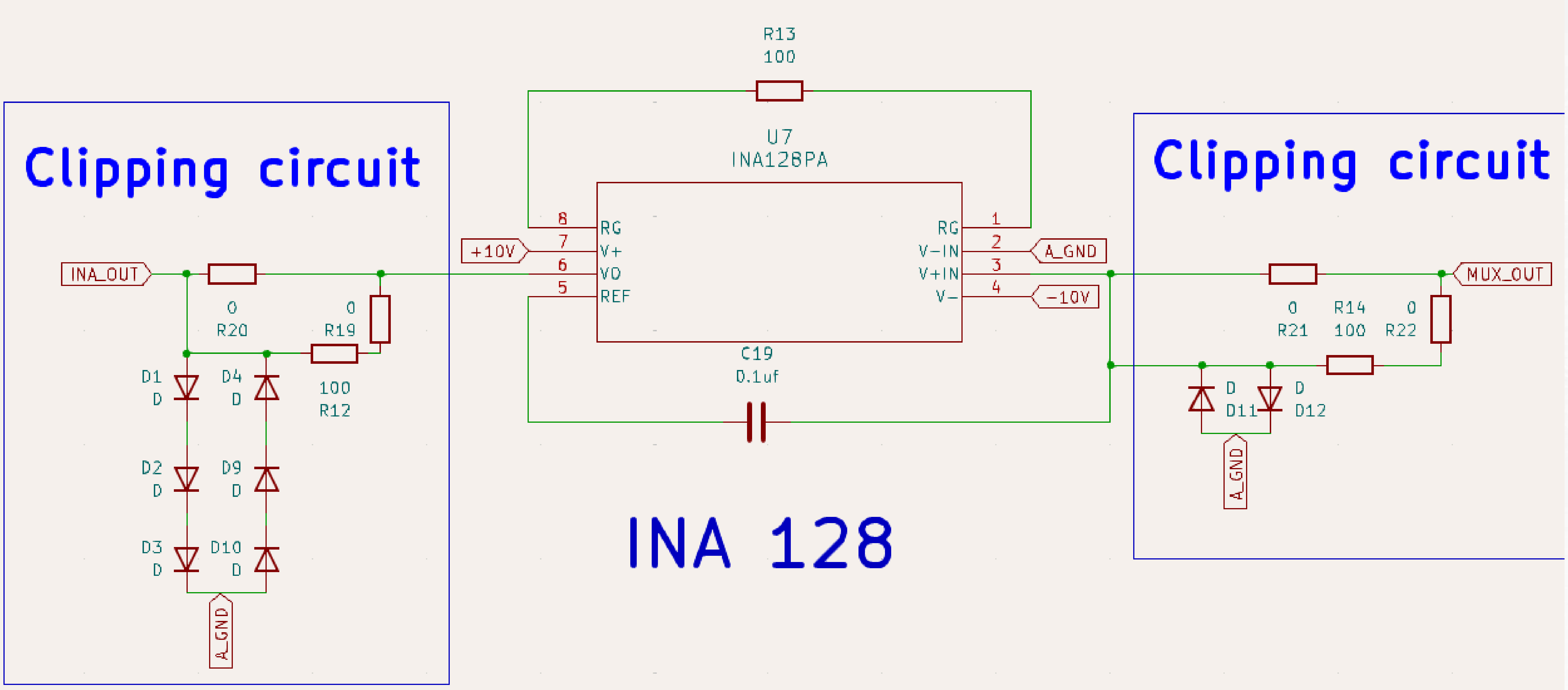
R8
10k
R9
5k
PWR_FLAG
+5V
18
VDD
19
VREF
CS_
16
CS_N
D_GND
17
R_W_N
D0
15
DB0_LSB
D1
14
DB1
D2
13
DB2
D3
12
DB3
D4
11
DB4
D5
10
DB5
D6
9
DB6
D7
8
DB7
D8
7
DB8
D9
6
DB9
D10
5
DB10
D11
4
DB11_MSB
RFB
20
IOUT1
1
IOUT2
2
GND
3
D_GND
U2
DAC7821IPWR
C15
C
A_GND
-10V
U8
TL072CP
1
1OUT
2
1IN-
3
1IN+
4
VCC-
VCC+
8
2OUT
7
2IN-
6
2IN+
5
+10V
A_GND
R10
10k
DAC_OUT
DAC Module

DSPIC33AK128MC106 MICROCONTROLLER

ELECTRONIC SWITCHES

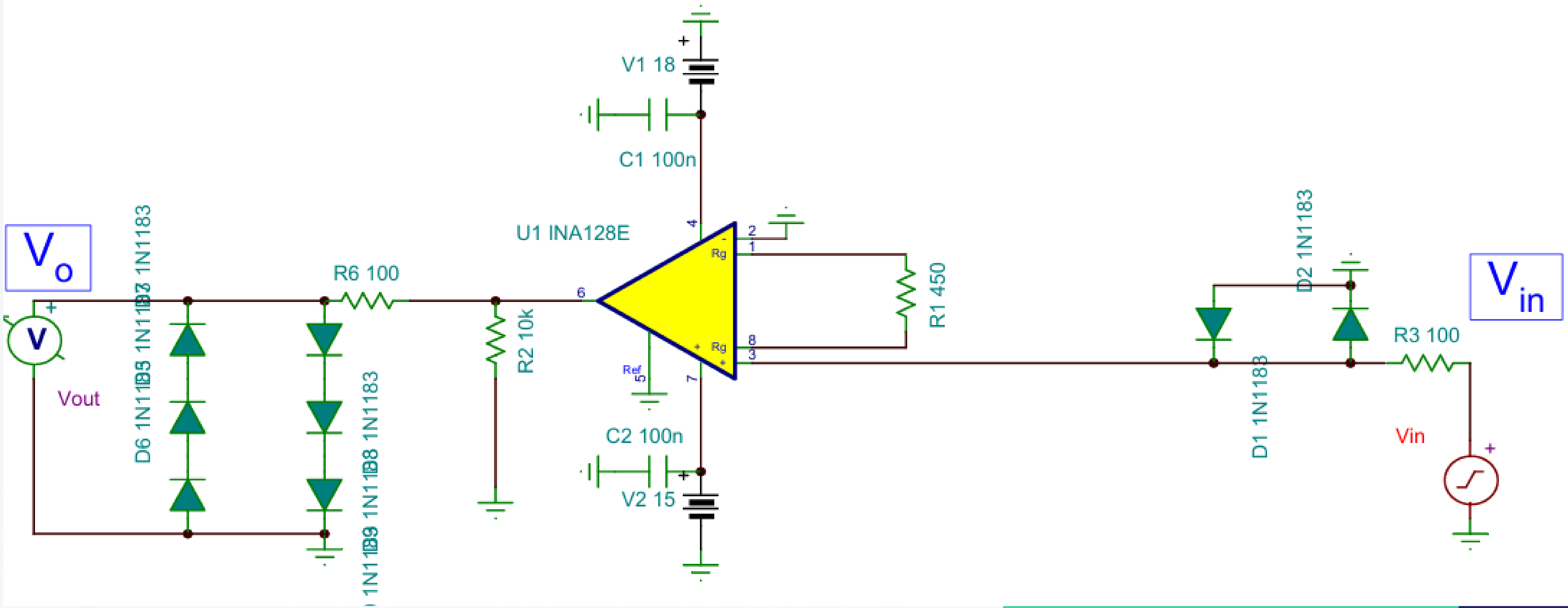


CLIPPING CIRCUIT+ INA128

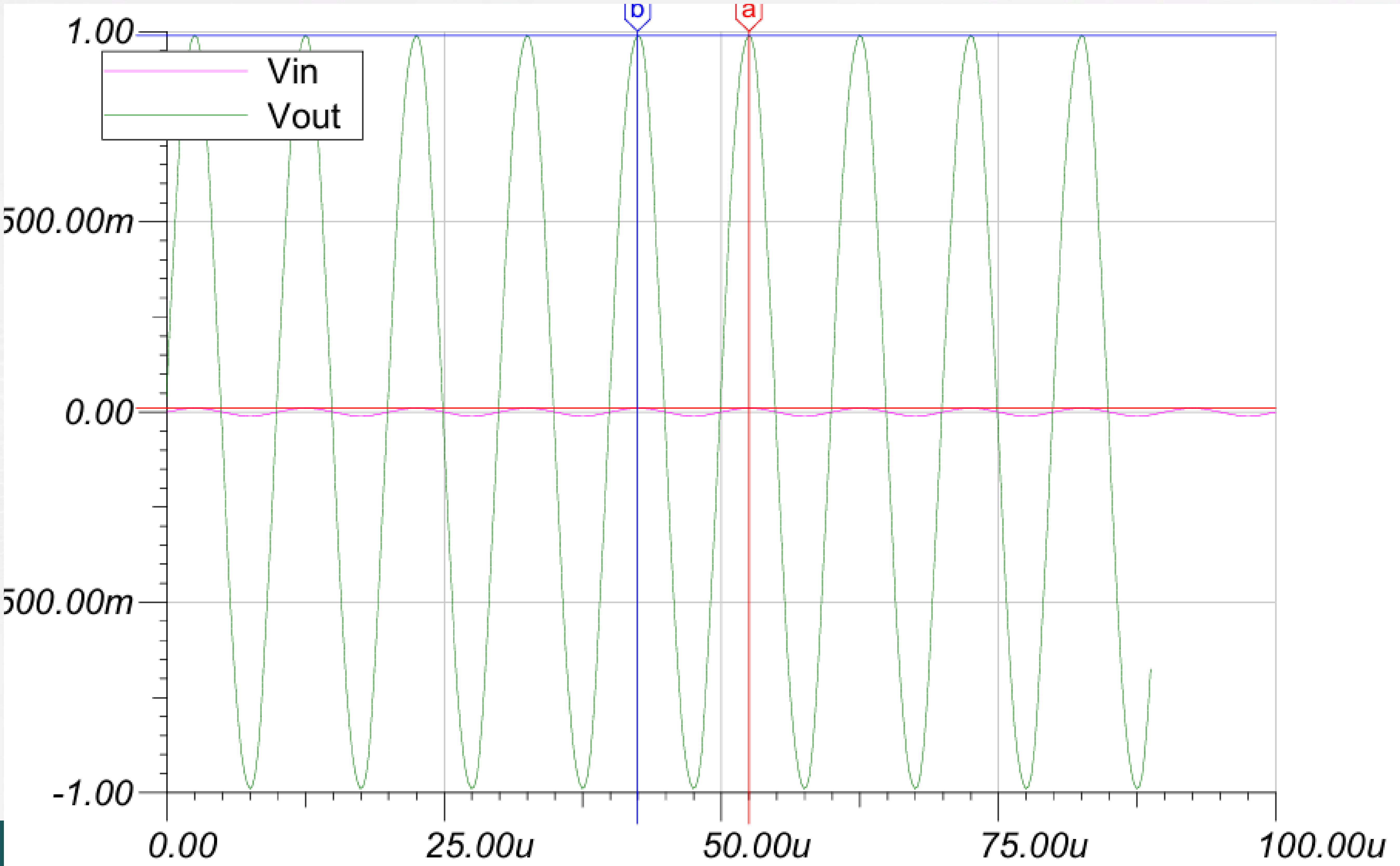


SIMULATIONS RESULTS

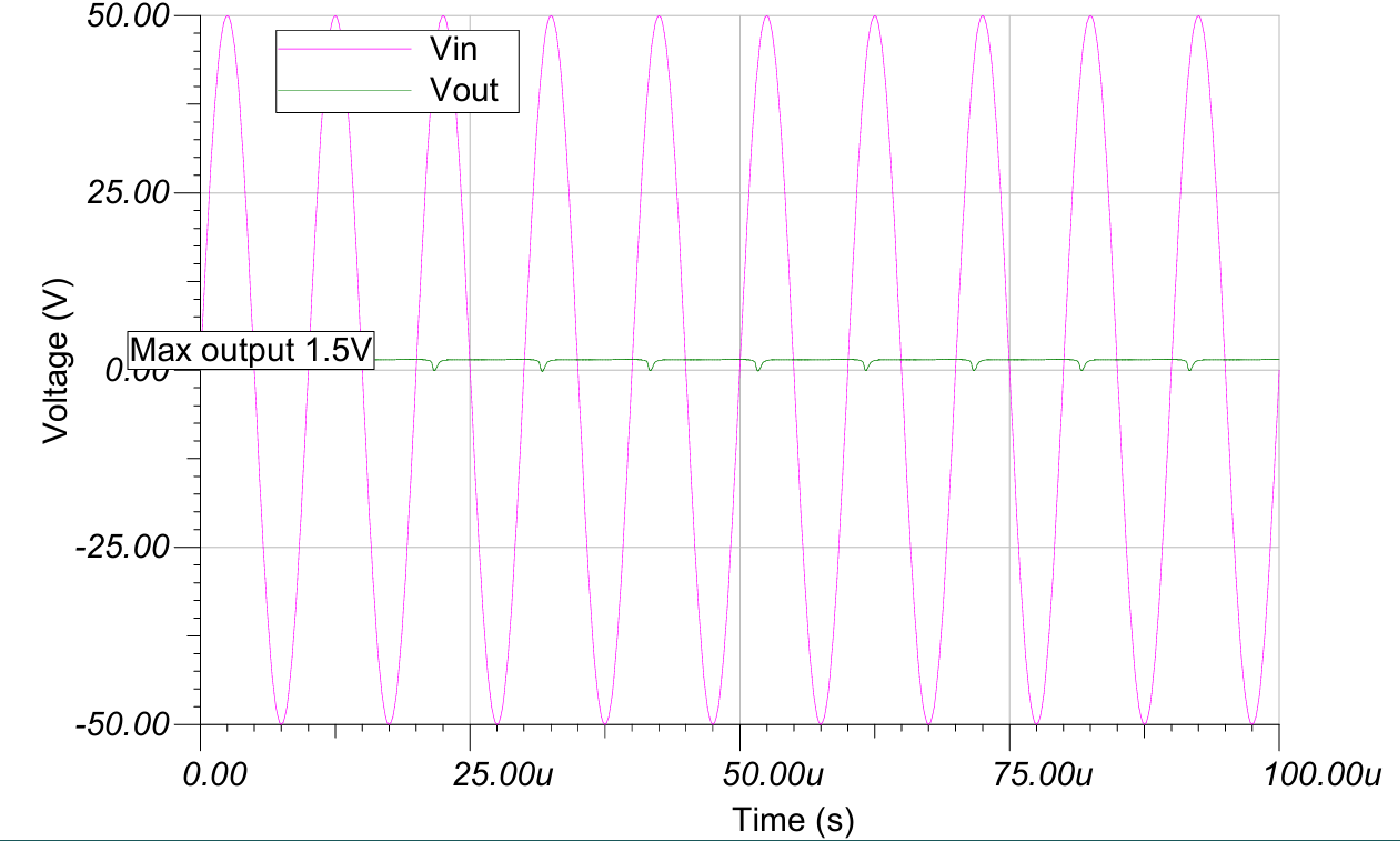
INA + CLIPPER CKT



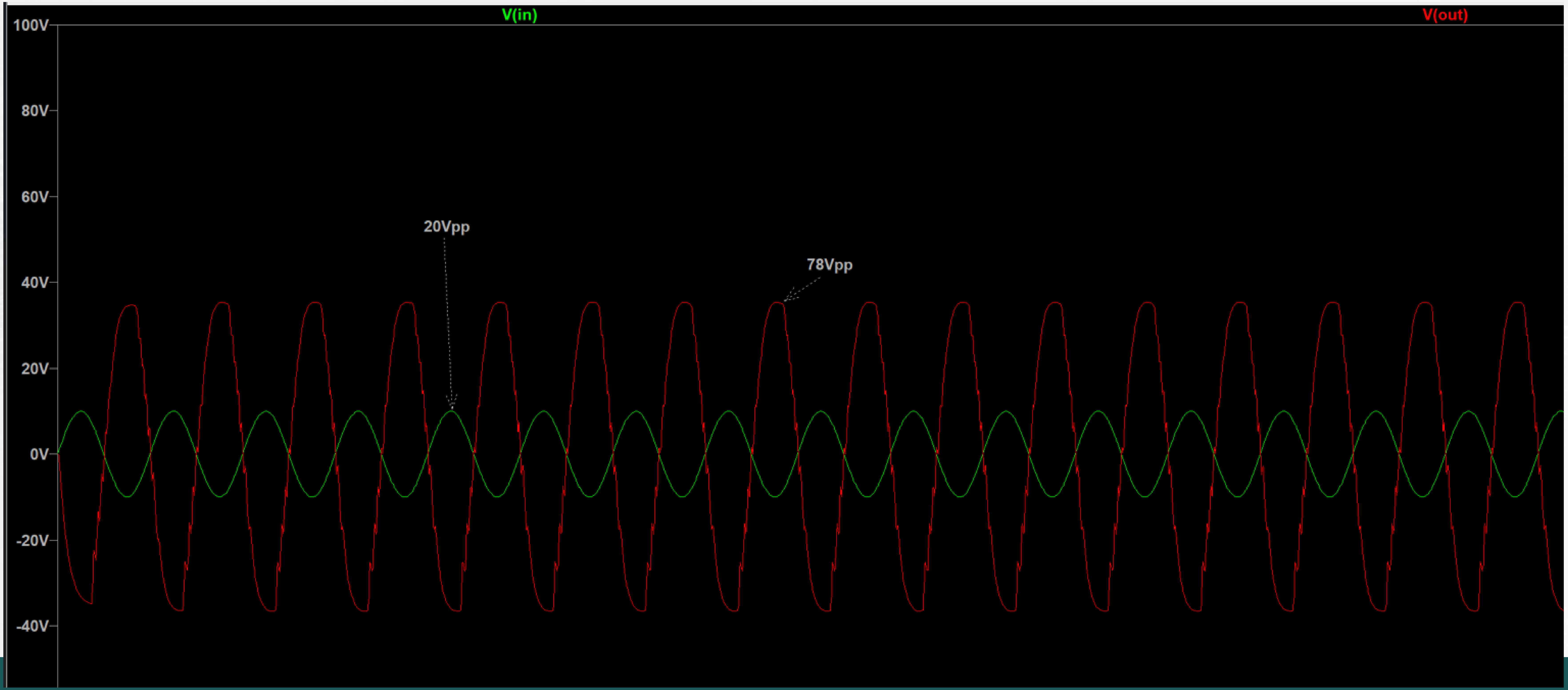
INA + CLIPPER FOR 1MV INPUT



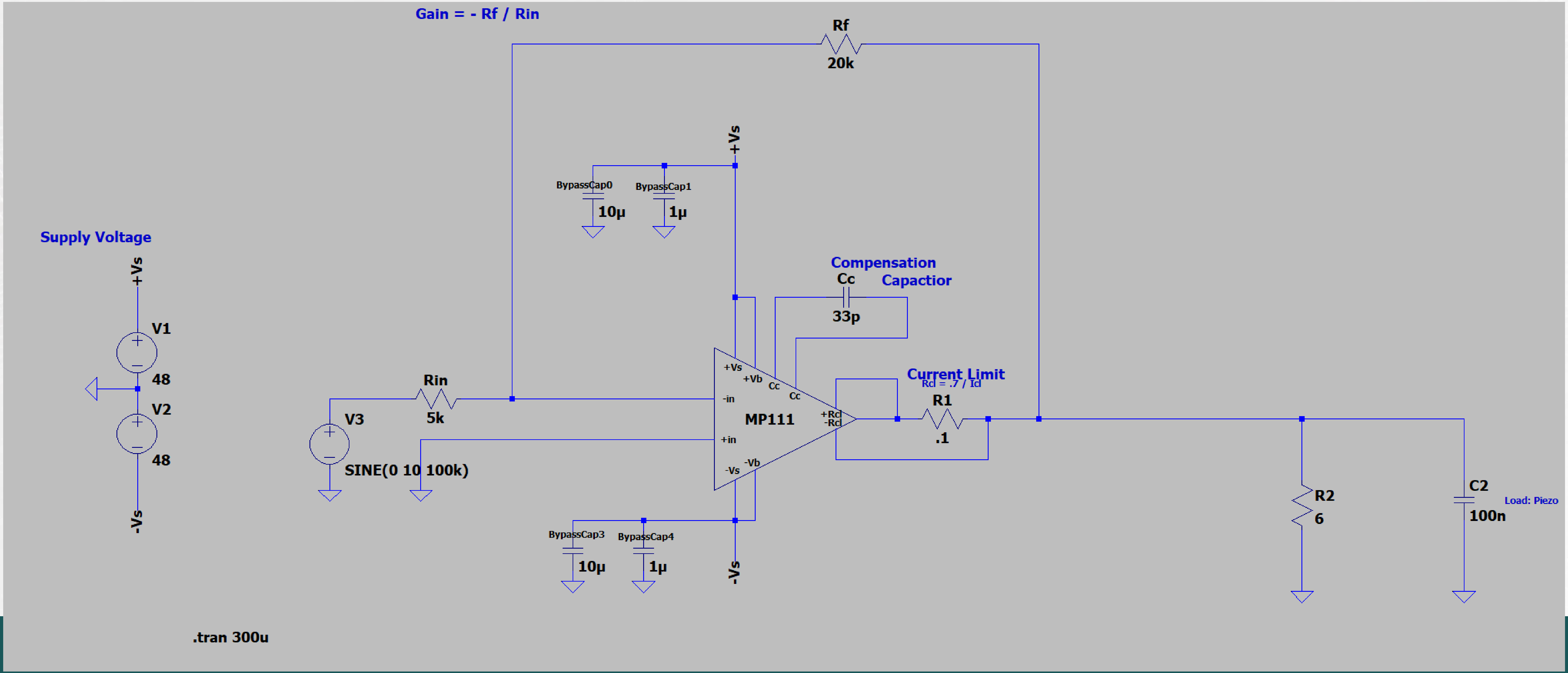
INA + CLIPPER FOR 50V INPUT



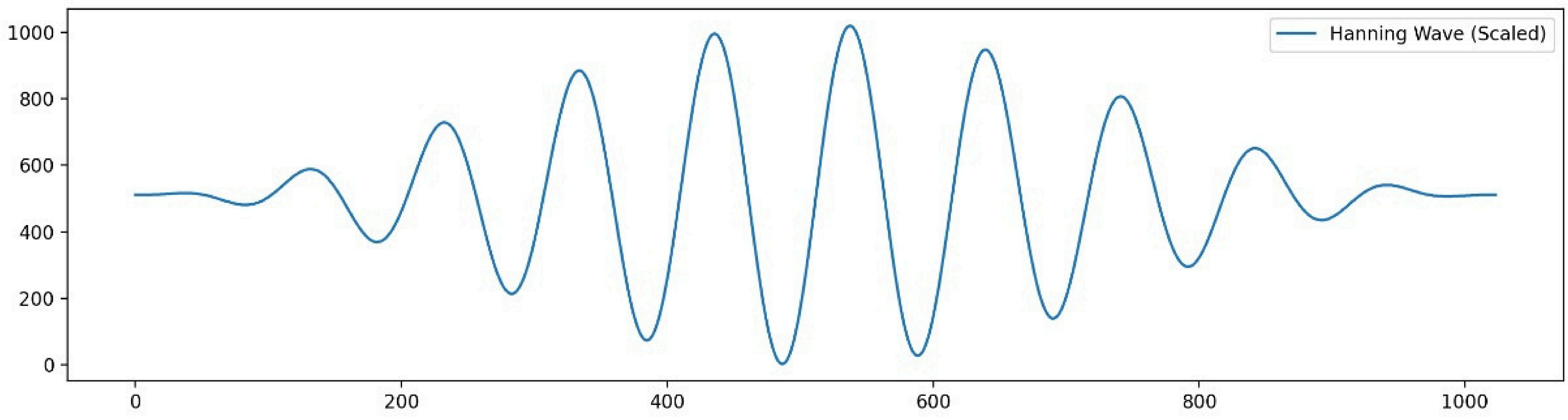
POWER AMPLIFIER



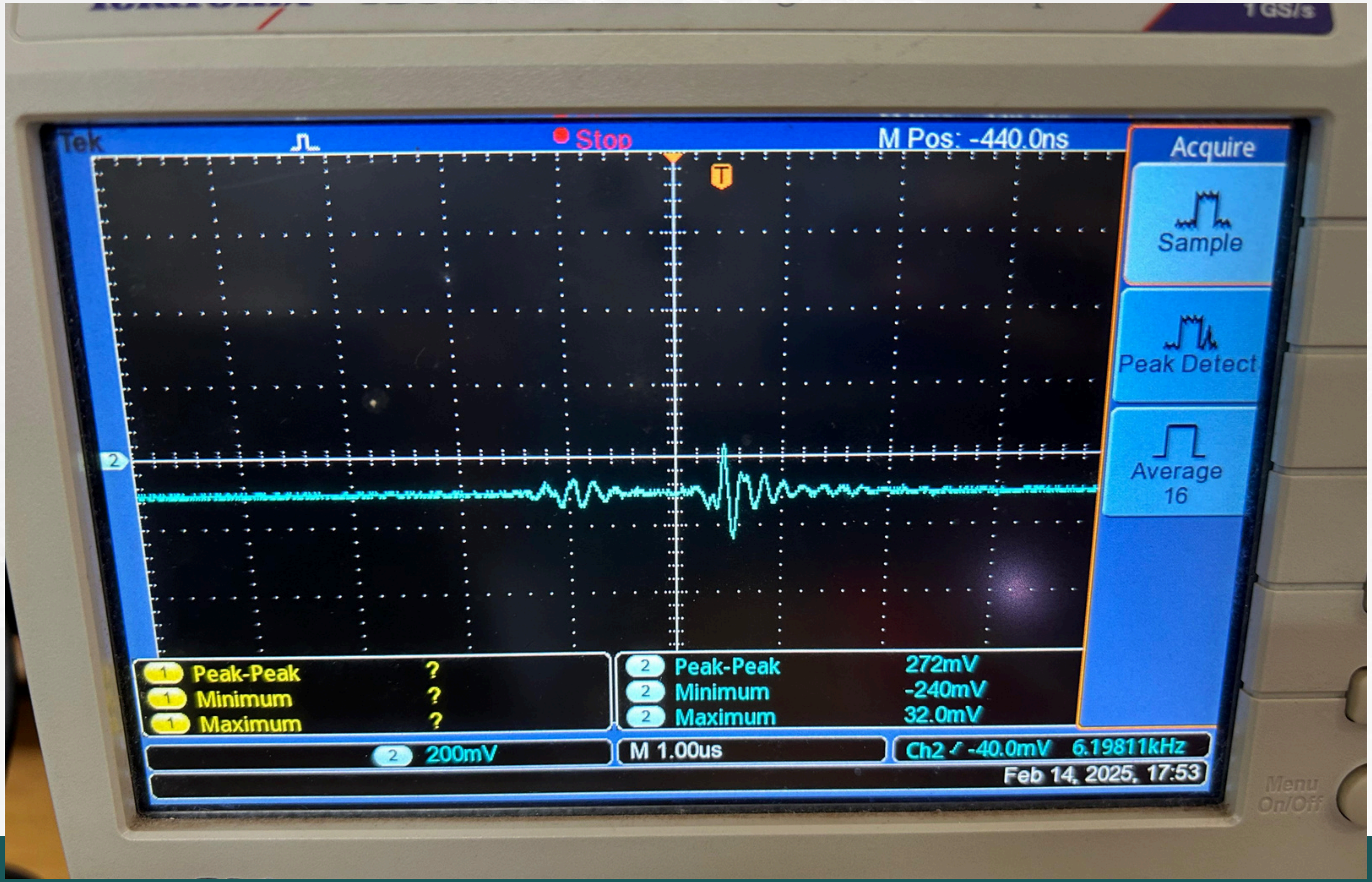
POWER AMPLIFIER



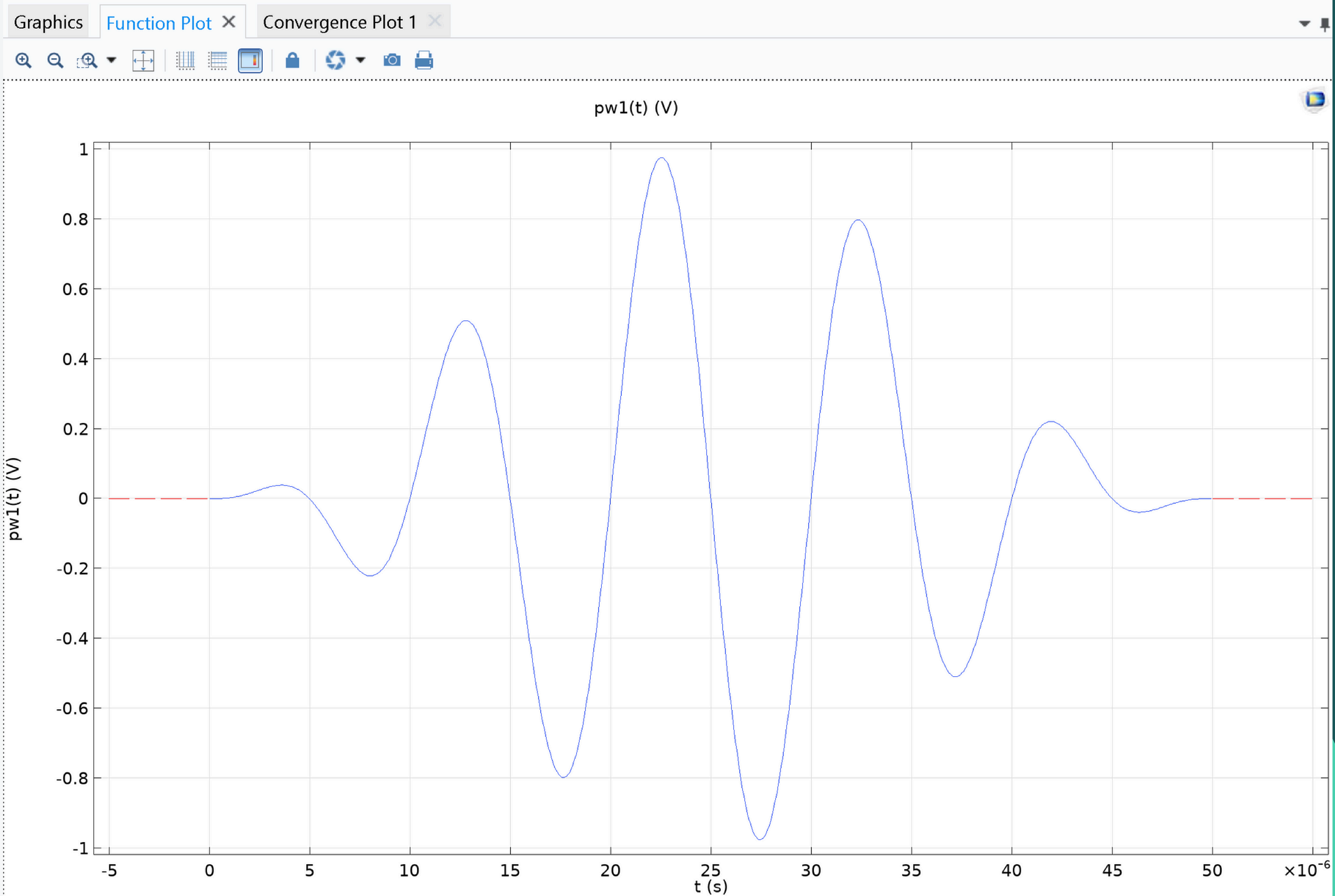
HANNING PULSE - PYTHON SIMULATION



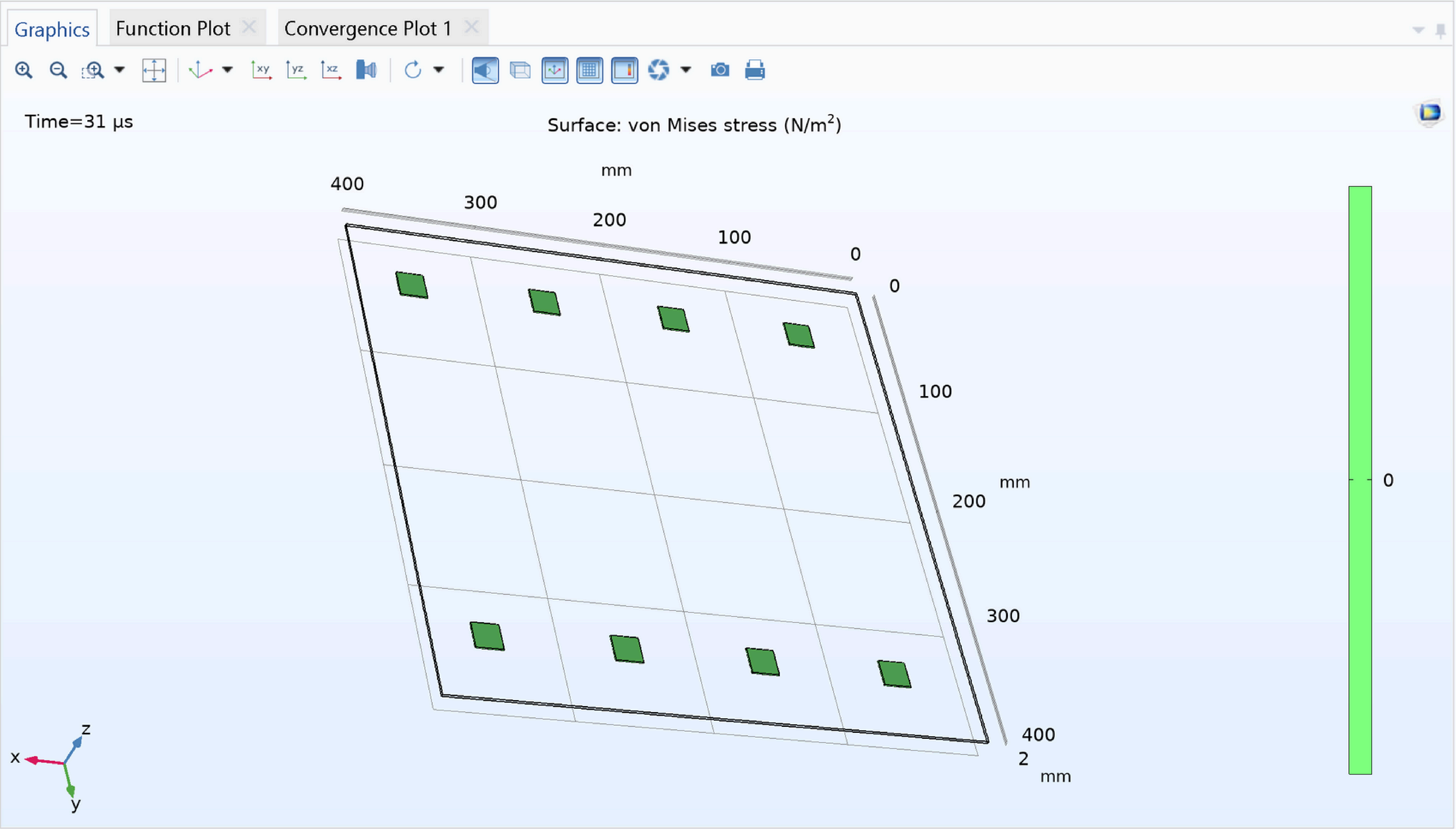
HANNING PULSE ON DSO WITH LESSER SLEW RATE OPAMP (LM741)



COMSOL SIMULATIONS

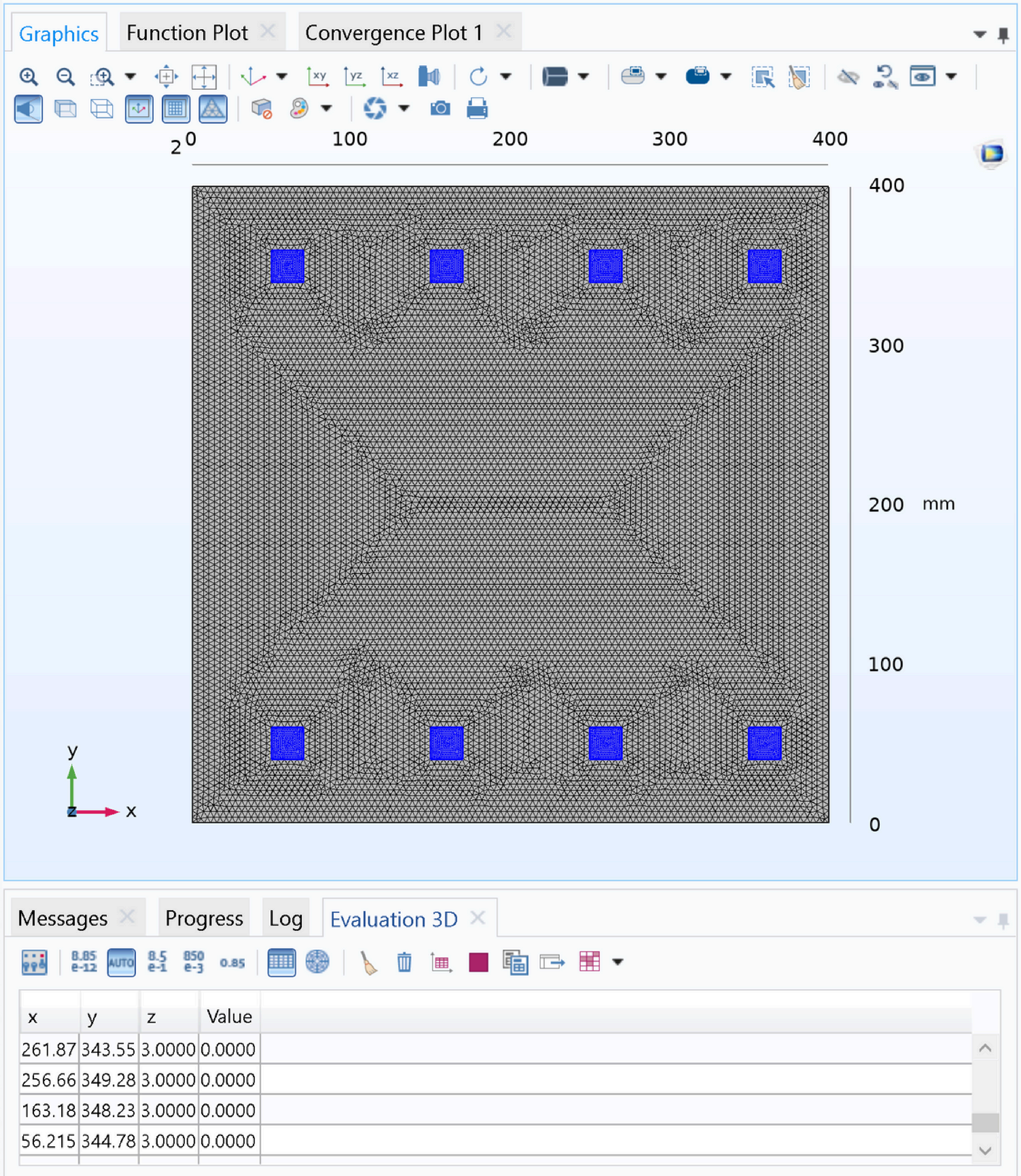


Graphics
Function Plot
Convergence Plot 1
pw1(t) (V)
t (s)
×10^-6



Messages | Progress | Log | Evaluation 3D

x	y	z	Value
261.87	343.55	3.0000	0.0000
256.66	349.28	3.0000	0.0000
163.18	348.23	3.0000	0.0000
56.215	344.78	3.0000	0.0000

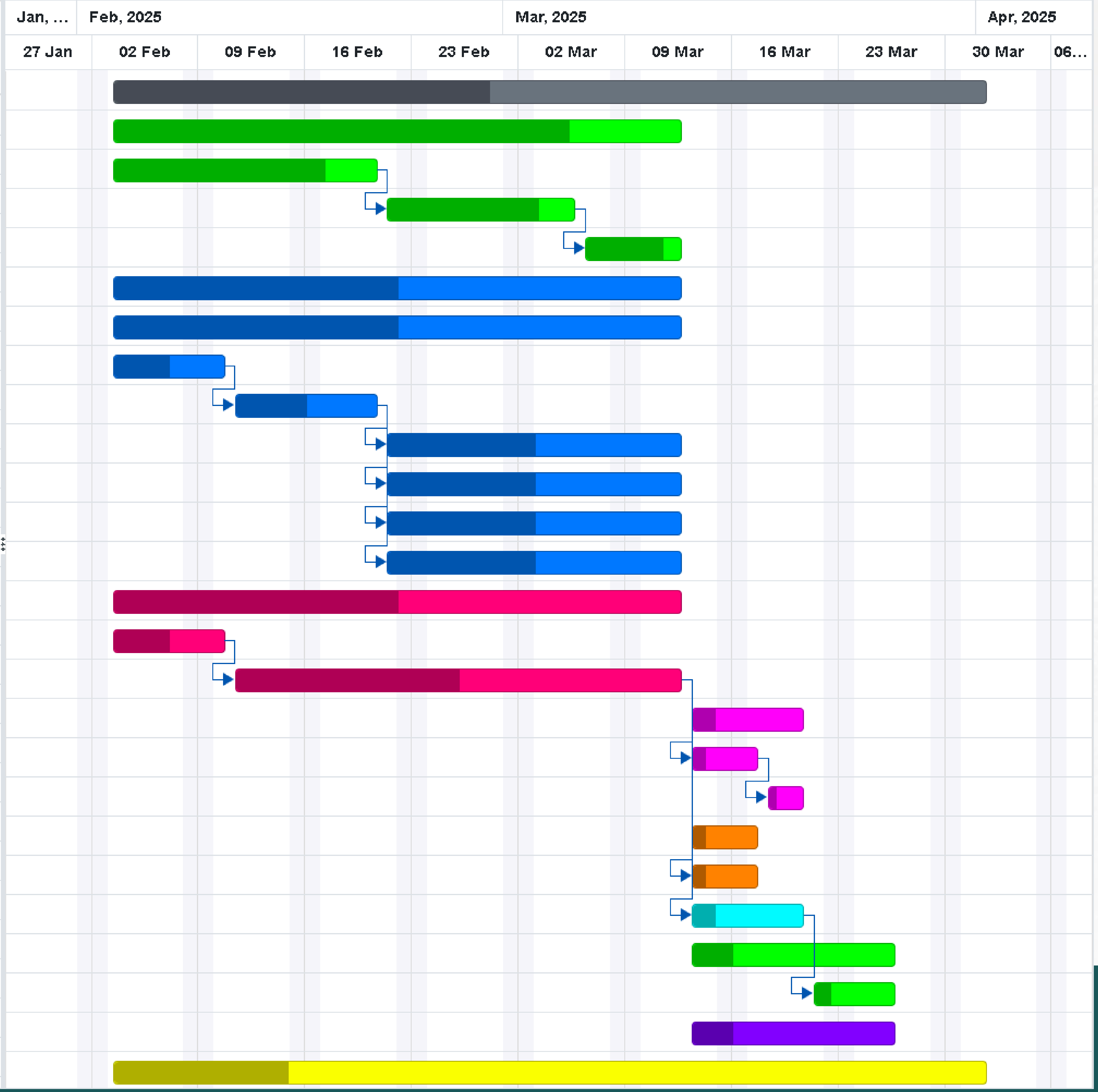

Graphics
Function Plot
Convergence Plot 1
0
100
200
300
400
mm
y
x
z
Messages
Progress
Log
Evaluation 3D
x y z Value
261.87 343.55 3.0000 0.0000
256.66 349.28 3.0000 0.0000
163.18 348.23 3.0000 0.0000
56.215 344.78 3.0000 0.0000

COMPLETE SCHEMATIC LINK

- https://drive.google.com/file/d/1pM-x1FfzuNWClZGZpETy26Dexs8zest_/view?usp=sharing

GANTT CHART FOR WORK DELEGATION

ID	Name
1	Example
2	PCB Design
8	Schematic
9	Placement
10	Routing
3	Microcontroller
11	Interfacing
28	DAC
15	ADC
16	Memory
29	Electronic Switch
27	Wi-Fi Module
18	MUX
12	Algorithm
19	Hanning Pulse (Tx)
20	Post Processing (Rx)
4	Soldering
21	Pick n Place Soldering
22	Hand Soldering
5	GUI
23	Display
30	DI Map
7	CAD Modelling
25	Design
26	Encasing



Deviations from original plan

1) We have now sub-divided our tasks into several more parts to be able to tackle various issues that may arise with each part efficiently.

2) Not all parts we needed to start PCB designing are available to us as a result we moved to algorithms and interfacing part and started it ahead while pushing soldering forward.

3) We spent some time on how to optimize providing power to various modules and reduced a few components by this method. This was because a few components had similar range of voltage requirements, so we decided to use fewer buck converters. This took us a few days.

DETAILS OF TEST PLANS

Part 1

- **Preliminary testing**

1. Physical and Simulation based testing of all the major blocks and components.
2. Checking all the circuitry and connection with the material available upto now.

Part 2

- **Intermediate testing**

Complete testing once all the components are available once for each component and then taking blocks.

Part 3

- **Final testing**

Running the complete handheld device with all the components onto an Al metal plate

PRELIMINARY TESTING

- So we got a skewed Hanning pulse during our initial testing, this was due to the fact that we chose LM741 for our current-to-voltage converter, which has a lower slew rate. So the high transitions per sample weren’t generated well.
- So we now have chosen TL072 which has a higher slew rate.
- This will ensure we sample the values and subsequently create the right analog waveform.
- Power Amplifier: Worked correctly on simulations and will next test on breadboard.

Thinking ahead to next milestone

- Upon receiving all the components we will finish the individual component simulations and physical testing by making the required circuitry .
- Then we will move onto writing the required code on uC and check for the proper functioning of the circuitry after dumping the code.
- After that we will let the PCB design (including the power amplifier) reviewed and once finalized take it to fabrication.
- Then we will test onto the PCB and CAD combined model and do the subsequent debugging.
- Once all that is finalized we will work on making a working prototype which will be a handheld device.