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無線感測網路下的位置管理策略設計與效能評估

Design and Performance Evaluation of Mobility
Management in Wireless Sensor Networks

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Design and Performance Evaluation of Mobility
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碩士論文

考慮匯流排腳位效應之匯流排導向平面佈局
Bus-Pin-Aware Bus-Driven Floorplanning

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Bus-Pin-Aware Bus-Driven Floorplanning

by

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Abstract

As the number of buses increase substantially in multi-core SoC designs, the bus planning problem has become the dominant factor in determining the performance and power consumption of SoC designs. To cope with the bus planning problem, it is desirable to consider this issue in early floorplanning stage. Recently, bus-driven floorplanning problem has attracted much attention in the literature. However, current algorithms adopt an over-simplified formulation ignoring the position and orientation of the bus pins, the chip performance may be deteriorated. In this paper, we propose the bus-driven floorplanning algorithm that fully considers the impacts of the bus pins. By fully utilizing the position and orientation of the bus pins, bus bendings are not restricted to occur at the modules on the bus, then it has more flexibility during bus routing. With more flexibility on the bus shape, the size of the solution space is increased and a better bus-driven floorplanning solution can be obtained. Compared with the bus-driven floorplanner[?], the experimental results show that our algorithm performs better in runtime by $3.5\times$, success rate by $1.2\times$, wirelength by $1.8\times$, and reduced the deadspace by $1.2\times$.

- **Keywords:** Floorplanning, Bus planning

摘要

由於在嵌入式系統中, 匯流排的數量急劇地上升, 匯流排規劃的品質好壞成為決定嵌入式系統效能與系統功率消耗的重要指標。為了不讓匯流排的問題造成晶片設計流程後期的限制, 在早期平面佈局時就將匯流排的因素加入考慮是比較理想的處理方式。近年來, 匯流排導向平面佈局的問題吸引了許多人的注意, 並且已有相當多的方法被提出於處理相關的問題。然而, 目前的演算法都採取了比較簡單的問題定義, 忽略了匯流排腳位的位置和方向等相關的資訊。忽略了上述的資訊可能會造成系統效能被高估的情況。因此, 我們提出了一個匯流排導向的平面佈局演算法, 我們所提出的演算法在規劃匯流排時也考慮到腳位的位置與方向的資訊, 讓演算法所得到的結果能夠更符合實際情況。由於在規劃匯流排的同時也考慮匯流排腳位的資訊, 匯流排轉彎的地方並不局限在匯流排所連接的方塊上。因此, 在處理匯流排繞線問題時也比較有彈性。隨著整個匯流排拓撲的形狀變得更有彈性, 匯流排繞線的成功率也相對地提高, 許多較佳的結果就能被發掘出來。將我們的演算法所得到的結果與目前最佳的匯流排導向平面佈局演算法所得到的結果比較, 我們演算法的執行時間相對快了 3.5 倍, 繞線成功率提高了 1.2 倍, 匯流排長度少了 1.8 倍, 並且將平面佈局中空白的區域降低了 1.2 倍。

• **關鍵字:** 平面規劃, 匯流排規劃

Acknowledgments

" 我思故我在, 我做故我存."

"I think, therefore I am. I do, that become valuable."

" 別人笑我太瘋癲，我笑他人看不穿."

"People laugh at me for my insane, but I laugh them because they don't see the truth."

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Chapter 1

Introduction

With the increasing design complexity, the amount of buses between different modules on a chip also increases rapidly. Bus routing has become a major concern of comparable importance to timing and power in multi-core SoC designs. To ease the efforts of bus routing in later routing stage, it is desirable to consider this issue in early floorplanning stage. Since buses are of different widths and required to go through different sets of modules, the bus routability is severely affected by the module position. Bus-driven floorplanning targets on obtaining a bus-routable floorplan such that the chip area and the bus area are minimized. Recently, many bus-driven floorplanning algorithms have been proposed in the literature[? ? ? ? ? ? ? ? ? ?]. However, these bus-driven floorplanning algorithms adopt an over-simplified formulation which ignores the practical issues such as the position and orientation of the bus pin. Without taking those practical issues into consideration, it may have the following impacts on bus routing:

- **Bus twisting:** It makes the signal wires cross at a point and decreases accessibilities of the bused pins.

- **Via increasing:** Several vias occur at the bend of a bus that have adverse effects on the bus delay.

- **Delay variation:** Different driver-load wirelength between different bus bits causes delay variation among all bus bits.
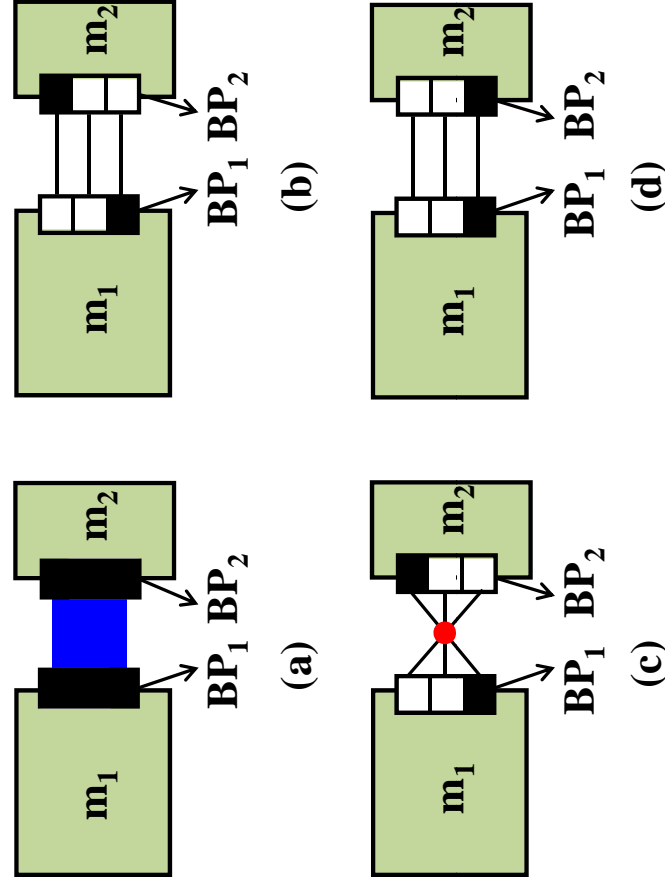

Figure 1.1: (a) One horizontal bus connects two bus pins. (b) Bus routing without considering the effect of the bus pin. (c) Bus twisting. (d) No bus twisting after flipping the bus pin.

One example of the bus twisting is given in Figure 1.1. In Figure 1.1 (a), two modules m_1 and m_2 are placed on the floorplan, and two bus pin BP_1 and BP_2 connected by one horizontal bus are placed on the boundary of the two modules. Since the effect of the bus pin is not considered during bus routing in current algorithms, the routing result in Figure 1.1 (b) is obtained, and some bits of the bus pin are not correctly connected by the wire. Therefore, the wrong signal is transmitted via the bus, the Most Significant Bit (MSB) of each bus pin is marked with black color in

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all figures of this paper. In this paper, the bus pin is carefully handled during bus routing, thus, each bus can be correctly connected by the wire as shown in Figure 1.1 (c). However, all wires are twisted at one point in the figure, the problem can be solved by flipping the bus pin BP_2 as shown in Figure 1.1 (d).

Therefore, an over-simplified bus-driven floorplanning formulation will make the routability and the solution quality in doubt.

Figure 1.2 illustrates the impact of the position and orientation of the bus pin. There are eight modules and one bus that connects two modules m_3 and m_5, i.e., bus modules. In Figure 1.2 (a), existing bus-driven floorplanning algorithms connect m_3 and m_5 by simply one vertical bus. However, by considering the actual positions of the bus pins in Figure 1.2 (b), the bus pins of these two modules can not be passed by only one vertical bus, and the wirelength is much longer than the simplified estimation.

Furthermore, current bus-driven floorplanning algorithms restrict a bus only bends above the bus modules, i.e., only horizontal and vertical connections on the bus modules are allowed. Such restriction limits the flexibility on the bus shape resulting a narrower solution space. Therefore, better bus-driven floorplanning solutions may be missed in such formulation. In this paper, we explore the diagonal connection between the bus modules to improve the solution quality. Compared with Figure 1.2 (b), a better solution with smaller area can be achieved by utilizing the diagonal connection between m_3 and m_5 as shown in Figure 1.2 (c). Although there are two bends occur at two modules m_4 and m_5, no extra vias are required at the bend of m_5 since vias exist anyway to connect to the bus modules m_5. Even extra vias are still required at another bend on the module m_4 which is not a bus module, it can be

eliminated by simply flipping the bus pin on the module m_3 and assigning the horizontal and vertical buses on the module m_4 to the same layer as shown in Figure 1.2 (d).

As mentioned earlier, different driver-load wirelength between bus bits causes delay variation among all bus bits. At a load, the wirelength difference among all bus bits is characterized by **wirelength deviation**. Different from Figure 1.2 (d), the driver-load bus delay among all bus bits is different, the deviation can be further optimized to 0 by flipping the bus pin on module m_5 as shown in Figure 1.2 (e).

In this paper, we propose a bus-driven floorplanning algorithm that fully considers the impact of the bus pins. By fully utilizing the position and orientation of the bus pins, we can obtain the high-quality results by exploring flexibility on the bus shape. Moreover, we also develop two effective algorithms to minimize the wirelength deviations and two wirelength reduction algorithms to optimize the total bus wirelength. Experimental results show that our algorithms are very promising.

1.1 Previous Works

The bus-driven floorplanning problem has recently attracted a lot of attention in the literature. Rafiq et al. proposed an integrated floorplanning for bus-based microprocessor designs[?]. Multiple topologies were produced for each bus, and a mixed integer/linear programming approach was adopted to arbitrate the conflicts between different buses. However, the algorithm was limited to single fanout buses. Xiang et al.[?] solved the bus-driven floorplanning problem by using a sequence pair (SP) representation based on a simulated annealing (SA) framework. Chen and Chang[?] handled the bus-driven floorplanning problem based on the B*-tree representation.

The drawback of the above two methods is that all modules are connected by either horizontal or vertical 0-bend buses; the solution space is thus restricted when a large number of the modules are involved for each bus. The bus shape problem was improved by?, where 0-bend, 1-bend, and 2-bend buses were allowed. Nevertheless, there are still limitations on the bus shape. In?, a multi-bend bus-driven floorplanning algorithm was proposed based on a TCG representation. It has more flexibility on bus shapes and obtains higher success rate.

In microprocessors and DSPs, many cores are involved and the signals are transmitted between different cores by the buses which play an important role in determining the chip performance. Therefore, some previous works were developed to deal with such floorplanning in microarchitectural design. Kim and Lim? presented a new bus routing algorithm based on Hanan grids and linear programming. In?, the authors proposed a bus-aware microarchitectural floorplanning which addressed the impact of bus routability on performance/power/thermal issues. However, the above two works aimed on optimizing IPC (Instructions Per Cycle) and had a different problem formulation from those aforementioned floorplanners.

There are still many works which consider other constraints during the bus planning. Xiang et al.? proposed an OPC-friendly bus driven floorplanning algorithm which carefully designed the pitch for buses to avoid the forbidden pitch. Sheng et al.? proposed an approach which was based on a deterministic algorithm Less Flexibility First, it run in a fixed-outline area and packed hard blocks one after another. In?, they presented a floorplan revising method which was based on linear programming model to minimize the number of reducible routing vias with a controllable loss on the chip area and wirelength. The authors? considered the bus pin issue

and explored the diagonal connection which makes the bus shape more flexible and improves the solution quality.

1.2   Our Contributions

In this paper, we propose a bus-driven floorplanning algorithm that fully considers the impact of the bus pins. The diagonal connection between different modules is explored to make the bus shape more flexible which improves the success rate. The contributions of this paper are listed as follows:

- **Deviation Minimization:** We develop two algorithms to minimize the wirelength deviation for signal integrity of the buses. First algorithm explores all possible topologies between any two modules, and it finally concludes some specific bus patterns, then the best deviation at each module can be quickly obtained from those specific bus patterns. In second algorithm, the procedure of determining the deviation at each module is divided into two steps --- deviation determination and accumulated deviation update. During determining the deviation at one module, all the accumulated deviation from the driver to its neighbors can also be calculated. Since the procedure of determining the deviation at each module is divided into two steps, the segment size for each comparison becomes smaller, then the total bus patterns can be further reduced to 10 types. Fewer bus patterns stands for less time is needed for searching the possible bus patterns. Experimental results show that the wirelength deviation can be effectively reduced.

- **Diagonal relation:** In this paper, we explore the diagonal relation between

different modules to make the bus shape more flexible, then the modified graph coloring algorithm is proposed to determine the layer of each bus. Experimental results show that our algorithm has $1.2\times$ improvement on the success rate compared with[?] .

- **Wirelength reduction:** To further enhance the solution quality, we present two wirelength reduction algorithms to improve the total bus wirelength. First algorithm reduces the total bus wirelength by minimizing the overlap between different bus components (for the multi-bend bus, each horizontal (vertical) part is called a bus component) during constructing the minimum spanning tree (MST). The second algorithm is used to optimize the bus wirelength by adjusting the coordinate of each horizontal (vertical) bus component.

The rest of this paper is organized as follows. Chapter **??** gives the problem formulation of the bus-driven floorplanning. Chapter **??** defines the constraints and terminologies used in this paper. Chapter **??** gives the details of the proposed bus-driven floorplanning algorithm. Experimental results are shown in Chapter **??**. Finally, a conclusion will be given in Chapter **??**.
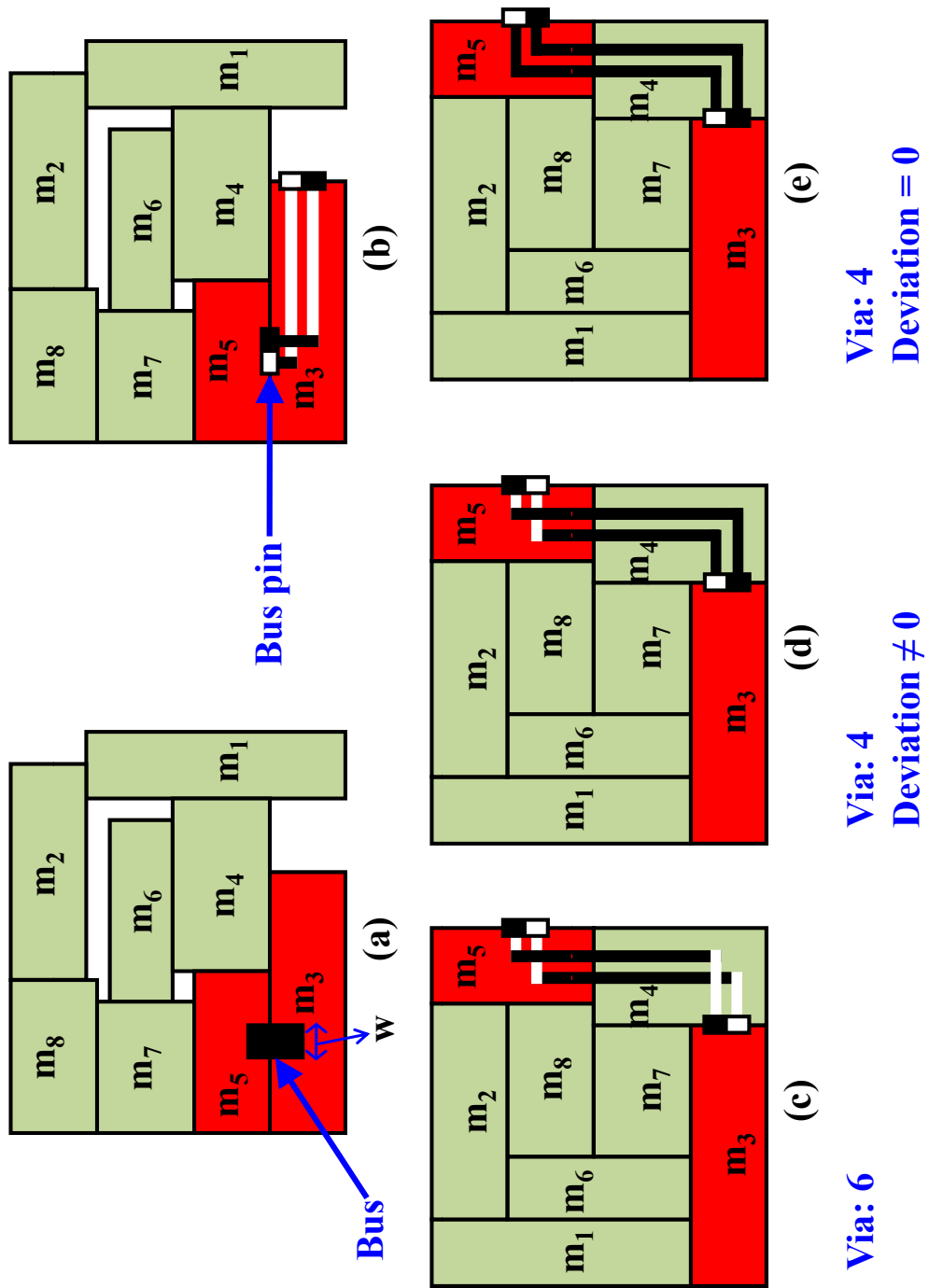
Figure 1.2: (a) Simplified bus routing. (b) Bus routing considering the bus pin. (c) Bus routing with the diagonal connection between the modules. (d) Via-aware bus routing with the diagonal connection between modules. (e) Bus routing considering both vias and wirelength deviation.

Chapter 2

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Bibliography