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資 訊 工 程 學 系

碩 士 論 文

無線感測網路下的位置管理策略設計與效能評估

Design and Performance Evaluation of Mobility Management in Wireless Sensor Networks

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Design and Performance Evaluation of Mobility Management in Wireless Sensor Networks

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碩士論文

考慮匯流排腳位效應之匯流排導向平面佈局
Bus-Pin-Aware Bus-Driven Floorplanning

研究生：吳柏勳

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Bus-Pin-Aware Bus-Driven Floorplanning

by

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Abstract

As the number of buses increase substantially in multi-core SoC designs, the bus planning problem has become the dominant factor in determining the performance and power consumption of SoC designs. To cope with the bus planning problem, it is desirable to consider this issue in early floorplanning stage. Recently, bus-driven floorplanning problem has attracted much attention in the literature. However, current algorithms adopt an over-simplified formulation ignoring the position and orientation of the bus pins, the chip performance may be deteriorated. In this paper, we propose the bus-driven floorplanning algorithm that fully considers the impacts of the bus pins. By fully utilizing the position and orientation of the bus pins, bus bendings are not restricted to occur at the modules on the bus, then it has more flexibility during bus routing. With more flexibility on the bus shape, the size of the solution space is increased and a better bus-driven floorplanning solution can be obtained. Compared with the bus-driven floorplanner [**?**], the experimental results show that our algorithm performs better in runtime by 3.5×, success rate by 1.2×, wirelength by 1.8×, and reduced the deadspace by 1.2×.

- **Keywords:** Floorplanning; Bus planning

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