

**RCA**

# COS/MOS Integrated Circuits

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**COS/MOS**

Digital Integrated Circuits



Selection Guide / Data / Application Notes

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# **RCA**

## **COS/MOS Integrated Circuits**

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This DATABOOK contains complete data and related application notes on COS/MOS digital integrated circuits presently available from RCA Solid State Division as standard products. For ease of type selection, functional diagrams are shown on pages 8-18. Data sheets are then included in type-number sequence, followed by output-drive-current test-circuit connections, terminal-assignment diagrams, and dimensional outlines for all types, by application notes in numerical order, and finally by a comprehensive subject index.

To simplify data reference, data sheets are arranged as nearly as possible in numerical sequence of device type numbers. Because some data sheets include more than one type number, however, some types may be out of sequence. If you don't find the type you're looking for where you expect it to be, please consult the Index to Devices on page 7.

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(Indicate order of interest if  
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- A  Linear IC's
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- C  Digital IC's, Bipolar
- D  Thyristors/Rectifiers
- E  Liquid Crystals
- F  Semiconductor Diodes
- G  RF Power Semiconductors
- H  MOSFETS
- I  Power Transistors
- J  Power Hybrid Circuits

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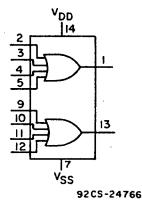
# Index to COS/MOS Integrated Circuits

(Circuits marked with an asterisk (\*) are also available in chip form.

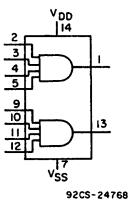
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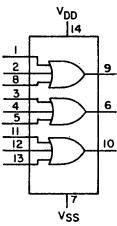
GATES  
NOR/NAND, OR/AND



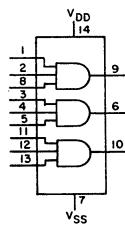
**CD4072B**  
**Dual 4-Input**  
**OR Gate**  
**File No. 807**



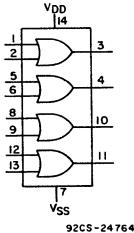
**CD4082B**  
**Dual 4-Input**  
**AND Gate**  
**File No. 806**



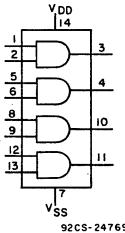
**CD4075B**  
**Triple 3-Input**  
**OR Gate**  
**File No. 807**



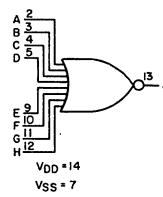
**CD4073B**  
**Triple 3-Input**  
**AND Gate**  
**File No. 806**



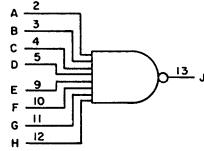
**CD4071B**  
**Quad 2-Input**  
**OR Gate**  
**File No. 807**



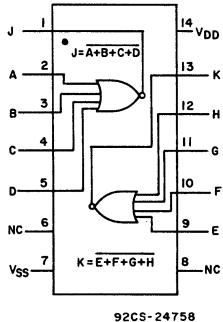
**CD4081B**  
**Quad 2-Input**  
**AND Gate**  
**File No. 806**



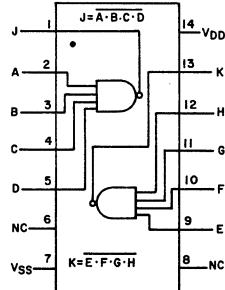
**CD4078B  
8-Input  
NOR Gate  
File No. 810**



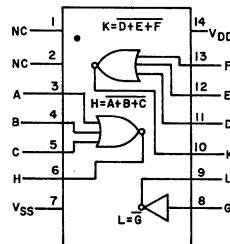
**CD4068B**  
**8-Input**  
**NAND Gate**  
**File No. 809**



**CD4002A  
Dual 4-Input  
NOR Gate  
File No. 479**

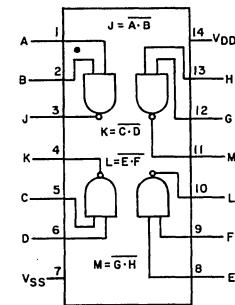
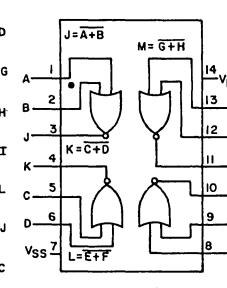
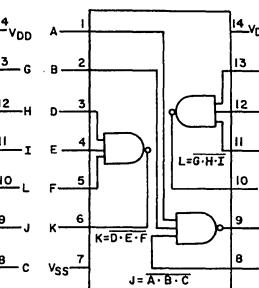
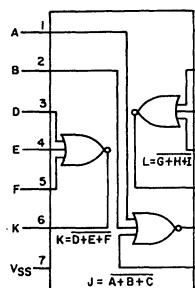


**CD4012A**  
**Dual 4-Input**  
**NAND Gate**  
**File No. 479**



**CD4000A**  
**Dual 3-Input NOR Gate**  
**Plus Inverter**  
**File No. 479**

**GATES**  
**NOR/NAND (Cont'd)**



**CD4025A**

Triple 3-Input  
NOR Gate  
File No. 479

**CD4023A**

Triple 3-Input  
NAND Gate  
File No. 479

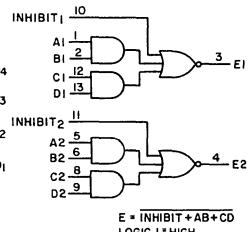
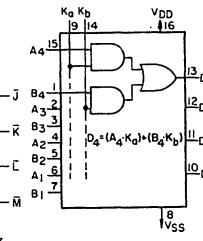
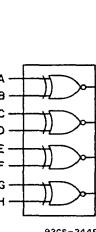
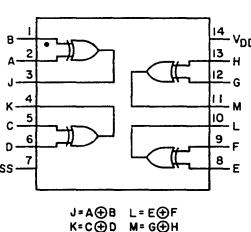
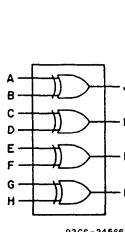
**CD4001A**

Quad 2-Input  
NOR Gate  
File No. 479

**CD4011A**

Quad 2-Input  
NAND Gate  
File No. 479

**MULTI- LEVEL/FUNCTIONAL**



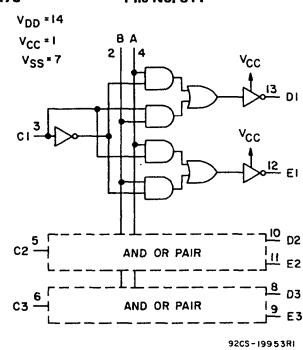
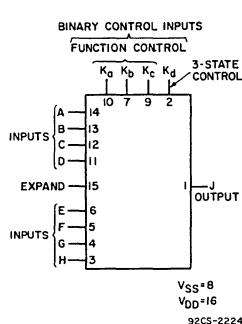
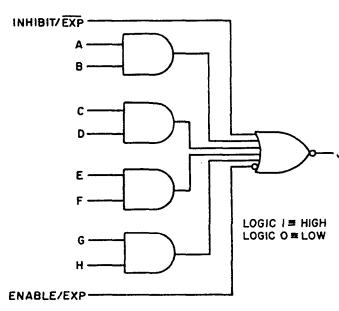
**CD4070B**  
Quad Exclusive-  
OR Gate  
Preliminary

**CD4030A**  
Quad Exclusive-  
OR Gate  
File No. 503

**CD4077B**  
Quad Exclusive-  
NOR Gate  
Preliminary

**CD4019A**  
Quad AND/OR  
Select Gate  
File No. 479

**CD4085B**  
Dual 2-Wide, 2-Input  
AND-OR Invert (AOI) Gate  
File No. 811

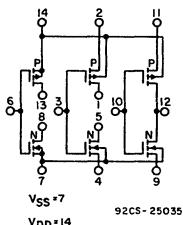


**CD4086B**  
Expandable 4-Wide, 2-Input  
AND-OR Invert (AOI) Gate  
File No. 812

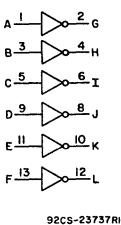
**CD4048A**  
Multifunctional Expandable  
8-Input Gate (3 Output States)  
File No. 636

**CD4037A**  
Triple AND-OR Bi-Phase Pairs  
File No. 576

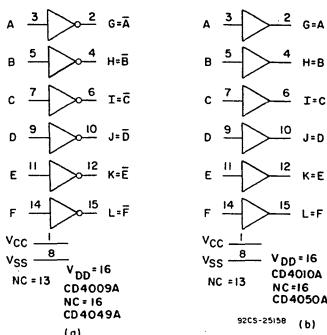
**GATES**  
Buffers & Inverters



**CD4007A**  
Dual Complementary  
Pair Plus Inverter  
File No. 479

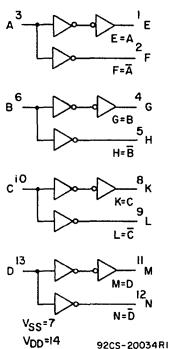


**CD4069B**  
Hex  
Inverter  
File No. 804



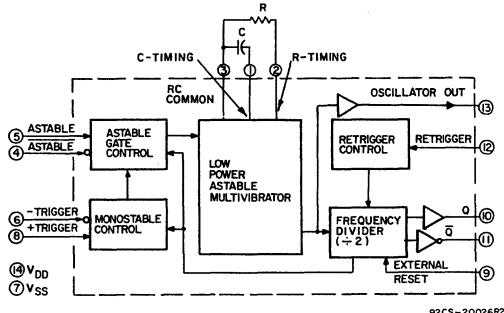
**CD4009A, CD4049A**  
File No. 479 File No. 599  
Hex Buffer/Converter  
Non-Inverting Type

**CD4010A, CD4050A**  
File No. 479 File No. 599  
Hex Buffer/Converter  
Inverting Type

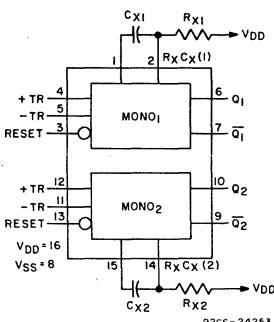


**CD4041A**  
Quad True/Complement  
Buffer  
File No. 572

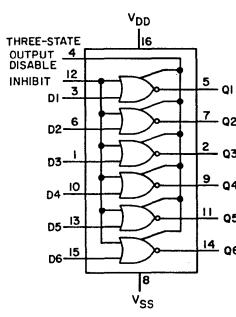
**MULTIVIBRATORS**



**CD4047A**  
Monostable/Astable  
Multivibrator  
File No. 623

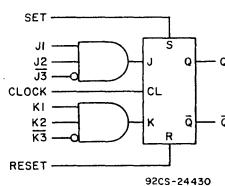
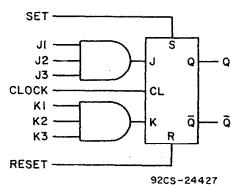
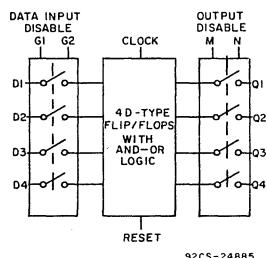
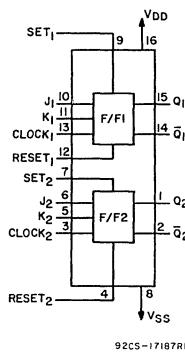
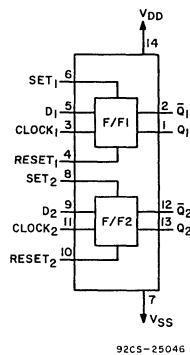


**CD4098B**  
Dual Monostable Multivibrator  
Preliminary

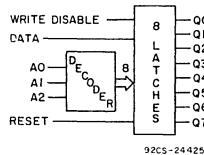
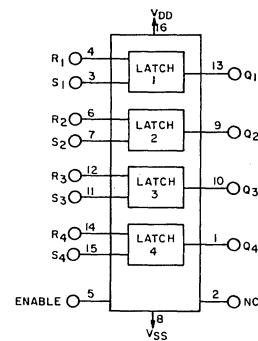
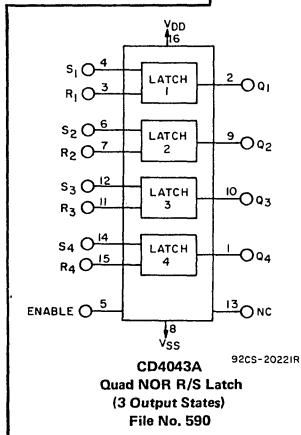
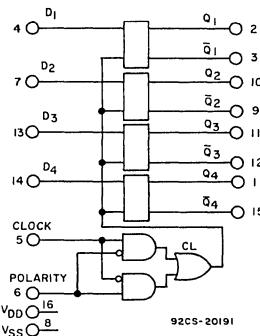


**CD4502B**  
Strobed  
Hex Inverter/Buffer  
Preliminary

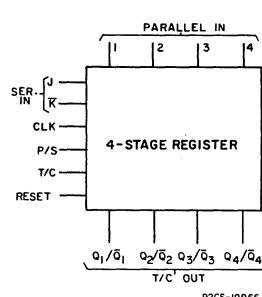
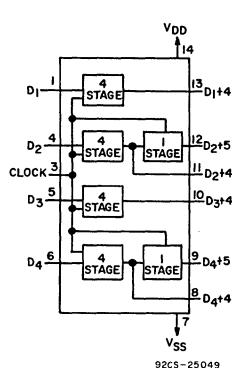
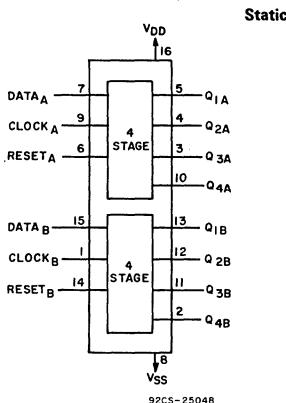
### FLIP-FLOPS



### LATCHES



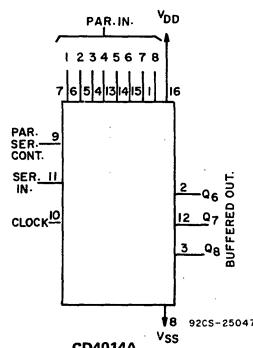
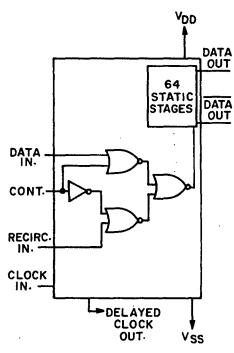
## SHIFT REGISTERS



92CS-25050

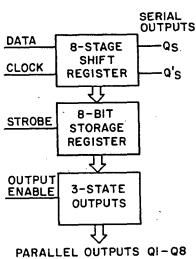
Dual 4-Stage with Serial Input/Parallel Output

File No. 479

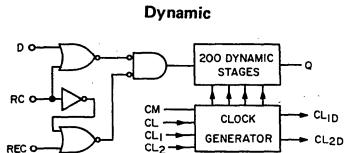
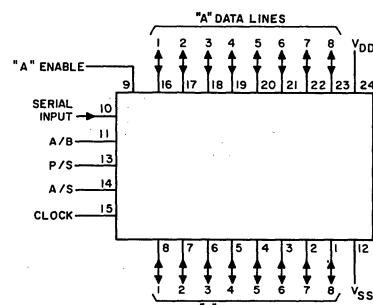


File No. 479

**CD4021A**  
Asynchronous Parallel Input/Serial Output  
Synchronous Serial Input/Serial Output  
File No. 479

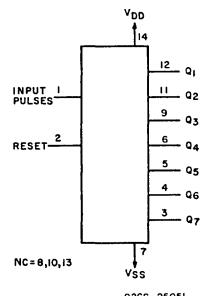


8-Stage Shift-and-Store Bus Register Preliminary

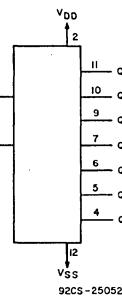


## COUNTERS

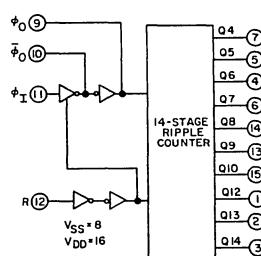
### Binary/Ripple



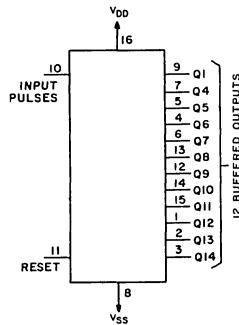
CD4024AD, AE, AF, AK



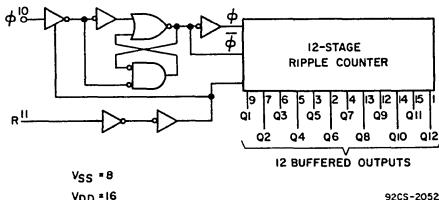
**CD4024AT**



92CS-23762R

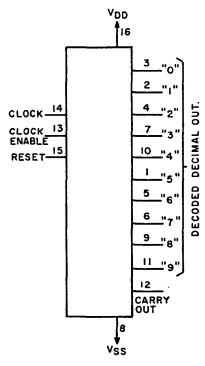


**CD4020A  
14-Stage  
File No. 479**

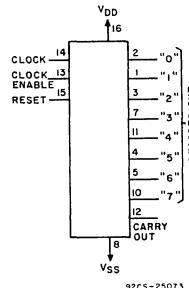


**CD4040A  
12-Stage  
File No. 624**

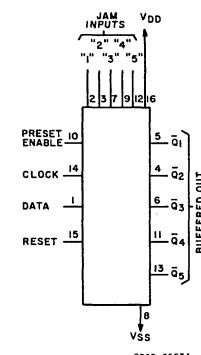
### Synchronous



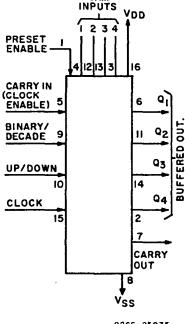
**CD4017A**  
**Decade Counter/Divider**  
**Plus 10 Decoded Decimal Outputs**  
**File No. 479**



**CD4022A**  
**Divide-by-8 Counter/Divider**  
**with 8 Decimal Outputs**  
**File No. 479**

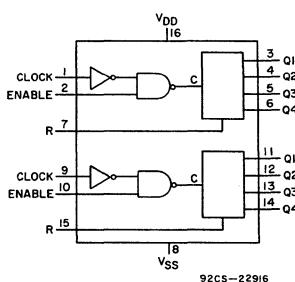
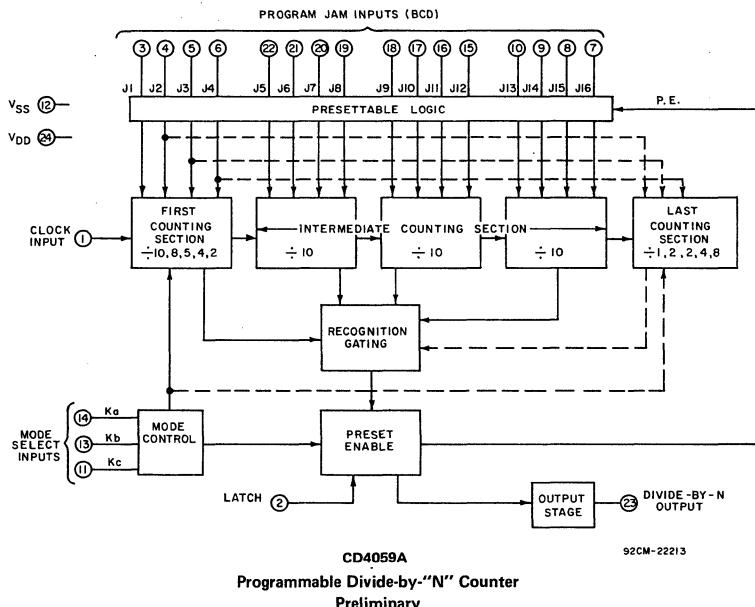


**CD4018A**  
**Presettable Divide-by-"N" Counter**  
**Fixed or Programmable**  
**File No. 479**



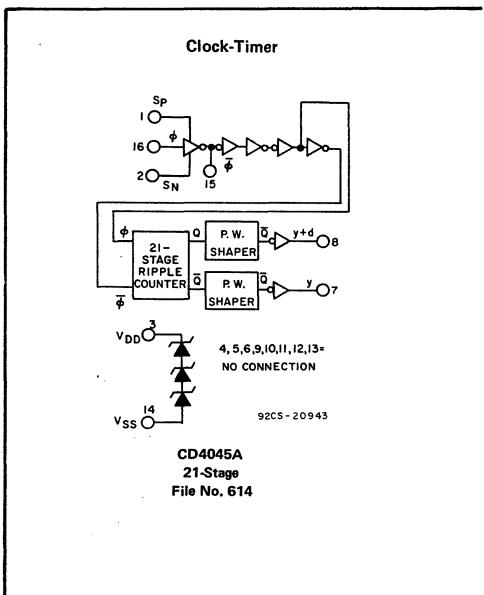
**CD4029A**  
**Presettalbe Up/Down Counter**  
**Binary or BCD-Decade**  
**File No. 503**

**COUNTERS**  
Synchronous (Cont'd)

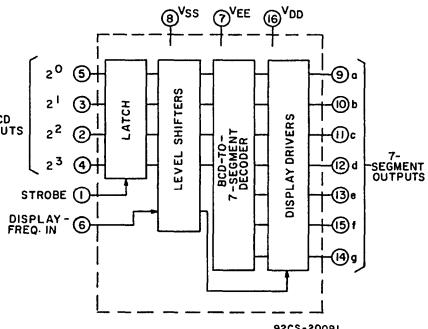
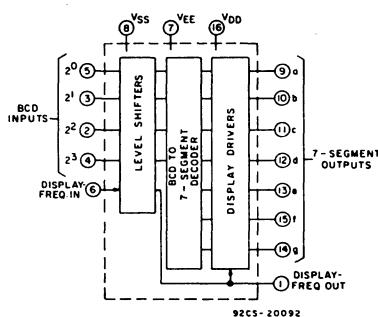
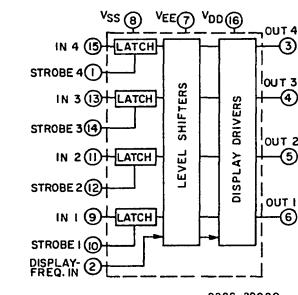
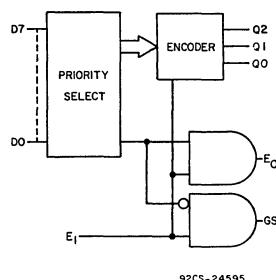
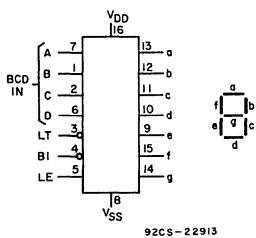
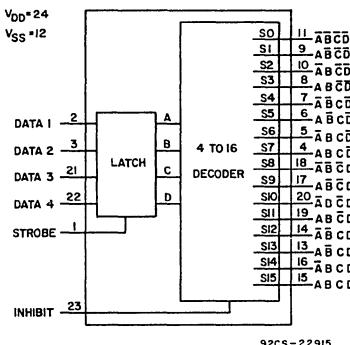
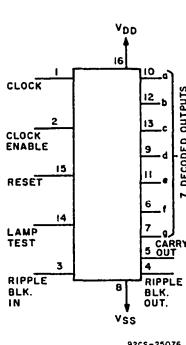
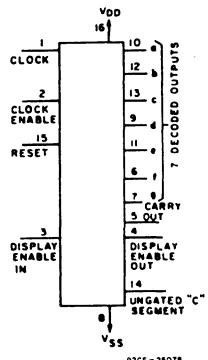


File No. 808

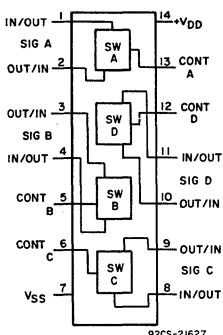
CD4520B  
Dual Binary  
Up-Counter



## DISPLAY COUNTERS/DECODERS/DRIVERS/ENCODERS



## MULTIPLEXERS



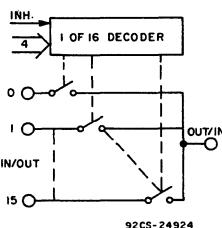
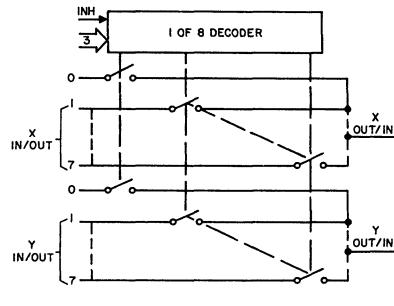
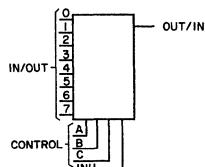
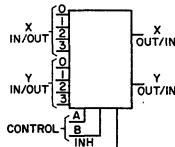
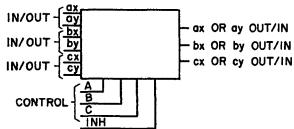
CD4016A

Quad Bilateral Switch

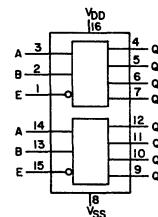
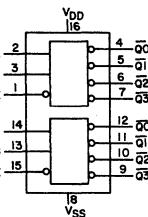
File No. 479

CD4066A

File No. 769

CD4067B  
16-Channel  
Multiplexer/Demultiplexer  
PreliminaryCD4097B  
Differential 8-Channel  
Multiplexer/Demultiplexer  
PreliminaryCD4051A  
Single 8-Channel  
PreliminaryCD4052A  
Differential 4-Channel  
PreliminaryCD4053A  
Triple 2-Channel  
Preliminary

92CS-22708

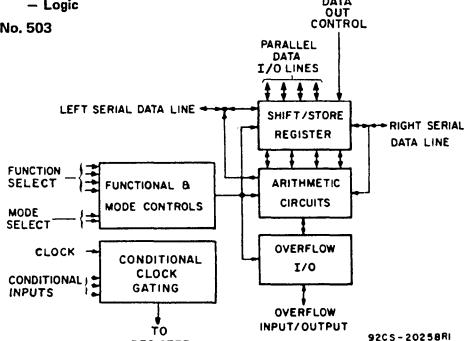
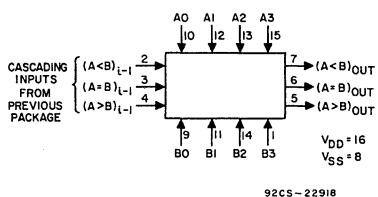
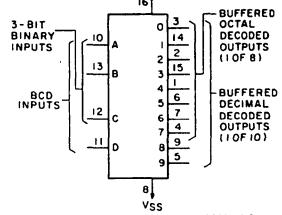
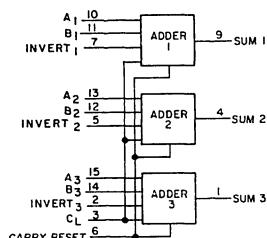
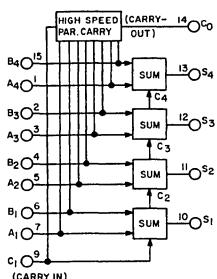
CD4555B  
Dual 1-of-4 Decoder/Demultiplexers  
Output High File No. 858  
CD4556B  
Output Low

92CS-22919

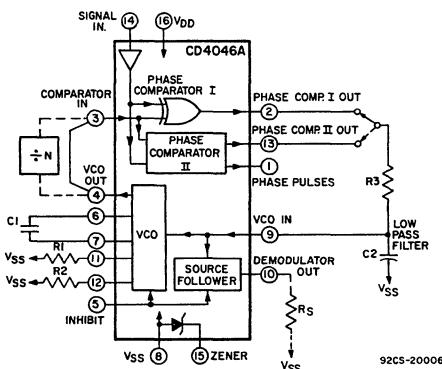
ENABLE	SELECT	INPUTS				OUTPUTS CD4555B				OUTPUTS CD4556B			
		B	A	Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$		
0	0	0	0	0	0	0	1	1	1	1	1	0	
0	0	1	0	0	0	1	0	1	1	0	1	1	
0	1	0	0	0	1	0	0	1	0	1	1	1	
0	1	1	1	1	0	0	0	0	1	1	1	1	
1	X	X	0	0	0	0	0	1	1	1	1	1	

X = DON'T CARE

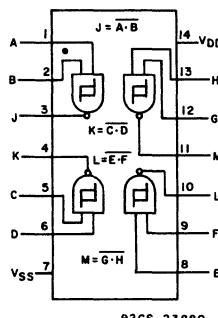
## ARITHMETIC CIRCUITS



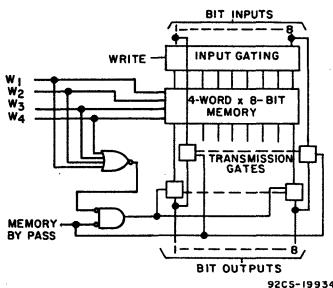
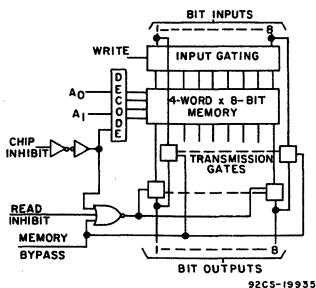
## PHASE-LOCKED LOOP



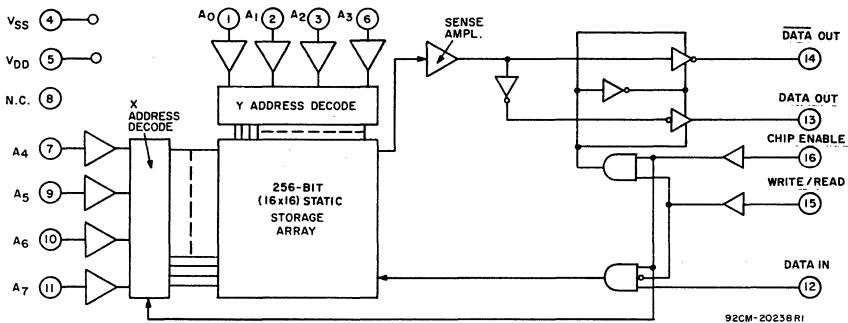
## SCHMITT TRIGGER



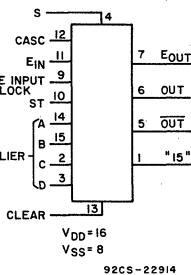
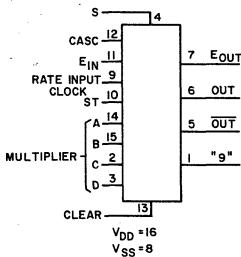
**MEMORIES**  
Word-Organized



Bit-Organized



RATE MULTIPLIERS



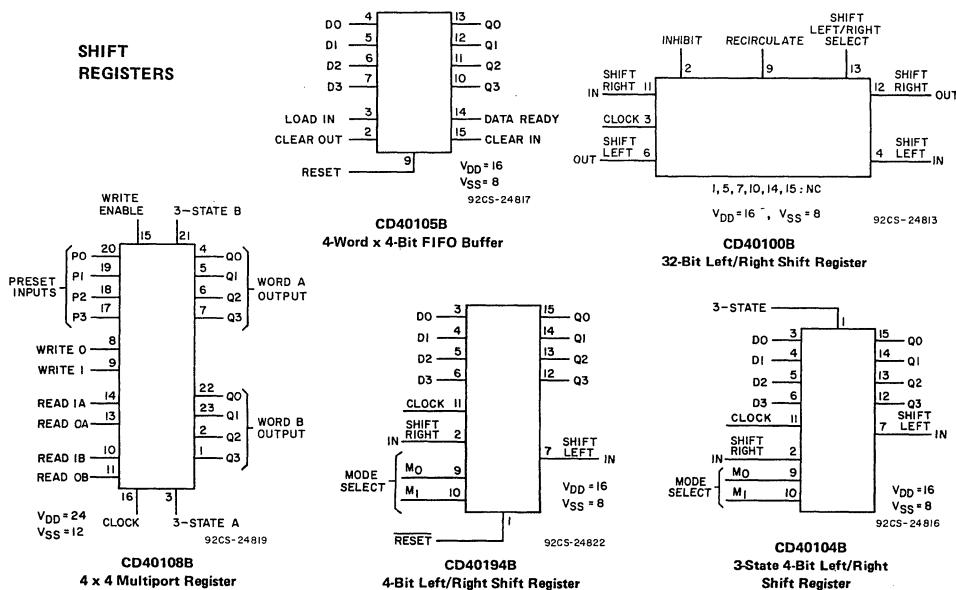
## NEW PRODUCTS PROGRAM

The CD Preliminary COS/MOS types listed below are some of the devices scheduled for introduction during 1975. Logic diagrams and terminal assignment diagrams are shown following the listing.

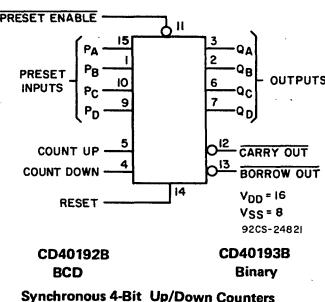
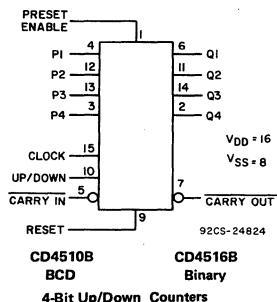
Additional types will also be announced throughout the year. For information concerning announcement dates and product availability, contact your RCA representative or supplier, or watch for announcement in the RCA Solid State Announcement Newsletter "What's New In Solid State" referred to on the inside front cover of this DATABOOK.

Preliminary CD Type	Circuit Description	Similar Industry Type
CD4508B	Dual 4-Bit Latch	MC14508
CD4510B	4-Bit BCD Up/Down Counter	MC14510
CD4516B	4-Bit Binary Up/Down Counter	MC14516
CD40100B	32-Bit Left/Right Shift Register	—
CD40101B	9-Bit Parity Generator & Checker	—
CD40102B	Presetable 8-Bit BCD Down Counter	—
CD40103B	Presetable 8-Bit Binary Down Counter	—
CD40104B	Three State 4-Bit Left/Right Shift Register	—
CD40105B	4-Word X 4-Bit FIFO Buffer	—
CD40106B	Hex Schmitt Trigger Inverter	—
CD40107B	Dual 2-Input NAND Buffer/Driver	—
CD40108B	4 X 4 Multiport Register	—
CD40181B	4-Bit Arithmetic Logic Unit	—
CD40182B	Look-Ahead Carry Block	—
CD40192B	Synchronous 4-Bit BCD Up/Down Counter (Dual Clock)	—
CD40193B	Synchronous 4-Bit Binary Up/Down Counter (Dual Clock)	—
CD40194B	4-Bit Left/Right Shift Register	—

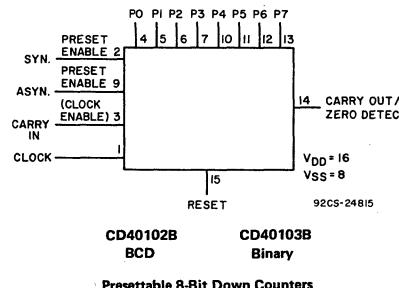
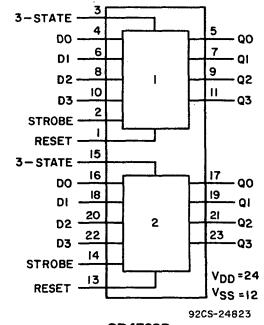
\*Because of the wide interest in COS/MOS parts, RCA reserves the right to limit sample quantities.



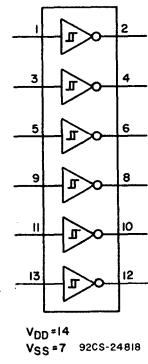
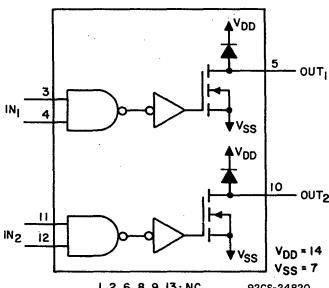
## COUNTERS



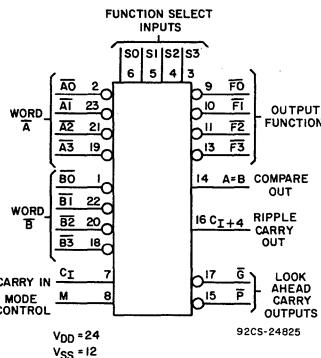
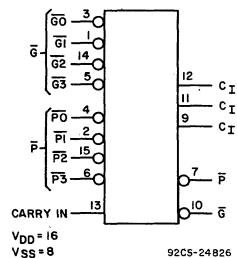
## LATCHES



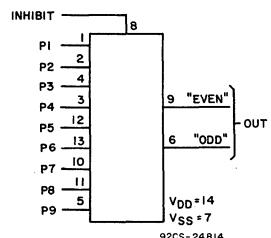
## BUFFERS AND INVERTERS



## ARITHMETIC CIRCUITS



## PARTY GENERATOR



# COS/MOS Design and Operating Considerations

The information on the following pages serves as a brief introduction to COS/MOS specifications, ratings, and performance characteristics. This information is included to help the user avoid problems in connection with over-all systems design. COS/MOS operation, design, and layout fundamentals are discussed in detail in the RCA COS/MOS Integrated Circuits Manual, CMS-271.

## Maximum Ratings

The maximum ratings for all the COS/MOS devices included in this book are as follows:

Characteristic	Symbol	"A" Series	"B" Series	Unit
Supply Voltage	$V_{DD}$ - $V_{SS}$	+15 to -0.5	+18 to -0.5	Vdc
Input Voltage, All Inputs	$V_I$	$V_{SS} \leq V_I \leq V_{DD}$		Vdc
Device Power Dissipation per package	$P_D$	200		mW
Operating-Temperature Range:	T			°C
Ceramic Packages		-55 to +125		°C
Plastic Package		-40 to +85		°C
Storage-Temperature Range:	$T_{stg}$	-65 to +150		°C
Lead Temperature (during soldering) at a distance of 1/16±1/32 inch (1.59±0.79 mm) from case for 10 sec.	$T_{lead}$	+265		°C

## Operating Supply-Voltage Range

COS/MOS integrated circuits are specified in one of two supply-voltage ranges: "A"-series devices operate from 3 to 15 volts, and "B"-series devices from 3 to 18 volts. Logic systems occasionally experience transient conditions on the power-supply line which, when added to the nominal power-bus voltage, could exceed the safe limits of circuits connected to the power bus. Recommended supply-voltage ranges which realistically assess these conditions are 4 to 12 volts for "A"-series devices, and 4 to 15 volts for "B"-series devices.

The recommended maximum power-supply limit is substantially below the minimum primary breakdown limit for the devices to allow for limited power-supply transient and regulation limits. The minimum recommended supply voltage of 4 volts also takes into account transient and regulation

limits. In addition, circuits that operate in a linear mode over a portion of the voltage range, such as RC or crystal oscillators, often require a supply voltage of at least 4 volts.

## Power Dissipation

Power dissipation in a COS/MOS device is composed of two terms, quiescent (dc) dissipation and dynamic (ac) dissipation,  $P_Q$  and  $P_{ac}$  respectively. Quiescent dissipation, generally varying from a few nanowatts for small devices to tens of microwatts for large devices, is due to a combination of leakage effects comprising parasitic junction diodes (normally reverse-biased) and surface effects. Dynamic dissipation is comprised of two elements: (1) "through"-current that exists during the transition from one logic level to the other, when both N-MOS and P-MOS devices are momentarily conducting simultaneously, and (2) power-supply current required to charge the node and output capacitance during switching.

The first component (internal switching) of dynamic dissipation is usually negligible compared to the component associated with charging capacitance, particularly for systems with fast rise and fall times. As transition times increase, however, through-current increases appreciably and the total current is a complex function of the transition times and capacitance.

In most circuits, the ac dissipation ( $P_{ac}$ ) in watts is equal to  $C_O V_{DD}^2 f$ , where  $C_O$  is the effective output capacitance (including load capacitance) in farads,  $V_{DD}$  is the supply voltage in volts, and  $f$  is the frequency in Hz. Because the output capacitance must be charged from  $V_{SS}$  to  $V_{DD}$  once each period, dynamic dissipation increases linearly with frequency and load capacitance, and as the square of the supply voltage  $V_{DD}$ . Each COS/MOS data sheet includes a curve showing dynamic power dissipation as a function of frequency. Fig. 1 shows switching current and voltage waveforms for different values of load capacitance and input rise and fall times.

## System Noise Considerations

In general, COS/MOS devices are much less sensitive to noise on power and ground lines than bipolar logic families (such as TTL or DTL). However, this sensitivity varies as a function of the power-supply voltage, and more importantly as a function of synchronization between noise spikes and input transitions. Good power distribution in digital systems requires that the power bus have a low dynamic impedance; for this purpose, discrete decoupling capacitors should be distributed across the power bus.

## Power-Source Rules

The safe operating procedures listed below can easily be understood by reference to the basic COS/MOS inverter and its gate-oxide protection network plus inherent diodes, as shown in Fig. 2.

- When separate power supplies are used for the COS/MOS

# COS/MOS Design and Operating Considerations

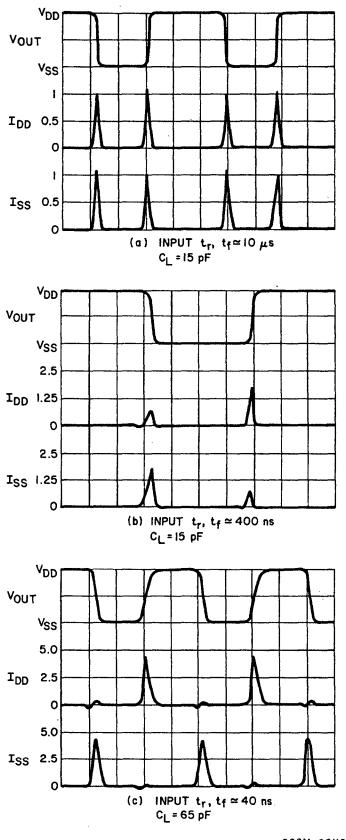


Fig. 1—Switching-current waveforms.

device and for the device inputs, the device power supply should always be turned on before the independent input signal sources, and the input signals should be turned off before the power supply is turned off ( $V_{SS} \leq V_I \leq V_{DD}$  as a maximum limit). This rule will prevent over-dissipation and possible damage of the D2 input-protection diode when the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result in undesired circuit operation although device damage should not result; ac inputs can be rectified by diode D2 to act as a power supply.

2. The power-supply operating voltage should be kept safely below the absolute maximum supply rating, as indicated previously.

3. The power-supply polarity for COS/MOS circuits should not be reversed. The data sheets state that the positive ( $V_{DD}$ ) terminal should never be more than 0.5 volt negative with respect to the negative ( $V_{SS}$ ) terminal ( $V_{DD} - V_{SS} > -0.5 \text{ V}$ ).

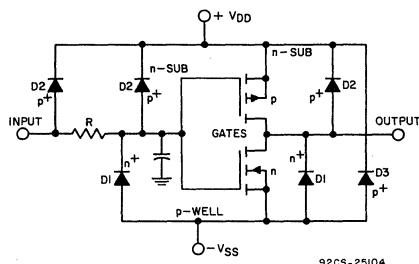


Fig. 2—COS/MOS inverter.

This absolute maximum rating means that reversal of polarity will forward-bias and short the structural and protection diodes between  $V_{DD}$  and  $V_{SS}$ .

4.  $V_{DD}$  should be equal to or greater than  $V_{CC}$  for COS/MOS buffers which have two power supplies (in particular, for CD4009A and CD4010A COS/MOS-to-TTL "down"-conversion devices).

5. Power-source current capability should be limited to as low a value as reasonable to assure good logic operation.

6. Large values of resistors in series with  $V_{DD}$  or  $V_{SS}$  should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

## Gate-Oxide Protection Networks

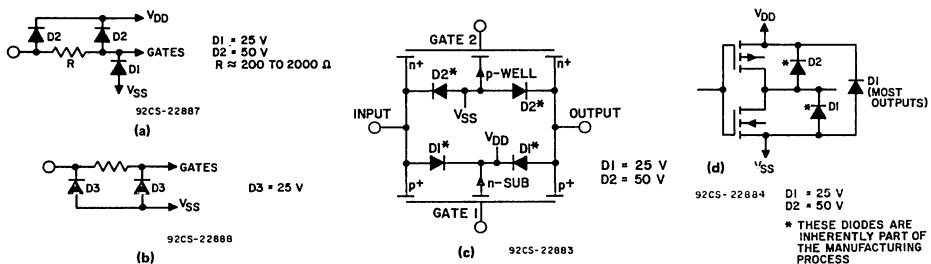
A problem occasionally encountered in handling and testing low-power semiconductor devices, including MOS and small-geometry bipolar devices, has been damage to gate oxide and/or p-n junctions. Fig. 3 shows the gate-oxide protection circuits used to protect COS/MOS circuits from static electricity damage. ICAN-6218 gives further information on protection circuits. Although these circuits are included in all COS/MOS devices, the handling precautions discussed in ICAN-6218 and in ICAN-6000 should be observed.

## Input Signals and Ratings

1. Input signals should be maintained within the power-supply voltage range,  $V_{SS} \leq V_I \leq V_{DD}$ . In applications such as astable and monostable multivibrators, input current can flow and should be limited to the microampere level by use of a resistor in series with the input terminal affected.

2. All COS/MOS inputs should be terminated. When COS/MOS inputs are wired to edge card connectors with COS/MOS drive coming from another PC board, a shunt resistor should be connected to  $V_{DD}$  or  $V_{SS}$  in case the inputs become unterminated with the power supply on.

# COS/MOS Design and Operating Considerations



**Fig. 3—Protection circuits used in COS/MOS devices:** (a) normal gate input protection; (b) CD4059A and CD4050A gate input protection; (c) transmission-gate input-output protection; (d) active (inverter) output protection.

3. When COS/MOS circuits are driven by TTL logic, a "pull-up" resistor should be connected from the COS/MOS input to 5 volts (further information is given in ICAN6602).

4. Input signals should be maintained within the recommended input-signal-swing range.

## Output Rules

1. The power dissipation in a COS/MOS package should not exceed 200 milliwatts. The actual dissipation should be calculated when (a) shorting outputs directly to  $V_{DD}$  or  $V_{SS}$ , (b) driving low-impedance loads, or (c) directly driving the base of a p-n-p or n-p-n bipolar transistor.

2. Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs or across power supplies greater than 5 volts can damage COS/MOS devices.

3. COS/MOS, like active pull-up TTL, cannot be connected in the "wire-OR" configuration because an "on" P-MOS and an "on" N-MOS transistor could be directly shorted across the power-supply rails.

4. Paralleling inputs and outputs of gates is recommended only when the gates are within the same IC package.

5. Output loads should return to a voltage within the supply-voltage range ( $V_{DD}$  to  $V_{SS}$ ).

6. Large capacitive loads (greater than 5000 pF) on COS/MOS buffers or high-current drivers act like short circuits and may over-dissipate output transistors.

7. Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.

## Noise Immunity

The complementary structure of the inverter, common to all COS/MOS logic devices, results in a near-ideal input-output transfer characteristic, with switching point midway (45% to 55%) between the 0 and 1 output logic levels. The result is high dc noise immunity.

Fig. 4 illustrates minimum and maximum transfer characteristics useful for defining noise immunity for an inverter and a

non-inverter. The noise-immunity voltage ( $V_{NL}$ ,  $V_{NH}$ ) is that noise voltage at any one input which will not propagate through the system. Minimum noise immunity is 30% of the supply voltage (20% for some buffer types). Some noise-immunity definitions are given below:

$V_{IL\ max}$  = the maximum input voltage at low-level input for which the output logic level does not change state.

$V_{IH\ min}$  = the minimum input voltage at high-level input for which the output logic level does not change state.

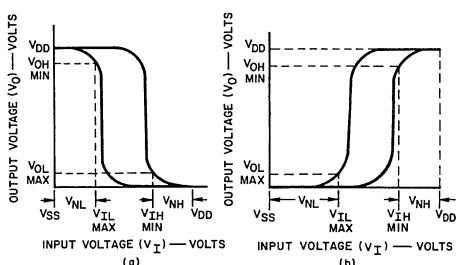
$$V_{NL} = V_{IL}$$

$$V_{NH} = V_{DD} - V_{IH}$$

$V_{OH\ min}$  = minimum high-level output voltage (logic 1 level) for rated  $V_{NL}$  (for an inverting logic function) or  $V_{NH}$  (for a non-inverting logic function).

$V_{OL\ max}$  = maximum low-level output voltage for rated  $V_{NH}$  (for an inverting logic function) or  $V_{NL}$  (for a non-inverting logic function).

Noise immunity increases as the input noise pulse width becomes less than the propagation delay of the circuit. This condition is often described as ac noise immunity. (Further information on noise immunity is given in ICAN-6176.)



**Fig. 4—Minimum and maximum transfer characteristics for (a) inverting logic function, and (b) non-inverting logic function.**

# COS/MOS Design and Operating Considerations

## Clock Rise- and Fall-Time Requirements

All COS/MOS clocked devices have maximum clock rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly because of data ripple-through, false triggering problems, etc. Long rise and fall times on COS/MOS buffer-type inputs cause increased power dissipation which may exceed device capability for power supplies above 5 volts.

## Parallel Clocking

Process variations leading to differences in input threshold voltage among random device samples can cause loss of data between certain synchronously clocked sequential circuits, as

shown in Fig. 5. This problem can be avoided if the clock rise time ( $t_{CL}$ ) is made less than the total of the fixed propagation delay plus the output transition time of the first stage, as determined from the device data for the specific loading condition in effect. Schmitt Trigger circuits such as the CD4093B are an ideal solution to applications requiring wave-shaping.

## Three-State Logic

Three-state logic can be easily implemented by use of a transmission gate in the output circuit; this technique provides a solution to the wire-OR problem in many cases.

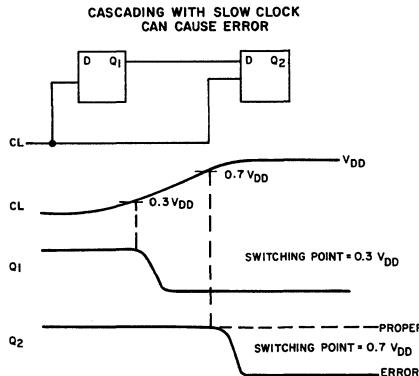


Fig. 5—Error effect that results from a slow clock in cascaded circuits.

# COS/MOS Family Characteristics

## Overview

CD4000A Series — RCA COS/MOS types designed for 3-to-15-volt operation; all package styles

CD4000B Series — RCA COS/MOS types designed for 3-to-18-volt operation; all package styles

CD4500B Series — RCA COS/MOS types similar to industry 4500-series types designed for 3-to-18-volt operation; all package styles

device-current test circuits are also shown on the individual data sheets.

**Output Voltage Levels ( $V_{OL}$  and  $V_{OH}$ ).**  $V_{OL}$  is the logic-“0” or low-level output voltage.  $V_{OH}$  is the logic-“1” or high-level output voltage.  $V_{OL}$  and  $V_{OH}$  are specified under no load with inputs set at  $V_{DD}$  or  $V_{SS}$  (i.e., noise-free input conditions). Values for both “A”-series and “B”-series devices are as follows:

### Low-Level Output ( $V_{OL}$ ):

Typical value at $+25^{\circ}\text{C}$ .....	Ground ( $V_{SS}$ )
Maximum value at $-40^{\circ}\text{C}/-55^{\circ}\text{C}$ .....	0.01V
Maximum value at $+85^{\circ}\text{C}/+125^{\circ}\text{C}$ .....	0.05V

### High-Level Output ( $V_{OH}$ ):

Typical value at $25^{\circ}\text{C}$ .....	$V_{DD}$
Minimum value at $-40^{\circ}\text{C}/-55^{\circ}\text{C}$ .....	( $V_{DD} - 0.01\text{ V}$ )
Minimum value at $+85^{\circ}\text{C}/+125^{\circ}\text{C}$ .....	( $V_{DD} - 0.05\text{ V}$ )

**Voltage and Current Transfer Characteristics.** Curves of voltage and current input/output characteristics are given in the individual data sheets for inverter, gate, and buffer devices.

**DC Noise Immunity ( $V_{NL}$  and  $V_{NH}$ ).** Noise-immunity definitions were covered previously. Values for both “A”-series and “B”-series devices are given below:

$V_{NL}$	$V_{DD}$	$V_{OH}$ (min.)		$V_{NL}$ (at $25^{\circ}\text{C}$ )	
		Inverting SSI Devices	Inverting MSI Devices	Typ.	Max.
	5	3.6	4.2	2.25	1.5
	10	7.2	9.0	4.5	3.0
	15*	10.8	13.5	6.75	—

$V_{NH}$	$V_{DD}$	$V_{OL}$ (max.)		$V_{NH}$ (at $25^{\circ}\text{C}$ )	
		Inverting SSI Devices	Inverting MSI Devices	Typ.	Max.
	5	0.95	1.4	0.8	2.25
	10	2.9	2.8	1.0	4.5
	15*	4.2	1.5	6.75	—

\*Specified for “B” series only.

## Static Electrical Characteristics

**Quiescent Device Current ( $I_L$ ).** The quiescent current is the device current drawn by an IC in the steady-state condition with no load on the output. The IC inputs are tied either to the positive ( $V_{DD}$ ) terminal or the negative ( $V_{SS}$ ) terminal when quiescent current is measured.

Most devices exhibiting typical or “low” leakage currents at room temperature ( $25^{\circ}\text{C}$ ) are dominated by p-n junction leakage. For these devices,  $I_L$  doubles approximately every  $11^{\circ}\text{C}$ . Devices exhibiting leakage currents close to the maximum rating are dominated by surface leakage and will not generally follow an exponential characteristic, i.e., surface leakage current will usually increase at a considerably slower rate than junction leakage as the temperature is increased.

Typical and minimum values for  $I_L$  are given on individual COS/MOS data sheets. For “B”-series devices, these values are standardized for SSI types and for MSI types. Quiescent-

Noise-immunity test circuits are shown on individual device data sheets.

**Output Drive Current ( $I_{DN}$  and  $I_{DP}$ ).**  $I_{DN}$  is the output sink current (existing in the N-MOS device) when the P-MOS device is “off” and the N-MOS device is “on”, i.e., logic “0” state.  $I_{DP}$  is the output source current (existing in the P-MOS device) when the N-MOS device is “off” and the P-MOS device is “on”, i.e., logic “1” state. Output-drive-current values are given in the individual data sheets. For CD4000B-series devices, these values are standardized as follows:

# COS/MOS Family Characteristics

CHARAC- TERISTIC	SYMBOL	$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Drive Current: N-Channel (Sink)	$I_{DN}$	0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	—	mA
		0.5	10	1.1	—	—	0.9	1.8	—	0.65	—	—	
		1.5	15	—	—	—	3	6	—	—	—	—	
P-Channel (Source)	$I_{DP}$	2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—	—	mA
		4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—	—	
		9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—	—	
		13.5	15	—	—	—	-3	-6	—	—	—	—	
Output Drive Current: N-Channel (Sink)	$I_{DN}$	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—	
		1.5	15	—	—	—	3	6	—	—	—	—	
P-Channel (Source)	$I_{DP}$	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—	
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—	
		13.5	15	—	—	—	-3	-6	—	—	—	—	

These charts show that at +25°C drive-current limits are the same for all package styles, i.e., they are standardized for all packages. "B"-series drive-current characteristics curves are also standardized. CD4500B-series devices have the same  $I_{DN}$  characteristics, but in some devices the  $I_{DP}$  capability differs from standard CD4000B-series standards, although it is identical with similar 4500-series industry types. Figs. 6 and 7 show the normalized variation of output currents (source and sink currents) with respect to temperature and voltage for typical "B"-series devices.

Fig. 8 shows a typical test setup for output drive current. The input switches S1, S2, S3, ..., SN are set to positions (or, in sequential logic, sequenced to positions) which will cause the output terminal under test to be at the desired logic level ("0" for  $I_{DN}$ , "1" for  $I_{DP}$ ). Output switch S4 is positioned to connect an ammeter from the output terminal under test to a separate power source which is to be set to the  $V_O$  value specified in the applicable data sheet. Drive current is measured by means of meter M1. Test-circuit connections for individual COS/MOS devices are given in the Appendix.

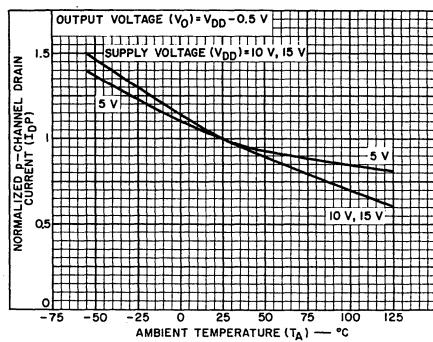
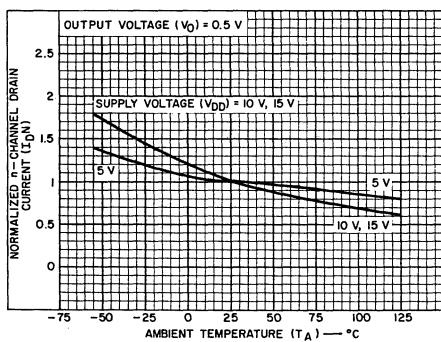


Fig. 6—Variation of normalized sink current ( $I_{DN}$ ) and source current ( $I_{DP}$ ) with temperature.

# COS/MOS Family Characteristics

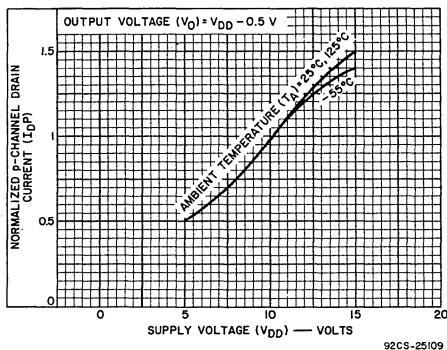
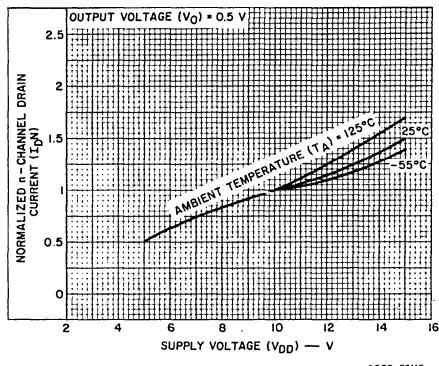


Fig. 7—Variations of normalized sink current ( $I_{DN}$ ) and source current ( $I_{DP}$ ) with supply voltage.

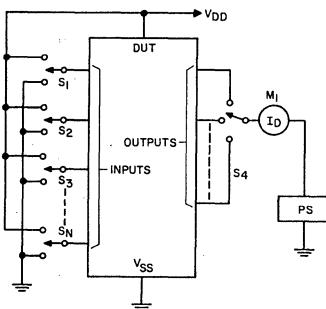


Fig. 8—Output-drive-current test circuit.

**Input Current ( $I_I$ ).** Input current  $I_I$  is the current measured in an input pin with the input voltage at  $V_{DD}$  or  $V_{SS}$ ; it consists only of leakage current existing primarily in protection-circuit diodes.

$I_I$  (typ.) =  $\pm 10 \text{ pA}$  for "A" and "B" series COS/MOS  
 $I_I$  (max.) =  $\pm 1 \mu\text{A}$  for "B" series COS/MOS at  $T_A = 25^\circ \text{C}$ ,  $V_{DD} = 15 \text{ V}$

Fig. 9 shows a typical test setup for input current. Switches  $S_1, S_2, S_3 \dots S_N$  are set to positions which connect the input

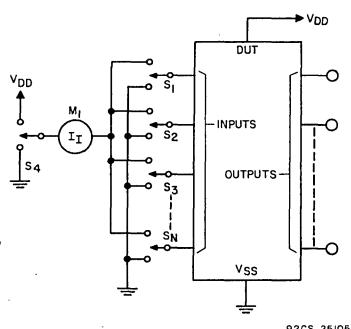


Fig. 9—Input-current test circuit.

terminal under test through current meter  $M_I$  to either  $V_{DD}$  or  $V_{SS}$  (determined by position of  $S_4$ ). Input terminals not under test are connected to  $V_{SS}$ . Output terminals are open. Input current is indicated by meter  $M_I$ .

**Threshold Voltage.** Threshold voltages of n- and p-channel devices generally range from 0.7 to 2.8 volts, centered around 1.5 volts. Noise-immunity specifications, which are shown on all COS/MOS data sheets, provide the necessary controls on device thresholds and are generally useful for commercial applications purposes. Values of threshold voltage are specified for high-reliability COS/MOS devices, and are shown in the High-Reliability Devices DATABOOK, SSD-207. Detailed circuits and connections for threshold-voltage tests are also shown in SSD-207.

## Dynamic Electrical Characteristics

For "A"-series COS/MOS devices, dynamic electrical characteristics are measured at  $V_{DD} = 5 \text{ V}$  and  $10 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ ,  $C_L = 15 \text{ pF}$  and input  $t_r$  and  $t_f = 20 \text{ ns}$ . Typical temperature coefficient for dynamic characteristics is  $|0.3\%/\text{°C}|$  (negative for maximum clock frequency, positive for other time parameters). "B"-series devices are measured at  $V_{DD} = 5 \text{ V}$ ,  $10 \text{ V}$ , and  $15 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ ,  $C_L = 50 \text{ pF}$ , and input  $t_r$  and  $t_f = 20 \text{ ns}$ . Figs. 10-12 show the normalized variation of transition time ( $t_{TLH}$  and  $t_{THL}$ ) and propagation delay time ( $t_{PHL}$  and  $t_{PLH}$ ) with respect to temperature and voltage for "B"-series devices.

# COS/MOS Family Characteristics

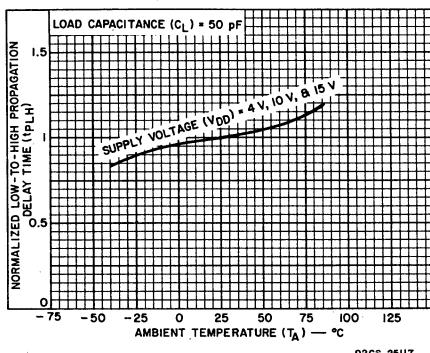
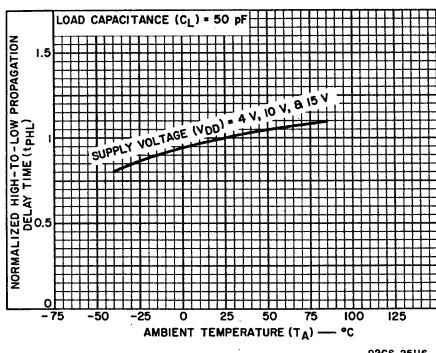
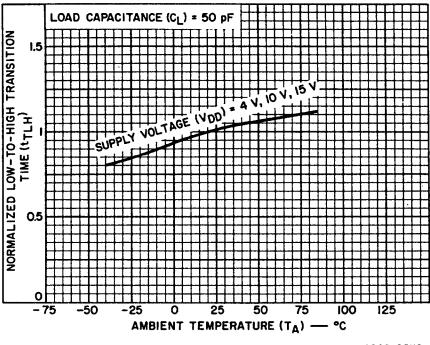
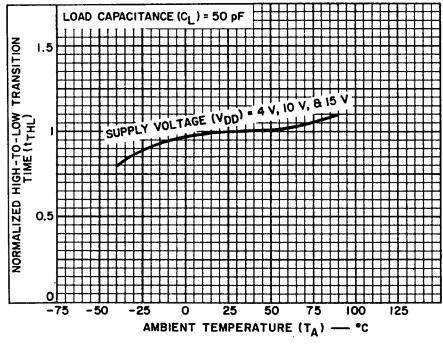


Fig. 10—Variation of normalized transition time ( $t_{TLH}$  and  $t_{THL}$ ) and propagation delay time ( $t_{pHL}$  and  $t_{pLH}$ ) with temperature.

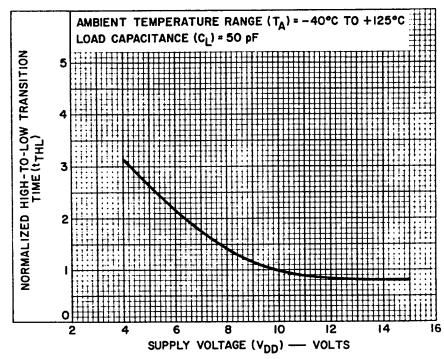
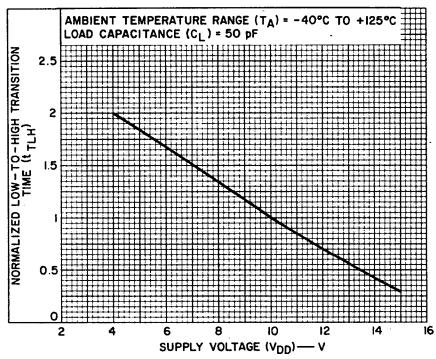


Fig. 11—Variation of normalized transition time ( $t_{TLH}$  and  $t_{THL}$ ) with supply voltage.

# COS/MOS Family Characteristics

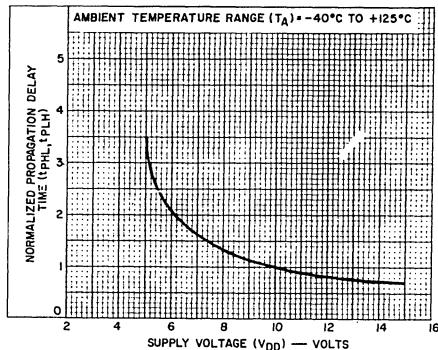


Fig. 12—Variation of normalized propagation delay time ( $t_{PHL}$  and  $t_{PLH}$ ) with supply voltage.

Waveforms for measurement of dynamic characteristics are shown at right. Typical curves of dynamic characteristics are given in the individual data sheets. For CD4000B-series devices, values for transition time ( $t_{TTL}$  and  $t_{THL}$ ) are standardized, as shown below:

$V_{DD}$	Typ.	Max.	Units
5	100	200	ns
10	50	100	ns
15	40	80	ns

Curves of transition time as a function of  $V_{DD}$  are also standardized for these devices, as shown in Fig. 13.

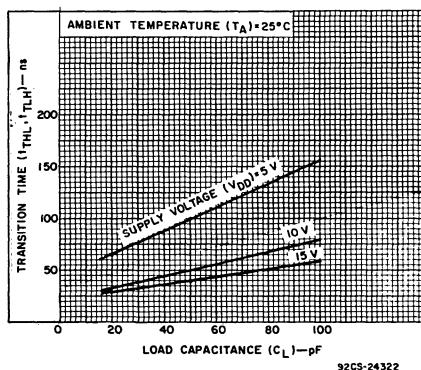
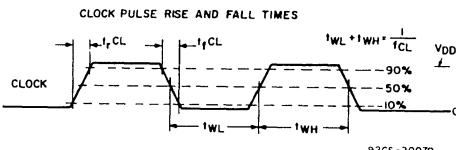
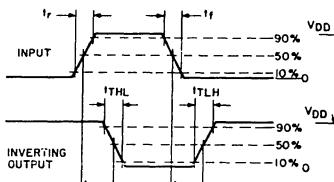
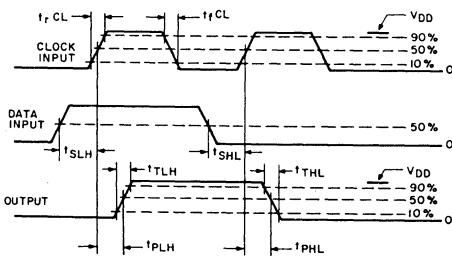


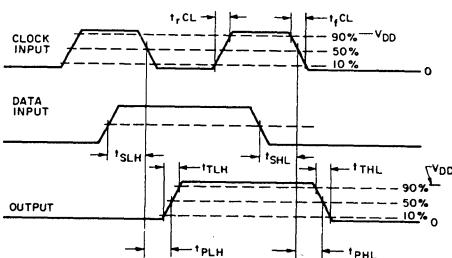
Fig. 13—Variation of transition time ( $t_{TTL}$  and  $t_{THL}$ ) with load capacitance at three levels of supply voltage.



## Transition Times and Propagation Delay Times for Combinational Logic Circuits



## Set-Up Times, Transition Times, and Propagation Delay Times for Positive-Edge-Trigged Sequential Logic Circuits



## Set-Up Times, Transition Times, and Propagation Delay Times for Negative-Edge-Trigged Sequential Logic Circuits

## ORDERING INFORMATION

COS/MOS IC's are available in a wide variety of package designs. These packages are identified by Suffix Letters indicated in the chart shown at right. When ordering COS/MOS devices, it is important that the appropriate suffix letter be affixed to the type number of the device required.

CD4000A and CD4000B Series

PACKAGE	Suffix Letters
Welded-Seal Ceramic Dual-In-Line	D
Plastic Dual-In-Line	E
Ceramic Dual-In-Line	F
Ceramic Flat Pack	K
Chip	H
TO-5 Style	T

## COS/MOS PACKAGES AND LEAD FORMS



H-1383R1



H-1703



H-1757



H-1803

14-Lead  
Flat Pack "K"

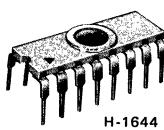
16-Lead  
Flat Pack "K"

24-Lead  
Flat Pack "K"

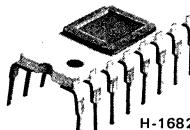
28-Lead  
Flat Pack "K"



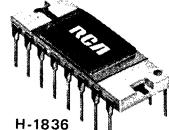
14-Lead Welded-Seal  
Dual-in-Line  
Ceramic "D"



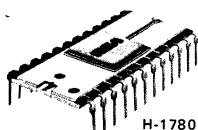
16-Lead Welded-Seal  
Dual-in-Line  
Ceramic "D"



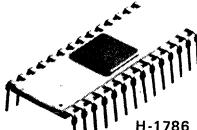
16-Lead Welded-Seal  
Dual-in-Line  
Ceramic "D"



16-Lead Welded-Seal  
Dual-in-Line Side-  
Brazed Ceramic "D"



24-Lead Welded-Seal  
Dual-in-Line  
Ceramic "D"



28-Lead Welded-Seal  
Dual-in-Line  
Ceramic "D"



14-Lead  
Dual-in-Line Ceramic "F"



16-Lead  
Dual-in-Line Ceramic "F"



14-Lead Dual-in-  
Line Plastic "E"



16-Lead Dual-in-  
Line Plastic "E"



12-Lead  
TO-5 "T"

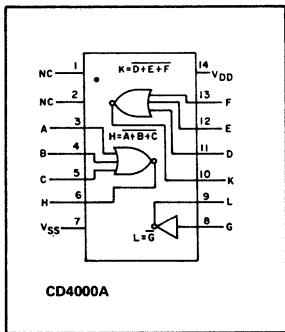
# **Technical Data**

**Digital Integrated Circuits**

Monolithic Silicon

**CD4000A, CD4001A****CD4002A, CD4025A**

Types

**COS/MOS NOR Gates  
(Positive Logic)***Special Features*

- Medium speed operation . . . . .  $t_{PHL} = t_{PLH} = 25 \text{ ns}$  (typ.) at  $C_L = 15 \text{ pF}$

- Low "high"- and "low"-level output impedance . . . . .  $500\Omega$  and  $200\Omega$  (typ.), respectively at  $V_{DD} - V_{SS} = 10 \text{ V}$

## Dual 3 Input

plus Inverter CD4000AD, CD4000AE, CD4000AF, CD4000AK

Quad 2 Input CD4001AD, CD4001AE, CD4001AF, CD4001AK

Dual 4 Input CD4002AD, CD4002AE, CD4002AF, CD4002AK

Triple 3 Input CD4025AD, CD4025AE, CD4025AF, CD4025AK

The combination of these devices and the RCA NAND positive logic gate types CD4011A, CD4012A, and CD4023A can account for appreciable package-count savings in various logic function configurations.

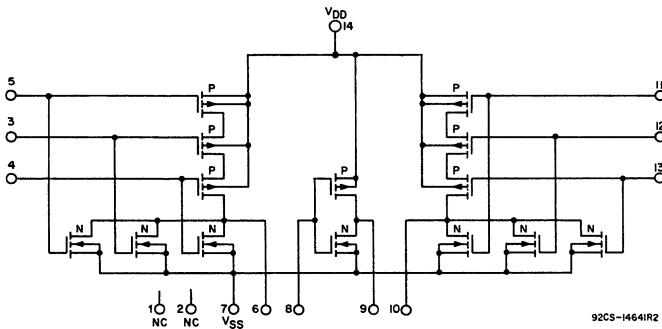
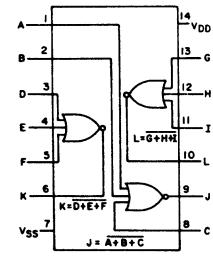
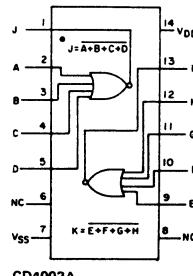
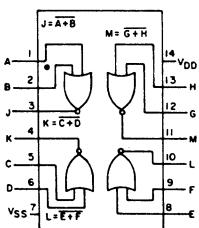


Fig.1.1—Schematic diagram for type CD4000A.

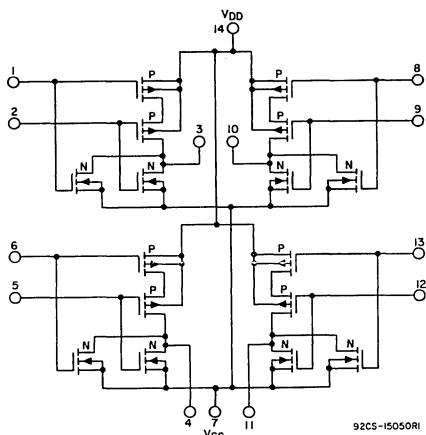


Fig. 1.2—Schematic diagram for type CD4001A.

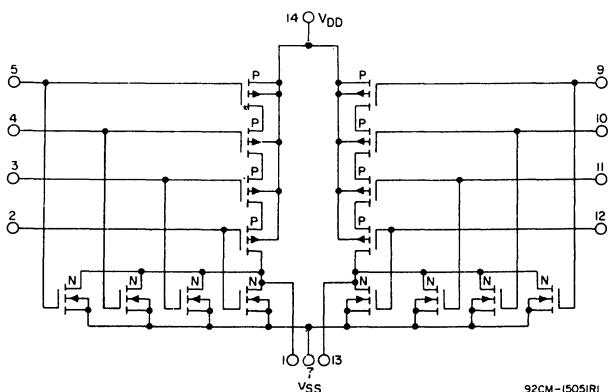


Fig. 1.3—Schematic diagram for type CD4002A.

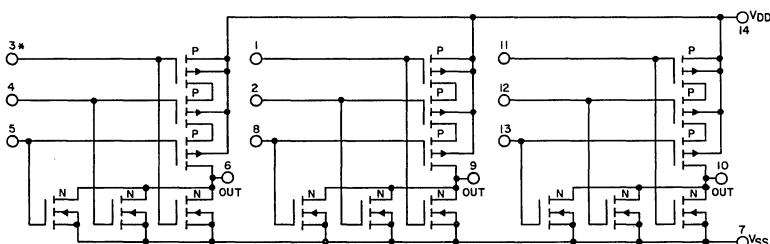


Fig. 1.4—Schematic diagram for type CD4025A.

92CS-17184

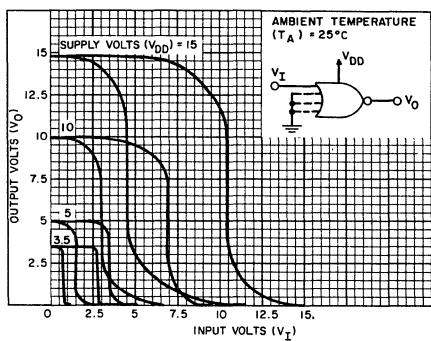
**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARAC TERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4000AD, CD4001AD, CD4002AD, CD4025AD, CD4000AK, CD4001AK, CD4002AK, CD4025AK, CD4000AF, CD4001AF, CD4002AF, CD4025AF								
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C		
Quiescent Device Current	$I_L$		5	—	—	0.05	—	0.001	0.05	—	—	3
			10	—	—	0.1	—	0.001	0.1	—	—	6
Quiescent Device Dissipation/Package	$P_D$		5	—	—	0.25	—	0.005	0.25	—	—	15
			10	—	—	1	—	0.01	1	—	—	60
Output Voltage: Low-Level	$V_{OL}$	$V_I = V_{DD}$ $I_O = OA$	5	—	—	0.01	—	0	0.01	—	—	0.05
			10	—	—	0.01	—	0	0.01	—	—	0.05
High-Level	$V_{OH}$	$V_I = V_{SS}$ $I_O = OA$	5	4.99	—	—	4.99	5	—	4.95	—	—
			10	9.99	—	—	9.99	10	—	9.95	—	—
Noise Immunity (Any Input) For Definition, See Appendix	$V_{NL}$	$I_O = O$	3.6	5	1.5	—	—	1.5	2.25	—	1.4	—
			7.2	10	3	—	—	3	4.5	—	2.9	—
	$V_{NH}$		0.95	5	1.4	—	—	1.5	2.25	—	1.5	—
			2.9	10	2.9	—	—	3	4.5	—	3	—
Output Drive Current: N-Channel	$I_{DN}$	$V_I = V_{DD}$	0.4*	5	0.5	—	—	0.40	1	—	0.28	—
			0.5	—	—	1.1	—	0.9	2.5	—	0.65	—
P-Channel	$I_{DP}$	$V_I = V_{SS}$	2.5#	5	-0.62	—	—	-0.5	-2	—	-0.35	—
			9.5	10	-0.62	—	—	-0.5	-1	—	-0.35	—
Input Current	$I_I$		—	—	—	—	—	10	—	—	—	pA

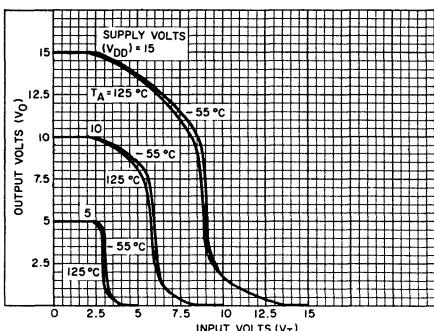
\* Maximum noise-free low-level Bipolar output voltage.

# Minimum noise-free high-level Bipolar output voltage.

◆ See Appendix.



92CS-17779



92CS-17780

Fig. 1.5—Min. & max. voltage transfer characteristics.

Fig. 1.6—Typ. voltage transfer characteristics as a function of temp.

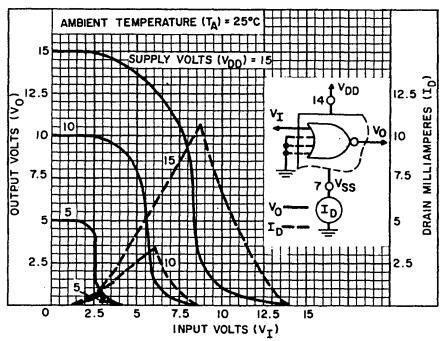
**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								CHARAC TERISTIC CURVES & TEST CIRCUITS Fig. No.			
				CD4000AE, CD4001AE, CD4002AE, CD4025AE											
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C					
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
				5	—	0.5	—	0.005	0.5	—	—	15	$\mu A$		
				10	—	—	5	—	0.005	5	—	30	$\mu A$		
Quiescent Device Dissipation/Package	$P_D$			5	—	—	2.5	—	0.025	2.5	—	—	$\mu W$		
				10	—	—	50	—	0.05	50	—	300	$\mu W$		
Output Voltage: Low-Level	$V_{OL}$	$V_I = V_{DD}$	$I_O = 0A$	5	—	—	0.01	—	0	0.01	—	—	0.05		
				10	—	—	0.01	—	0	0.01	—	—	0.05		
High-Level	$V_{OH}$	$V_I = V_{SS}$	$I_O = 0A$	5	4.99	—	—	4.99	5	—	4.95	—	V		
				10	9.99	—	—	9.99	10	—	9.95	—	V		
Noise Immunity (Any Input) For Definition, See Appendix	$V_{NL}$	$I_O = 0$	3.6	5	1.5	—	1.5	2.25	—	1.4	—	—	V		
			7.2	10	3	—	3	4.5	—	2.9	—	—	V		
	$V_{NH}$		0.95	5	1.4	—	1.5	2.25	—	1.5	—	—	V		
			2.9	10	2.9	—	3	4.5	—	3	—	—	V		
Output Drive Current: N-Channel	$I_{DN}$	$V_I = V_{DD}$	0.4*	5	0.35	—	0.3	1	—	0.24	—	—	mA		
			0.5	10	0.72	—	0.6	2.5	—	0.48	—	—	mA		
P-Channel	$I_{DP}$	$V_I = V_{SS}$	2.5#	5	0.35	—	-0.3	-2	—	-0.24	—	—	mA		
			9.5	10	-0.3	—	-0.25	-1	—	-0.2	—	—	mA		
Input Current	$I_I$	—				—	—	—	10	—	—	—	pA		

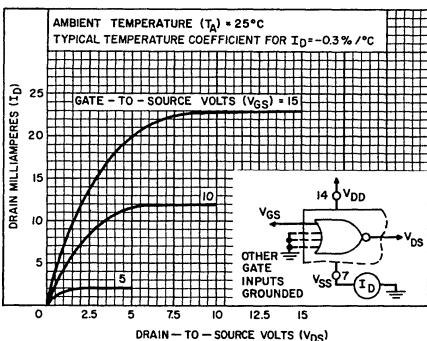
\* Maximum noise-free low-level Bipolar output voltage.

# Minimum noise-free high-level Bipolar output voltage.

♦ See Appendix.



92CS-17776



92CS-17777

Fig. 1.7—Typ. current & voltage transfer characteristics.

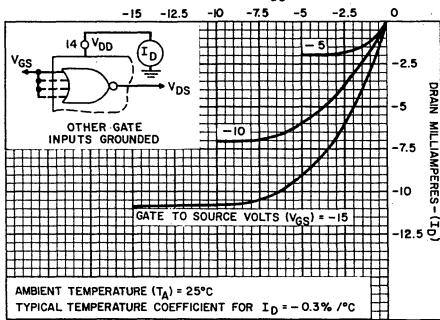
Fig. 1.8—Typ. n-channel drain characteristics.

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15\text{pF}$ , and input rise and fall times = 20 ns**Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\% / ^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4000AD, AF, AK CD4001AD, AF, AK CD4002AD, AF, AK CD4025AD, AF, AK			CD4000AE, CD4001AE CD4002AE, CD4025AE					
			V <sub>DD</sub> (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>		5	—	35	50	—	35	80	ns	1.13
			10	—	25	40	—	25	55		
Low-to-High Level	t <sub>PLH</sub>		5	—	35	95	—	35	120	ns	1.13
			10	—	25	45	—	25	65		
Transition Time: High-to-Low Level	t <sub>THL</sub>		5	—	65	125	—	65	200	ns	1.14
			10	—	35	70	—	35	115		
Low-to-High Level	t <sub>TLH</sub>		5	—	65	175	—	65	300	ns	1.14
			10	—	35	75	—	35	125		
Input Capacitance	C <sub>I</sub>	Any Input	—	5	—	—	5	—	pF	—	—

**DYNAMIC ELECTRICAL CHARACTERISTICS (Driving TTL,DTL) AT  $T_A = 25^\circ\text{C}$ ,  $V_{DD}-V_{SS} = 5\text{V}$ ,  $C_L = 5\text{pF}$** 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES Fig. No.	
			CD4000AD, AF, AK CD4001AD, AF, AK CD4002AD, AF, AK CD4025AD, AF, AK			CD4000AE, CD4001AE CD4002AE, CD4025AE					
			Driving TTL,DTL	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time: High-To-Low Level	t <sub>PHL</sub>	$R_L = 2\text{k}\Omega$ Med. Power	—	35	—	—	35	—	—	ns	1.15
		$R_L = 20\text{k}\Omega$ Low Power	—	35	—	—	35	—	—		
Low-To-High Level	t <sub>PLH</sub>	$R_L = 2\text{k}\Omega$ Med. Power	—	15	—	—	15	—	—	ns	1.16
		$R_L = 20\text{k}\Omega$ Low Power	—	20	—	—	20	—	—		
Transition Time	t <sub>THL</sub>	$R_L = 2\text{k}\Omega$ Med. Power	—	40	—	—	40	—	—	ns	—
	t <sub>TLH</sub>	$R_L = 20\text{k}\Omega$ Low Power	—	40	—	—	40	—	—		

DRAIN-TO-SOURCE VOLTS ( $V_{DS}$ )

92CS-17776

Fig.1.9-Typ. p-channel drain characteristics.

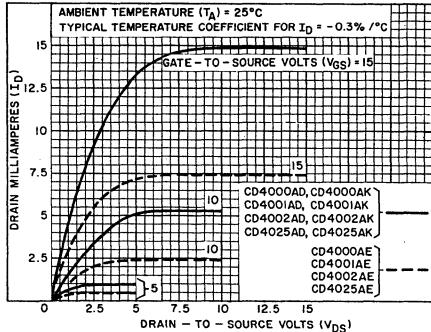


Fig.1.10-Min. n-channel drain characteristics.

92CS-17853

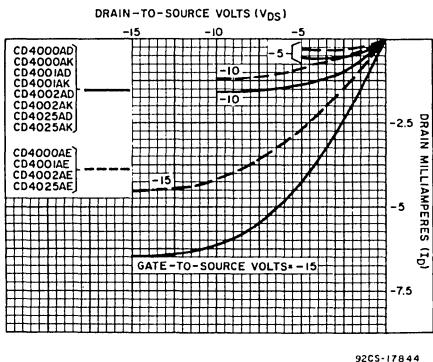
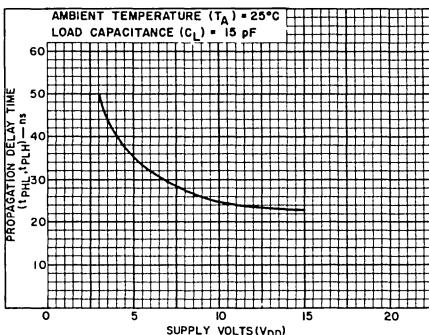
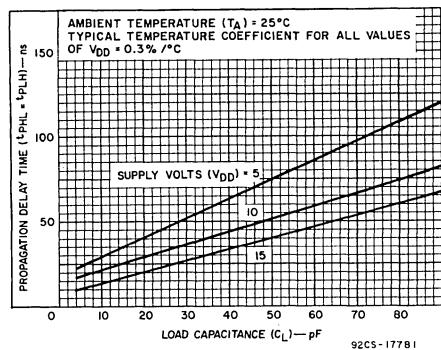
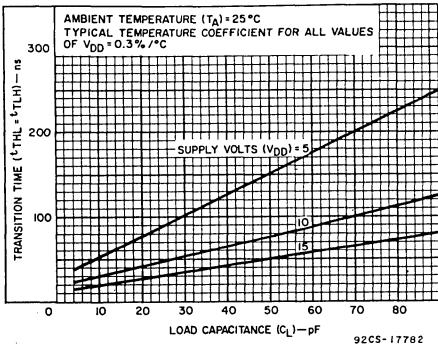
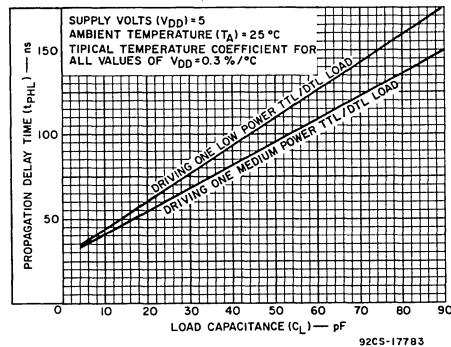
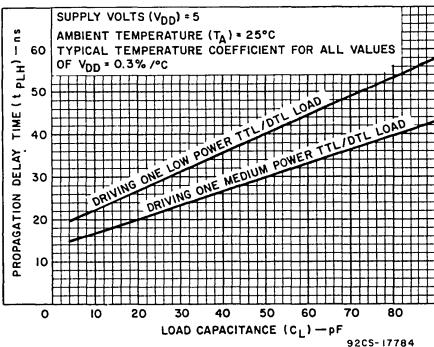


Fig. 1.11—Min. p-channel drain characteristics.

Fig. 1.12—Typ. propagation delay time vs.  $V_{DD}$ .Fig. 1.13—Typ. propagation delay time vs.  $C_L$ .Fig. 1.14—Typ. transition time vs.  $C_L$ .Fig. 1.15—Typ. low-level propagation delay time vs.  $C_L$  — driving TTL & DTL.Fig. 1.16—Typ. high-level propagation delay time vs.  $C_L$  — driving TTL & DTL.

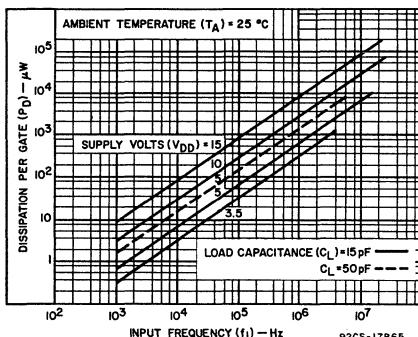


Fig. 1.17 — Typ. dissipation characteristics.

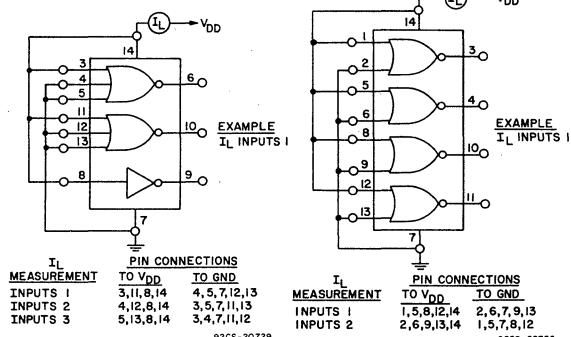


Fig. 1.18 — Quiescent device current test circuit for CD4000A.

Fig. 1.19 — Quiescent device current test circuit for CD4001A.

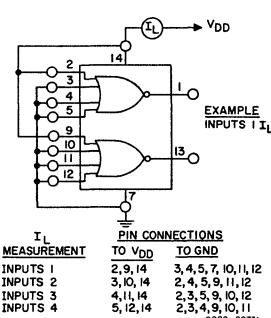


Fig. 1.20 — Quiescent device current test circuit for CD4002A.

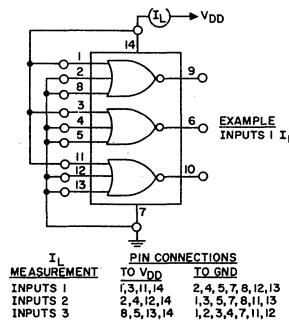


Fig. 1.21 — Quiescent device current test circuit for CD4025A.

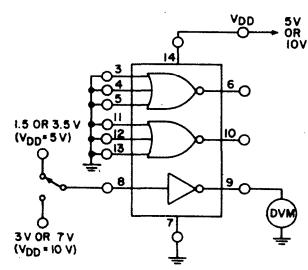


Fig. 1.22 — Noise immunity test circuit for CD4000A.

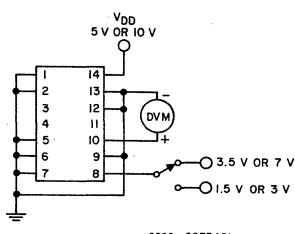


Fig. 1.23 — Noise immunity test circuit for CD4001A.

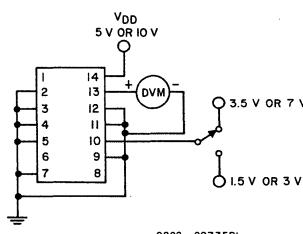


Fig. 1.24 — Noise immunity test circuit for CD4002A.

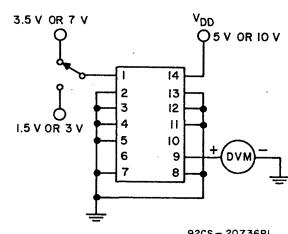
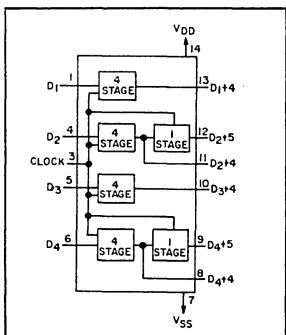


Fig. 1.25 — Noise immunity test circuit for CD4025A.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4006AD, CD4006AF****CD4006AE, CD4006AK**

## COS/MOS 18-Stage Static Shift Register

### Special Features

- Fully static operation
- Up to 5 MHz shifting rates
- Permanent register storage with clock line "high" or "low" — no information recirculation required

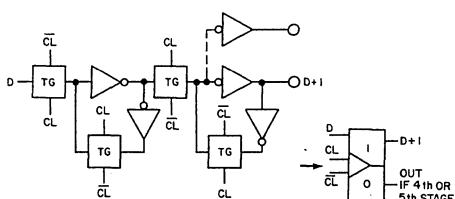
### Applications

- Serial shift registers
- Time delay circuits
- Frequency division

CD4006A types are comprised of 4 separate "shift register" sections; two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent "single rail" data path.

A common clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the clock.

Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.

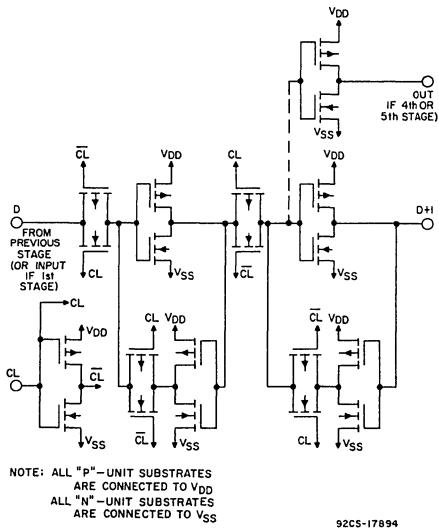


TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL ▲	D+1
0	/	0
1	/	1
X	/	NC

NC = NO CHANGE  
X = DON'T CARE  
▲ = LEVEL CHANGE

92CS-17887

Fig.3.2—Schematic diagram (one register stage)  
for type CD4006A.Fig.3.1—Logic diagram and truth table (one register stage)  
for type CD4006A.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.
				CD4006AD, CD4006AK, CD4006AF										
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C				
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
	5	10	-	-	0.5	-	0.01	0.5	-	-	30	μA	3.11	
Quiescent Device Dissipation/Package			$P_D$			-	-	1	-	0.01	1	-	-	60
	5	10	-	-	2.5	-	0.05	2.5	-	-	150			
Output Voltage: Low-Level			$V_{OL}$			-	-	10	-	0.1	10	-	-	600
	5	10	-	-	0.01	-	0	0.01	-	-	0.05			
High-Level	$V_{OH}$	5	10	4.99	-	--	4.99	5	-	4.95	-	-	V	-
				9.99	-	--	9.99	10	-	9.95	-	-		
Noise Immunity (Any Input)	$V_{NL}$	0.8	5	1.5	-	-	1.5	2.25	-	1.4	-	-	V	3.12
			1	10	3	-	-	3	4.5	-	2.9	-	-	V
<i>For Definition, See Appendix</i>	$V_{NH}$	4.2	5	1.4	-	-	1.5	2.25	-	1.5	-	-		
			9	10	2.9	-	-	3	4.5	-	3	-	-	
Output Drive Current: N-Channel	$I_{DN}$	0.5	5	0.155	-	-	0.125	0.25	-	0.085	-	-	mA	3.3
			0.5	10	0.31	-	-	0.25	0.5	-	0.175	-	-	
P-Channel	$I_{DP}$	4.5	5	-0.125	-	-	-0.1	-0.15	-	-0.07	-	-	mA	3.4
			9.5	10	-0.25	-	-	-0.2	-0.3	-	-0.14	-	-	
Input Current	$I_I$			-	-	-	-	10	-	-	-	-	pA	-

♦ See Appendix.

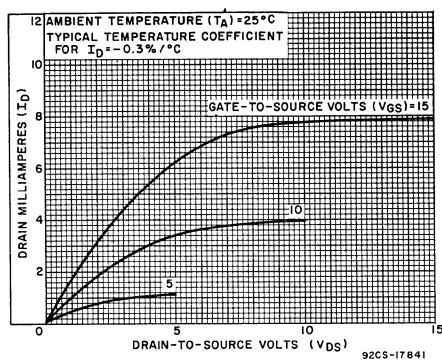


Fig.3.3—Typ. n-channel drain characteristics.

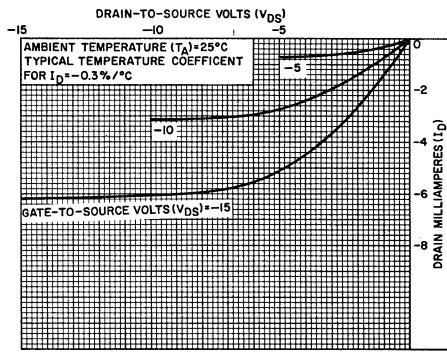


Fig.3.4—Typ. p-channel drain characteristics.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS			
			CD4006AE													
			-40°C			25°C			85°C							
Quiescent Device Current	$I_L$		5	—	—	5	—	0.03	5	—	—	70	$\mu A$	3.11		
			10	—	—	10	—	0.05	10	—	—	140				
Quiescent Device Dissipation/Package	$P_D$		5	—	—	25	—	0.15	25	—	—	350	$\mu W$	—		
			10	—	—	100	—	0.5	100	—	—	1400				
Output Voltage: Low-Level	$V_{OL}$		5	—	—	0.01	—	0	0.01	—	—	0.05	V	—		
			10	—	—	0.01	—	0	0.01	—	—	0.05				
High-Level	$V_{OH}$		5	4.99	—	—	4.99	5	—	4.95	—	—	V	—		
			10	9.99	—	—	9.99	10	—	9.95	—	—				
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	V	3.12		
			1	10	3	—	—	3	4.5	—	2.9	—				
For Definition, See Appendix	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	V	3.12		
			9	10	2.9	—	—	3	4.5	—	3	—				
Output Drive Current: N-Channel	$I_{DN}$		0.5	5	0.072	—	—	0.06	0.25	—	0.048	—	mA	3.3 3.5♦		
			0.5	10	0.15	—	—	0.125	0.5	—	0.10	—				
P-Channel	$I_{DP}$		4.5	5	-0.06	—	—	-0.05	-0.15	—	-0.04	—	mA	3.4 3.6♦		
			9.5	10	-0.12	—	—	-0.1	-0.3	—	-0.08	—				
Input Current	$I_I$		—	—	—	—	—	10	—	—	—	—	pA	—		

♦ See Appendix.

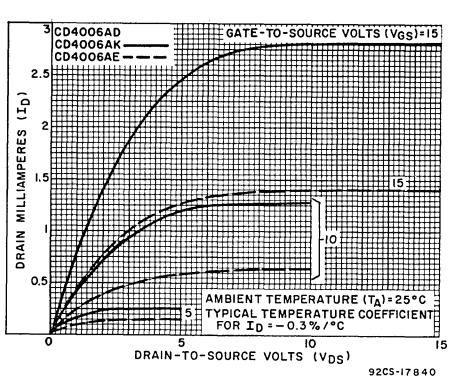


Fig. 3.5—Min. n-channel drain characteristics.

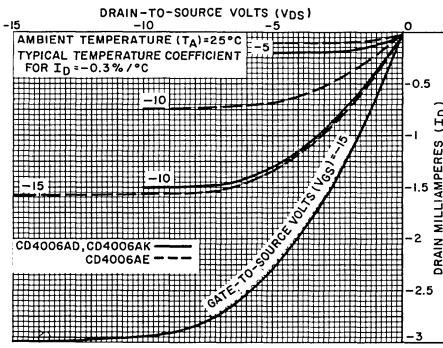


Fig. 3.6—Min. p-channel drain characteristics.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns except  $t_{rCL}, t_{fCL}$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$  (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	$V_{DD}$ (Volts)	LIMITS						CHARAC- TERIS- TIC CURVES & TEST CIRCUITS Fig. No.	
				CD4006AD, CD4006AK CD4006AF			CD4006AE				
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time	$t_{PHL} =$ $t_{PLH}$		5	—	250	400	—	250	500	ns	3.7
			10	—	125	200	—	125	250		
Transition Time	$t_{THL} =$ $t_{TLH}$		5	—	250	400	—	250	500	ns	3.8
			10	—	125	200	—	125	250		
Minimum Clock Pulse Width	$t_{WL} =$ $t_{WH}$		5	—	200	500	—	200	830	ns	—
			10	—	100	200	—	100	250		
Clock Rise & Fall Time	$t_{rCL} =$ $t_{fCL}^*$		5	—	—	15	—	—	15	$\mu\text{s}$	—
			10	—	—	5	—	—	5		
Set-Up Time			5	—	50	80	—	50	100	ns	—
			10	—	25	40	—	25	50		
Maximum Clock Frequency	$f_{CL}$		5	1	2.5	—	0.6	2.5	—	MHz	3.10
			10	2.5	5	—	2	5	—		
Input Capacitance	$C_I$	Data Input Clock Input	—	—	5	—	—	5	—	pF	—

- \* If more than one unit is cascaded  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the output driving stage for the estimated capacitive load.

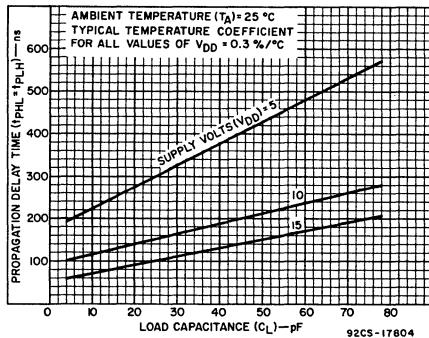


Fig. 3.7—Typ. propagation delay time vs.  $C_L$ .

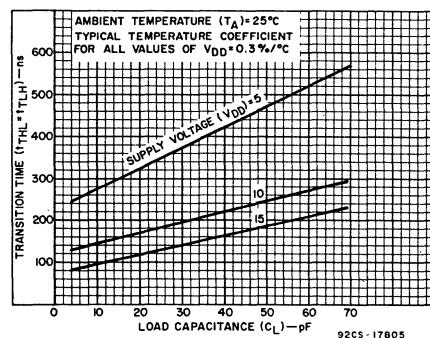


Fig. 3.8—Typ. transition time vs.  $C_L$ .

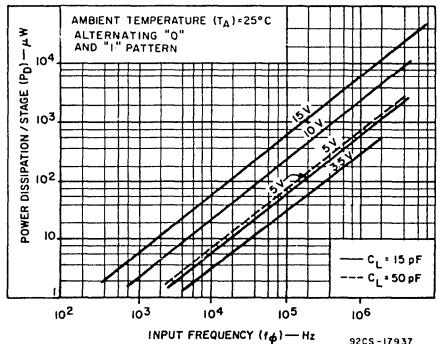


Fig.3.9—Typ. dissipation characteristics.

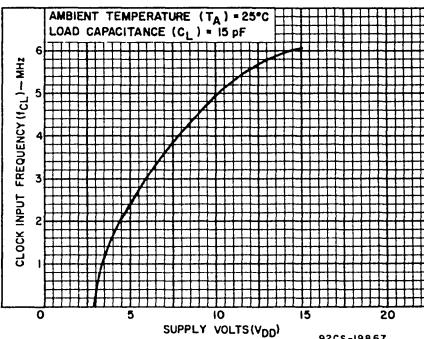
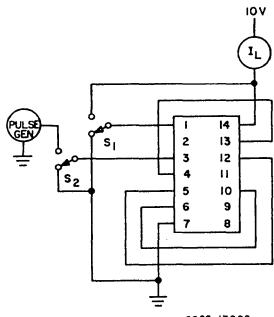
Fig.3.10—Typ. input clock frequency vs.  $V_{DD}$ .

Fig.3.11—Quiescent device current test current.

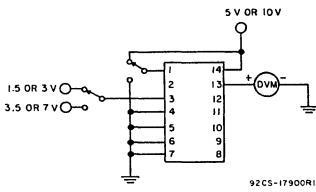


Fig.3.12—Noise immunity test circuit.

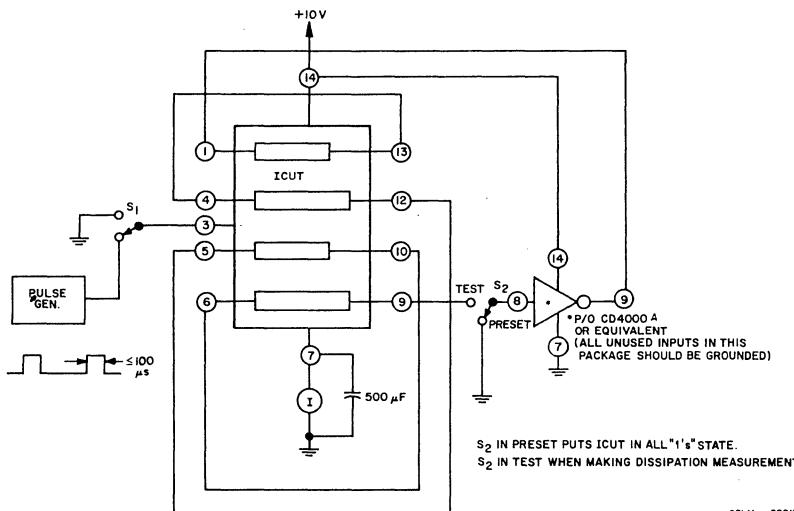
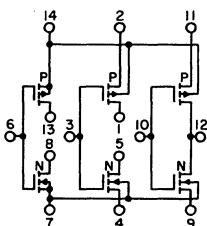


Fig.3.13—Device Dissipation Test Setup.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4007AD, CD4007AF****CD4007AE, CD4007AK**Terminal No. 14 = V<sub>DD</sub>Terminal No. 7 = V<sub>SS</sub>**COS/MOS Dual Complementary Pair Plus Inverter***Special Features*

- Medium speed operation . . . t<sub>PHL</sub> = t<sub>PLH</sub> = 20 ns (typ.) at C<sub>L</sub> = 15 pF
- Low "high"- and "low"-output impedance . . . 500Ω (typ.) at V<sub>DD</sub> - V<sub>SS</sub> = 10 V

*Applications*

- Extremely high-input impedance amplifiers; inverters, shapers, linear amplifiers, threshold detector

CD4007A types are comprised of three N-Channel and three P-Channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits shown in Fig. 4.1.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed. For proper operation V<sub>SS</sub> ≤ V<sub>I</sub> ≤ V<sub>DD</sub> must be satisfied.

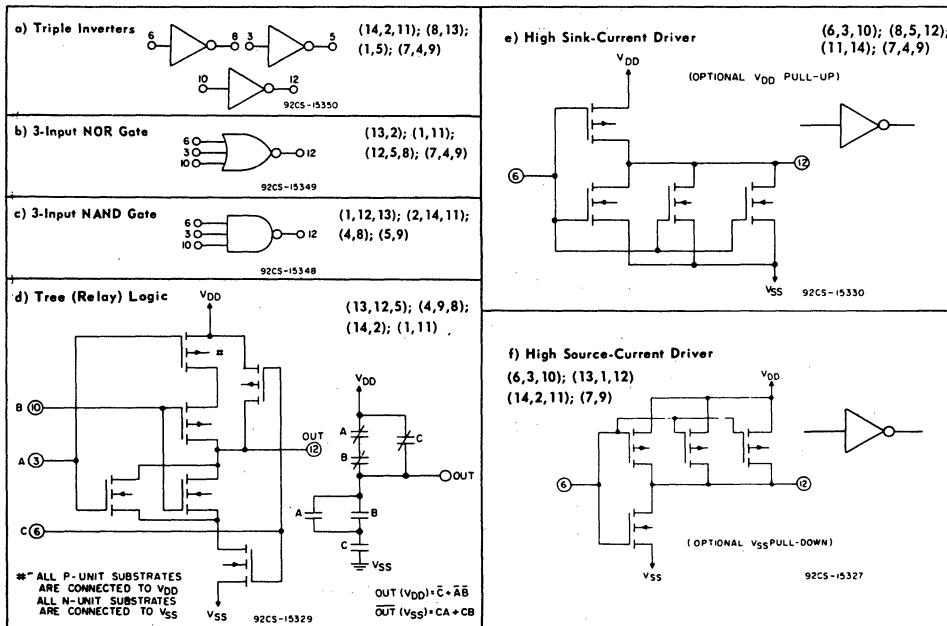


Fig. 4.1—Sample COS/MOS logic circuit arrangements using type CD4007A.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4007AD, CD4007AK, CD4007AF											
		$V_o$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C					
Quiescent Device Current	$I_L$			5	-	-	0.05	-	0.001	0.05	-	-	3	$\mu A$	4.15
				10	-	-	0.1	-	0.001	0.1	-	-	6		
Quiescent Device Dissipation/Package	$P_D$			5	-	-	0.25	-	0.005	0.25	-	-	15	$\mu W$	-
				10	-	-	1	-	0.01	1	-	-	60		
Output Voltage: Low-Level	$V_{OL}$			5	-	-	0.01	-	0	0.01	-	-	0.05	V	4.2
				10	-	-	0.01	-	0	0.01	-	-	0.05		4.3
High-Level	$V_{OH}$			5	4.99	-	-	4.99	5	-	4.95	-	-	V	4.4
				10	9.99	-	-	9.99	10	-	9.95	-	-		1.5
Noise Immunity (Any Input)	$V_{NL}$		3.6	5	1.5	-	-	1.5	2.25	-	1.4	-	-	V	4.16
			7.2	10	3	-	-	3	4.5	-	2.9	-	-		
	$V_{NH}$		0.95	5	1.4	-	-	1.5	2.25	-	1.5	-	-	V	4.16
			2.9	10	2.9	-	-	3	4.5	-	3	-	-		
Output Drive Current: N-Channel	$I_{DN}$	$V_I = V_{DD}$	0.44	5	0.75	-	-	0.6	1	-	0.4	-	-	mA	4.7
			0.5	10	1.6	-	-	1.3	2.5	-	0.95	-	-		4.9
P-Channel	$I_{DP}$	$V_I = V_{SS}$	2.57	5	-1.75	-	-	-1.4	-4	-	-1	-	-		4.8
			9.5	10	-1.35	-	-	-1.1	-2.5	-	-0.75	-	-		4.10
Input Current	$I_I$			-	-	-	-	-	10	-	-	-	-	pA	-

▲ Maximum noise-free low-level Bipolar output voltage.

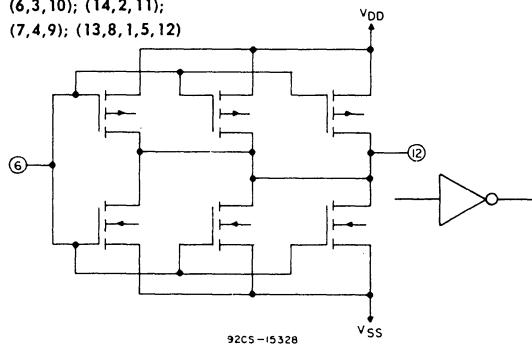
#### ◆ See Appendix

<sup>#</sup> Minimum noise-free high-level Bipolar output voltage.

### g) High Sink- and Source-Current Driver

(6,3,10); (14,2,11);

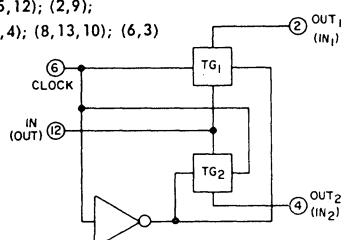
(7.4.9): (13.8, 1.5, 12)



### b) Dual Bi-Directional Transmission Gating

(1.5, 12); (2.9);

(11, 4) · (8, 13, 10) · (6, 3)



*Fig.4.1—Sample COS/MOS logic circuit arrangements using type CD4007A.*

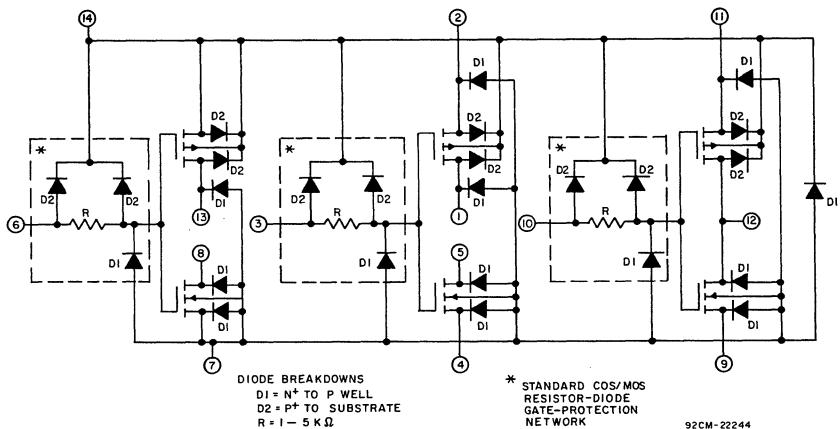
**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
			CD4007AE													
			-40°C			25°C			85°C							
Quiescent Device Current	$I_L$		5	—	—	0.5	—	0.005	0.5	—	—	15	$\mu A$	4.15		
			10	—	—	1	—	0.005	1	—	—	30				
Quiescent Device Dissipation/Package	$P_D$		5	—	—	2.5	—	0.025	2.5	—	—	75	$\mu W$	—		
			10	—	—	10	—	0.05	10	—	—	300				
Output Voltage: Low-Level	$V_{OL}$		5	—	—	0.01	—	0	0.01	—	—	0.05	V	4.2 4.3 4.4		
			10	—	—	0.01	—	0	0.01	—	—	0.05				
High-Level	$V_{OH}$		5	4.99	—	—	4.99	5	—	4.95	—	—	V	1.5 4.6		
			10	9.99	—	—	9.99	10	—	9.95	—	—				
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		3.6	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	4.16	
			7.2	10	3	—	—	3	4.5	—	2.9	—	—			
	$V_{NH}$		0.95	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	—	
			2.9	10	2.9	—	—	3	4.5	—	3	—	—			
Output Drive Current: N-Channel	$I_{DN}$	$V_I = V_{DD}$	0.4*	5	0.35	—	—	0.3	1	—	0.24	—	—	mA	4.7 4.9	
			0.5	10	1.2	—	—	1	2.5	—	0.8	—	—			
P-Channel	$I_{DP}$	$V_I = V_{SS}$	2.5*	5	-1.3	—	—	-1.1	-4	—	-0.9	—	—	mA	4.8 4.10	
			9.5	10	-0.65	—	—	-0.55	-2.5	—	-0.45	—	—			
Input Current	$I_I$		—	—	—	—	—	10	—	—	—	—	—	pA	—	

\* Maximum noise-free low-level Bipolar output voltage.

≠ Minimum noise-free high-level Bipolar output voltage.

♦ See Appendix.



Detailed schematic diagram showing input, output, and parasitic diodes.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$  and input rise and fall times = 20 ns

Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$  (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4007AD, CD4007AK CD4007AF			CD4007AE				
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.		
			5	—	35	60	—	35	75	
Propagation Delay Time: High-to-Low Level	$t_{PHL}$		10	—	20	40	—	20	50	ns 4.11 4.13
			5	—	35	60	—	35	75	
Low-to-High Level	$t_{PLH}$		10	—	20	40	—	20	50	ns 4.12
			5	—	35	60	—	30	50	
Transition Time: High-to-Low Level	$t_{THL}$		10	—	30	40	—	30	50	ns 4.12
			5	—	50	75	—	50	100	
Low-to-High Level	$t_{TLH}$		10	—	30	40	—	30	50	ns 4.12
			5	—	50	75	—	50	100	
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—

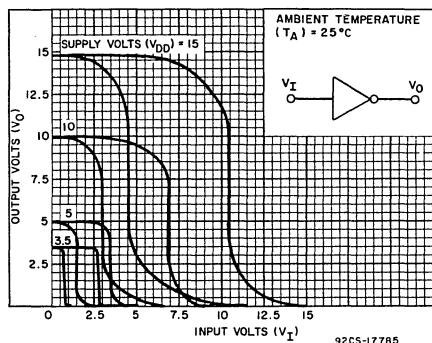


Fig. 4.2—Min. & max. voltage transfer characteristics for inverter.

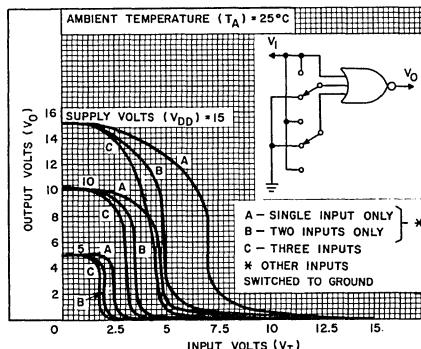


Fig. 4.3—Typ. voltage transfer characteristics for NOR gate.

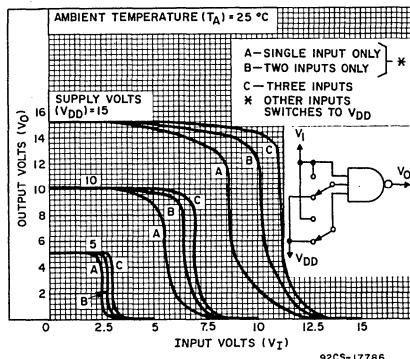


Fig. 4.4—Typ. voltage transfer characteristics for NAND gate.

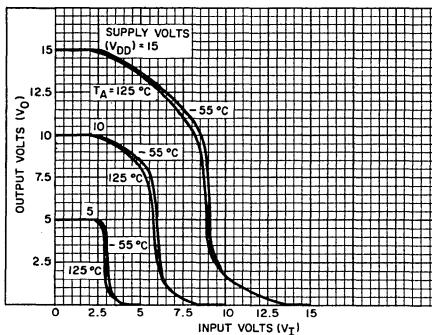


Fig. 4.5—Typ. voltage transfer characteristics as a function of temp.

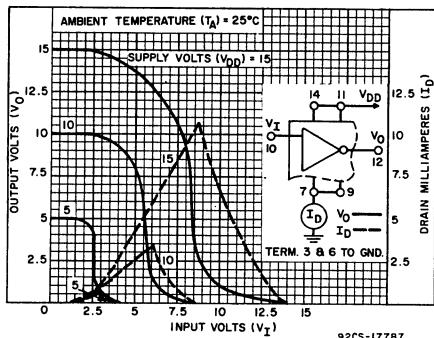


Fig. 4.6—Typ. current and voltage transfer characteristics for inverter.

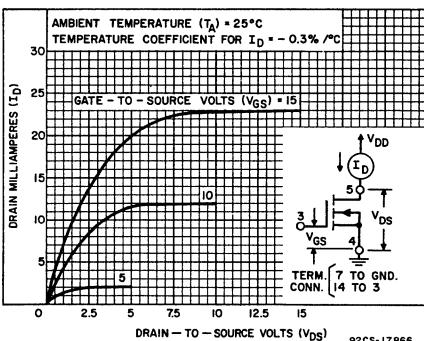


Fig. 4.7—Typ. n-channel drain characteristics.

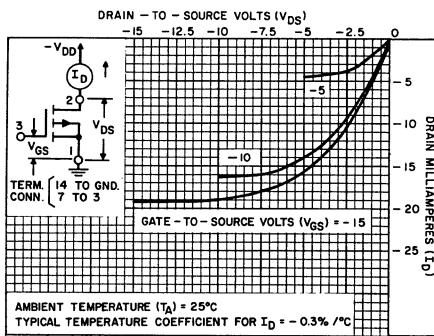


Fig. 4.8—Typ. p-channel drain characteristics.

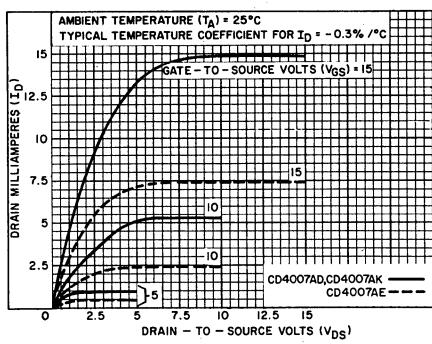


Fig. 4.9—Min. n-channel drain characteristics.

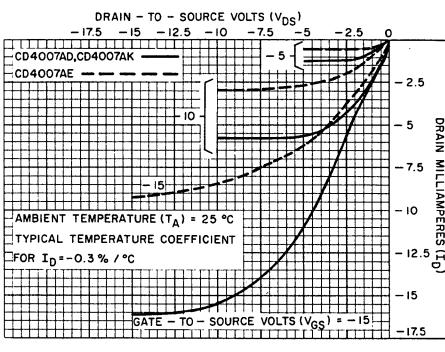


Fig. 4.10—Min. p-channel drain characteristics.

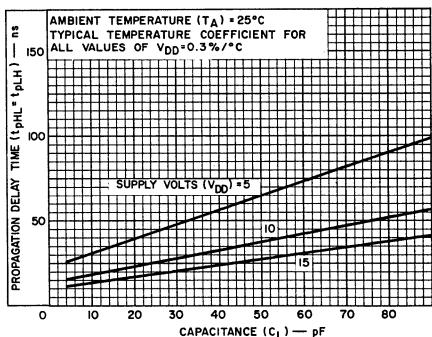


Fig. 4.11—Typ. propagation delay time vs.  $C_L$ .

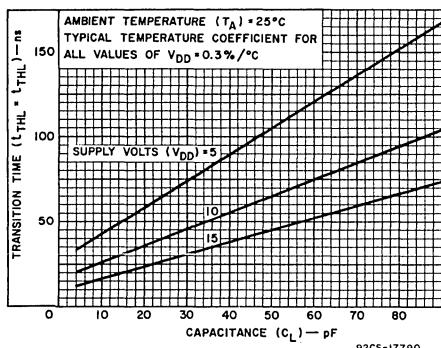
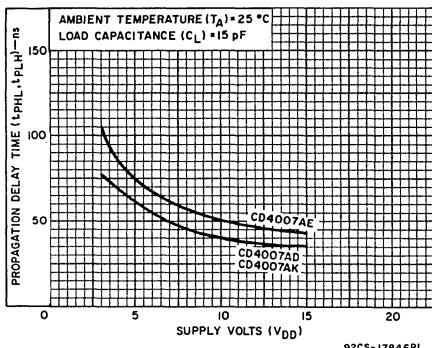
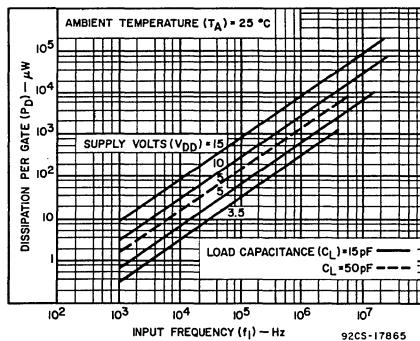
Fig. 4.12—Typ. transition time vs.  $C_L$ .Fig. 4.13—Max. propagation delay time vs.  $V_{DD}$ .

Fig. 4.14—Typ. dissipation characteristics.

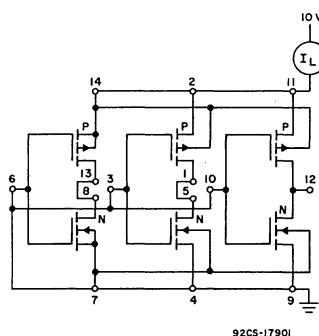


Fig. 4.15—Quiescent device current test circuit.

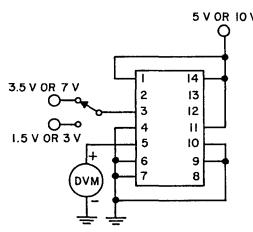
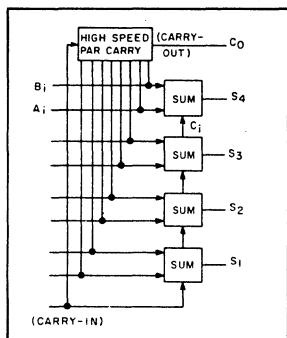


Fig. 4.16—Noise immunity test circuit.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4008AD, CD4008AF  
CD4008AE, CD4008AK****COS/MOS Four-Bit Full Adder****With Parallel Carry Out****Special Features**

- MSI complexity on a single chip. . . . . 4 Sum Outputs plus parallel Carry-Output
- High speed operation. . . . . Carry-In to Carry-Out delay,  $t_{PHL}$ ,  $t_{PLH} = 45 \text{ ns at } C_L = 15 \text{ pF}$

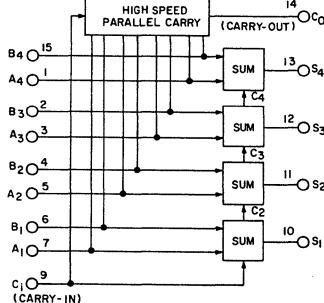
**Applications**

- Binary addition/arithmetic units

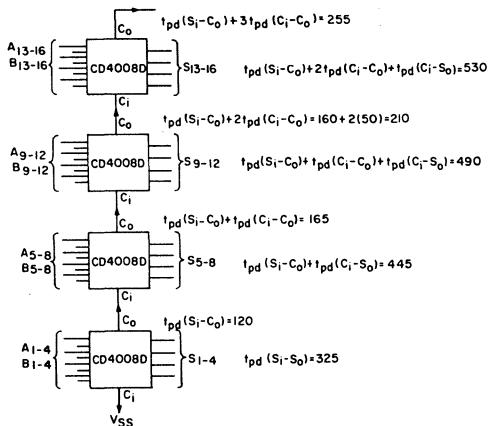
TRUTH TABLE

A <sub>i</sub>	B <sub>j</sub>	C <sub>i</sub>	C <sub>0</sub>	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A<sub>1</sub> to A<sub>4</sub> and B<sub>1</sub> to B<sub>4</sub>, in addition to the "Carry In" bit from a previous section. CD4008A outputs include the four sum bits, S<sub>1</sub> and S<sub>4</sub>, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008A section.

TERMINAL NO.16 = V<sub>DD</sub>, TERMINAL NO.8 = V<sub>SS</sub>

92CS-15842



## NOTES

- ALL "A" & "B" INPUT BITS OCCUR AT  $t = 0$
- ALL SUMS SETTLED AT  $t = 530\text{ns}$
- $C_L = 15 \text{ pF}, T_A = 25^\circ\text{C}, V_{DD} - V_{SS} = +10 \text{ V}$

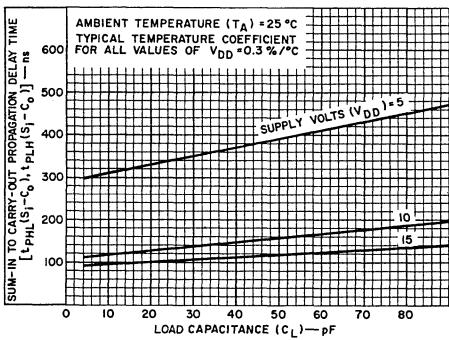
92CS-17761

Fig.5.1—Logic diagram for type CD4008A.

Fig.5.2—Typical speed characteristics of a 16-bit adder.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS												UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.				
			CD4008AD, CD4008AK, CD4008AF																	
			-55°C			25°C			125°C											
			V <sub>O</sub> Volts	V <sub>DD</sub> Volts		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.						
Quiescent Device Current	I <sub>L</sub>		5	-	-	5	-	0.3	5	-	-	300	-	-	μA	5.8				
			10	-	-	10	-	0.5	10	-	-	600	-	-						
Quiescent Device Dissipation/Package	PD		5	-	-	25	-	1.5	25	-	-	1500	-	-	μW	—				
			10	-	-	100	-	5	100	-	-	6000	-	-						
Output Voltage: Low-Level	VOL		5	-	-	0.01	-	0	0.01	-	-	0.05	-	-	V	—				
			10	-	-	0.01	-	0	0.01	-	-	0.05	-	-						
High-Level	VOH		5	4.99	-	-	4.99	5	-	4.95	-	-	-	-	V	—				
			10	9.99	-	-	9.99	10	-	9.95	-	-	-	-						
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	VNL		0.95	5	1.5	-	-	1.5	2.25	-	1.4	-	-	-	V	5.9♦				
			2.9	10	3	-	-	3	4.5	-	2.9	-	-	-						
	VNH		3.6	5	1.4	-	-	1.5	2.25	-	1.5	-	-	-	V					
			7.2	10	2.9	-	-	3	4.5	-	3	-	-	-						
Output Drive Current N-Channel	I <sub>DN</sub>	Carry Output	0.5	5	0.31	-	-	0.25	0.5	-	0.175	-	-	-	mA	♦				
			0.5	10	0.93	-	-	0.75	1.5	-	0.53	-	-	-						
		Sum Output	3	5	0.012	-	-	0.01	0.2	-	0.007	-	-	-						
			3	10	0.31	-	-	0.25	0.5	-	0.175	-	-	-						
P-Channel	I <sub>DP</sub>	Carry Output	4.5	5	-0.31	-	-	-0.25	-0.5	-	-0.175	-	-	-	mA	♦				
			9.5	10	-0.93	-	-	-0.75	-1.5	-	-0.53	-	-	-						
		Sum Output	2	5	0.012	-	-	-0.01	-0.2	-	0.007	-	-	-						
			7	10	-0.185	-	-	-0.15	-0.3	-	-0.105	-	-	-						
Input Current	I <sub>I</sub>		-	-	-	-	-	10	-	-	-	-	-	-	pA	-				

◆ See Appendix



*Fig. 5.3—Sum-in to carry out propagation delay time vs.  $C_L$*

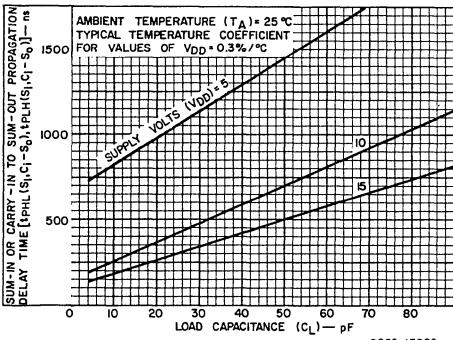


Fig. 5.4—Sum-in or carry-in to sum-out propagation delay time vs.  $C_L$

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4008AE											
				-40°C			25°C			85°C					
Quiescent Device Current	$I_L$		$V_O$ Volts	5	—	—	50	—	0.5	50	—	700	$\mu A$	5.8	
				10	—	—	100	—	1	100	—	1400			
Quiescent Device Dissipation/Package	$P_D$		$V_{DD}$ Volts	5	—	—	250	—	2.5	250	—	3500	$\mu W$	—	
				10	—	—	1000	—	10	1000	—	14000			
Output Voltage: Low-Level	$V_{OL}$		$V_O$ Volts	5	—	—	0.01	—	0	0.01	—	0.05	V	—	
				10	—	—	0.01	—	0	0.01	—	0.05			
High-Level	$V_{OH}$		$V_O$ Volts	5	4.99	—	—	4.99	5	—	4.95	—	V	—	
				10	9.99	—	—	9.99	10	—	9.95	—			
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		0.95	5	1.5	—	—	1.5	2.25	—	1.4	—	V	5.9*	
			2.9	10	3	—	—	3	4.5	—	2.9	—			
	$V_{NH}$		3.6	5	1.4	—	—	1.5	2.25	—	1.5	—	V	—	
			7.2	10	2.9	—	—	3	4.5	—	3	—			
Output Drive Current N-Channel	$I_{DN}$		Carry Output	0.5	5	0.155	—	—	0.13	0.5	—	0.105	—	mA	—
			Sum Output	0.5	10	0.6	—	—	0.5	1.5	—	0.4	—		
P-Channel	$I_{DP}$		Carry Output	4.5	5	-0.155	—	—	-0.13	-0.5	—	-0.105	—	mA	—
			Sum Output	9.5	10	-0.6	—	—	-0.5	-1.5	—	-0.4	—		
			Carry Output	2	5	-0.008	—	—	-0.007	-0.2	—	-0.005	—		
			Sum Output	7	10	-0.12	—	—	-0.1	-0.3	—	-0.08	—		
Input Current	$I_I$			—	—	—	—	—	10	—	—	—	pA	—	

\* See Appendix

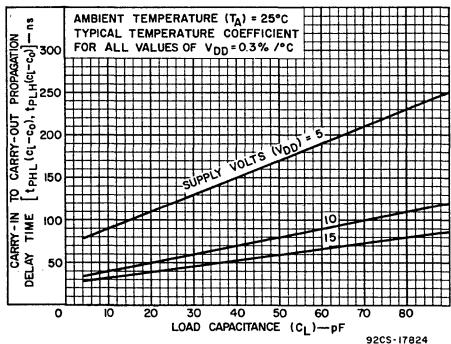


Fig. 5.5—Carry-in to carry-out propagation delay time vs.  $C_L$ .

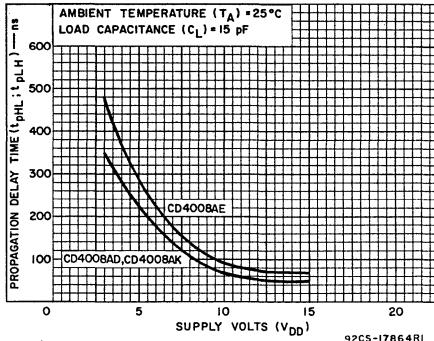


Fig. 5.6—Max. propagation delay time vs.  $V_{DD}$  for carry-in to carry-out.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$  and input rise and fall times = 20 ns  
 Typical Temperature Coefficient for all values of  $V_{DD}$  =  $0.3\%/\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4008AD, CD4008AK CD4008AF			CD4008AE				
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.		
Propagation Delay Time: At Sum Outputs; From Sum Input	$t_{PHL}, t_{PLH}$		5	—	900	1300	—	900	2000	ns 5.4
			10	—	325	500	—	325	650	
			5	—	900	1300	—	900	2000	
			10	—	325	500	—	325	650	
			5	—	320	600	—	320	800	ns 5.3
			10	—	120	200	—	120	240	
			5	—	100	175	—	100	200	ns 5.5
			10	—	45	75	—	45	90	
Transition Time: At Sum Outputs	$t_{THL}, t_{TLH}$		5	—	1250	2200	—	1250	2900	ns —
			10	—	550	900	—	550	1100	
			5	—	125	225	—	125	290	ns —
			10	—	45	75	—	45	90	
Input Capacitance	$C_I$	Any Input	—	10	—	—	10	—	pF	—

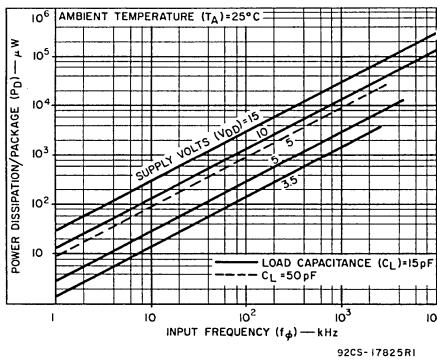


Fig.5.7—Typ. dissipation characteristics.

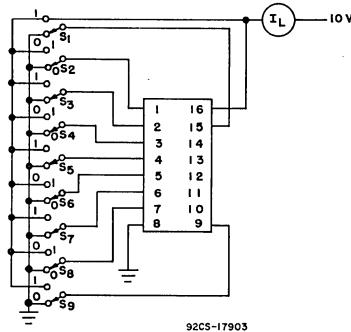


Fig.5.8—Quiescent device current test circuit.

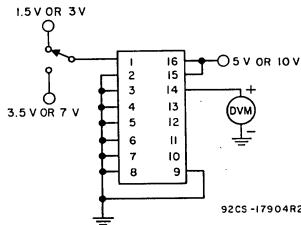
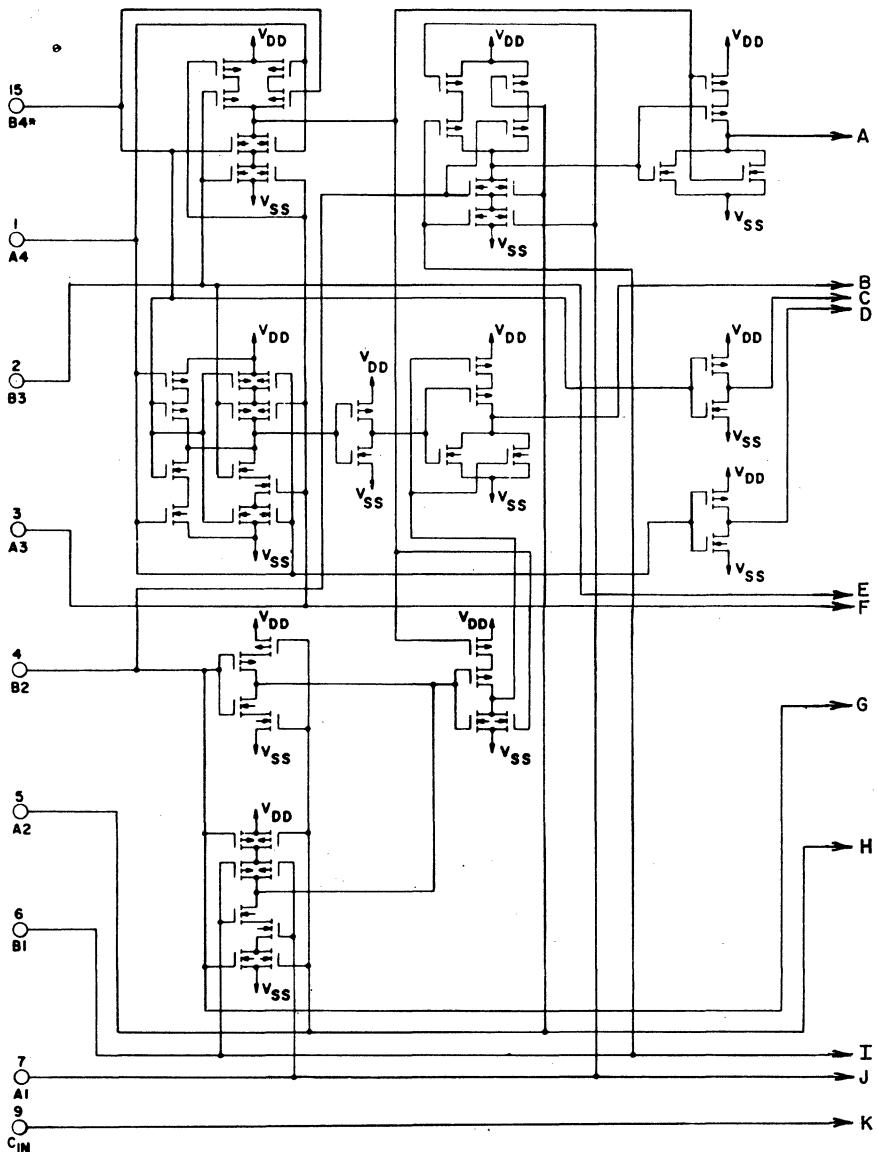


Fig.5.9—Noise immunity test circuit.



ALL P UNIT (—) SUBSTRATES CONNECTED TO V<sub>DD</sub>  
ALL N UNIT (—) SUBSTRATES CONNECTED TO V<sub>SS</sub>

 DRAIN & SOURCE REGION WIDTHS=3 MILS	 DRAIN & SOURCE REGION WIDTHS=10 MILS
 DRAIN & SOURCE REGION WIDTHS ON ALL OTHER DEVICES=1.1 MIL	

Fig.5.10—Schematic diagram.

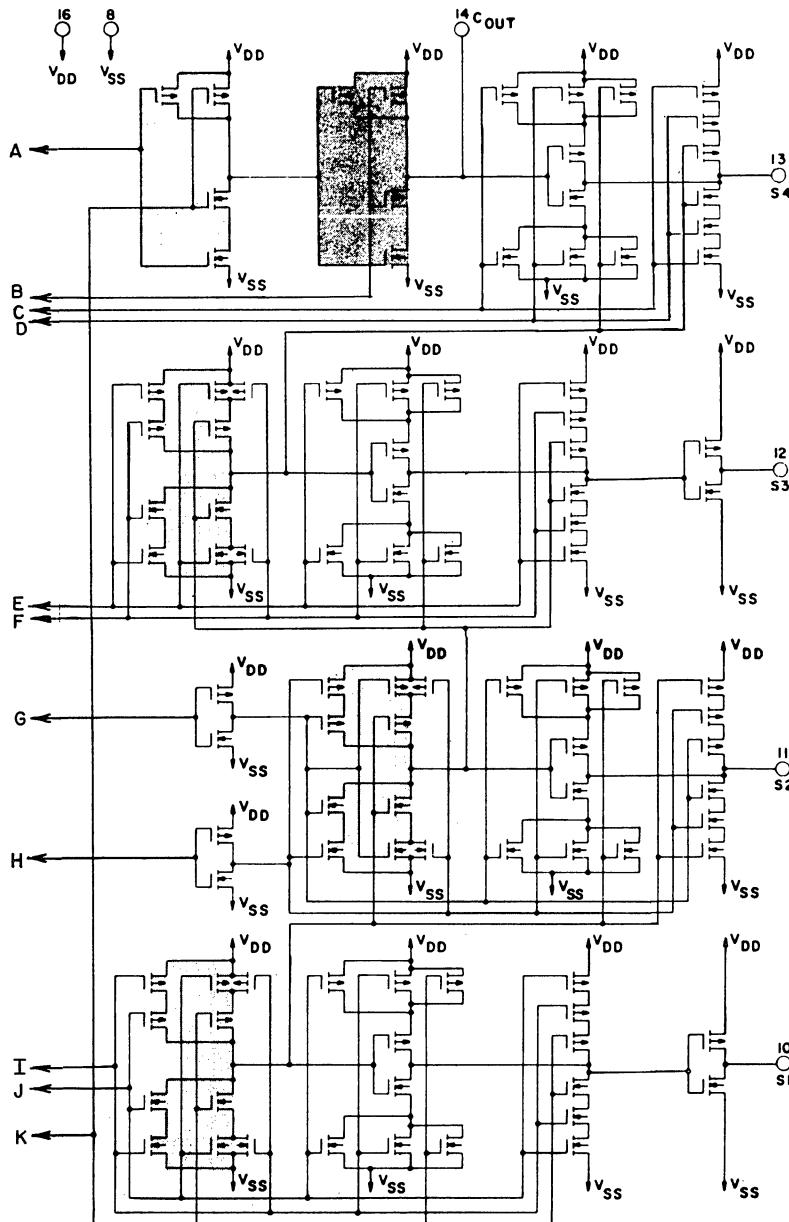


Fig.5.10 – Schematic diagram.

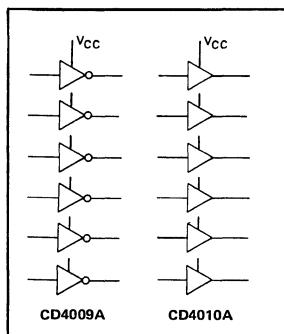
92SL-4299

**Digital Integrated Circuits**

Monolithic Silicon

**CD4009A, CD4010A**

Types

**COS/MOS Hex Buffers/Converters**

Inverting Type: CD4009AD, CD4009AE, CD4009AK

Non-Inverting Type: CD4010AD, CD4010AE, CD4010AK

*Special Features (Each Buffer)*

- High current sinking capability. . . . . 8 mA (min.) at  $V_{OL} = 0.5$  V and  $V_{DD} = +10$  V

*Applications*

- COS/MOS to DTL/TTL hex converter
- COS/MOS logic-level converter
- COS/MOS current "sink" or "source" driver
- Multiplexer—1 to 6 or 6 to 1

**CAUTION:**

**V<sub>CC</sub> VOLTAGE LEVEL MUST BE EQUAL TO OR LESS THAN V<sub>DD</sub>. FOR 10.5- TO 15-VOLT SUPPLIES, C<sub>LOAD</sub> MUST BE EQUAL TO OR LESS THAN 5000 pF.**

CD4009A types may be used as a hex COS/MOS inverter, a COS/MOS to DTL or TTL logic-level converter, or a COS/MOS current driver.

The CD4049A and CD4050A are preferred Hex Buffer replacements for the CD4009A and CD4010A, respectively, in all applications except multiplexers.

CD4010A types may be used as a COS/MOS to DTL or TTL hex converter or a COS/MOS current driver.

Conversion ranges are from COS/MOS logic operating at +3 V to +15 V supply levels to DTL or TTL logic operating at +3 V to +6 V supply levels. Conversion to logic output levels greater than +6 V is permitted providing  $V_{CC}(\text{DTL/TTL}) \leq V_{DD}(\text{COS/MOS})$ .

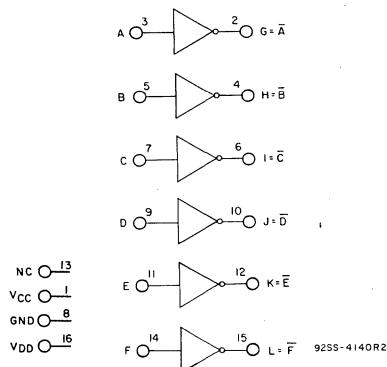


Fig. 6.1—Logic diagram for types CD4009A.

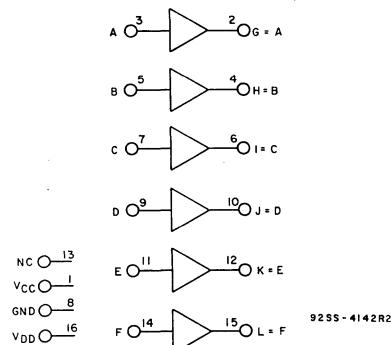


Fig. 6.2—Logic diagram for types CD4010A.

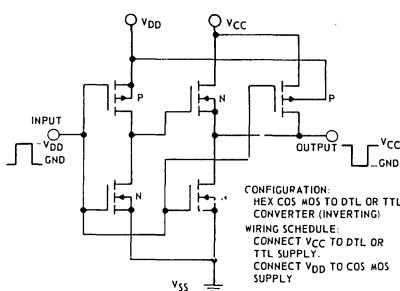


Fig.6.3—Schematic diagram for types CD4009A.  
1 of 6 identical stages.

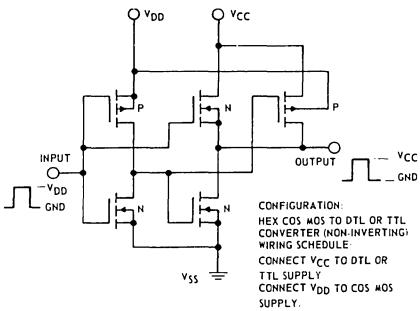


Fig.6.4—Schematic diagram for types CD4010A.  
1 of 6 identical stages.

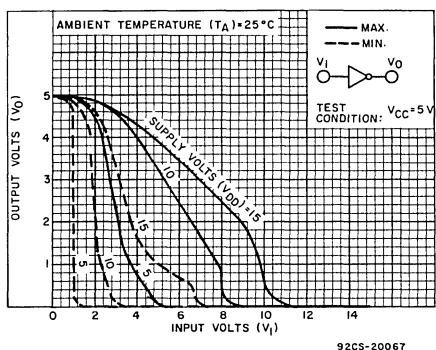


Fig.6.5—Min. & max. voltage transfer characteristics — CD4009A.

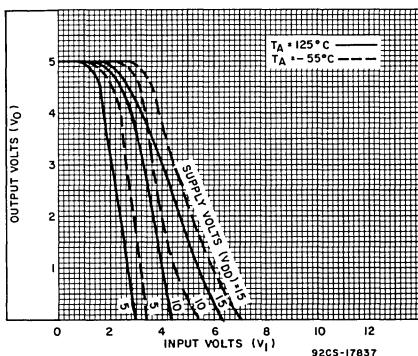


Fig.6.6—Typ. voltage transfer characteristics  
as function of temp. — CD4009A.

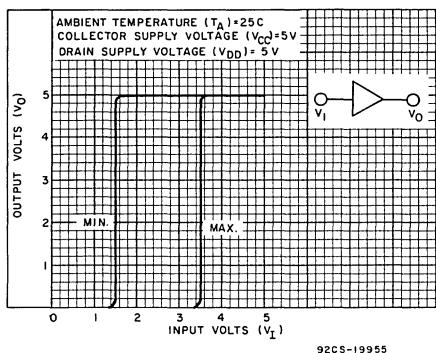


Fig.6.7—Min. & max. voltage transfer characteristics (V<sub>DD</sub> = 5) — CD4010A.

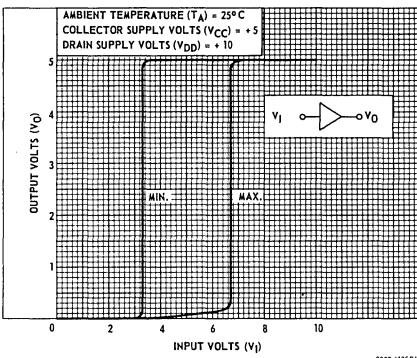


Fig.6.8—Min. & max. voltage transfer characteristics (V<sub>D</sub> = 10) — CD4010A.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4009AD, CD4009AK, CD4010AD, CD4010AK											
			-55°C			25°C			125°C					
			VO Volts	V <sub>DD</sub> Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	UNITS
Quiescent Device Current:	I <sub>L</sub>				5	—	—	0.3	—	0.01	0.3	—	20	μA
					10	—	—	0.5	—	0.01	0.5	—	30	6.22
Quiescent Device Dissipation/Package	P <sub>D</sub>				5	—	—	1.5	—	0.05	1.5	—	100	μW
					10	—	—	5	—	0.1	5	—	300	—
Output Voltage: Low-Level	V <sub>OL</sub>				5	—	—	0.01	—	0	0.01	—	0.05	V
					10	—	—	0.01	—	0	0.01	—	0.05	6.5 through 6.10
High-Level	V <sub>OH</sub>				5	4.99	—	—	4.99	5	—	4.95	—	V
					10	9.99	—	—	9.99	10	—	9.95	—	—
Noise Immunity ♦ (Any Input) CD4009A	V <sub>NL</sub>		3.6											6.23
			5	1	—	—	—	1	2.25	—	0.9	—	—	
			7.2	10	2	—	—	2	4.5	—	1.9	—	—	
			0.95	5	1.5	—	—	1.5	2.25	—	1.4	—	—	
CD4010A	V <sub>NH</sub>		2.9	10	3	—	—	3	4.5	—	2.9	—	—	6.23
			0.95	5	1.4	—	—	1.5	2.25	—	1.5	—	—	
			2	10	2.9	—	—	3	4.5	—	3	—	—	
			3.6	5	1.4	—	—	1.5	2.25	—	1.5	—	—	
CD4009A	V <sub>DN</sub>		7.2	10	2.9	—	—	3	4.5	—	3	—	—	6.12 6.13 ♦
			0.95	5	1.4	—	—	1.5	2.25	—	1.5	—	—	
			2	10	2.9	—	—	3	4.5	—	3	—	—	
			3.6	5	1.4	—	—	1.5	2.25	—	1.5	—	—	
CD4010A	V <sub>DP</sub>		7.2	10	2.9	—	—	3	4.5	—	3	—	—	♦
			0.4	5	3.75	—	—	3	4	—	2.1	—	—	
			0.5	10	10	—	—	8	10	—	5.6	—	—	
			2.5	5	-1.85	—	—	-1.25	-1.75	—	-0.9	—	—	
Output Drive Current: N-Channel	I <sub>DN</sub>		9.5	10	-0.9	—	—	-0.6	-0.8	—	-0.4	—	—	mA
P-Channel	I <sub>DP</sub>													mA
Input Current	I <sub>I</sub>					—	—	—	—	10	—	—	—	pA

♦ See Appendix.

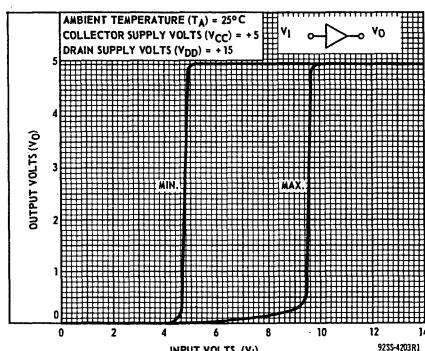


Fig.6.9—Min. & max. voltage transfer characteristics ( $V_{DD} = 15$ ) — CD4010A.

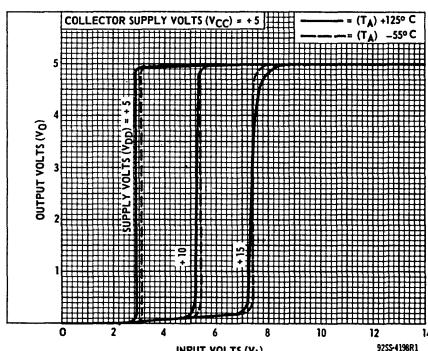


Fig.6.10—Typ. voltage transfer characteristics as a function of temperature — CD4010A.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS			
			CD4009AE, CD4010AE													
			-40°C			25°C			85°C							
Quiescent Device Current:	$I_L$		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	-	-	μA		
Quiescent Device Current:	$I_L$		5	-	3	0.03	3	-	-	42	-	-	-	μA		
Quiescent Device Current:	$I_L$		10	-	5	0.05	5	-	-	70	-	-	-	μA		
Quiescent Device Dissipation/Package	$P_D$		5	-	15	0.15	15	-	-	210	-	-	-	μW		
Quiescent Device Dissipation/Package	$P_D$		10	-	50	0.5	50	-	-	700	-	-	-	μW		
Output Voltage: Low-Level	$V_{OL}$		5	-	0.01	0	0.01	-	-	0.05	-	-	-	V		
Output Voltage: Low-Level	$V_{OL}$		10	-	0.01	0	0.01	-	-	0.05	-	-	-	V		
Output Voltage: High-Level	$V_{OH}$		5	4.99	-	4.99	5	-	4.95	-	-	-	-	V		
Output Voltage: High-Level	$V_{OH}$		10	9.99	-	9.99	10	-	9.95	-	-	-	-	V		
Noise Immunity ♦ (Any Input) CD4009A	$V_{NL}$	3.6	5	1	-	1	2.25	-	0.9	-	-	-	-	6.23		
Noise Immunity ♦ (Any Input) CD4009A		7.2	10	2	-	2	4.5	-	1.9	-	-	-	-			
Noise Immunity ♦ (Any Input) CD4010A		0.95	5	1.5	-	1.5	2.25	-	1.4	-	-	-	-			
Noise Immunity ♦ (Any Input) CD4010A		2.9	10	3	-	3	4.5	-	2.9	-	-	-	-			
CD4009A	$V_{NH}$	0.95	5	1.4	-	3	2.25	-	1.5	-	-	-	-	V		
CD4009A		2	10	2.9	-	3	4.5	-	1.5	-	-	-	-	V		
CD4010A		3.6	5	1.4	-	3	2.25	-	1.5	-	-	-	-	V		
CD4010A		7.2	10	2.9	-	3	4.5	-	1.5	-	-	-	-	V		
Output Drive Current: N-Channel	$I_{DN}$	0.4	5	3.6	-	3	4	-	2.4	-	-	-	-	mA		
Output Drive Current: N-Channel	$I_{DN}$	0.5	10	9.6	-	8	10	-	6.4	-	-	-	-	mA		
Output Drive Current: P-Channel	$I_{DP}$	2.5	5	-1.5	-	-	-1.25	-1.75	-	-1	-	-	-	mA		
Output Drive Current: P-Channel	$I_{DP}$	9.5	10	-0.72	-	-	-0.6	-0.8	-	-0.48	-	-	-	mA		
Input Current	$I_I$	-	-	-	-	-	10	-	-	-	-	-	-	pA		

♦ See Appendix.

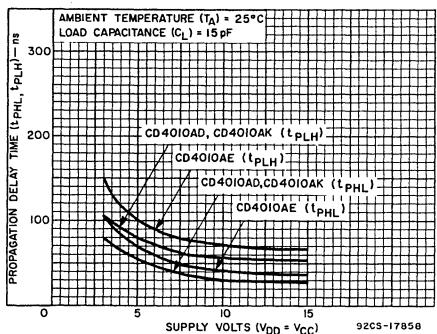


Fig.6.11—Max. propagation delay time vs.  $V_{DD} - CD4010A$ .

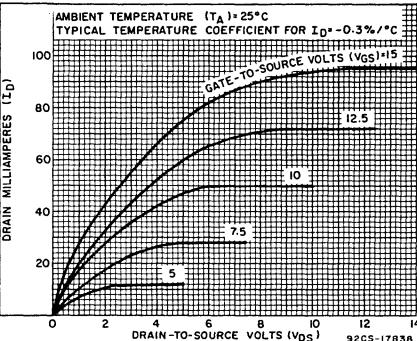


Fig.6.12—Typ. n-channel drain characteristics — CD4009A, CD4010A.

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \mu\text{F}$ , and input rise and fall times = 20 ns**Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4009AD, CD4009AK CD4010AD, CD4010AK			CD4009AE CD4010AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>	$V_{CC} = V_{DD}$	5	—	15	55	—	15	70	ns	6.14
			10	—	10	30	—	10	40		
		$V_{DD} = 10\text{V}$ $V_{CC} = 5\text{V}$	—	—	10	25	—	10	35		
Low-to-High Level	t <sub>PLH</sub>	$V_{CC} = V_{DD}$	5	—	50	80	—	50	100	ns	6.15
			10	—	25	55	—	25	70		
		$V_{DD} = 10\text{V}$ $V_{CC} = 5\text{V}$	—	—	15	30	—	15	40		
Transition Time: High-to-Low Level	t <sub>THL</sub>	$V_{CC} = V_{DD}$	5	—	20	45	—	20	60	ns	6.18
			10	—	16	40	—	16	50		
Low-to-High Level	t <sub>TLH</sub>	$V_{CC} = V_{DD}$	5	—	80	125	—	80	160	ns	6.19
			10	—	50	100	—	50	120		
Input Capacitance (Any Input)	C <sub>I</sub>	CD4009A	—	—	15	—	—	15	—	pF	—
		CD4010A	—	—	5	—	—	5	—		

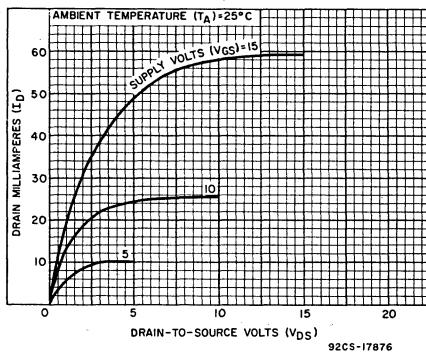
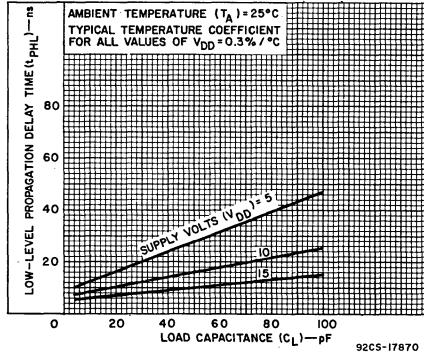


Fig. 6.13—Min. n-channel drain characteristics.

Fig. 6.14—Typ. high-to-low level propagation delay time vs.  $C_L$  — CD4009A, CD4010A.

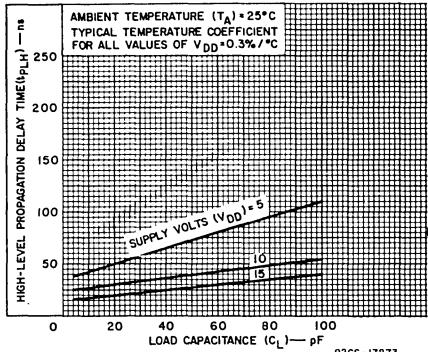


Fig. 6.15—Typ. low-to-high level propagation delay time vs.  $C_L$  — CD4009A, CD4010A.

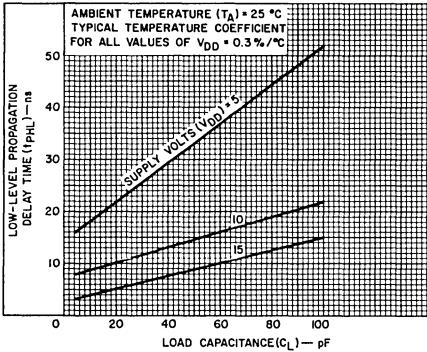


Fig. 6.16—Typ. high-to-low level propagation delay time vs.  $C_L$  (driving TTL, DTL) — CD4009A, CD4010A.

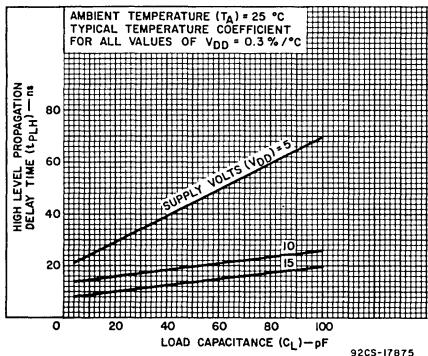


Fig. 6.17—Typ. low-to-high level propagation delay time vs.  $C_L$  (driving TTL, DTL) — CD4009A, CD4010A.

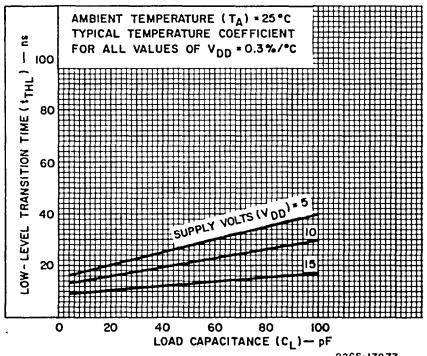


Fig. 6.18—Typ. high-to-low level transition time vs.  $C_L$  — CD4009A, CD4010A.

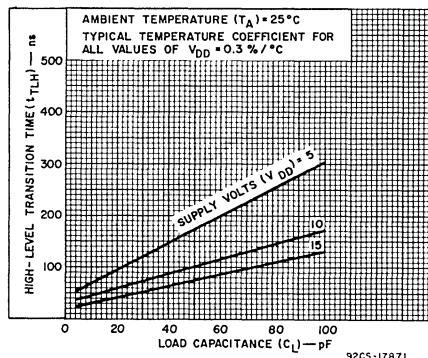


Fig. 6.19—Typ. low-to-high level transition time vs.  $C_L$  — CD4009A, CD4010A.

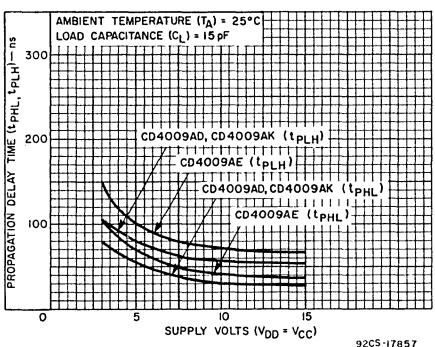


Fig. 6.20—Max. propagation delay time vs.  $V_{DD}$  — CD4009A.

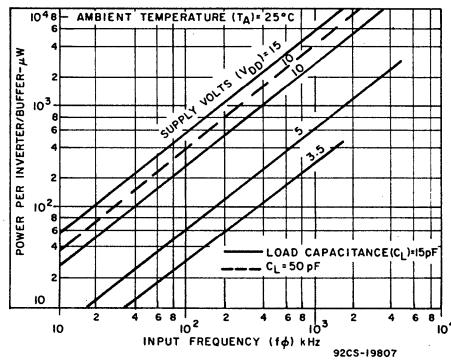


Fig.6.21—Typ. dissipation characteristics —  
CD4009A, CD4010A.

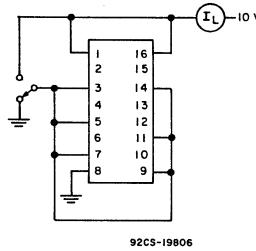


Fig.6.22 — Quiescent dissipation test circuit.

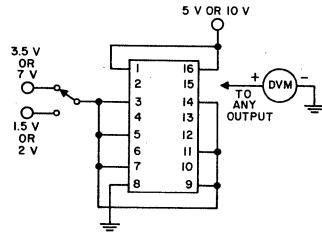


Fig.6.23 — Noise immunity test circuit for CD4009A.

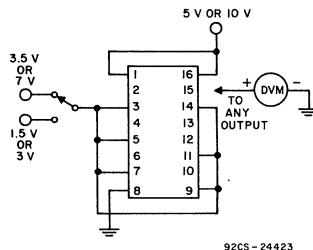


Fig.6.24 — Noise immunity test circuit for CD4010A.

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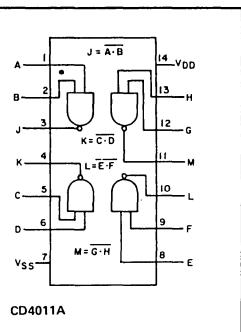
Monolithic Silicon

**CD4011A, CD4012A, CD4023A****COS/MOS NAND Gates  
(Positive Logic)**

Quad 2 Input • • • CD4011AD, CD4011AE, CD4011AF, CD4011AK  
 Dual 4 Input • • • CD4012AD, CD4012AE, CD4012AF, CD4012AK  
 Triple 3 Input • • • CD4023AD, CD4023AE, CD4023AF, CD4023AK

*Special Features*

- Medium speed operation . . . . .  $t_{PHL} = t_{PLH} = 25 \text{ ns (typ.)}$   
 $\text{at } C_L = 15 \text{ pF}$
- Low "high"- and "low"-level output impedance . . . . .  $400 \text{ and } 800\Omega \text{ (typ.)}$   
 $\text{respectively at } V_{DD} - V_{SS} = 10 \text{ V}$



The combination of these devices and the RCA NOR positive logic gate types CD4000A, CD4001A, CD4002A, and CD4025A can account for appreciable package-count savings in various logic function configurations.

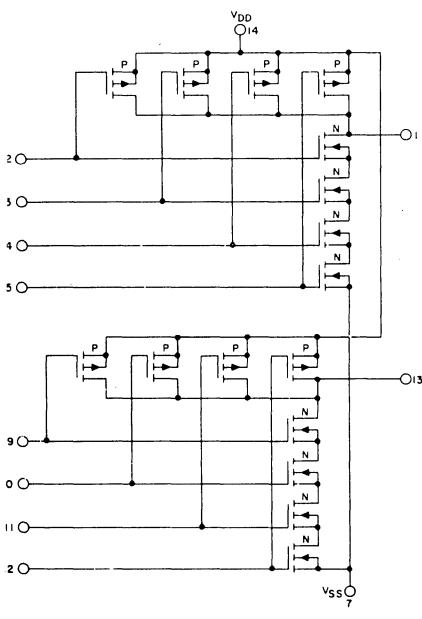
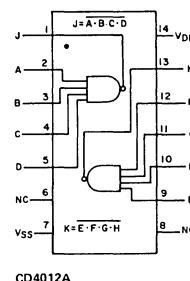
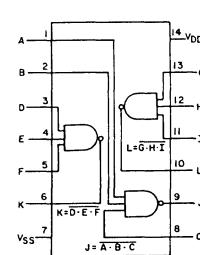


Fig.7.1 – Schematic diagram for type CD4012A.

**COS/MOS NAND Gates  
(Positive Logic)**

CD4012A



CD4023A

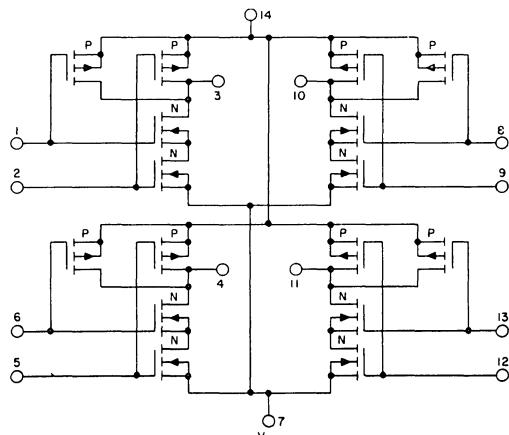


Fig.7.2 – Schematic diagram for type CD4011A.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4011AD, CD4011AK, CD4011AF, CD4012AD, CD4012AK, CD4012AF, CD4023AD, CD4023AK, CD4023AF											
		$V_o$ Volts	$V_{DD}$ Volts	$-55^{\circ}\text{C}$		$25^{\circ}\text{C}$		$125^{\circ}\text{C}$							
Quiescent Device Current	$I_L$			5	—	—	0.05	—	0.001	0.05	—	—	3	$\mu\text{A}$	—
				10	—	—	0.1	—	0.001	0.1	—	—	6	$\mu\text{A}$	—
Quiescent Device Dissipation/Package	$P_D$			5	—	—	0.25	—	0.005	0.25	—	—	15	$\mu\text{W}$	—
				10	—	—	1	—	0.01	1	—	—	60	$\mu\text{W}$	—
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V	7.4
				10	—	—	0.01	—	0	0.01	—	—	0.05	V	7.5
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V	7.6
				10	9.99	—	—	9.99	10	—	9.95	—	—	V	7.7
Noise Immunity (Any Input)	$V_{NL}$			3.6	5	1.5	—	—	1.5	2.25	—	1.4	—	V	—
For Definition, See Appendix				7.2	10	3	—	—	3	4.5	—	2.9	—	V	—
	$V_{NH}$			0.95	5	1.4	—	—	1.5	2.25	—	1.5	—	V	—
				2.9	10	2.9	—	—	3	4.5	—	3	—	V	—
Output Drive Current				0.5	5	0.31	—	—	0.25	0.5	—	0.175	—	mA	◆
N-Channel	$I_{DN}$	CD4011A Series	0.5	10	0.62	—	—	0.5	0.6	—	0.35	—	—	mA	
		CD4012A Series	0.5	5	0.15	—	—	0.12	0.25	—	0.085	—	—	mA	
			0.5	10	0.31	—	—	0.25	0.6	—	0.175	—	—	mA	
P-Channel	$I_{DP}$		4.5	5	-0.31	—	—	-0.25	-0.5	—	-0.175	—	—	mA	
			9.5	10	-0.75	—	—	-0.6	-1.2	—	-0.4	—	—	mA	
Input Current	$I_I$					—	—	—	—	10	—	—	—	pA	—

◆ See Appendix.

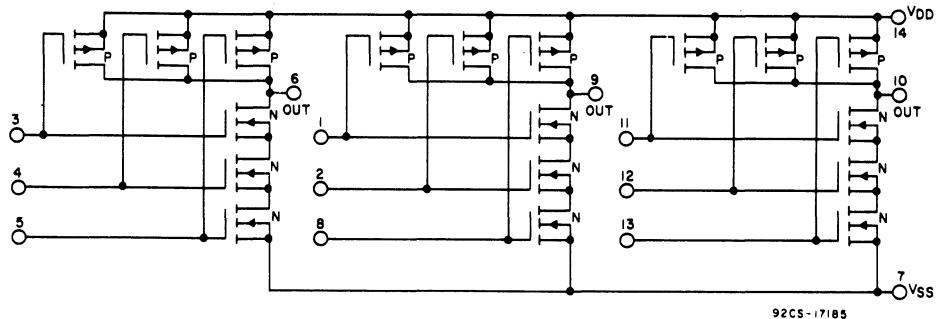


Fig.7.3 – Schematic diagram for type CD4023A.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4011AE, CD4012AE, CD4023AE											
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C					
Quiescent Device Current	$I_L$			5	—	—	0.5	—	0.005	0.5	—	—	15	$\mu A$	—
			10	—	—	5	—	0.005	5	—	—	30			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	2.5	—	0.025	2.5	—	—	75	$\mu W$	—
				10	—	—	50*	—	0.05	50	—	—	300		
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	$V$	7.4
				10	—	—	0.01	—	0	0.01	—	—	0.05		7.5
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	$V$	7.6
				10	9.99	—	—	9.99	10	—	9.95	—	—		7.7
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		3.6	5	1.5	—	—	1.5	2.25	—	1.4	—	—	$V$	—
			7.2	10	3	—	—	3	4.5	—	2.9	—	—		—
	$V_{NH}$		0.95	5	1.4	—	—	1.5	2.25	—	1.5	—	—	$V$	—
			2.9	10	2.9	—	—	3	4.5	—	3	—	—		—
Output Drive Current	$I_D$		CD4011A Series	0.5	5	0.145	—	—	0.12	0.5	—	0.095	—	$mA$	◆
			CD4023A Series	0.5	10	0.3	—	—	0.25	0.6	—	0.2	—		
			CD4012A Series	0.5	5	0.072	—	—	0.06	0.25	—	0.05	—		
			0.5	10	0.155	—	—	0.13	0.6	—	0.105	—	—		
P-Channel	$I_{DP}$		4.5	5	0.145	—	—	-0.12	-0.5	—	-0.095	—	—	$mA$	◆
			9.5	10	-0.35	—	—	-0.3	-1.2	—	-0.24	—	—		
Input Current	$I_I$				—	—	—	—	10	—	—	—	—	$pA$	—

♦ See Appendix

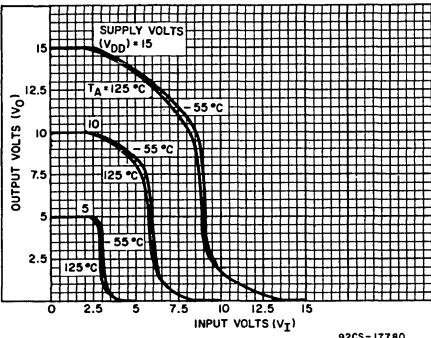
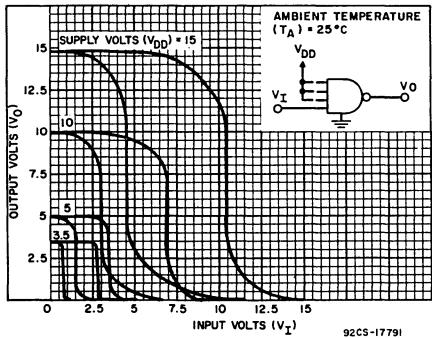


Fig. 7.4—Min. & max. voltage transfer characteristics.

Fig. 7.5—Typ. voltage transfer characteristics as a function of temperature.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns  
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$  (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4011AD, AF, AK			CD4011AE CD4012AE CD4023AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time: Low-to-High Level	tPLH		5	—	50	75	—	50	100	ns	7.13
			10	—	25	40	—	25	50		7.19
High-to-Low Level CD4011A and CD4023A Series	tPHL		5	—	50	75	—	50	100	ns	7.14
			10	—	25	40	—	25	50		7.19
			5	—	100	150	—	100	200	ns	7.15
			10	—	50	75	—	50	100		7.19
Transition Time: Low-to-High Level	tTLH		5	—	75	100	—	75	125	ns	7.16
			10	—	40	60	—	40	75		—
High-to-Low Level CD4011A and CD4023A Series	tTHL		5	—	75	125	—	75	150	ns	7.17
			10	—	50	75	—	50	100		—
			5	—	250	375	—	250	500	ns	7.18
			10	—	125	200	—	125	250		—
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—

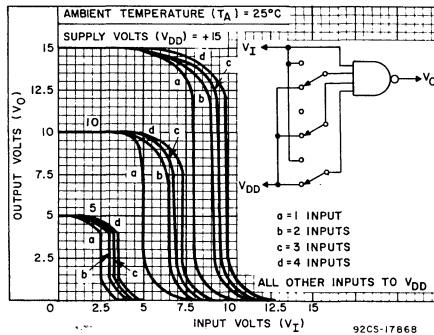


Fig.7.6 – Typ. multiple input switching transfer charact. for CD4012A.

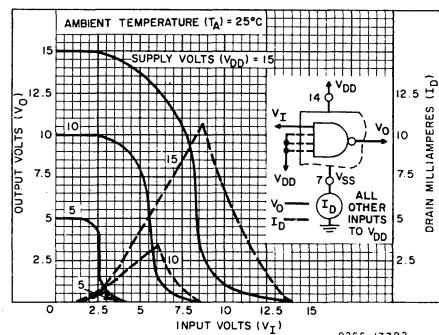


Fig.7.7 – Typ. current & voltage transfer characteristics.

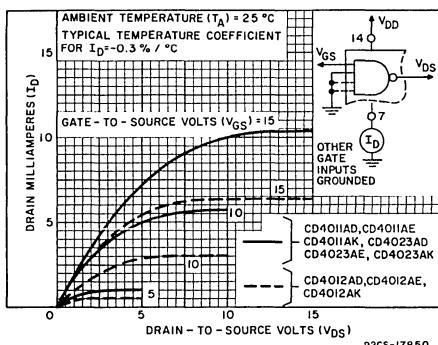


Fig. 7.8 - Typ. n-channel drain characteristics.

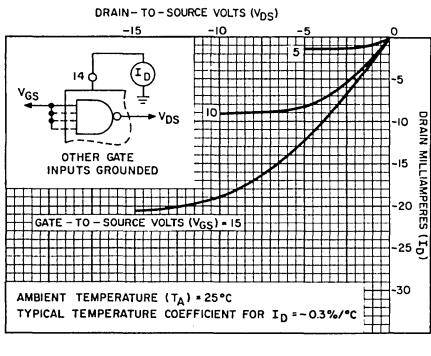


Fig. 7.9 - Typ. p-channel drain characteristics.

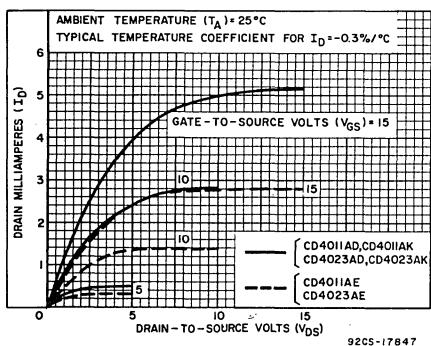
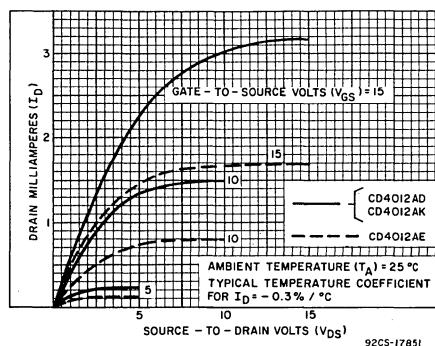
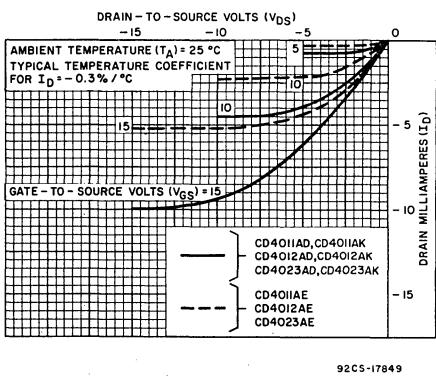
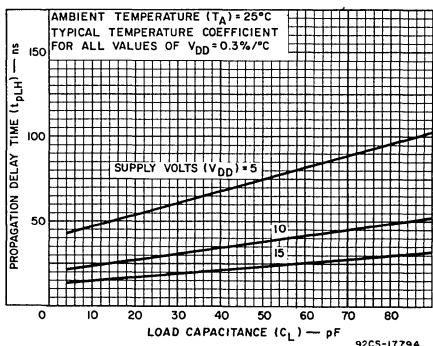
Fig. 7.10 - Min. n-channel drain characteristics  
- CD4011A & CD4023A.Fig. 7.11 - Min. n-channel drain characteristics  
- CD4012A.

Fig. 7.12 - Min. p-channel drain characteristics.

Fig. 7.13 - Typ. low-to-high level propagation delay time vs.  $C_L$ .

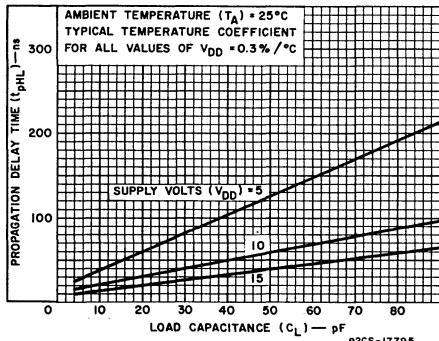


Fig. 7.14—Typ. high-to-low level propagation delay time vs.  $C_L$  — CD4011A,  
& CD4023A.

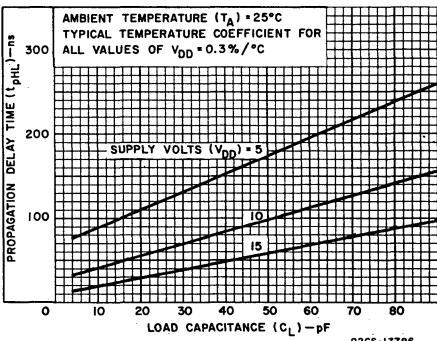


Fig. 7.15—Typ. high-to-low level propagation delay time vs.  $C_L$  — CD4012A.

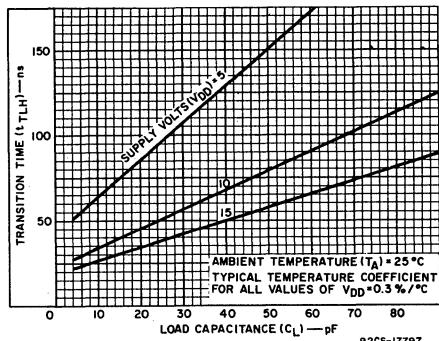


Fig. 7.16—Typ. low-to-high transition time vs.  $C_L$ .

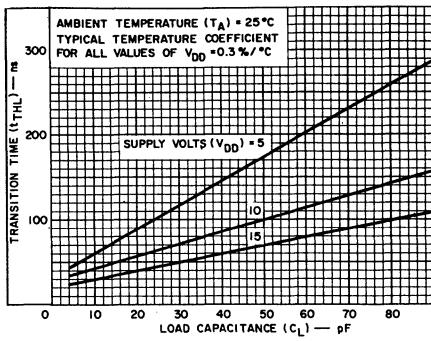


Fig. 7.17—Typ. high-to-low level transition time vs.  $C_L$  — CD4011A & CD4023A.

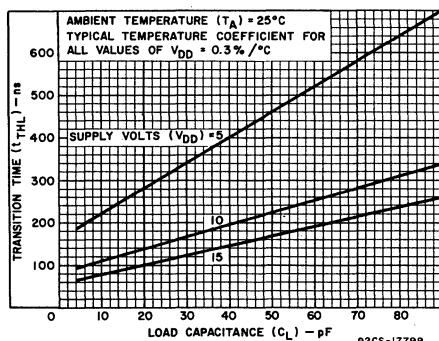


Fig. 7.18—Typ. high-to-low level transition time vs.  $C_L$  — CD4012A.

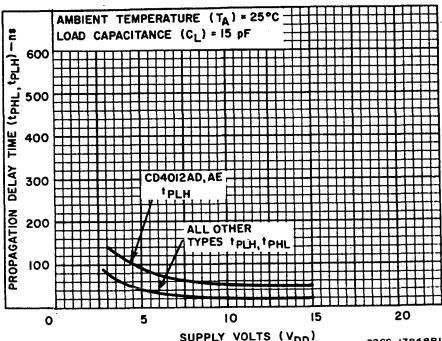


Fig. 7.19—Typ. propagation delay time vs.  $V_{DD}$ .

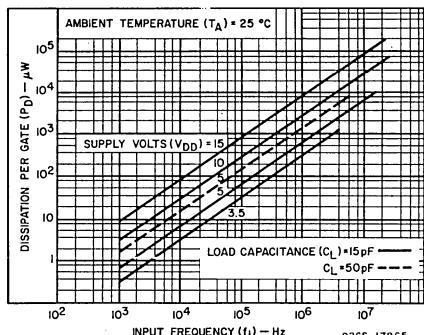


Fig. 7.20—Typ. dissipation characteristics.

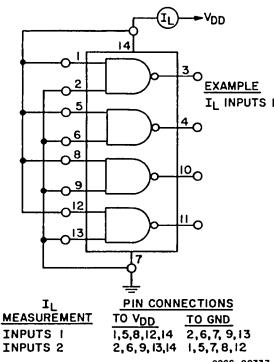


Fig. 7.21—Quiescent device current test circuit for CA4011A.

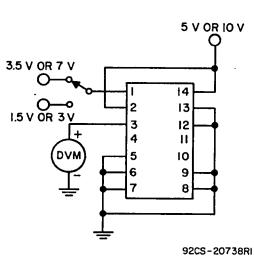


Fig. 7.22—Noise-immunity test circuit for CD4011A.

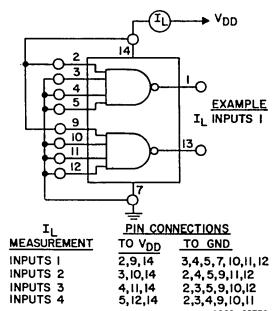


Fig. 7.23—Quiescent device current test circuit for CD4012A.

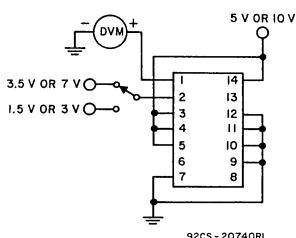


Fig. 7.24—Noise-immunity test circuit for CD4012A.

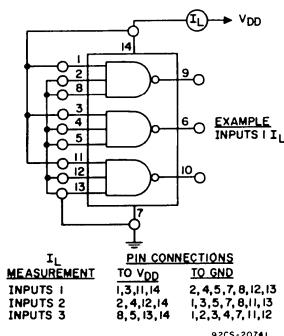


Fig. 7.25—Quiescent device current test circuit for CD4023A.

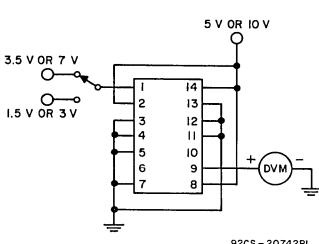
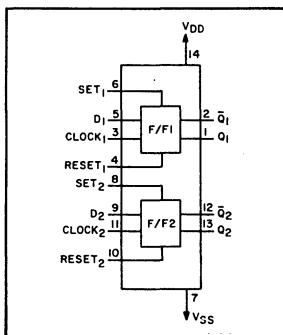


Fig. 7.26—Noise-immunity test circuit for CD4023A.

# Digital Integrated Circuits

Monolithic Silicon

**CD4013AD, CD4013AF****CD4013AE, CD4013AK**

## Dual 'D'-Type Flip-Flop

### With Set-Reset Capability

#### Special Features

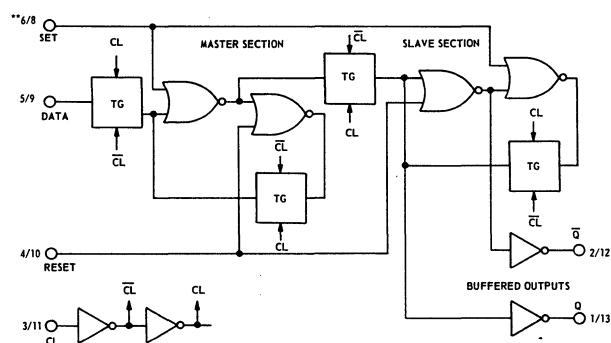
- Static flip-flop operation..... retains state indefinitely with clock level either "high" or "low"
- Medium speed operation..... 10 MHz (typ.) clock toggle rate at  $V_{DD} - V_{SS} = 10$  V
- Low "high"- and "low" output impedance.....  $400\Omega$  and  $200\Omega$ , respectively at  $V_{DD} - V_{SS} = 10$  V

#### Applications

- Registers, counters, control circuits.

CD4013A types consist of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "Q̄" outputs. These devices can be used for shift register applications, and, by connecting "Q̄" output to the data input, for counter and

toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.



TRUTH TABLE

CL <sup>a</sup>	D	R	S	Q	Q̄
/	0	0	0	0	1
/	1	0	0	1	0
/	X	0	0	Q	Q̄
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

NO CHANGE

<sup>a</sup> = LEVEL CHANGE

X = DON'T CARE CASE

\*\* = FF1/FF2 TERMINAL ASSIGNMENTS

Fig.8.1—Logic diagram and truth table (one of two identical flip-flops).

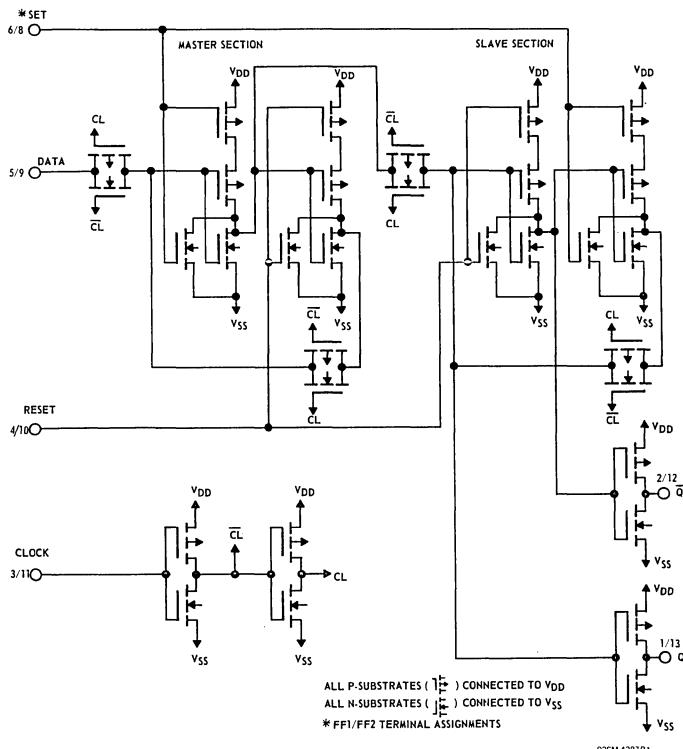


Fig.8.2—Schematic diagram (1 of two identical flip-flops).

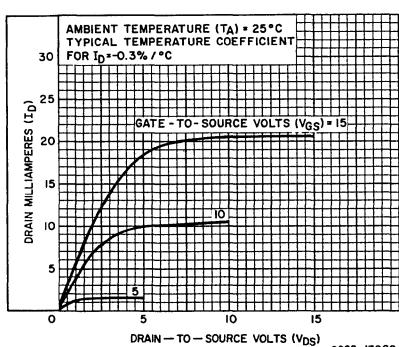


Fig.8.3—Typ. n-channel drain characteristics.

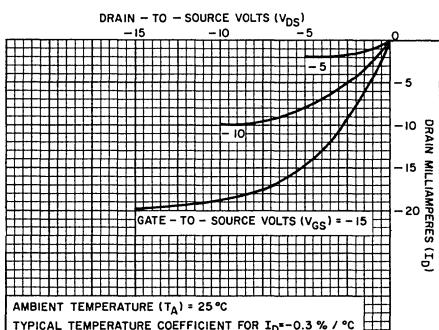


Fig.8.4—Typ. p-channel drain characteristics.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4013AD, CD4013AK, CD4013AF								
		$V_o$ Volts	$V_{DD}$ Volts	-55°C		25°C		125°C				
Quiescent Device Current	$I_L$			5	—	1	—	0.005	1	—	60	$\mu A$ 8.9
				10	—	2	—	0.005	2	—	120	
Quiescent Device Dissipation/Package	$P_D$			5	—	5	—	0.025	5	—	300	$\mu W$ 8.7
				10	—	20	—	0.05	20	—	1200	8.9
Output Voltage: Low-Level	$V_{OL}$			5	—	0.01	—	0	0.01	—	0.05	V —
				10	—	0.01	—	0	0.01	—	0.05	
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	V —
				10	9.99	—	—	9.99	10	—	9.95	
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	V 8.10
			1.0	10	3	—	—	3	4.5	—	2.9	
			4.2	5	1.4	—	—	1.5	2.25	—	1.5	V 8.10
			9.0	10	2.9	—	—	3	4.5	—	3	
Output Drive Current: N-Channel	$I_{DN}$		0.5	5	0.65	—	—	0.5	1	—	0.35	mA ◆
			0.5	10	1.25	—	—	1	2.5	—	0.75	
P-Channel	$I_{DP}$		4.5	5	-0.31	—	—	-0.25	-0.5	—	-0.175	mA
			9.5	10	-0.8	—	—	-0.65	-1.3	—	-0.45	
Input Current	$I_I$		—	—	—	—	—	10	—	—	—	pA —

◆ See Appendix

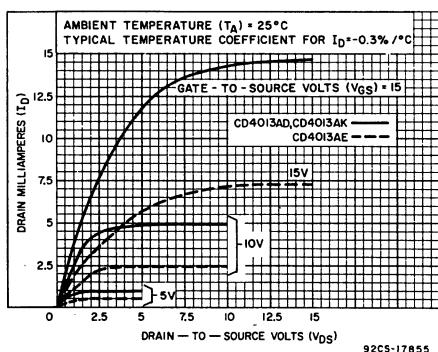


Fig. 8.5—Min. n-channel drain characteristics.

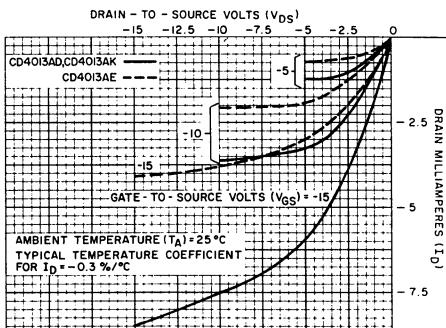


Fig. 8.6—Min. p-channel drain characteristics.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS										CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS
				CD4013AE											
		$V_o$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C					
Quiescent Device Current	$I_L$			5	—	—	10	—	0.01	10	—	—	140		
	10	—	—	—	—	20	—	0.02	20	—	—	280	μA	8.9	
Quiescent Device Dissipation/Package	$P_D$	5	—	—	50	—	0.05	50	—	—	700	—	—	μW	8.7
		10	—	—	200	—	0.2	200	—	—	2800	—	—	μW	8.9
Output Voltage: Low-Level	$V_{OL}$	5	—	—	0.01	—	0	0.01	—	—	0.05	—	—	V	—
		10	—	—	0.01	—	0	0.01	—	—	0.05	—	—	V	—
High-Level	$V_{OH}$	5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	V	—
		10	9.99	—	—	9.99	10	—	9.95	—	—	—	—	V	—
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—	V	8.10
		1.0	10	3	—	—	3	4.5	—	2.9	—	—	—	V	8.10
	$V_{NH}$	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—	V	8.10
		9.0	10	2.9	—	—	3	4.5	—	3	—	—	—	V	8.10
Output Drive Current: N-Channel	$I_{DN}$	0.5	5	0.35	—	—	0.3	1	—	0.24	—	—	—	mA	◆
		0.5	10	0.72	—	—	0.6	2.5	—	0.5	—	—	—	mA	
P-Channel	$I_{DP}$	4.5	5	-0.17	—	—	-0.14	-0.5	—	-0.12	—	—	—	mA	
		9.5	10	-0.4	—	—	-0.33	-1.3	—	-0.27	—	—	—	mA	
Input Current	$I_I$			—	—	—	—	10	—	—	—	—	—	pA	—

♦ See Appendix

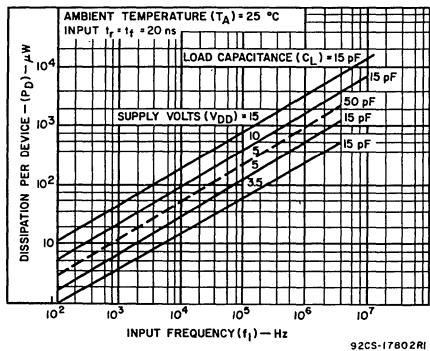


Fig.8.7—Typ. dissipation characteristics.

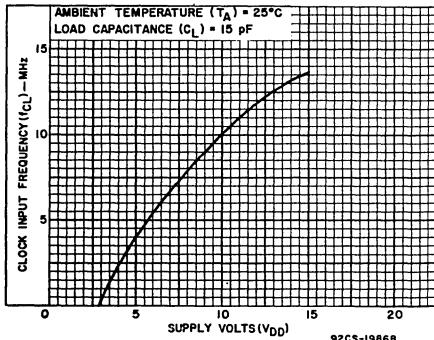


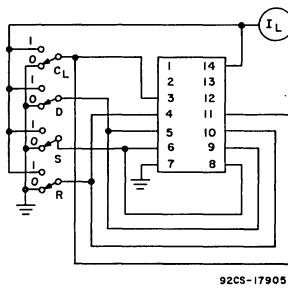
Fig.8.8—Typ. clock frequency vs.  $V_{DD}$ .

**DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns except  $t_{rCL}$ ,  $t_{fCL}$**   
 (See Appendix for Waveforms)

Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4013AD, CD4013AK			CD4013AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>CLOCKED OPERATION</b>											
Propagation Delay Time:	$t_{PHL} = t_{PLH}$		5	—	150	<b>300</b>	—	150	<b>350</b>	ns	—
			10	—	75	110	—	75	125		
Transition Time	$t_{THL} = t_{TLH}$		5	—	75	125	—	75	150	ns	—
			10	—	50	70	—	50	75		
Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		5	—	125	<b>200</b>	—	125	<b>500</b>	ns	—
			10	—	50	80	—	50	100		
Clock Rise & Fall Time	$*t_{rCL} = t_{fCL}$		5	—	—	<b>15</b>	—	—	<b>15</b>	$\mu\text{s}$	—
			10	—	—	5	—	—	5		
Set-Up Time			5	—	20	40	—	20	50	ns	—
			10	—	10	20	—	10	25		
Maximum Clock Frequency	$f_{CL}$		5	<b>2.5</b>	4	—	<b>1</b>	4	—	MHz	8.8
			10	7	10	—	5	10	—		
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF		
<b>SET &amp; RESET OPERATION</b>											
Propagation Delay Time:	$t_{PHL(R)} = t_{PLH(R)}$		5	—	175	<b>300</b>	—	175	<b>350</b>	ns	—
			10	—	75	110	—	75	125		
Minimum Set and Reset Pulse Widths	$t_{WHS}, t_{WR}$		5	—	125	<b>250</b>	—	125	<b>500</b>	ns	—
			10	—	50	<b>100</b>	—	50	<b>125</b>		

\* If more than one unit is cascaded in a parallel clocked operation,  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.



Test performed with  
the following sequence  
of "1's" and "0's".

C <sub>L</sub>	D	S	R
0	1	0	1
0	0	1	1
0	0	1	0
1	0	1	0

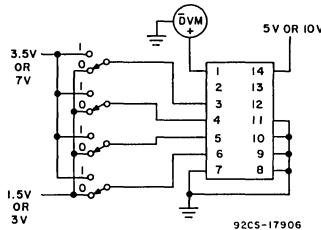
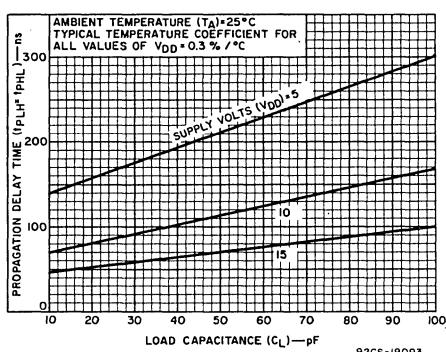
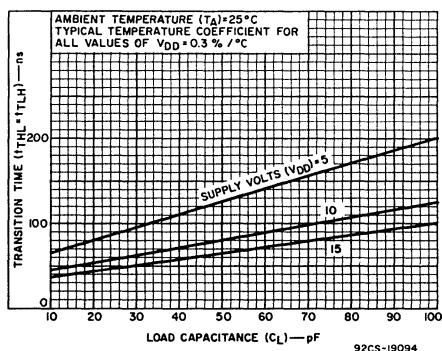


Fig.8.9—Quiescent device current test circuit.

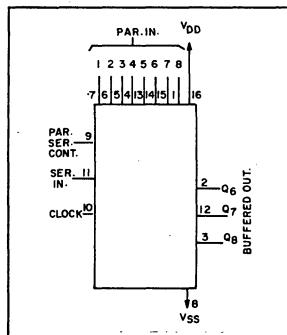
Fig.8.10—Noise immunity test circuit.

Fig.8.11—Typ. propagation delay time vs. C<sub>L</sub>.Fig.8.12—Typ. transition time vs. C<sub>L</sub>.

# **Digital Integrated Circuits**

## **Monolithic Silicon**

**CD4014AD, CD4014AF  
CD4014AE, CD4014AK**



## **COS/MOS 8-Stage**

## **Static Shift Register**

## SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT

## *Special Features*

- Medium speed operation . . . . . 5 MHz (typ.) clock rate at  $V_{DD} - V_{SS} = 10\text{ V}$
  - Fully static operation
  - MSI complexity on a single chip . . . . . 8 master-slave flip-flops plus output buffering and control gating

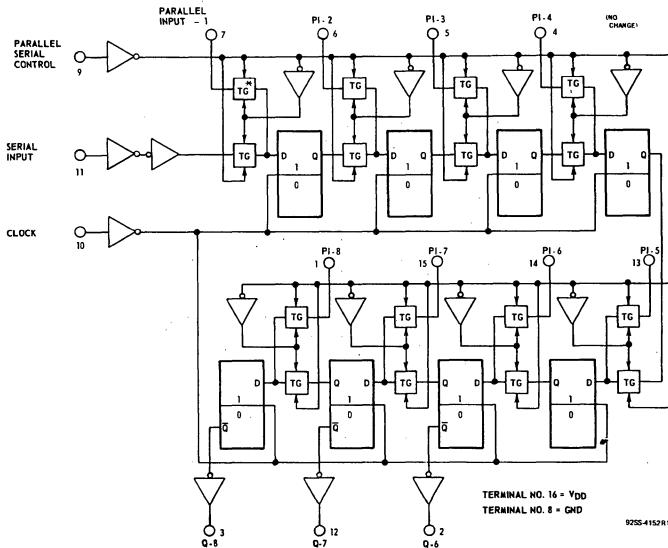
## *Applications*

- Synchronous parallel input/serial output data queueing
  - Parallel to serial data conversion
  - General purpose register

CD4014A types are 8-stage parallel-input/serial output registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7.

Parallel as well as serial entry is made into the register synchronously with the positive clock line transition and under control of the Parallel/Serial Control input. When the

Parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the Parallel/Serial Control input is "high", data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple CD40114A packages is permitted.

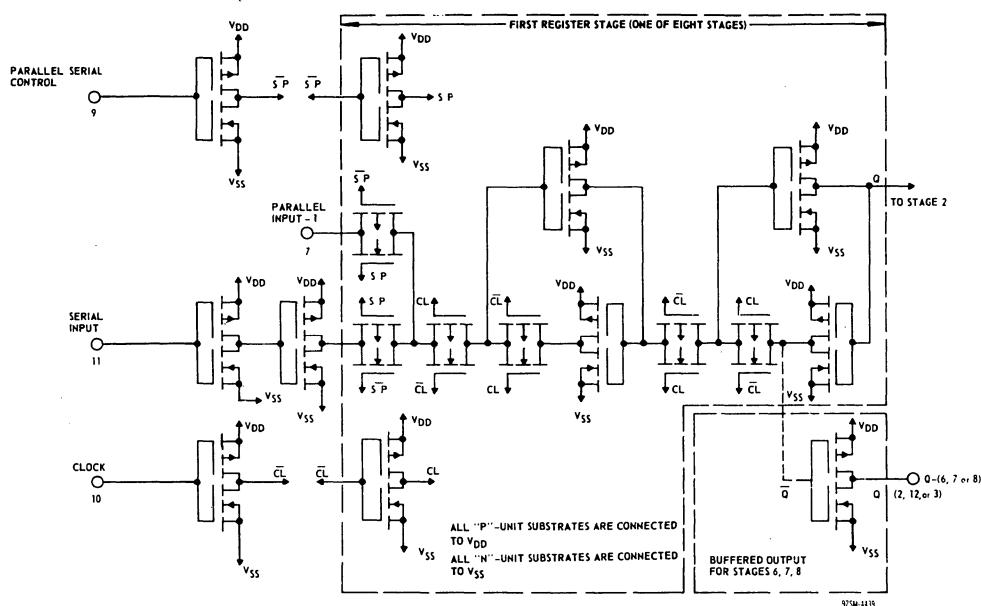


**Fig.9.1 – Logic block diagram.**

TRUTH TABLE

CL <sup>▲</sup>	SER. IN	PAR SER CONTROL	P <sub>i-1</sub>	P <sub>i-n</sub>	Q <sub>1</sub> (INTERNAL)	Q <sub>n</sub>
/	X	1	0	0	0	0
/	X	1	1	0	1	0
/	X	1	0	1	0	1
/	X	1	1	1	1	1
/	0	0	X	X	0	Q <sub>n-1</sub>
/	1	0	X	X	1	Q <sub>n-1</sub>
/	X	X	X	X	Q <sub>1</sub>	Q <sub>n</sub>

X = DON'T CARE CASE      ▲ = LEVEL CHANGE

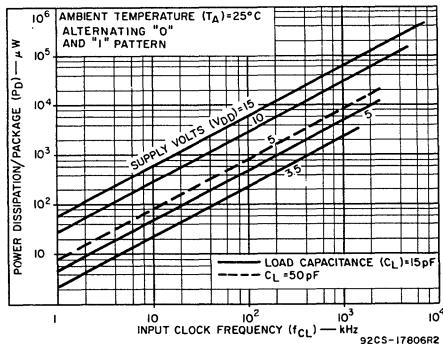


9.2—Schematic diagram — CD4014A.

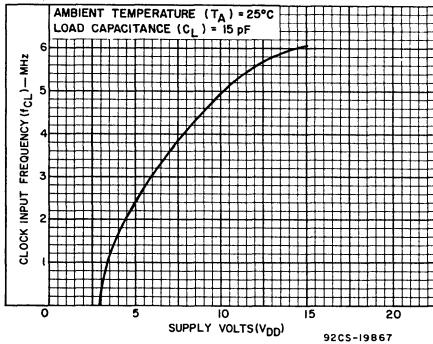
**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4014AD, CD4014AK, CD4014AF											
		$V_O$ Volts	$V_{DD}$ Volts	$-55^\circ C$			$25^\circ C$			$125^\circ C$					
Quiescent Device Current	$I_L$			5	—	—	5	—	0.5	5	—	—	300	$\mu A$	9.7
				10	—	—	10	—	1	10	—	—	600		
Quiescent Device Dissipation/Package	$P_D$			5	—	—	25	—	2.5	25	—	—	1500	$\mu W$	—
				10	—	—	100	—	10	100	—	—	6000		
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	V	9.8
				1.0	10	3	—	—	3	4.5	—	2.9	—		
	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	V	—
				9.0	10	2.9	—	—	3	4.5	—	3	—		
Output Drive Current: N-Channel	$I_{DN}$			0.5	5	0.15	—	—	0.12	0.3	—	0.085	—	mA	◆
				0.5	10	0.31	—	—	0.25	0.5	—	0.175	—		
P-Channel	$I_{DP}$			4.5	5	-0.1	—	—	-0.08	-0.16	—	-0.055	—	mA	◆
				9.5	10	-0.25	—	—	-0.20	-0.44	—	-0.14	—		
Input Current	$I_I$			—	—	—	—	10	—	—	—	—	—	pA	

♦ See Appendix



9.3 — Typ. dissipation characteristics.

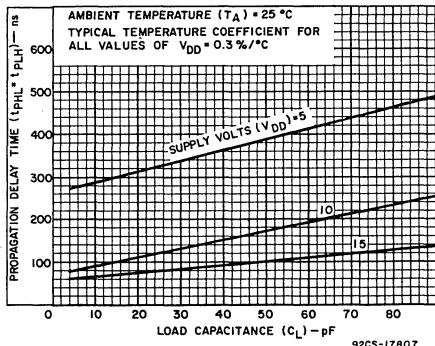
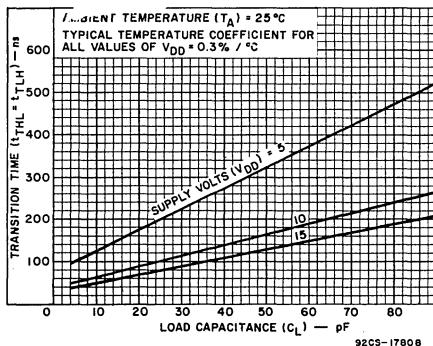


9.4 — Max. input clock frequency vs.  $V_{DD}$

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								CHARAC. TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS				
				CD4014AE													
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C							
Quiescent Device Current	$I_L$			5	—	—	50	—	0.5	50	—	—	700	μA	9.7		
				10	—	—	100	—	1	100	—	—	1400				
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	2.5	250	—	—	3500	μW	—		
				10	—	—	1000	—	10	1000	—	—	14000				
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—		
				10	—	—	0.01	—	0	0.01	—	—	0.05				
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V	—		
				10	9.99	—	—	9.99	10	—	9.95	—	—				
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	9.8		
			1.0	10	3	—	—	3	4.5	—	2.9	—	—				
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	—		
			9.0	10	2.9	—	—	3	4.5	—	3	—	—				
Output Drive Current: N-Channel	$I_{DN}$		0.5	5	0.072	—	—	0.06	0.3	—	0.05	—	—	mA	◆		
			0.5	10	0.12	—	—	0.1	0.5	—	0.08	—	—				
P-Channel	$I_{DP}$		4.5	5	-0.06	—	—	-0.05	-0.16	—	-0.04	—	—	mA	◆		
			9.5	10	-0.12	—	—	-0.1	-0.44	—	-0.08	—	—				
Input Current	$I_I$			—	—	—	—	10	—	—	—	—	—	pA			

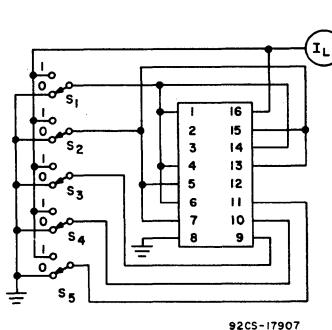
♦ See Appendix

9.5 — Typ. propagation delay time vs.  $C_L$ .9.6 — Typ. transition time vs.  $C_L$ .

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns except  $t_rCL$ ,  $t_fCL$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.			
			CD4014AD CD4014AK CD4014AF			CD4014AE							
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.				
				5	—	300	750	—	300	1000			
Propagation Delay Time:	$t_{PHL} = t_{PLH}$			10	—	100	225	—	100	300	ns	9.5	
				5	—	150	300	—	150	400			
Transition Time	$t_{THL} = t_{TLH}$			10	—	75	125	—	75	150	ns	9.6	
				5	—	200	500	—	200	830			
Minimum Clock Pulse Width	$t_{WL} = t_{WH}$			10	—	100	175	—	100	200	ns	—	
				5	—	—	15	—	—	15			
Clock Rise & Fall Time	$t_{rCL}^* = t_{fCL}$			10	—	—	15	—	—	15	$\mu\text{s}$	—	
				5	—	100	350	—	100	500			
Set-Up Time				10	—	50	80	—	50	100	ns	—	
				5	1	2.5	—	0.6	2.5	—			
Maximum Clock Frequency	$f_{CL}$			10	3	5	—	2.5	5	—	MHz	—	
				5	—	—	—	—	—	—			
Input Capacitance	$C_I$	ANY INPUT	—	—	5	—	—	5	—	pF	—	—	

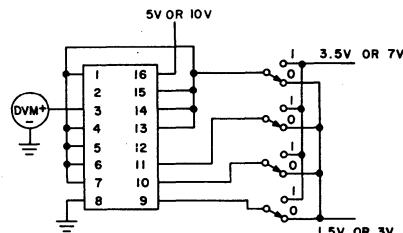
\* If more than one unit is cascaded in a parallel clocked operation,  $t_rCL$  should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.



Test performed with the following sequence of "1's" and "0's"

	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>
Don't	0	1	1	0	0
Test	0	1	1	1	0
Test	1	0	0	0	0
Test	1	0	1	1	1
Test	1	0	0	0	1

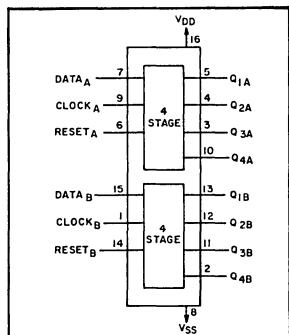
9.7—Quiescent device current test circuit.



9.8—Noise immunity test circuit.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4015AD, CD4015AF  
CD4015AE, CD4015AK****COS/MOS Dual 4-Stage Static Shift Register**

With Serial Input/Parallel Output

**Special Features**

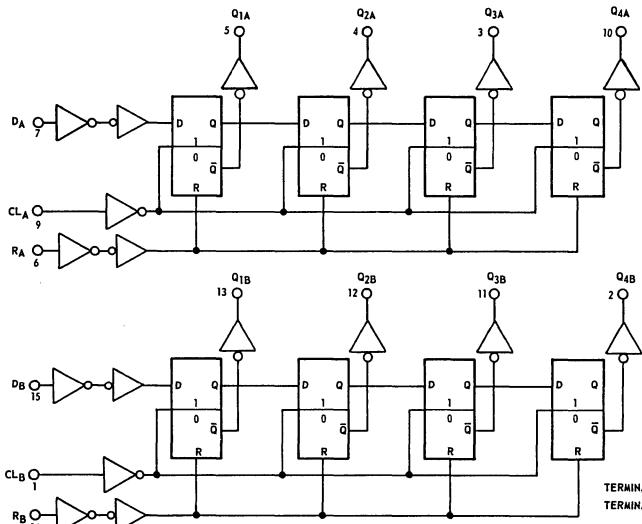
- Medium speed operation . . . . . 5 MHz (typ.) clock rate at  $V_{DD} - V_{SS} = 10$  V
- Fully static operation
- MSI complexity on a single chip . . . . . 8 master-slave flip-flops plus output buffering

**Applications**

- Serial to parallel data conversion
- Serial-input/parallel-output data queueing
- General purpose register

RCA CD4015A types consist of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs as well as a single serial "Data" input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the

data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015A package, or to more than 8 stages using additional CD4015A's is possible.



TRUTH TABLE

CL <sup>A</sup>	D	R	Q <sub>1</sub>	Q <sub>n</sub>
/	0	0	0	Q <sub>n-1</sub>
/	1	0	1	Q <sub>n-1</sub>
X	0	Q <sub>1</sub>	Q <sub>n</sub>	(NO CHANGE)
X	1	0	0	

<sup>A</sup> = LEVEL CHANGE  
X = DON'T CARE CASE

TERMINAL NO. 16 = V<sub>DD</sub>  
TERMINAL NO. 8 = GND

92SS-4155R2

Fig. 10.1—Logic diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4015AD, CD4015AK, CD4015AF											
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C					
Quiescent Device Current	$I_L$			5	—	—	5	—	0.5	5	—	—	300	$\mu A$	10.6
	10	—	—	10	—	1	10	—	—	—	—	600			
Quiescent Device Dissipation/Package	$P_D$	5	—	—	25	—	2.5	25	—	—	—	—	1500	$\mu W$	—
		10	—	—	100	—	10	100	—	—	—	—	6000		
Output Voltage: Low-Level	$V_{OL}$	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—	
		10	—	—	0.01	—	0	0.01	—	—	0.05	—			
High-Level	$V_{OH}$	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—	
		10	9.99	—	—	9.99	10	—	9.95	—	—	—			
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	10.7	
		1.0	10	3	—	—	3	4.5	—	2.9	—	—			
	$V_{NH}$	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—			
		9.0	10	2.9	—	—	3	4.5	—	3	—	—			
Output Drive Current:	$I_{DN}$	0.5	5	0.15	—	—	0.12	0.3	—	0.085	—	—	mA	◆	
		0.5	10	0.31	—	—	0.25	0.5	—	0.175	—	—			
P-Channel	$I_{DP}$	4.5	5	-0.1	—	—	-0.08	-0.16	—	-0.055	—	—	mA	◆	
		9.5	10	-0.25	—	—	-0.20	-0.44	—	-0.14	—	—			
Input Current	$I_I$			—	—	—	—	10	—	—	—	—	pA		

◆ See Appendix.

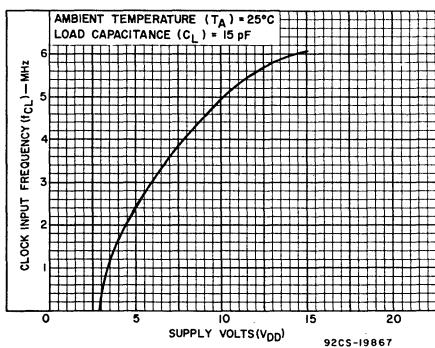


Fig. 10.2—Typ. clock frequency vs.  $V_{DD}$ .

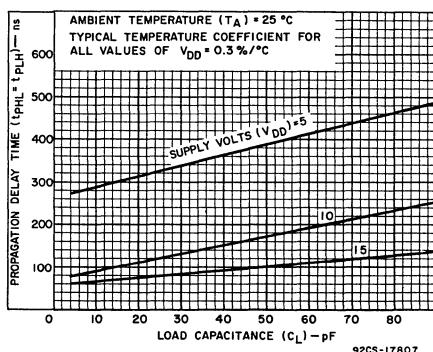


Fig. 10.3—Typ. propagation delay time vs.  $C_L$ .

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_O$ Volts	$V_{DD}$ Volts	LIMITS									CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
				CD4015AE												
				-40°C			25°C			85°C						
Quiescent Device Current	$I_L$			5	—	—	50	—	0.5	50	—	—	700	$\mu A$		
				10	—	—	100	—	1	100	—	—	1400			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	2.5	250	—	—	3500	$\mu W$		
				10	—	—	1000	—	10	1000	—	—	14000			
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V		
				10	—	—	0.01	—	0	0.01	—	—	0.05			
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V		
				10	9.99	—	—	9.99	10	—	9.95	—	—			
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V		
			1.0	10	3	—	—	3	4.5	—	2.9	—	—			
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V		
			9.0	10	2.9	—	—	3	4.5	—	3	—	—			
Output Drive Current:	$I_{DN}$		0.5	5	0.072	—	—	0.06	0.3	—	0.05	—	—	mA		
			0.5	10	0.12	—	—	0.1	0.5	—	0.08	—	—			
P-Channel	$I_{DP}$		4.5	5	-0.06	—	—	-0.05	-0.16	—	-0.04	—	—	mA		
			9.5	10	-0.12	—	—	-0.1	-0.44	—	-0.08	—	—			
Input Current	$I_I$			—	—	—	—	10	—	—	—	—	—	pA		

♦ See Appendix.

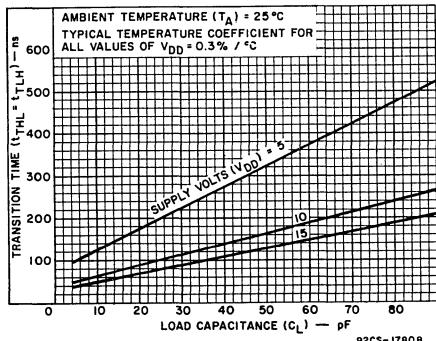


Fig.10.4—Typ. transition time vs.  $C_L$ .

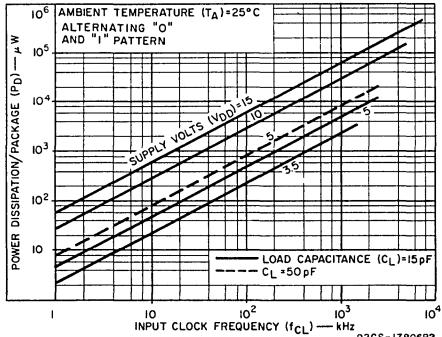


Fig.10.5—Typ. dissipation characteristics.

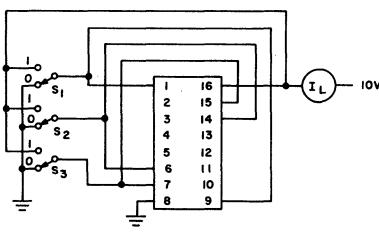
DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  and  $C_L = 15 \text{ pF}$ Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4015AD			CD4015AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>CLOCKED OPERATION</b>											
Propagation Delay Time	$t_{PHL} = t_{PLH}$		5	—	300	750	—	300	1000	ns	10.3
			10	—	100	225	—	100	300		
Transition Time	$t_{THL} = t_{TLH}$		5	—	150	300	—	150	400	ns	10.4
			10	—	75	125	—	75	150		
Minimum Clock Pulse Width	$t_{VWL} = t_{WH}$		5	—	200	500	—	200	830	ns	
			10	—	100	175	—	100	200		
Clock Rise & Fall Time	$*t_{rCL} = t_{fCL}$		5	—	—	15	—	—	15	$\mu\text{s}$	
			10	—	—	15	—	—	15		
Set-Up Time			5	—	100	350	—	100	500	ns	
			10	—	50	80	—	50	100		
Maximum Clock Frequency	$f_{CL}$		5	1	2.5	—	0.6	2.5	—	MHz	
			10	3	5	—	2.5	5	—		
Input Capacitance	$C_I$		—	5	—	—	5	—	pF		
<b>RESET OPERATION</b>											
Propagation Delay Time	$t_{PHL(R)}$		5	—	300	750	—	300	1000	ns	
			10	—	100	225	—	100	300		
Minimum Set and Reset Pulse Widths	$t_{WH(R)}$		5	—	200	500	—	200	830	ns	
			10	—	100	175	—	100	200		

- If more than one unit is cascaded in a parallel clocked operation,  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.

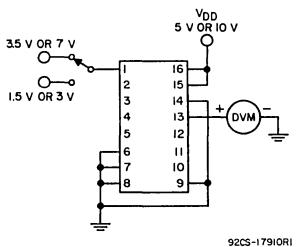
Test performed with the following sequence of "1's" and "0's"

	$S_1$	$S_2$	$S_3$
Test	0	1	0
Don't Test	0	0	1
Don't Test	1	0	1
Don't Test	0	0	0
Don't Test	1	0	0
Don't Test	0	0	1
Test	1	0	1
Don't Test	0	0	0
Test	1	0	0

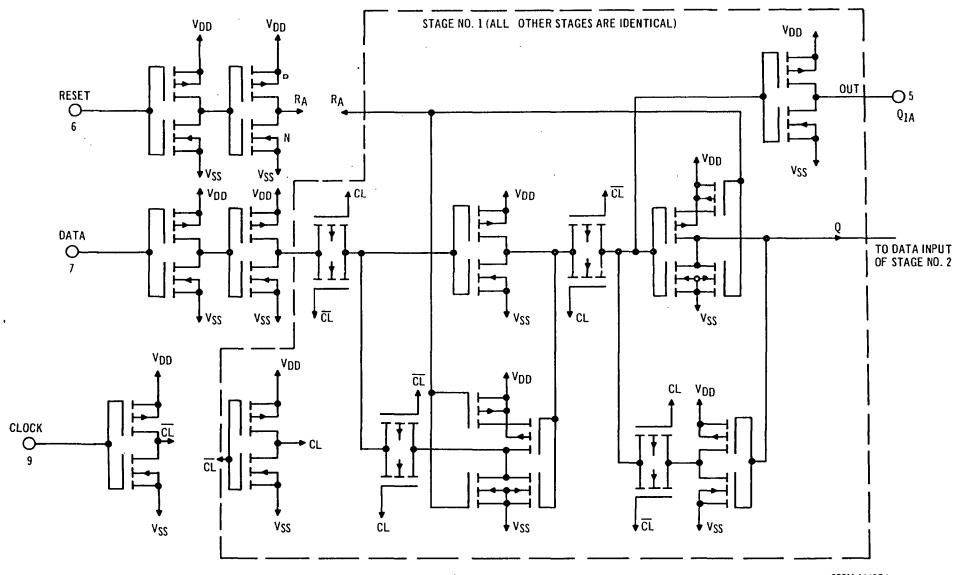


92CS-17909

Fig.10.6 – Quiescent device current test circuit.



*Fig. 10.7 – Noise immunity test circuit.*



*Fig. 10.8 – Schematic diagram.*

# Digital Integrated Circuits

Monolithic Silicon

**CD4016AD, CD4016AF  
CD4016AE, CD4016AK**

## COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

### Special Features

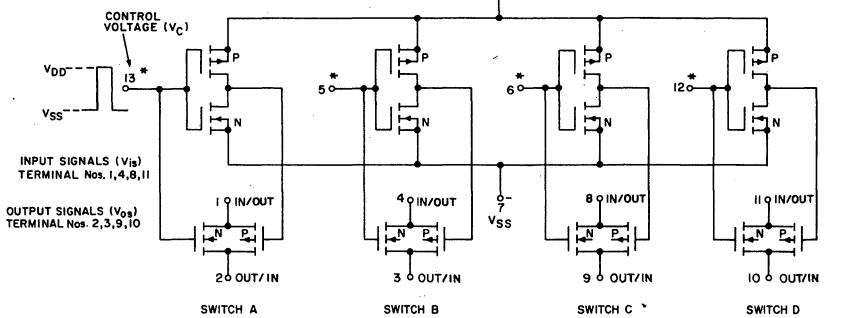
- Wide range of digital and analog signal levels —  
Digital or analog signal to 15 V peak  
Analog signal  $\pm 7.5$  V peak
- Low "ON" resistance —  
 $300\ \Omega$  typ. over 15 V p-p signal input range, for  $V_{DD} - V_{SS} = 15$  V
- Matched switch characteristics —  
 $40\ \Omega$  typ. difference between  $R_{ON}$  values at a fixed bias point over 15 V p-p signal input range  $V_{DD} - V_{SS} = 15$  V
- High "On/Off" output voltage ratio —  $-65$  dB typ. @  $f_{IS} = 10$  kHz,  $R_L = 10\ k\Omega$
- High degree of linearity —  $< 0.5\%$  distortion typ. @  $f_{IS} = 1$  kHz,  
 $V_{IS} = 5$  V p-p,  $V_{DD} - V_{SS} \geq 10$  V,  $R_L = 10\ k\Omega$ .

### Applications

- Analog signal switching/multiplexing  
Signal gating  
Squelch control  
Chopper
- Digital signal switching/Multiplexing
- COS/MOS logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Modulator  
Demodulator  
Commutating switch

- Extremely low "OFF" switch leakage resulting in very low offset current and high effective "OFF" resistance —  
 $10\ pA$  typ. @  $V_{DD} - V_{SS} = 10$  V,  $T_A = 25^\circ C$
- Extremely high control input impedance (control circuit isolated from signal circuit) —  $10^{12}\ \Omega$  typ.
- Low crosstalk between switches —  
 $-50$  dB typ. @  $f_{IS} = 0.9$  MHz,  $R_L = 1\ k\Omega$
- Matched control-input to signal-output capacitances — Reduces output signal transients
- Transmits frequencies up to 10 MHz



NOTE: All switch P-channel substrates are internally connected to terminal No. 14.  
All switch N-channel substrates are internally connected to terminal No. 7.

### NORMAL OPERATION:

#### Control-Line Biasing

Switch "ON":  $V_C = V_{DD}$   
Switch "OFF":  $V_C = V_{SS}$

#### SIGNAL-LEVEL RANGE:

$V_{SS} \leq V_I \leq V_{DD}$

#### Caution:

If  $V_I$  exceeds  $V_{DD}$ , input currents must not be allowed to exceed 5 mA.

Fig. 11.1—Schematic diagram.

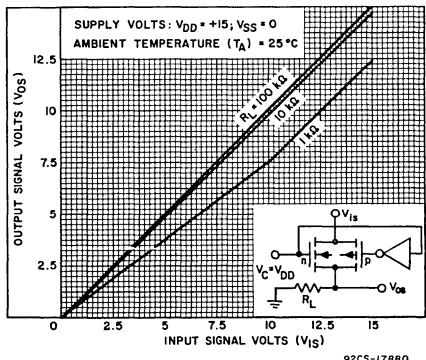


Fig.11.2—Typ. "ON" characteristics for 1 of  
4 switches with  $V_{DD} = +15V$ ,  
 $V_{SS} = OV$ .

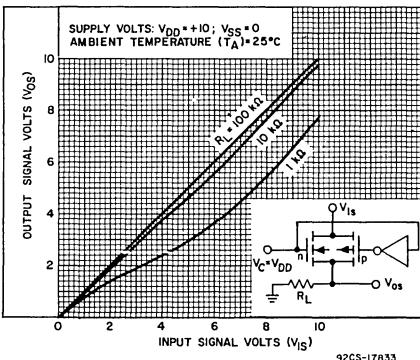


Fig.11.3—Typ. "ON" characteristics for 1 of  
4 switches with  $V_{DD} = +10V$ ,  
 $V_{SS} = OV$ .

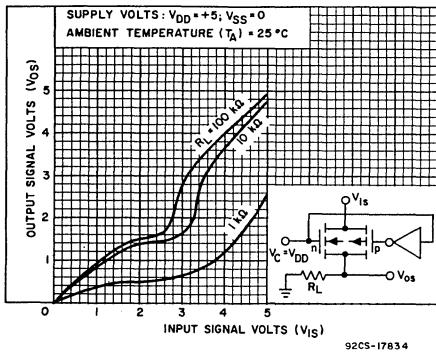


Fig.11.4—Typ. "ON" characteristics for 1 of  
4 switches with  $V_{DD} = +5V$ ,  
 $V_{SS} = OV$ .

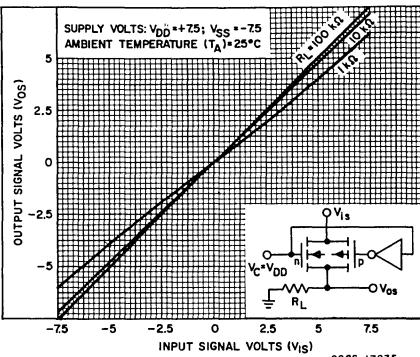


Fig.11.5—Typ. "ON" characteristics for 1 of  
4 switches with  $V_{DD} = +2.5V$ ,  
 $V_{SS} = -2.5V$ .

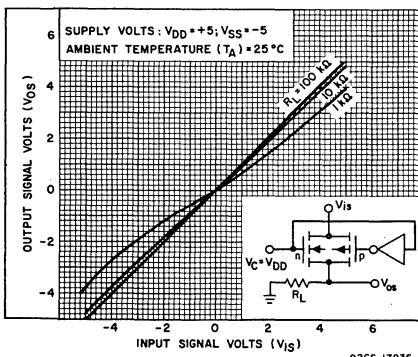


Fig.11.6—Typ. "ON" characteristics for 1 of  
4 switches with  $V_{DD} = +5V$ ,  
 $V_{SS} = -5V$ .

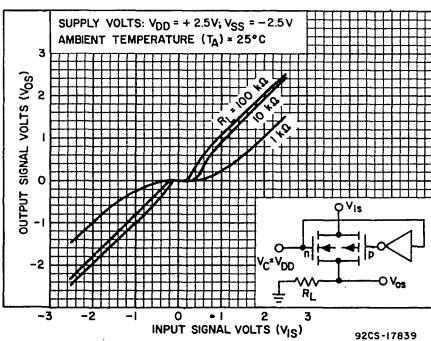


Fig.11.7—Typ. "ON" characteristics for 1 of  
4 switches with  $V_{DD} = +2.5V$ ,  
 $V_{SS} = -2.5V$ .

**ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	
			CD4016AD		CD4016AK		CD4016AF			
			-55°C	25°C	25°C	125°C	Typ.	Max.		
Quiescent Dissipation per Package	$P_T$	$V_{DD}$ 14	VOLTS TERMINALS APPLIED +10							
All Switches "OFF"		$V_{SS}$ 7	GND	-	5	0.1	5	-	300 $\mu$ W	
		$V_C$ 5, 6, 12, 13	GND							
		$V_{IS}$ 1, 4, 8, 11	$\leq +10$							
		$V_{OS}$ 2, 3, 9, 10	$\leq +10$							
All Switches "ON"		$V_{DD}$ 14	VOLTS TERMINALS APPLIED +10							
		$V_{SS}$ 7	GND	-	5	0.1	5	-	300 $\mu$ W	
		$V_C$ 5, 6, 12, 13	+10							
		$V_{IS} = V_{OS}$ 1, 4, 8, 11	$\leq +10$							
SIGNAL INPUTS ( $V_{IS}$ ) AND OUTPUTS ( $V_{OS}$ )										
"ON" Resistance	$R_{ON}$	$V_C = V_{DD}$	$V_{SS}$	$V_{IS}$	120	360	200	400	300	600
		+7.5V	-7.5V	+7.5V	120	360	200	400	300	600
		+7.5V	-7.5V	-7.5V	120	360	200	400	300	600
		+7.5V	-7.5V	+0.25V	130	775	280	850	470	1230
		+5V	-5V	+5V	130	600	250	660	400	960
		+5V	-5V	-5V	130	600	250	660	400	960
		+5V	-5V	+0.25V	325	1870	580	2000	900	2600
		+15V	0V	+15V	120	360	200	400	300	600
		+15V	0V	+0.25V	120	360	200	400	300	600
		+15V	0V	9.3V	150	775	300	850	490	1230
$\Delta$ "ON" Resistance Between Any 2 of 4 Switches	$\Delta R_{ON}$	+10V	0V	+10V	130	600	250	660	400	960
		+10V	0V	+0.25V	130	600	250	660	400	960
		+10V	0V	5.6V	300	1870	560	2000	880	2600
Sine-Wave Response (Distortion)		+7.5V	-7.5V	$\pm 7.5V$	-	-	10	-	-	-
		+5V	-5V	$\pm 5V$	-	-	15	-	-	-
Input or Output Leakage-Switch "OFF" (Effective "OFF" Resistance)	$R_L = 10k\Omega$	$R_L = 10k\Omega$	$V_C = V_{SS}$	$V_{IS}$	-	-	0.4	-	-	%
		+5V	-5V	5V(p p) $\Delta$	-	-	-	-	-	
		+5V	-5V	$\pm 5V$	-	-	-	-	-	
Frequency-Response-Switch "ON" (Sine Wave Input)	$R_L = 1k\Omega$	$V_C = V_{DD} = -5V$	$V_{SS} = -5V$	$V_{OS} = -3k\Omega$	-	-	$\pm 100$	-	-	pA
		$V_{DD} = -5V$	$V_C = V_{SS} = -5V$	$V_{OS} = -50k\Omega$	-	-	-	$\pm 125$	-	nA
Feedthrough Switch "OFF"		$V_{IS} = 5V(p p)$	$V_{DD} = -5V$	$V_{OS} = -50k\Omega$	-	-	-	-	-	MHz
Crosstalk Between Any 2 of the 4 Switches (Frequency at -50 dB)		$R_L = 1k\Omega$	$V_C(A) = V_{DD} = -5V$	$V_C(B) = V_{SS} = -5V$	-	-	0.9	-	-	MHz
		$V_{IS}(A) = 5V(p p)$	$V_{OS}(B) = -50k\Omega$	$V_{OS}(A) = -50k\Omega$	-	-	-	-	-	
Capacitance Input	$C_{IS}$	$V_{DD} = +5V$	$V_C = V_{SS} = -5V$		-	-	4	-	-	
Output	$C_{OS}$				-	-	4	-	-	
Feedthrough	$C_{IOS}$				-	-	0.2	-	-	pF
Propagation Delay Signal Input to Signal Output	$t_{pd}$	$V_C = V_{DD} = +10V$	$V_{SS} = GND$	$C_L = 15pF$	-	-	10	-	-	ns
		$V_{IS} = 10V$ (square wave)			-	-	-	-	-	
		$t_f = t_p = 20$ ns (input signal)			-	-	-	-	-	

•  $\pm 10 \times 10^{-3}$ 

▲ Symmetrical about 0 volts

\* Limit determined by minimum feasible leakage measurement for automatic testing.

**ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_i \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS			
			CD4016AE									
			-40°C		25°C		85°C					
			Typ.	Max.	Typ.	Max.	Typ.	Max.				
Quiescent Dissipation per Package	$P_T$	$V_{DD}$ $V_{SS}$ $V_C$ $V_{is}$ $V_{os}$	TERMINALS 14	VOLTS +10	-	5	0.1	5	-	80	$\mu W$	
			$V_{SS}$	GND	-	5	0.1	5	-	80	$\mu W$	
			$V_C$	GND	-	5	0.1	5	-	80	$\mu W$	
			$V_{is}$	$\leq +10$	-	5	0.1	5	-	80	$\mu W$	
			$V_{os}$	$\leq +10$	-	5	0.1	5	-	80	$\mu W$	
		$V_{DD}$ $V_{SS}$ $V_C$ $V_{is} = V_{os}$ $V_{is}$	TERMINALS 14	VOLTS +10	-	5	0.1	5	-	80	$\mu W$	
			$V_{SS}$	GND	-	5	0.1	5	-	80	$\mu W$	
			$V_C$	+10	-	5	0.1	5	-	80	$\mu W$	
			$V_{is} = V_{os}$	$\leq +10$	-	5	0.1	5	-	80	$\mu W$	
			$V_{is}$	$\leq +10$	-	5	0.1	5	-	80	$\mu W$	
SIGNAL INPUTS ( $V_{is}$ ) AND OUTPUTS ( $V_{os}$ )												
"ON" Resistance	$R_{ON}$	$R_L = 10k\Omega$ $f_{is} = 1kHz$	$V_C - V_{DD}$	$V_{SS}$	$V_{is}$	130	370	200	400	260	520	$\Omega$
			+7.5V	-7.5V	+7.5V	130	370	200	400	260	520	$\Omega$
			+7.5V	-7.5V	-7.5V	130	370	200	400	260	520	$\Omega$
			+7.5V	-7.5V	$\pm 0.25V$	160	790	280	850	400	1080	$\Omega$
			+5V	-5V	+5V	150	610	250	660	340	840	$\Omega$
			+5V	-5V	-5V	150	610	250	660	340	840	$\Omega$
			+5V	-5V	$\pm 0.25V$	370	1900	580	2000	770	2380	$\Omega$
			+15V	0V	+15V	130	370	200	400	260	520	$\Omega$
			+15V	0V	$\pm 0.25V$	130	370	200	400	260	520	$\Omega$
			+15V	0V	9.3V	180	790	300	850	400	1080	$\Omega$
$\Delta$ "ON" Resistance Between Any 2 of 4 Switches	$\Delta R_{ON}$	$R_L = 10k\Omega$ $f_{is} = 1kHz$	+10V	0V	+10V	150	610	250	660	340	840	$\Omega$
			+10V	0V	$\pm 0.25V$	150	610	250	660	340	840	$\Omega$
			+7.5V	-7.5V	$\pm 7.5V$	-	-	10	-	-	-	$\Omega$
Sine-Wave Response (Distortion)		$R_L = 10k\Omega$ $f_{is} = 1kHz$	+5V	-5V	$\pm 5V$	-	-	0.4	-	-	-	%
			+5V	-5V	$\pm 5V$	-	-	15	-	-	-	%
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		$R_L = 10k\Omega$ $f_{is} = 1kHz$	$V_{DD}$	$V_C = V_{SS}$	$V_{is}$	-	-	$\pm 100$	-	-	-	pA
			+7.5V	-7.5V	$\pm 7.5V$	-	-	*	-	-	-	nA
Frequency-Response-Switch "ON" (Sine Wave Input)		$R_L = 1k\Omega$ $f_{is} = 1kHz$	+5V	-5V	$5V(p\ p)$	-	-	0.4	-	-	-	%
			+5V	-5V	$\pm 5V$	-	-	10	-	-	-	%
Feedthrough Switch "OFF"		$R_L = 1k\Omega$ $f_{is} = 1kHz$	$V_C$	$V_{DD} = +5V$	$V_{SS} = -5V$	-	-	40	-	-	-	MHz
			$V_{DD} = +5V$	$V_C = V_{SS} = -5V$	$\frac{V_{DD}}{20 \log_{10} \frac{V_C}{V_{SS}}} = -3dB$	-	-	1.25	-	-	-	MHz
Crosstalk Between Any 2 of the 4 Switches (Frequency at -50 dB)		$R_L = 1k\Omega$ $f_{is} = 1kHz$	$V_{is}(A) = 5V(p\ p)$	$V_{DD} = +5V$	$V_{SS} = -5V$	-	-	0.9	-	-	-	MHz
			$V_{is}(A) = 5V(p\ p)$	$V_{DD} = +5V$	$V_{SS} = -5V$	-	-	$\frac{V_{is}(B)}{20 \log_{10} \frac{V_{is}(B)}{V_{is}(A)}} = -50dB$	-	-	-	MHz
Capacitance	$C_{IS}$	$V_{DD} = +5V$ $V_C = V_{SS} = -5V$	-	-	4	-	-	-	-	-	pF	
	$C_{OS}$		-	-	4	-	-	-	-	-	pF	
	$C_{IOS}$		-	-	0.2	-	-	-	-	-	pF	
Propagation Delay Signal Input to Signal Output	$t_{pd}$	$V_C = V_{DD} = +10V$	$V_{SS} = GND$	$C_L = 15pF$	$V_{is} = 10V$ (square wave)	-	-	10	-	-	-	ns
		$t_i = t_f = 20\text{ ns}$ (input signal)				-	-	-	-	-	-	

•  $\pm 10 \times 10^{-3}$

\* Limit determined by minimum feasible leakage measurement for automatic testing.

▲ Symmetrical about 0 volts

**ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										UNITS	
			CD4016AD, CD4016AK, CD4016A F			-55°C			25°C			125°C		
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	
<b>CONTROL (<math>V_C</math>)</b>														
Switch Threshold Voltage*	$V_{THN}$	$V_{is} \leq V_{DD}$	$V_{DD} - V_{SS} = 15V, 10V,$ $5V; I_{IS} = 10\mu A$	0.7	-	2.9	0.5	1.5	2.7	0.2	-	2.4	V	
Input Current	$I_C$		$V_{DD} - V_{SS} = 10V,$ $V_C \leq V_{DD} - V_{SS}$	-	-	-	-	$\pm 10$	-	-	-	-	pA	
Average Input Capacitance	$C_C$			-	-	-	-	5	-	-	-	-	pF	
Crosstalk (Control Input to Signal Output)			$V_{DD} - V_{SS} = 10V,$ $V_C = 10V$	$R_L = 10k\Omega$	-	-	-	50	-	-	-	-	mV	
Turn "ON" Propagation Delay	$t_{pdC}$		(square wave); $t_C = t_C = 20\text{ ns}$	$V_{is} \leq 10V, C_L = 15\text{ pF}$	-	-	-	20	-	-	-	-	ns	
Maximum Allowable Control Input Repetition Rate			$V_{DD} = 10V, V_{SS} = GND, R_L = 1k\Omega$ $C_L = 15\text{ pF}$ $V_C = 10V$ (square wave) $t_C = t_C = 20\text{ ns}$	-	-	-	-	10	-	-	-	-	MHz	

**TYPICAL "ON" RESISTANCE CHARACTERISTICS**

CHARAC- TERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS						TYPICAL CHARAC- TERISTIC CURVE Fig. No.
			$R_L = 1k\Omega$		$R_L = 10k\Omega$		$R_L = 100k\Omega$		
	$V_{DD}$ (V)	$V_{SS}$ (V)	VALUE (Ω)	$V_{is}$ (V)	VALUE (Ω)	$V_{is}$ (V)	VALUE (Ω)	$V_{is}$ (V)	
$R_{ON}$	+15	0	200	+15	200	+15	180	+15	11.2
			200	0	200	0	200	0	
$R_{ON(max.)}$	+15	0	300	+11	300	+9.3	320	+9.2	11.3
			290	+10	250	+10	240	+10	
$R_{ON}$	+10	0	290	0	250	0	300	0	11.4
			500	+7.4	560	+5.6	610	+5.5	
$R_{ON}$	+ 5	0	860	+ 5	470	+ 5	450	+ 5	11.5
			600	0	580	0	800	0	
$R_{ON(max.)}$	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7	11.6
			200	+7.5	200	+7.5	180	+7.5	
$R_{ON}$	+7.5	-7.5	200	-7.5	200	-7.5	180	-7.5	11.7
			290	$\pm 0.25$	280	$\pm 25$	400	$\pm 0.25$	
$R_{ON}$	+ 5	- 5	260	+ 5	250	+ 5	240	+ 5	11.8
			310	- 5	250	- 5	240	- 5	
$R_{ON(max.)}$	+ 5	- 5	600	$\pm 0.25$	580	$\pm 0.25$	760	$\pm 0.25$	11.9
			590	+2.5	450	+2.5	490	+2.5	
$R_{ON}$	+2.5	-2.5	720	-2.5	520	-2.5	520	-2.5	12.0
			232k	$\pm 0.25$	300k	$\pm 0.25$	870k	$\pm 0.25$	

\* Variation from a perfect switch:  $R_{OFF} = 0\Omega$ .

**ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS												UNITS					
			CD4016A E																	
			-40°C			25°C			85°C			Min.			Typ.			Max.		
CONTROL ( $V_C$ )			-	-	-	0.5	1.5	2.7	-	-	-	-	-	-	-	-	-	-	-	-
Switch Threshold Voltage*	$V_{THN}$	$V_{IS} \leq V_{DD}$	$V_{DD} - V_{SS} = 15V, 10V,$ $5V; I_{IS} = 10\mu A$	-	-	-	0.5	1.5	2.7	-	-	-	-	-	-	-	-	-	-	V
Input Current	$I_C$		$V_{DD} - V_{SS} = 10V,$ $V_C \leq V_{DD} - V_{SS}$	-	-	-	-	$\pm 10$	-	-	-	-	-	-	-	-	-	-	-	pA
Average Input Capacitance	$C_C$		-	-	-	-	-	5	-	-	-	-	-	-	-	-	-	-	-	pF
Crosstalk (Control Input to Signal Output)		$V_{DD} - V_{SS} = 10V,$ $V_C = 10V$ (square wave), $t_{rc} = t_{lc} = 20\text{ ns}$	$R_L = 10k\Omega$	-	-	-	-	50	-	-	-	-	-	-	-	-	-	-	-	mV
Turn "ON" Propagation Delay	$t_{pdC}$		$V_{IS} \leq 10V, C_L = 15pF$	-	-	-	-	20	-	-	-	-	-	-	-	-	-	-	-	ns
Maximum Allowable Control Input Repetition Rate		$V_{DD} = 10V, V_{SS} = GND, R_L = 1k\Omega$ $C_L = 15pF$ $V_C = 10V$ (square wave) $t_f = t_r = 20\text{ ns}$	-	-	-	-	-	10	-	-	-	-	-	-	-	-	-	-	-	MHz

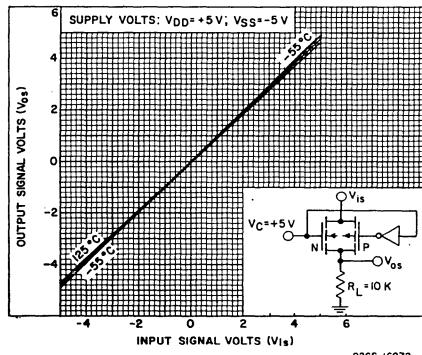


Fig. 11.8—Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with  $V_{DD} = +5V$ ,  $V_{SS} = -5V$ .

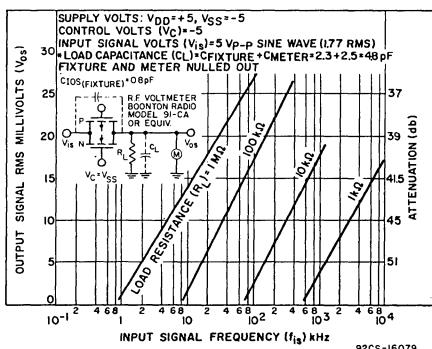
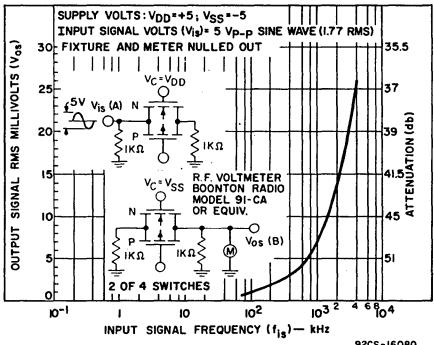
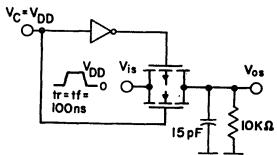


Fig. 11.9—Typ. feedthru vs. freq. — switch "OFF".



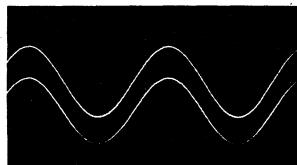
*Fig. 11.10—Typ. crosstalk between switch circuits in the same package.*



ALL UNUSED TERMINALS  
ARE CONNECTED TO V<sub>SS</sub>

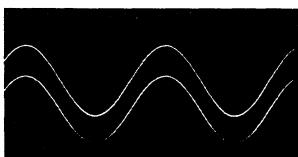
92CS-16086

*Fig. 11.12—Test circuit for square wave response.*



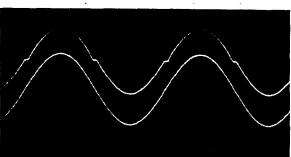
SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV  
 $V_{DD} = V_C = +7.5V$ ,  $V_{SS} = -7.5V$ ,  $R_L = 10\text{K}\Omega$   
 $C_L = 15 \text{ pF}$   
 $f_{IS} = 1 \text{ KHz}$   $V_{IS} = 5V \text{ p-p}$   
 DISTORTION = 0.2 %

Fig. 11.14—Typ. sine wave response of  $V_{DD} = +7.5V$ ,  $V_{SS} = -7.5V$ .



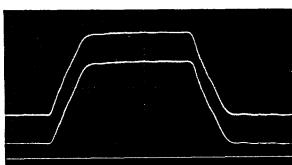
**SCALE:** X = 0.2 ms/DIV Y = 2.0 V/DIV  
**VDD** =  $V_C$  = +5 V,  $V_{SS}$  = -5 V,  $R_L$  = 10K $\Omega$   
**CL** = 15 pF  
**fJS** = 1 KHz  $V_{IS}$  = 5 V p-p  
**DISTORTION** = 0.4 %

*Fig. 11.15—Typ. sine wave response of  $V_{DD} = +5V$ ,  $V_{SS} = -5V$ .*



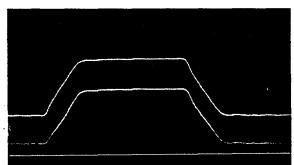
**SCALE:** X = 0.2 ms/DIV Y = 2.0 V/DIV  
**VDD** =  $V_C$  = +2.5V,  $V_{SS}$  = -2.5V,  $R_L$  = 10K $\Omega$   
**CL** = 15 pF  
**f1** = 1 KHz **V1S** = 5V p-p  
**DISTORTION** = 3 %

Fig. 11.16—Typ. sine wave response of  $V_{DD} = +2.5V$ ,  $V_{SS} = -2.5V$ .



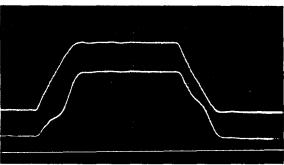
SCALE: X = 100 ns/DIV  
Y = 5.0 V/DIV

Fig. 11.17—Typ. square wave response at  
 $V_{DD} = V_C = +15V$ ,  $V_{SS} = Gnd.$



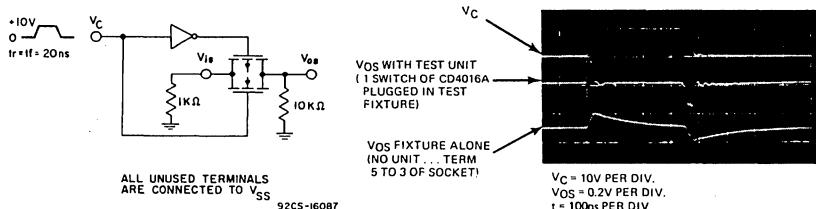
SCALE: X = 100 ns/DIV  
Y = 5.0 V/DIV

*Fig. 11.18—Typ. square wave response at  
 $V_{DD} = V_C = +10V$ ,  $V_{SS} = Gnd.$*

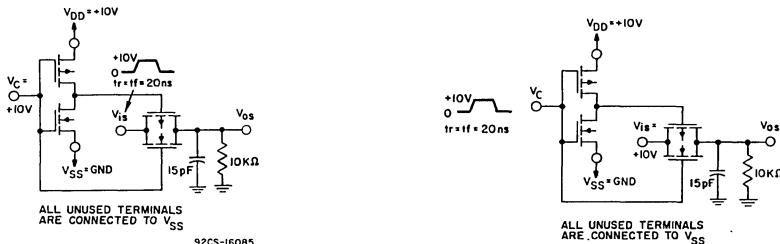


SCALE: X = 100 ns/DIV  
Y = 2 V/DIV

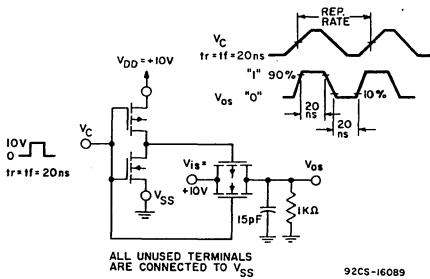
*Fig. 11.19—Typ. square wave response at  
 $V_{DD} = V_C = +5V$ ,  $V_{SS} = Gnd.$*



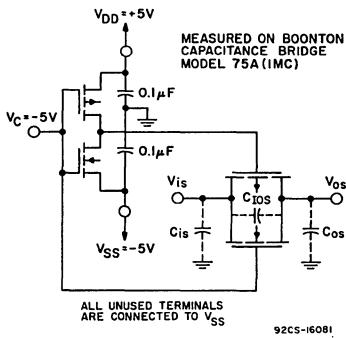
*Fig. 11.20—Crosstalk-control input to signal output.*



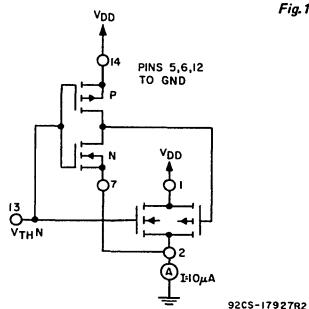
**Fig. 11.21**—Propagation delay time signal input ( $V_{IS}$ ) to signal output ( $V_{OS}$ ).



*Fig. 11.23—Max. allowable control-input repetition rate.*



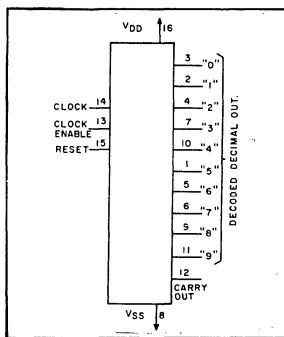
*Fig. 11.24—Capacitance  $C_{10S}$  and  $C_{0S}$ .*



*Fig. 11-25—Switch threshold voltage -N-channel test circuit.*

**Digital Integrated Circuits**

Monolithic Silicon

**CD4017AD, CD4017AF****CD4017AE, CD4017AK**

CD4017A types consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a "Clock", a "Reset", and a "Clock Enable" signal.

The decade counter is advanced one count at the positive clock signal transition if the clock enable signal is "low". Counter advancement via the clock line is inhibited when the clock enable signal is "high". A "high" reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally "low" and go "high" only at their respective decimal time slot. Each

## COS/MOS Decade Counter/Divider

### Plus 10 Decoded Decimal Outputs

#### *Special Features*

- Medium speed operation . . . . . 5 MHz (typ.) at  $V_{DD} - V_{SS} = 10$  V
- Fully static operation
- MSI complexity on a single chip . . . . . decade counter plus 10 decoded outputs

#### *Applications*

- Decade counter/decimal decode display applications
- Frequency division
- Counter control/timers
- Divide by N counting  
 $N = 2 - 10$  with one CD4017A and one CD4001A  
 $N > 10$  with multiple CD4017A's
- For further application information, see ST4166  
"COS/MOS MSI Counter and Register Design & Applications"

decoded output remains "high" for one full clock cycle. A carry-out ( $C_{OUT}$ ) signal completes one cycle every 10 clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

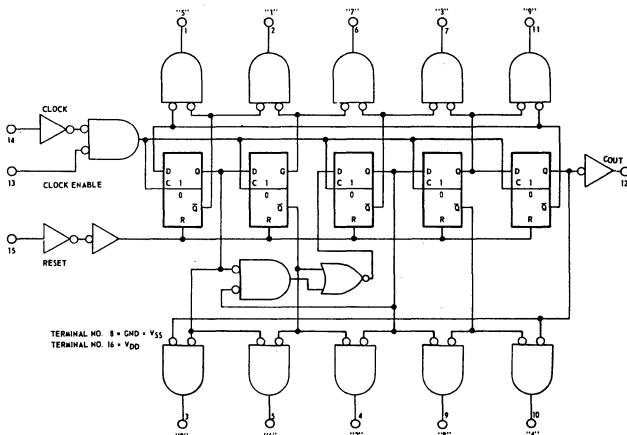


Fig.12.1 – Logic diagram.

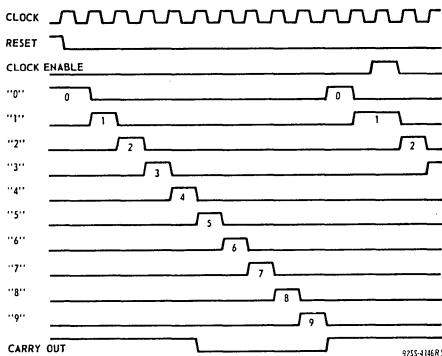
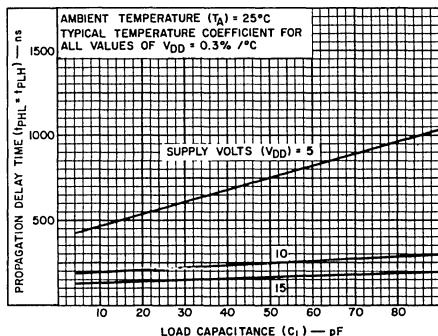
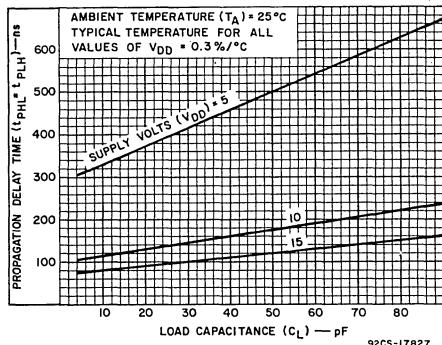
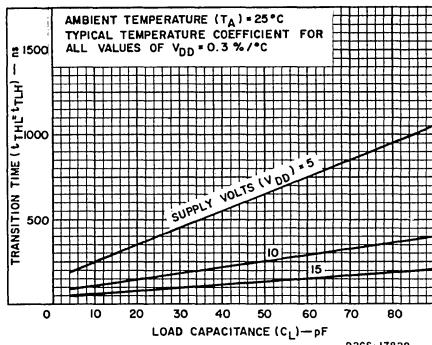
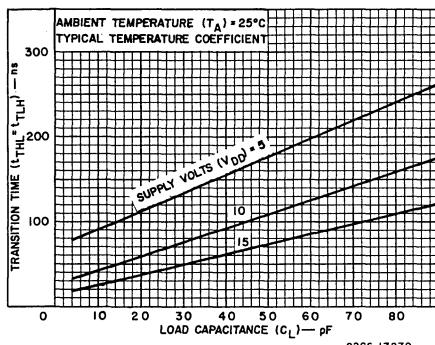
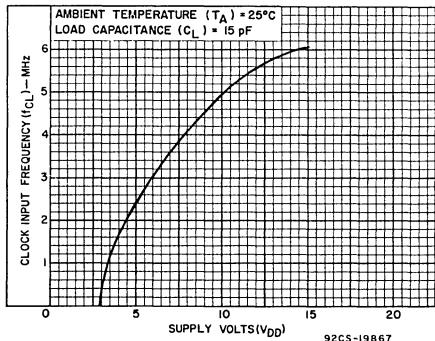


Fig.12.2 – Timing diagram.

Fig.12.3 – Typ. propagation delay time vs.  $C_L$  for decoded outputs.Fig.12.4 – Typ. propagation delay time vs.  $C_L$  for carry output.Fig.12.5 – Typ. transition time vs.  $C_L$  for decoded outputs.Fig.12.6 – Typ. transition time vs.  $C_L$  for carry output.Fig.12.7 – Typ. clock frequency vs.  $V_{DD}$ .

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4017AD, CD4017AK, CD4017AF													
			-55°C			25°C			125°C							
		$V_O$ Volts	$V_{DD}$ Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	$I_L$			5	—	—	5	—	0.3	5	—	—	300	$\mu A$ 12.9		
				10	—	—	10	—	0.5	10	—	—	600			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	25	—	1.5	25	—	—	1500	$\mu W$ —		
				10	—	—	100	—	5	100	—	—	6000			
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	$V$ —		
				10	—	—	0.01	—	0	0.01	—	—	0.05			
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	$V$ —		
				10	9.99	—	—	9.99	10	—	9.95	—	—			
Noise Immunity (Any Input)	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	$V$		
For Definition, See Appendix				1.0	10	3	—	—	3	4.5	—	2.9	—			
	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	$V$ 12.10		
				9.0	10	2.9	—	—	3	4.5	—	3	—			
Output Drive Current:																
N-Channel	$I_{DN}$	Decoded Outputs	0.5	5	0.06	—	—	0.05	0.1	—	0.035	—	—	$mA$		
			0.5	10	0.12	—	—	0.1	0.4	—	0.07	—	—			
		Carry Output	0.5	5	0.185	—	—	0.15	0.4	—	0.105	—	—			
			0.5	10	0.45	—	—	0.35	1	—	0.25	—	—			
P-Channel	$I_{DP}$	Decoded Outputs	4.5	5	-0.0375	—	—	-0.03	-0.075	—	-0.021	—	—	$mA$		
			9.5	10	-0.12	—	—	-0.1	-0.2	—	-0.07	—	—			
		Carry Output	4.5	5	-0.185	—	—	-0.15	-0.4	—	-0.105	—	—			
			9.5	10	-0.45	—	—	-0.35	-1	—	-0.25	—	—			
Input Current	$I_I$			—	—	—	—	—	10	—	—	—	—	$pA$ —		

\* See Appendix.

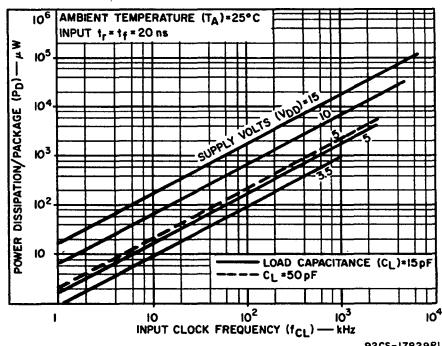


Fig. 12.8—Typ. dissipation characteristics.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4017AE											
		$V_o$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C					
Quiescent Device Current	$I_L$			5	—	—	50	—	0.5	50	—	—	700	$\mu A$	12.9
				10	—	—	100	—	1	100	—	—	1400		
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	2.5	250	—	—	3500	$\mu W$	—
				10	—	—	1000	—	10	1000	—	—	14,000		
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	12.10
			1.0	10	3	—	—	3	4.5	—	2.9	—	—		
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	—
			9.0	10	2.9	—	—	3	4.5	—	3	—	—		
Output Drive Current: N-Channel	$I_{DN}$	Decoded Outputs	0.5	5	0.03	—	—	0.025	0.1	—	0.02	—	—	mA	◆
		Carry Output	0.5	10	0.085	—	—	0.07	0.4	—	0.055	—	—		
		Decoded Outputs	4.5	5	-0.018	—	—	-0.015	-0.075	—	-0.012	—	—		
		Carry Output	9.5	10	-0.085	—	—	-0.07	-0.2	—	-0.055	—	—		
P-Channel	$I_{DP}$	Decoded Outputs	4.5	5	-0.095	—	—	-0.08	-0.4	—	-0.065	—	—	mA	◆
		Carry Output	9.5	10	-0.3	—	—	-0.24	-1	—	-0.20	—	—		
Input Current	$I_I$					—	—	—	10	—	—	—	—	pA	—

◆ See Appendix.

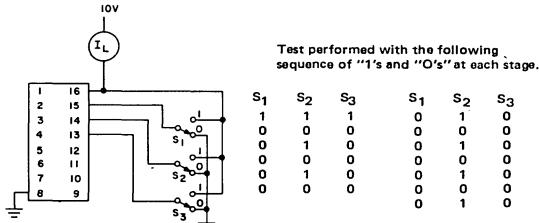


Fig. 12.9—Quiescent device current test circuit.

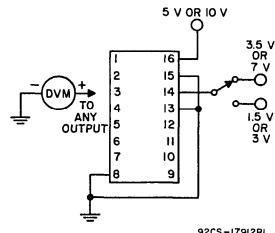


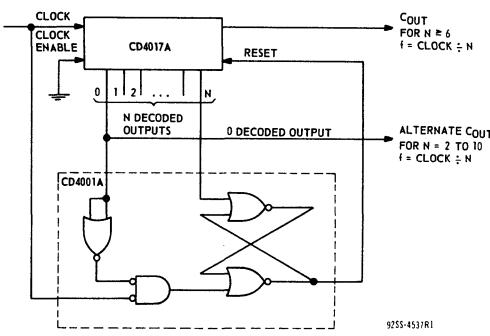
Fig. 12.10—Noise immunity test circuit.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns except  $t_{\text{fCL}}$ ,  $t_{\text{rCL}}$

Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4017AD CD4017AK CD4017AF			CD4017AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>CLOCKED OPERATION</b>											
Propagation Delay Time: Carry Out Line	$t_{\text{PHL}} =$ $t_{\text{PLH}}$	$t_{\text{PHL}}$	5	—	350	1000	—	350	1300	ns	12.4
			10	—	125	250	—	125	300	ns	—
		$t_{\text{PLH}}$	5	—	500	1200	—	500	1600	ns	12.3
			10	—	200	400	—	200	500	ns	—
Transition Time: Carry Out Line	$t_{\text{THL}} =$ $t_{\text{TLH}}$	$t_{\text{THL}}$	5	—	100	300	—	100	350	ns	12.6
			10	—	50	150	—	50	200	ns	—
		$t_{\text{TLH}}$	5	—	300	900	—	300	1200	ns	12.5
			10	—	125	350	—	125	450	ns	—
Minimum Clock Pulse Width	$t_{\text{WL}} =$ $t_{\text{WH}}$		5	—	200	500	—	200	830	ns	—
			10	—	100	170	—	100	250	ns	—
Clock Rise & Fall Time	$t_{\text{rCL}} =$ $t_{\text{fCL}}$		5	—	—	15	—	—	15	μs	—
			10	—	—	15	—	—	15	μs	—
Clock Enable Set-Up Time			5	—	175	500	—	175	700	ns	—
			10	—	75	200	—	75	300	ns	—
Maximum Clock Frequency	$f_{\text{CL}}^*$		5	1	2.5	—	0.6	2.5	—	MHz	—
			10	3	5	—	2	5	—	MHz	—
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—
<b>RESET OPERATION</b>											—
Propagation Delay Time: To Carry Out Line	$t_{\text{PHL(R)}}$	$t_{\text{PHL(R)}}$	5	—	350	1000	—	350	1300	ns	—
			10	—	125	250	—	125	300	ns	—
		$t_{\text{WH(R)}}$	5	—	450	1200	—	450	1600	ns	—
			10	—	200	400	—	200	500	ns	—
Reset Pulse Width	$t_{\text{WH(R)}}$		5	—	200	500	—	200	830	ns	—
			10	—	100	165	—	100	250	ns	—
Reset Removal Time			5	—	300	750	—	300	1000	ns	—
			10	—	100	225	—	100	275	ns	—

\* Measured with respect to carry output line

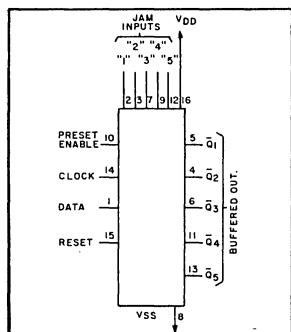


When the  $N^{\text{th}}$  decoded output is reached ( $N^{\text{th}}$  clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001A) generates a reset pulse which clears the CD4017A to its zero count. At this time, if the  $N^{\text{th}}$  decoded output is greater than or equal to 6, the  $\text{Q}_{\text{OUT}}$  line goes "high" to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of the clock "low" and decoded "0" output "low" resets the S-R flip flop to enable the CD4017A. If the  $N^{\text{th}}$  decoded output is less than 6, the  $\text{Q}_{\text{OUT}}$  line will not go "high" and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next count.

Fig. 12.11—Divide by  $N$  counter ( $N \leq 10$ ) with  $N$  decoded outputs.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4018AD, CD4018AF****CD4018AE, CD4018AK****COS/MOS****Presettable Divide-By-'N' Counter***Special Features*

- Medium speed operation. . . . . 5 MHz (typ.) at  $V_{DD} - V_{SS} = 10$  V
- Fully static operation
- MSI complexity on a single chip

*Applications*

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-'N' counters/frequency synthesizers
- Frequency division
- Counter control/timers

CD4018A types consist of 5 Johnson-Counter stages, buffered  $\bar{Q}$  outputs from each stage, and counter preset control gating. "Clock", "Reset", "Data", "Preset Enable", and 5 individual "Jam" inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the  $\bar{Q}_5$ ,  $\bar{Q}_4$ ,  $\bar{Q}_3$ ,  $\bar{Q}_2$ ,  $\bar{Q}_1$  signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package

to properly gate the feedback connection to the Data input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A "high" Reset signal clears the counter to an "all-zero" condition. A "high" Preset-Enable signal allows information on the Jam inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

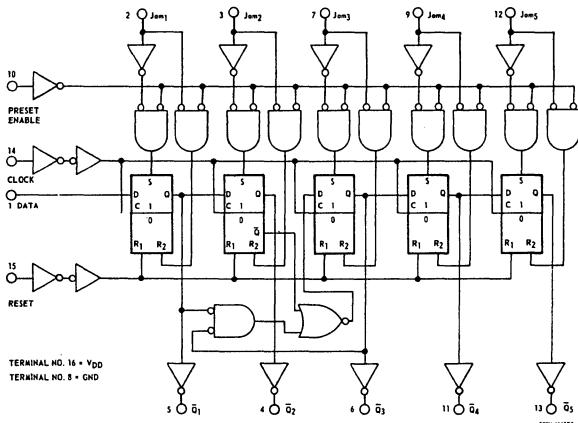


Fig.13.1 – Logic diagram.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS										CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
				CD4018AD, CD4018AK, CD4018AF													
		$V_o$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C							
Quiescent Device Current	$I_L$			5	—	—	5	—	0.3	5	—	—	300	$\mu A$	13.9		
				10	—	—	10	—	0.5	10	—	—	600				
Quiescent Device Dissipation/Package	$P_D$	5	10	—	—	25	—	1.5	25	—	—	1500	$\mu W$	—			
				—	—	100	—	5	100	—	—	6000					
Output Voltage: Low-Level	$V_{OL}$	5	10	—	—	0.01	—	0	0.01	—	—	0.05	V	—			
				—	—	0.01	—	0	0.01	—	—	0.05					
High-Level	$V_{OH}$	5	10	4.99	—	—	4.99	5	—	4.95	—	—	V	—			
				9.99	—	—	9.99	10	—	9.95	—	—					
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	13.10			
			1.0	10	3	—	—	3	4.5	—	2.9	—	—				
	$V_{NH}$	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	—			
			9.0	10	2.9	—	—	3	4.5	—	3	—	—				
Output Drive Current: N-Channel	$I_D^N$	$\bar{Q}_5$	0.5	5	0.18	—	—	0.15	0.4	—	0.105	—	—	mA	◆		
			0.5	10	0.45	—	—	0.35	1	—	0.25	—	—				
P-Channel		$\bar{Q}_1, \bar{Q}_2,$	0.5	5	0.06	—	—	0.05	0.1	—	0.035	—	—				
			0.5	10	0.25	—	—	0.2	0.4	—	0.14	—	—				
		$\bar{Q}_5$	4.5	5	-0.185	—	—	0.15	-0.4	—	0.105	—	—		mA		
			9.5	10	-0.45	—	—	-0.35	-1	—	-0.25	—	—				
Input Current	$I_I$												pA	—			

♦ See Appendix.

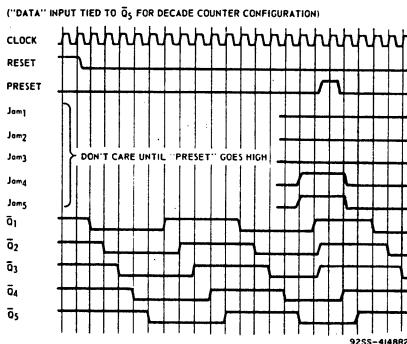


Fig. 13.2 – Timing diagram.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs  $V_{I1} \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_o$ Volts	$V_{DD}$ Volts	LIMITS												CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
				CD4018AE															
				-40°C			25°C			85°C									
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	$I_L$			5	—	—	50	—	0.5	50	—	—	700	—	—	$\mu A$	13.9		
				10	—	—	100	—	1	100	—	—	1400	—	—				
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	2.5	250	—	—	3500	—	—	$\mu W$	—		
				10	—	—	1000	—	10	1000	—	—	14000	—	—				
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	—	—	V	—		
				10	—	—	0.01	—	0	0.01	—	—	0.05	—	—				
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	V	—		
				10	9.99	—	—	9.99	10	—	9.95	—	—	—	—				
Noise Immunity (Any Input) For Definition, See Appendix	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—	V	13.10		
				1.0	10	3	—	—	3	4.5	—	2.9	—	—	—				
	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—	V	—		
				9.0	10	2.9	—	—	3	4.5	—	3	—	—	—				
Output Drive Current: N-Channel	$I_{DN}$			$\bar{Q}_5$	0.5	5	0.095	—	—	0.08	0.4	—	0.065	—	—	mA	◆		
				$\bar{Q}_5$	0.5	10	0.3	—	—	0.25	1	—	0.2	—	—				
	$I_{DP}$			$\bar{Q}_1, \bar{Q}_2$	0.5	5	0.03	—	—	0.025	0.1	—	0.02	—	—	mA	◆		
				$\bar{Q}_3, \bar{Q}_4$	0.5	10	0.18	—	—	0.15	0.4	—	0.12	—	—				
Input Current	$I_I$			$\bar{Q}_5$	4.5	5	-0.095	—	—	-0.08	-0.4	—	-0.065	—	—	pA	—		
				$\bar{Q}_5$	9.5	10	-0.3	—	—	-0.25	-1	—	-0.2	—	—				

♦See Appendix

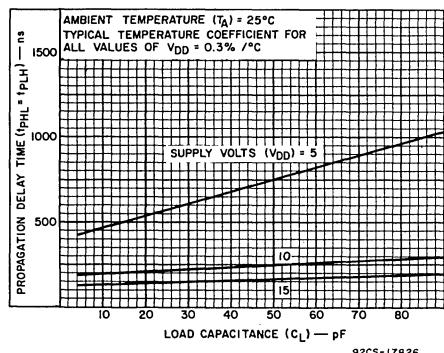


Fig.13.3—Typ. propagation delay time vs.  $C_L$  for decoded outputs.

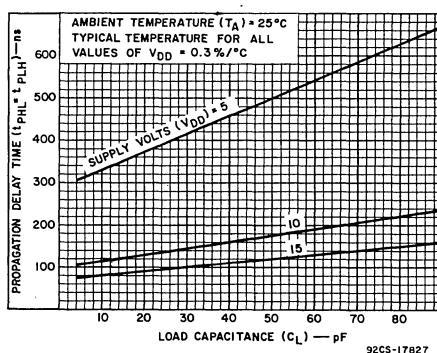


Fig.13.4—Typ. propagation delay time vs.  $C_L$  for  $\bar{Q}_5$  output.

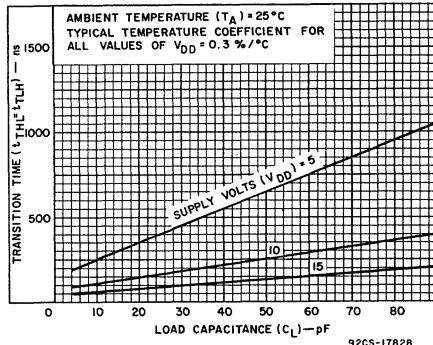


Fig. 13.5—Typ. transition time vs.  $C_L$  for decoded outputs.

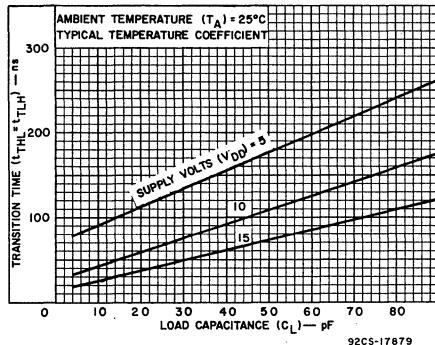


Fig. 13.6—Typ. transition time vs.  $C_L$  for  $\bar{Q}_5$  output.

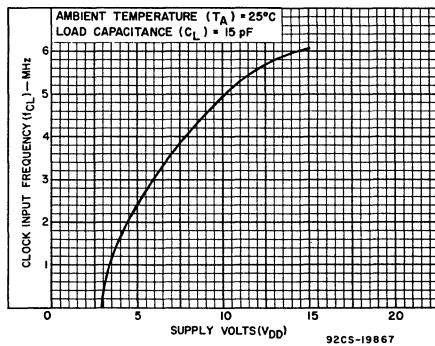


Fig. 13.7—Typical clock frequency vs.  $V_{DD}$ .

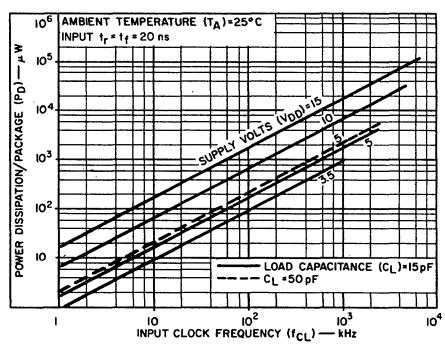


Fig. 13.8—Typ. dissipation characteristics

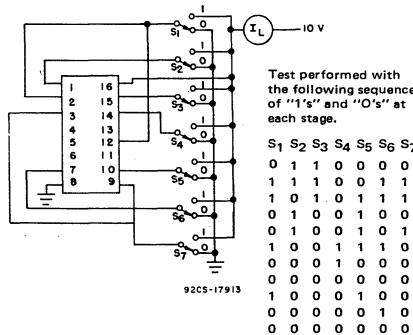


Fig. 13.9—Quiescent device current test circuit.

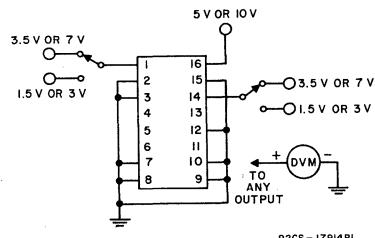


Fig. 13.10—Noise immunity test circuit.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns except  $t_{rCL}, t_{fCL}$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$  (See Appendix for Waveforms)

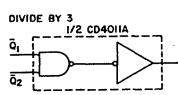
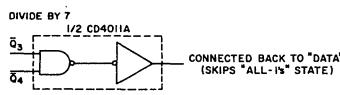
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4018AD CD4018AK CD4018AF			CD4018AE						
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.			
<b>CLOCKED OPERATION</b>												
Propagation Delay Time: To $\bar{Q}_5$ Output	$t_{PHL} =$ $t_{PLH}$		5	—	350	1000	—	350	1300	ns	13.4	
			10	—	125	250	—	125	300			
Transition Time: To $\bar{Q}_5$ Output	$t_{THL} =$ $t_{TLH}$		5	—	500	1200	—	500	1600	ns	13.3	
			10	—	200	400	—	200	500			
To Other Outputs			5	—	300	900	—	300	1200	ns	13.5	
			10	—	125	350	—	125	450			
Minimum Clock Pulse Width	$t_{WL} =$ $t_{WH}$		5	—	200	500	—	200	830	ns	—	
			10	—	100	170	—	100	250			
Clock Rise & Fall Time	$t_{rCL} =$ $t_{fCL}$		5	—	—	15	—	—	15	$\mu\text{s}$	—	
			10	—	—	15	—	—	15			
Data Input Set-Up Time			5	—	175	500	—	175	700	ns	—	
			10	—	75	200	—	75	300			
Maximum Clock Frequency	$f_{CL}$		5	1	2.5	—	0.6	2.5	—	MHz	—	
			10	3	5	—	2	5	—			
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—	
<b>PRESET* OR RESET OPERATION</b>											—	
Propagation Delay Time: To $\bar{Q}_5$ Output	$t_{PLH(R)} =$ $t_{PHL(PR)}$		5	—	350	1000	—	350	1300	ns	—	
			10	—	125	250	—	125	300			
To Other Outputs	$t_{PLH(PR)} =$ $t_{PHL(PR)}$		5	—	500	1200	—	500	1600	ns	—	
			10	—	200	400	—	200	500			
Preset or Reset Pulse Width	$t_{WH(R)} =$ $t_{WH(PR)}$		5	—	200	500	—	200	830	ns	—	
			10	—	100	165	—	100	250			
Preset or Reset Removal Time			5	—	300	750	—	300	1000	ns	—	
			10	—	100	225	—	100	275			

\* At Preset Enable or Jam Inputs.

#### EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

DIVIDE BY 10       $\bar{Q}_5$   
 DIVIDE BY 8       $\bar{Q}_4$  CONNECTED BACK TO "DATA"  
 DIVIDE BY 6       $\bar{Q}_3$  "DATA"  
 DIVIDE BY 4       $\bar{Q}_2$

NO EXTERNAL COMPONENTS REQUIRED



#### DIVIDE BY 9

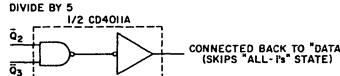
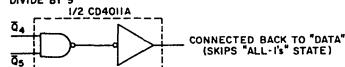
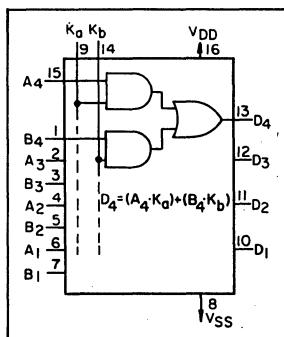


Fig.13.11 – External connections for divide by 10,9,8,7,6,5,4,3 operation.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4019AD, CD4019AF****CD4019AE, CD4019AK****COS/MOS Quad  
AND-OR Select Gate***Special Features*

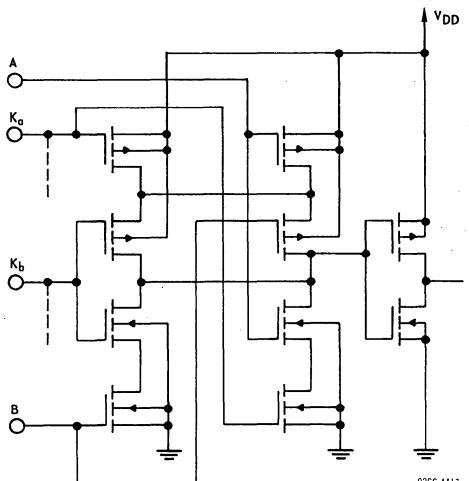
- Medium-speed operation.....  $t_{PHL} = t_{PLH} = 50 \text{ ns (typ.)}$  at  $C_L = 15 \text{ pF}$

*Applications*

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection

CD4019A types are comprised of four "AND-OR Select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K<sub>a</sub> and K<sub>b</sub>. In addition to

selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.



*Fig.14.1—Schematic diagram for 1 of 4 identical stages.*

## TYPICAL CD4019A APPLICATIONS

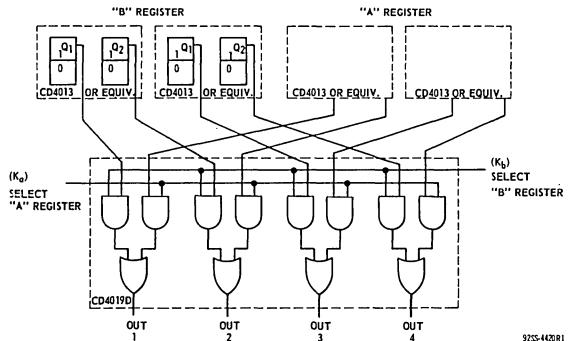


Fig. 14.2—AND/OR select gating.

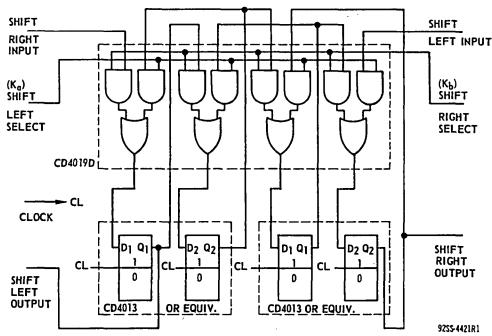


Fig. 14.3—"Shift left/shift right" register.

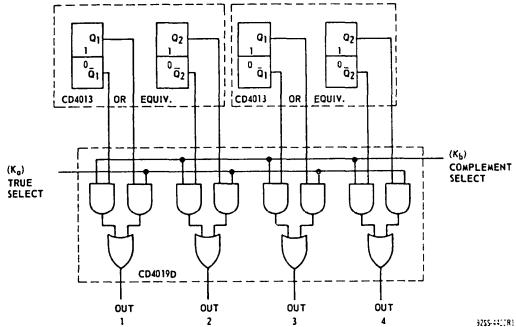


Fig. 14.4 — "True" complement selector.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4019AD, CD4019AK, CD4019AF										
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C				
Quiescent Device Current	I <sub>L</sub>			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
	5	—	—	5	—	0.03	5	—	—	300	—	μA	14.10	
Quiescent Device Dissipation/Package	P <sub>D</sub>	10	—	—	10	—	0.05	10	—	—	600	—	μW	—
		5	—	—	25	—	0.15	25	—	—	1500	—	—	—
Output Voltage: Low-Level	V <sub>OL</sub>	10	—	—	100	—	0.5	100	—	—	6000	—	V	—
		5	—	—	0.01	—	0	0.01	—	—	0.05	—	—	—
High-Level	V <sub>OH</sub>	10	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—
		10	9.99	—	—	9.99	10	—	9.95	—	—	—	—	—
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	V <sub>NL</sub>	0.95	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	14.11
	V <sub>NH</sub>	2.9	10	3	—	—	3	4.5	—	2.9	—	—	V	
Output Drive Current: N-Channel	I <sub>DN</sub>	3.6	5	1.4	—	—	1.5	2.25	—	1.5	—	—	mA	◆
	I <sub>DP</sub>	7.2	10	2.9	—	—	3	4.5	—	3	—	—	mA	
Input Current	I <sub>I</sub>	—	—	—	—	—	—	10	—	—	—	—	pA	—

◆ See Appendix.

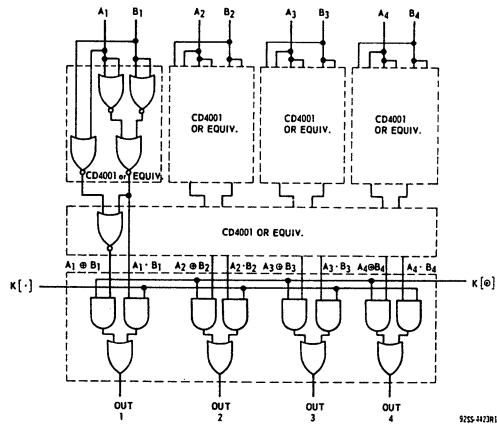


Fig.14.5 – AND/OR Exclusive-OR selector.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS										CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS
				CD4019AE											
		$V_o$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C					
Quiescent Device Current	$I_L$			5	—	—	50	—	0.1	50	—	—	700	$\mu A$	14, 10
	10	—	—	—	100	—	0.2	100	—	—	1400				
Quiescent Device Dissipation/Package	$P_D$	5	—	—	250	—	0.5	250	—	—	3500	—	$\mu W$	—	
		10	—	—	1000	—	2	1000	—	—	14000	—			
Output Voltage: Low-Level	$V_{OL}$	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—	
		10	—	—	0.01	—	0	0.01	—	—	0.05	—			
High-Level	$V_{OH}$	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—	
		10	9.99	—	—	9.99	10	—	9.95	—	—	—			
Noise Immunity (Any Input) For Definition, See Appendix	$V_{NL}$	0.95	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	14, 11	
		2.9	10	3	—	—	3	4.5	—	2.9	—	—			
	$V_{NH}$	3.6	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	—	
		7.2	10	2.9	—	—	3	4.5	—	3	—	—			
Output Drive Current: N-Channel	$I_{DN}$	0.5	5	0.37	—	—	0.30	1.0	—	0.23	—	—	mA	◆	
		0.5	10	0.8	—	—	0.65	1.5	—	0.5	—	—			
P-Channel	$I_{DP}$	4.5	5	-0.145	—	—	-0.12	-0.5	—	-0.095	—	—	mA	—	
		9.5	10	-0.6	—	—	-0.5	-1.5	—	-0.4	—	—			
Input Current	$I_I$	—	—	—	—	—	10	—	—	—	—	—	pA	—	

\*See Appendix.

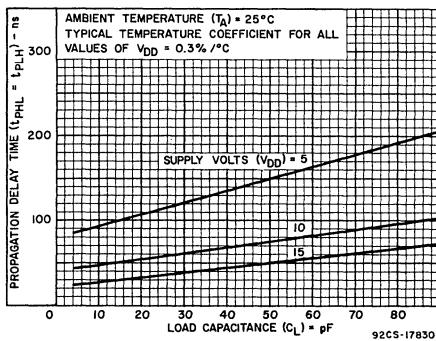


Fig. 14.6—Typ. propagation delay time vs.  $C_L$ .

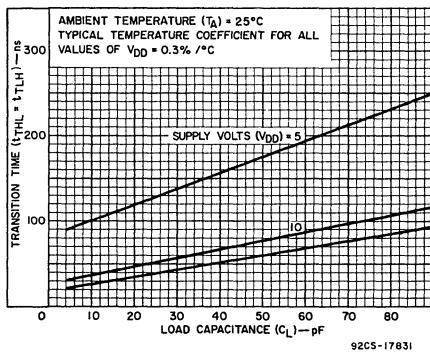


Fig. 14.7—Typ. transition time vs.  $C_L$ .

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \mu\text{F}$ , and input rise and fall times = 20 ns  
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$  (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4019AD, CD4019AK, CD4019AF			CD4019AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time:	$t_{PHL}$ , $t_{PLH}$		5	—	100	225	—	100	300	ns	14.6
			10	—	50	100	—	50	125		
Transition Time	$t_{THL}$ , $t_{TLH}$		5	—	100	200	—	100	275	ns	14.7
			10	—	40	65	—	40	80		
Input Capacitance	$C_I$	All A and B Inputs	—	5	—	—	5	—	—	$\mu\text{F}$	—
		$K_A$ and $K_B$ Inputs	—	12	—	—	12	—	—		

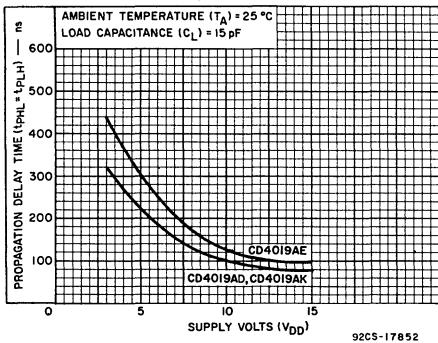
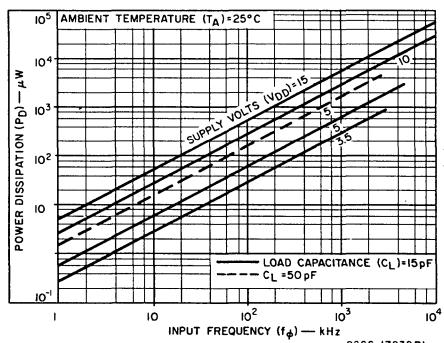
Fig.14.8—Max. propagation delay time vs  $V_{DD}$ .

Fig.14.9—Typ. dissipation characteristics per output.

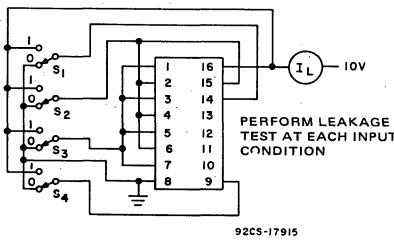


Fig.14.10—Quiescent device current test circuit.

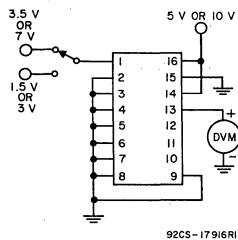
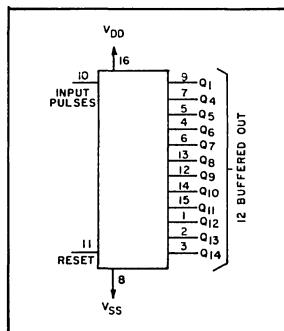


Fig.14.11—Noise immunity test circuit.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4020AD, CD4020AF  
CD4020AE, CD4020AK**

## **COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider**

### *Special Features*

- Medium speed operation. .... 7 MHz (typ.) at  $V_{DD} - V_{SS} = 10$  V
- Low "high"- and "low"-level output impedance. ....  $1000\Omega$  (typ.) at  $V_{DD} - V_{SS} = 10$  V
- MSI complexity on a single chip. .... 14 fully static, master-slave stages
- COS/MOS gate-input loading at both Reset and Input-pulse lines

CD4020A types consist of a pulse input shaping circuit, reset line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1, and 4 through 14. The counter is reset to its "all zeroes" state by a high level on the reset inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each input pulse.

### *Applications*

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- Counting functions

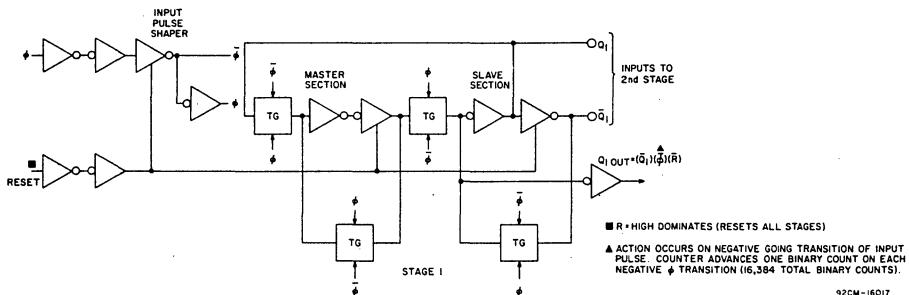


Fig. 15.1 — Logic diagram for 1 of 14 binary stages.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_O$ Volts	$V_{DD}$ Volts	LIMITS												CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
				CD4020AD, CD4020AK, CD4020AF															
				-55°C			25°C			125°C									
Quiescent Device Current	$I_L$			5	—	—	15	—	0.5	15	—	—	900	—	—	$\mu A$	15.11		
				10	—	—	25	—	1	25	—	—	1500	—	—				
Quiescent Device Dissipation Package	$P_D$			5	—	—	75	—	2.5	75	—	—	4500	—	—	$\mu W$	15.10		
				10	—	—	250	—	10	250	—	—	15000	—	—				
Output Voltage Low Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	—	—	V	—		
				10	—	—	0.01	—	0	0.01	—	—	0.05	—	—				
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	V	—		
				10	9.99	—	—	9.99	10	—	9.95	—	—	—	—				
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—	V	15.12		
				1.0	10	3.0	—	—	3	4.5	—	2.9	—	—	—				
	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—	V	15.13		
				9.0	10	2.9	—	—	3	4.5	—	3.0	—	—	—				
Output Drive Current: N Channel	$I_{DN}$			0.5	5	0.09	—	—	0.075	0.2	—	0.05	—	—	—	mA	◆		
				0.5	10	0.185	—	—	0.15	0.4	—	0.105	—	—	—				
P Channel	$I_{DP}$			4.5	5	-0.11	—	—	-0.09	-0.25	—	-0.065	—	—	—	mA	◆		
				9.5	10	-0.25	—	—	-0.20	-0.5	—	-0.14	—	—	—				
Input Current	$I_I$			—	—	—	—	—	10	—	—	—	—	—	—	pA	—		

◆ See Appendix.

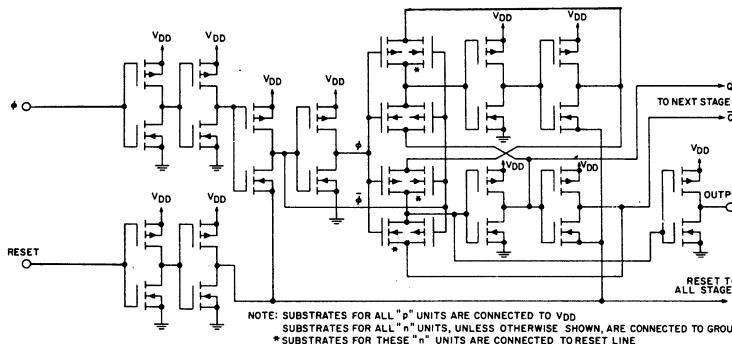


Fig. 15.2 – Schematic diagram of pulse shapers and 1 of 14 binary stages.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.
				CD4020AE										
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C				
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
	5				50		1	50			700	$\mu A$	15.11	
		10				100		2	100			1400		
Quiescent Device Dissipation Package	$P_D$	5				250		5	250			3500	$\mu W$	15.10
		10				1000		20	1000			14000		
Output Voltage Low Level	$V_{OL}$	5				0.01		0	0.01			0.05	V	—
		10				0.01		0	0.01			0.05		
High-Level	$V_{OH}$	5	4.99				4.99	5		4.95		—	V	—
		10	9.99				9.99	10		9.95		—	V	—
Noise Immunity (Any Input)	$V_{NL}$	0.8	5	1.5			1.5	2.25		1.4		—	V	15.12
		1.0	10	3.0			3	4.5		2.9		—	V	15.13
	$V_{NH}$	4.2	5	1.4			1.5	2.25		1.5		—	V	—
		9.0	10	2.9			3	4.5		3.0		—	V	—
Output Drive Current N-Channel	$I_{DN}$	0.5	5	0.09			0.08	0.33		0.065		—	mA	◆
		0.5	10	0.16			0.10	0.5		0.10		—	mA	—
P-Channel	$I_{DP}$	4.5	5	-0.09			-0.06	-0.25		-0.05		—	mA	—
		9.5	10	-0.18			-0.15	-0.5		-0.12		—	mA	—
Input Current	$I_I$							10					$pA$	—

♦ See Appendix.

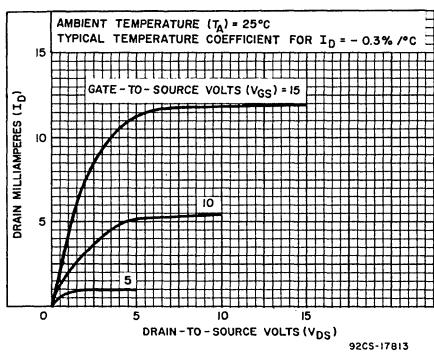


Fig.15.3—Typ. n-channel drain characteristics.

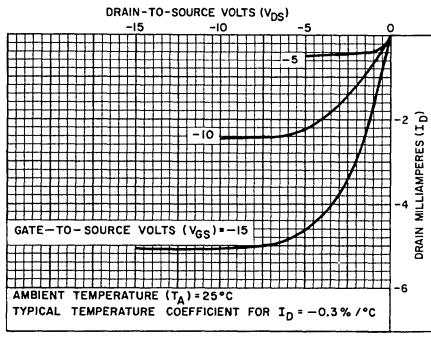


Fig.15.4—Typ. p-channel drain characteristics.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns except  $t_{\text{fCL}}$ ,  $t_{\text{fCL}}$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4020AD CD4020AK CD4020AF			CD4020AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>CLOCKED OPERATION</b>											
Propagation Delay Time:	$t_{\text{PHL}} = t_{\text{PLH}}$		5	—	450	600	—	450	650	ns	15.7
			10	—	150	225	—	150	250		
Transition Time	$t_{\text{TTL}} = t_{\text{TLH}}$		5	—	450	600	—	450	650	ns	15.8
			10	—	200	300	—	200	350		
Minimum Clock Pulse Width	$t_{\text{WL}} = t_{\text{WH}}$		5	—	200	335	—	200	500	ns	—
			10	—	70	125	—	70	165		
Clock Rise & Fall Time	$t_{\text{fCL}} = t_{\text{fCL}}$		5	—	—	15	—	—	15	$\mu\text{s}$	—
			10	—	—	15	—	—	15		
Maximum Clock Frequency	$f_{\text{CL}}$		5	1.5	2.5	—	1	2.5	—	MHz	15.9
			10	4	7	—	3	7	—		
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—
<b>RESET OPERATION</b>											—
Propagation Delay Time:	$t_{\text{PHL(R)}}$		5	—	2000	3000	—	2000	3500	ns	15.7
			10	—	500	775	—	500	900		
Minimum Reset Pulse Width	$t_{\text{WH(R)}}$		5	—	1800	2500	—	1800	3000	ns	—
			10	—	300	475	—	300	550		

\*Propagation Delay is from clock input to  $Q_1$  output.

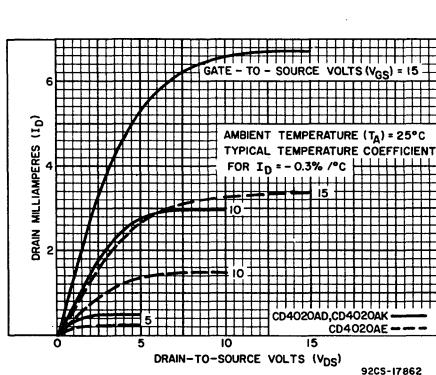


Fig. 15.5—Min. n-channel drain characteristics.

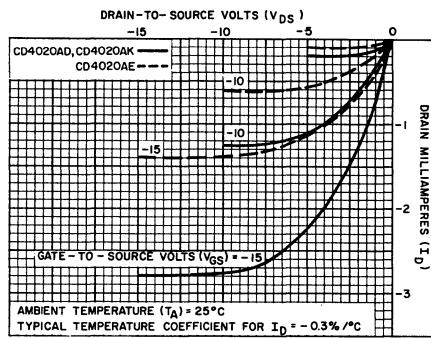


Fig. 15.6—Min. p-channel drain characteristics.

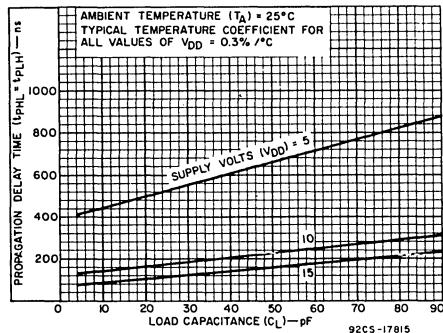
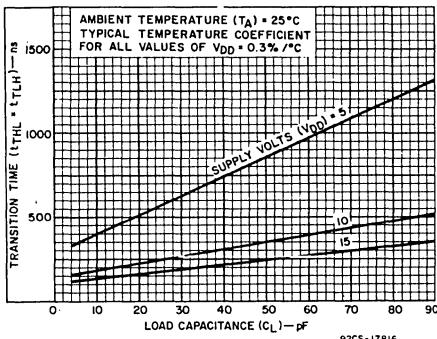
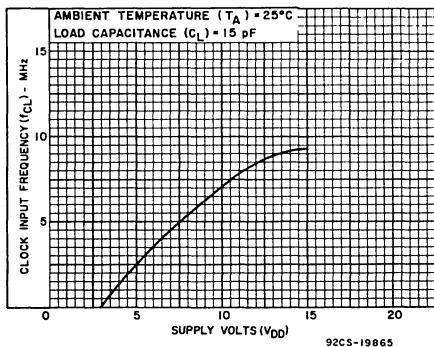
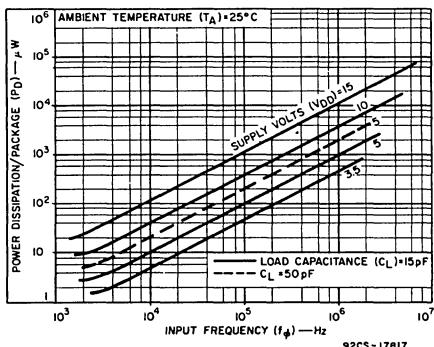
Fig. 15.7—Typ. propagation delay time vs.  $C_L$ .Fig. 15.8—Typ. transition time vs.  $C_L$ .Fig. 15.9—Typ. clock frequency vs.  $V_{DD}$ .

Fig. 15.10—Typ. dissipation characteristics.

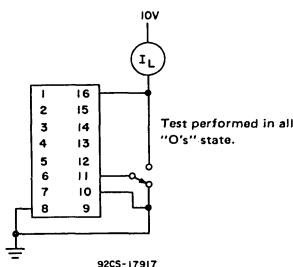


Fig. 15.11—Quiescent device dissipation test.

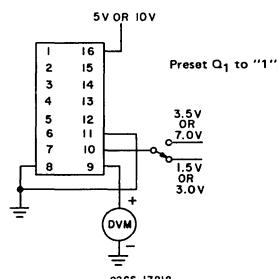


Fig. 15.12—Noise immunity test circuit.

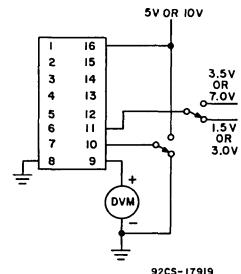
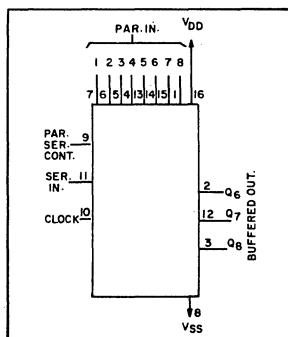


Fig. 15.13—Reset noise immunity test circuit.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4021AD, CD4021AF  
CD4021AE, CD4021AK**


## COS/MOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output,  
Synchronous Serial Input/Serial Output

### Special Features

- Asynchronous parallel or synchronous serial operation under control of parallel/serial control-input
- Individual "jam" inputs to each register stage
- Master-slave flip-flop register stages
- Fully static operation..... DC to 5 MHz

CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common Clock and Parallel/Serial Control inputs, a single Serial Data input, and individual parallel "Jam" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. "Q" outputs are available from the sixth, seventh, and eighth stages.

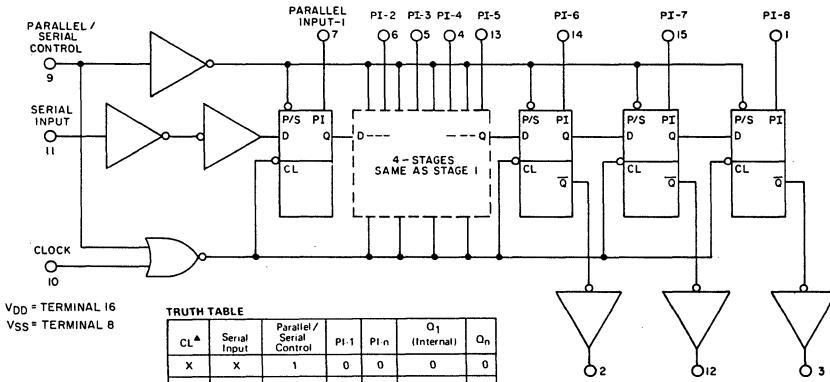
When the parallel/Serial Control input is "low", data is serially shifted into the 8-stage register synchronously with the positive-going transition of the Clock pulse.

### Applications

- Asynchronous parallel input/serial output data queueing
- Parallel to serial data conversion ■ General purpose register

When the Parallel/Serial Control input is "high", data is jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

Register expansion is possible using additional CD4021A packages.



V<sub>DD</sub> = TERMINAL 16  
V<sub>SS</sub> = TERMINAL 8

### TRUTH TABLE

CL <sup>▲</sup>	Serial Input	Parallel / Serial Control	PI-1	PI-n	$Q_1$ (Internal)	$Q_n$
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
	0	0	X	X	0	$Q_{n-1}$
	1	0	X	X	1	$Q_n$
X	X	0	X	X	$Q_1$	$Q_n$

▲ = LEVEL CHANGE      X = DON'T CARE CASE

NO CHANGE

92CM - 1714IR1

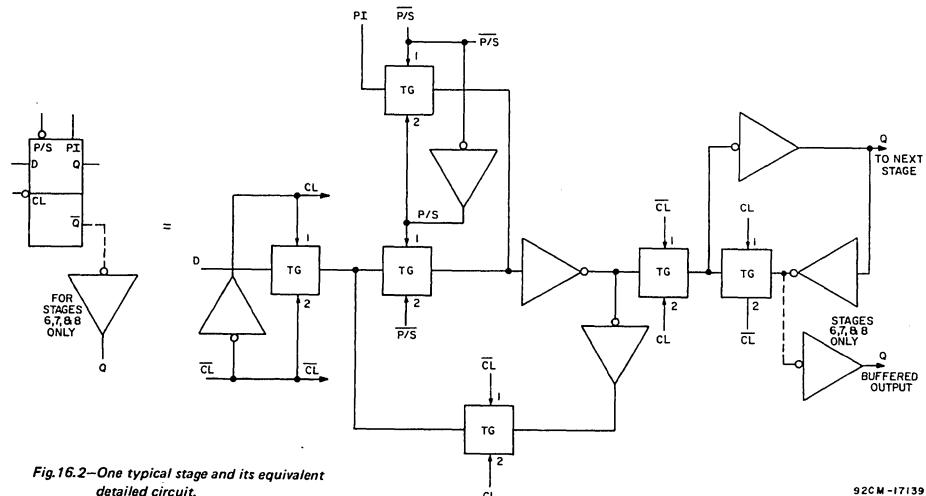


Fig. 16.2—One typical stage and its equivalent detailed circuit.

92CM-17139R1

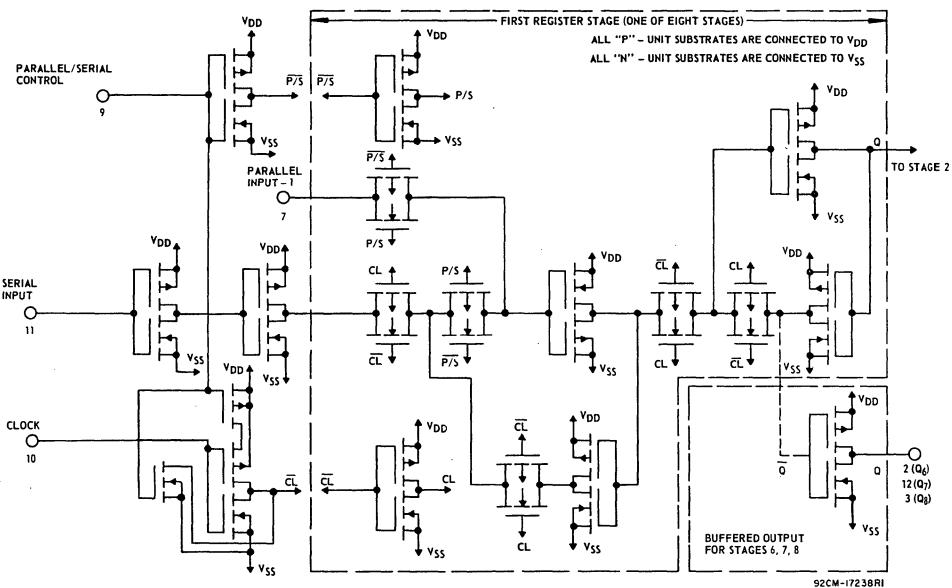


Fig. 16.3—Schematic diagram — CD4021A.

STATIC ELECTRICAL CHARACTERISTICS (All inputs  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS										CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
				CD4021AD, CD4021AK, CD4021AF													
				-55°C			25°C			125°C							
Quiescent Device Current	$I_L$			5	—	—	5	—	0.5	5	—	—	300	μA	16.8		
				10	—	—	10	—	1	10	—	—	600	μA			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	25	—	2.5	25	—	—	1500	μW	—		
				10	—	—	100	—	10	100	—	—	6000	μW			
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—		
				10	—	—	0.01	—	0	0.01	—	—	0.05	V			
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V	—		
				10	9.99	—	—	9.99	10	—	9.95	—	—	V			
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	16.9		
For Definition, See Appendix			1.0	10	3	—	—	3	4.5	—	2.9	—	—	V			
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V			
			9.0	10	2.9	—	—	3	4.5	—	3	—	—	V			
Output Drive Current: N-Channel	$I_{DN}$		0.5	5	0.15	—	—	0.12	0.3	—	0.085	—	—	mA	◆		
			0.5	10	0.31	—	—	0.25	0.5	—	0.175	—	—	mA			
P-Channel	$I_{DP}$		4.5	5	-0.1	—	—	-0.08	-0.16	—	-0.055	—	—	mA			
			9.5	10	-0.25	—	—	-0.20	-0.44	—	-0.14	—	—	mA			
Input Current	$I_I$		—	—	—	—	—	10	—	—	—	—	—	pA			

\*See Appendix.

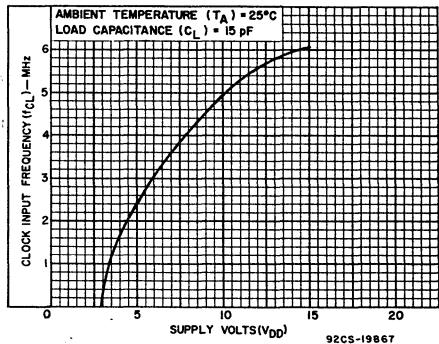


Fig. 16.4—Typ. clock frequency vs.  $V_{DD}$ .

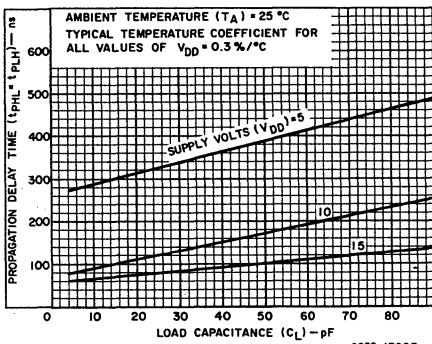


Fig. 16.5—Typ. propagation delay time vs.  $C_L$ .

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS	
				CD4021AE											
		$V_O$ Volts	$V_{DD}$ Volts	$-40^\circ C$			$25^\circ C$			$85^\circ C$					
Quiescent Device Current	$I_L$			5	—	—	50	—	0.5	50	—	—	700	$\mu A$	16.8
				10	—	—	100	—	1	100	—	—	1400		
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	2.5	250	—	—	3500	$\mu W$	—
				10	—	—	1000	—	10	1000	—	—	14000		
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (Any Input) <i>For Definition, See Appendix</i>	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	16.9
			1.0	10	3	—	—	3	4.5	—	2.9	—	—		
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	—
			9.0	10	2.9	—	—	3	4.5	—	3	—	—		
Output Drive Current: N-Channel	$I_{DN}$		0.5	5	0.072	—	—	0.06	0.3	—	0.05	—	—	mA	◆
			0.5	10	0.12	—	—	0.1	0.5	—	0.08	—	—		
P-Channel	$I_{DP}$		4.5	5	-0.06	—	—	-0.05	-0.16	—	-0.04	—	—	mA	◆
			9.5	10	-0.12	—	—	-0.1	-0.44	—	-0.08	—	—		
Input Current	$I_I$			—	—	—	—	—	10	—	—	—	—	pA	

\*See Appendix.

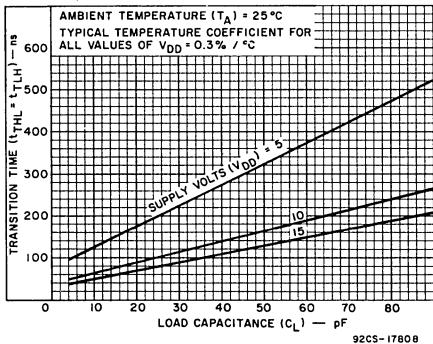


Fig. 16.6—Typ. transition time vs.  $C_L$ .

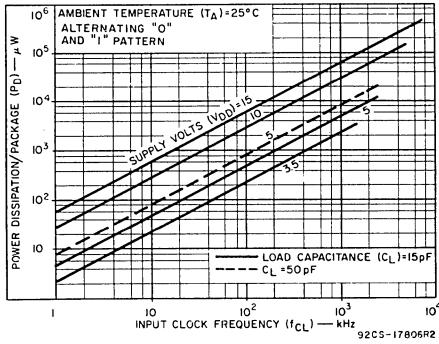


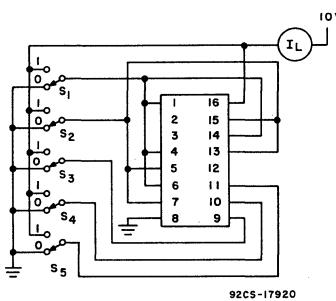
Fig. 16.7—Typ. dissipation characteristics.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$  and input rise and fall times = 20 ns except  $t_{fCL}$ ,  $t_{rCL}$   
 Typical Temperature Coefficient for all values of  $V_{DD}$  =  $0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			$V_{DD}$ (Volts)	CD4021AD CD4021AK CD4021AF			CD4021AE				
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time **	$t_{PHL} = t_{PLH}$		5	—	300	750	—	300	1000	ns	16.5
			10	—	100	225	—	100	300		
Transition Time	$t_{THL} = t_{TLH}$		5	—	150	300	—	150	400	ns	16.6
			10	—	75	125	—	75	150		
Minimum Clock Pulse Width	$t_{WL} = t_{WH}$		5	—	200	500	—	200	830	ns	—
			10	—	100	175	—	100	200		
Minimum High-Level Parallel/Serial Control Pulse Width	$t_{WH(P/S)}$		5	—	200	500	—	200	830	ns	—
			10	—	100	175	—	100	200		
Clock Rise & Fall Time	$*t_{rCL} = t_{fCL}$		5	—	—	15	—	—	15	$\mu\text{s}$	—
			10	—	—	15	—	—	15		
Set-Up Time			5	—	100	350	—	100	500	ns	—
			10	—	50	80	—	50	100		
Maximum Clock Frequency	$f_{CL}$		5	1	2.5	—	0.6	2.5	—	MHz	—
			10	3	5	—	2.5	5	—		
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—

\*\* From Clock or Parallel/Serial Control Input

- If more than one unit is cascaded in a parallel clocked operation,  $t_{fCL}$  should be made less than or equal to the sum of the fixed propagation delay time at 15pF and the transition time of the output driving stage for the estimated capacitive load.



Test performed with the following sequence of "One's" and "Zero's".

S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>
0	0	1	0	0
1	0	1	1	1
1	0	1	0	1
0	1	1	1	1
0	1	0	0	0

Fig. 16.8—Quiescent device current test circuit.

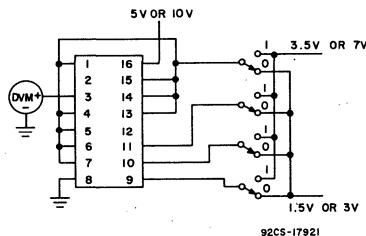
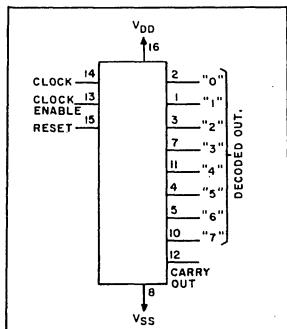


Fig. 16.9—Noise immunity test circuit.

**Digital Integrated Circuits**

Monolithic Silicon

**CD4022AD, CD4022AF****CD4022AE, CD4022AK**

## **COS/MOS Divide - By - 8 Counter/Divider with 8 Decoded Outputs**

### *Special Features*

- Medium speed operation . . . . . 5 MHz (typ.) at  $V_{DD} - V_{SS} = 10$  V
- MSI complexity on a single chip
- Divide by N counting;  $N = 2$  to 8 with one CD4022A plus one CD4001A, package

### *Applications*

- Binary counting/decoding
- Binary frequency division
- Binary counter control/timers

CD4022A types consist of a 4-stage divide-by-8 Johnson counter, associated decode output gating and a carry-out bit. The counter is cleared to its zero count by a "high" reset signal. The counter is advanced on the positive clock-signal transition provided the clock enable signal is "low".

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and

spike-free decoder outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decode gating outputs are normally "low" and go "high" only at their respective decoded time slot. Each decode gate output remains "high" for one full clock cycle. The carry-out signal completes one cycle every 8 clock-input cycles and is used as a ripple-carry signal to directly clock a succeeding counter package in a multi-package counting system.

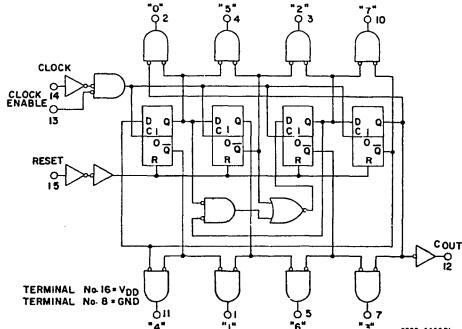


Fig. 17.1—Logic diagram.

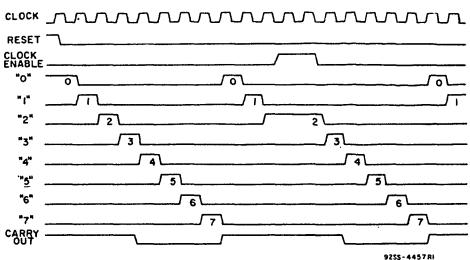


Fig. 17.2—Timing diagram.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_O$ Volts	$V_{DD}$ Volts	LIMITS								UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.				
				CD4022AD, CD4022AK, CD4022AF													
				-55°C			25°C			125°C							
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	$\mu A$	17.9			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	5	—	0.3	5	—	300	$\mu W$	—			
				10	—	—	10	—	0.5	10	—	600	$\mu W$	—			
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	0.05	V	—			
				10	—	—	0.01	—	0	0.01	—	0.05	V	—			
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	V	—			
				10	9.99	—	—	9.99	10	—	9.95	—	V	—			
Noise Immunity (Any Input) For Definition, See Appendix	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	V	17.10			
				1.0	10	3	—	—	3	4.5	—	2.9	—	V			
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	V				
				9.0	10	2.9	—	—	3	4.5	—	3	—	V			
Output Drive Current N-Channel	$I_{DN}$		Decoded Outputs	0.5	5	0.062	—	—	0.05	0.15	—	0.035	—	mA	◆		
				0.5	10	0.12	—	—	0.1	0.3	—	0.07	—	mA			
P-Channel			Carry Output	0.5	5	0.185	—	—	0.15	0.5	—	0.105	—	mA			
				0.5	10	0.375	—	—	0.3	1	—	0.21	—	mA			
$I_{DP}$			Decoded Outputs	4.5	5	-0.038	—	—	-0.03	-0.075	—	-0.021	—	ns	◆		
				9.5	10	-0.12	—	—	-0.11	-0.15	—	-0.07	—	ns			
Input Current	$I_I$			Carry Output	4.5	5	-0.185	—	—	-0.15	-0.4	—	-0.105	—	ns	◆	
					9.5	10	-0.375	—	—	-0.3	-0.8	—	-0.21	—	ns		

◆ See Appendix.

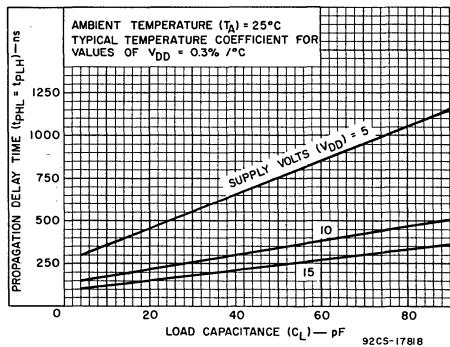


Fig.17.3—Typ. propagation delay time vs.  $C_L$  for decoded outputs.

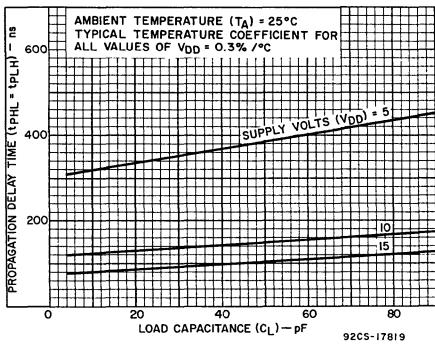


Fig.17.4—Typ. propagation delay time vs.  $C_L$  for carry output.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4022AE										
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C				
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
	5	—	—	50	—	0.5	50	—	—	700	—	$\mu A$	17.9	
Quiescent Device Dissipation/Package	$P_D$	10	—	—	100	—	1	100	—	—	1400	—	$\mu W$	—
		5	—	—	250	—	2.5	250	—	—	3500	—	$\mu W$	—
Output Voltage: Low-Level	$V_{OL}$	10	—	—	1000	—	10	1000	—	—	14000	—	V	—
		5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—
High-Level	$V_{OH}$	10	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—
		5	9.99	—	—	9.99	10	—	9.95	—	—	—	V	—
Noise Immunity (Any Input) For Definition, See Appendix	$V_{NL}$	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	17.10
		1.0	10	3	—	—	3	4.5	—	2.9	—	—	V	
	$V_{NH}$	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	
		9.0	10	2.9	—	—	3	4.5	—	3	—	—	V	
Output Drive Current N-Channel	$I_{DN}$	Decoded Outputs	0.5	5	0.03	—	—	0.025	0.15	—	0.02	—	—	mA
			0.5	10	0.06	—	—	0.05	0.3	—	0.04	—	—	
	$I_{DP}$	Carry Output	0.5	5	0.095	—	—	0.08	0.5	—	0.065	—	—	
			0.5	10	0.155	—	—	0.13	1	—	0.105	—	—	
P-Channel	$I_{DP}$	Decoded Outputs	4.5	5	-0.018	—	—	-0.015	-0.075	—	-0.012	—	—	mA
			9.5	10	-0.06	—	—	-0.05	-0.15	—	-0.04	—	—	
	$I_{DP}$	Carry Output	4.5	5	-0.095	—	—	-0.08	-0.4	—	-0.065	—	—	
			9.5	10	-0.155	—	—	-0.13	-0.8	—	-0.105	—	—	
Input Current	$I_I$			—	—	—	—	10	—	—	—	—	pA	

♦ See Appendix.

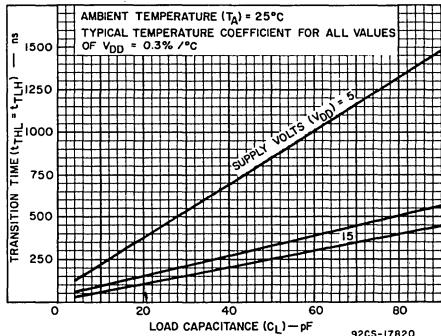


Fig.17.5—Typ. transition time vs.  $C_L$  for decoded outputs.

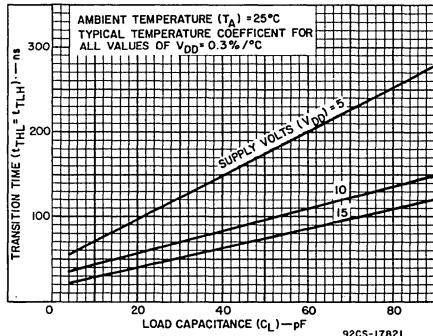
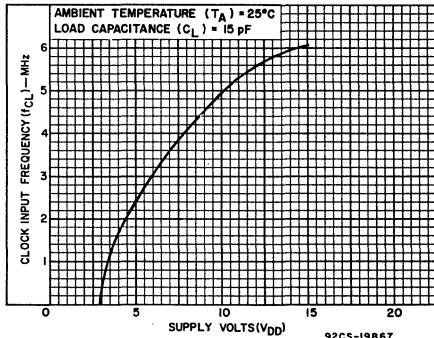
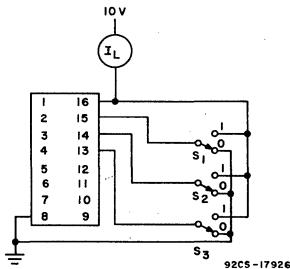


Fig.17.6—Typ. transition time vs.  $C_L$  for carry output.

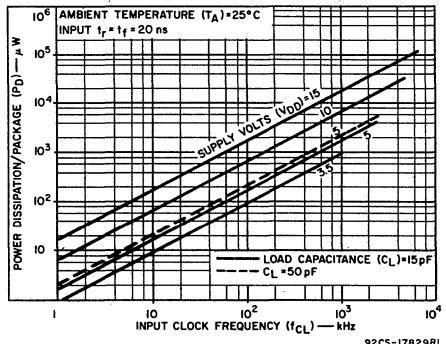


*Fig. 17.7—Typical clock frequency vs.  $V_{DD}$ .*

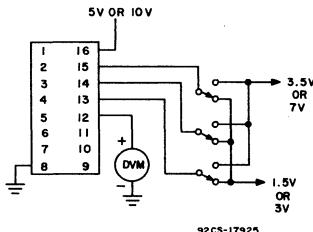


**Measure the leakage current of the device for all switch combinations.**

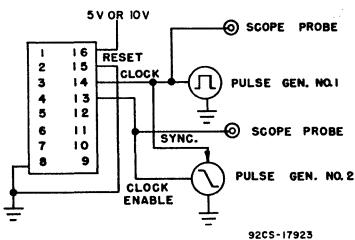
*Fig. 17.9—Quiescent device current test circuit.*



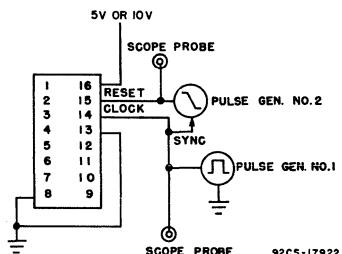
*Fig. 17.8—Typical dissipation characteristics.*



*Fig. 17.10—Noise immunity test circuit.*



*Fig. 17.12—Clock enable and set-up time test circuit.*



*Fig. 17.13—Reset propagation delay time and minimum reset pulse duration.*

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns except  $t_rCL$ ,  $t_fCL$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$  (See Appendix for Waveforms)

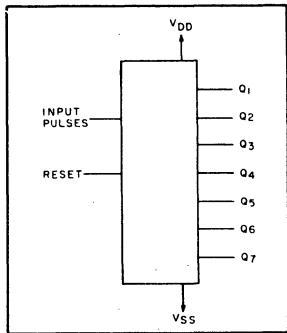
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4022AD, CD4022AK CD4022AF			CD4022AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>CLOCKED OPERATION</b>											
Propagation Delay Time: Carry-Out Line	$t_{PHL}, t_{PLH}$		5	—	325	1000	—	325	1300	ns	17.4
			10	—	125	250	—	125	500		
Decode Out Lines	$t_{THL}, t_{TLH}$		5	—	400	1200	—	400	1600	ns	17.3
			10	—	200	400	—	200	800		
Transition Time: Carry-Out Line	$t_{THL}, t_{TLH}$		5	—	85	300	—	85	340	ns	17.6
			10	—	50	100	—	50	200		
Decode-Out Lines	$t_{WL}, t_{WH}$		5	—	300	900	—	300	1200	ns	17.5
			10	—	125	250	—	125	500		
Minimum Clock Pulse Width	$t_{WL}, t_{WH}$		5	—	250	500	—	250	830	ns	17.11
			10	—	85	170	—	85	250		
Clock Rise & Fall Time	$t_{rCL}, t_{fCL}$		5	—	—	15	—	—	15	$\mu\text{s}$	17.11
			10	—	—	15	—	—	15		
Clock Enable Set-Up Time			5	350	175	—	700	175	—	ns	17.12
			10	150	75	—	300	75	—		
Maximum Clock Frequency	$f_{CL}$		5	1	2.5	—	0.6	2.5	—	MHz	17.7
			10	3	5	—	2	5	—		
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—
<b>RESET OPERATION</b>											—
Propagation Delay Time: Carry-Out Line	$t_{PHL}, t_{PLH}$		5	—	300	900	—	300	1200	ns	—
			10	—	125	250	—	125	500		
Decode-Out Line			5	—	500	1250	—	500	2500	ns	—
			10	—	200	400	—	200	800		
Minimum Reset Pulse Width	$t_{WL}, t_{WH}$		5	—	150	300	—	150	600	ns	17.13
			10	—	75	150	—	75	300		



# Digital Integrated Circuits

Monolithic Silicon

**CD4024AD, CD4024AE, CD4024AF  
CD4024AK, CD4024AT**



## COS/MOS 7-Stage Binary Counter

With Buffered Reset

### Special Features:

- Medium speed operation . . . . . 7 MHz (typ.) input pulse rate at  $V_{DD}-V_{SS} = 10$  V
- Low "high" and "low" level output impedance . . . . .  $700\Omega$  and  $500\Omega$  (typ.), respectively at  $V_{DD}-V_{SS} = 10$  V
- Logic block complexity on a single chip . . . . . each output accessible and resettable
- Static counter operation — counter retains state indefinitely with input pulse level "low" or "high"
- COS/MOS gate input loading on both reset and input-pulse lines

The CD4024A types consist of an input pulse shaping circuit, reset line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.

\* Formerly developmental type TA5385C.

### Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- D/A counter and switch on one chip

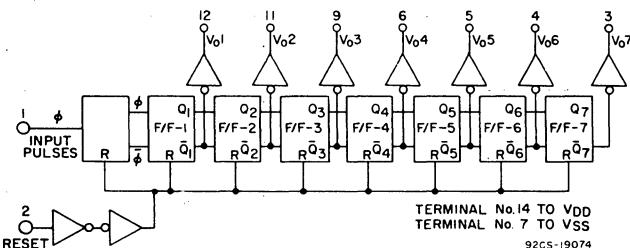


Fig.1-1 — Functional diagram for CD4024AD, AK, AE, AF.

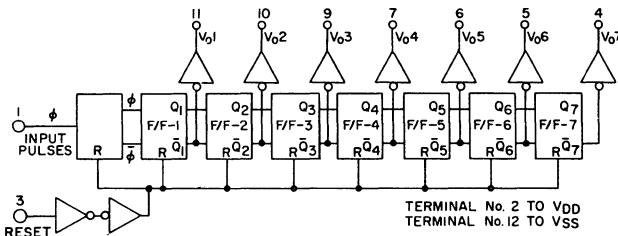
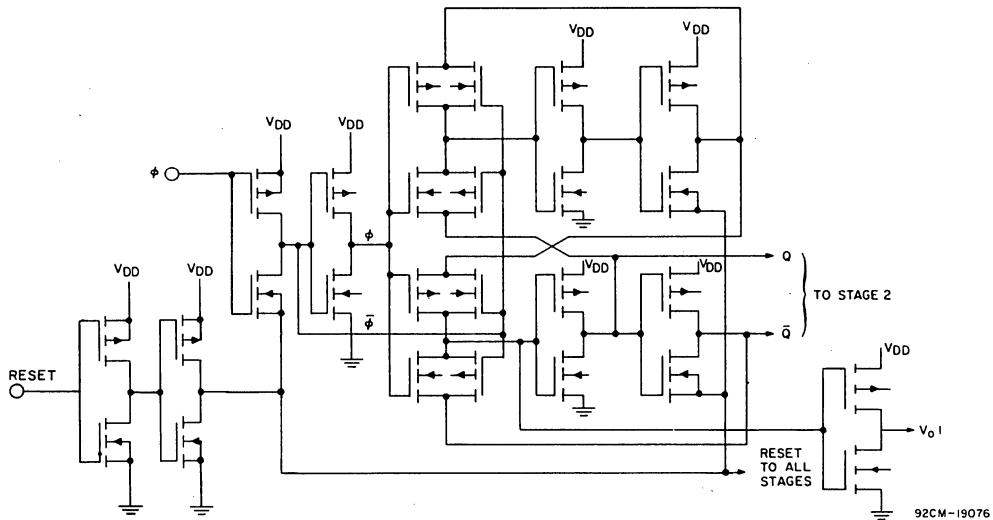
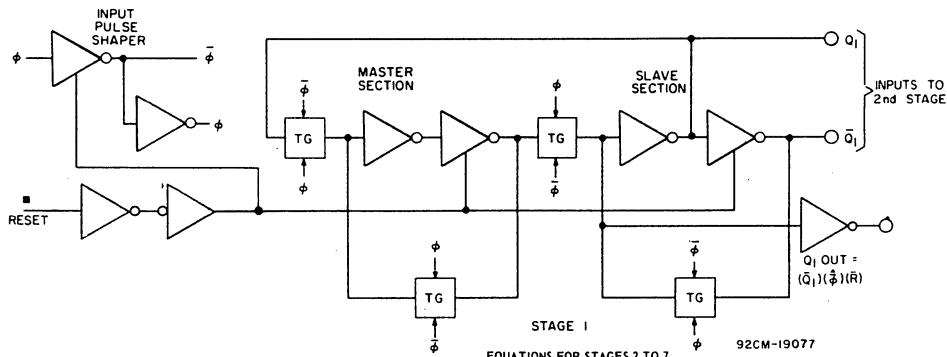


Fig.1-2 — Functional diagram for CD4024AT.



NOTE: SUBSTRATES FOR ALL "P" UNITS ARE CONNECTED TO  $V_{DD}$   
SUBSTRATES FOR ALL "N" UNITS, UNLESS OTHERWISE SHOWN, ARE CONNECTED TO GROUND.

Fig. 1-3 — Schematic diagram (pulse shaper and 1 binary stage).



• R = HIGH DOMINATES (RESETS ALL STAGES).

^ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE.  
COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE  $\phi$  TRANSITION  
(128 TOTAL BINARY COUNTS).

$$Q_{2OUT} = (\bar{Q}_2)(Q_1)(\frac{\phi}{\bar{\phi}})(R)$$

$$Q_{3OUT} = (\bar{Q}_3)(Q_1)(Q_2)(\frac{\phi}{\bar{\phi}})(R)$$

$$Q_{4OUT} = (\bar{Q}_4)(Q_1)(Q_2)(Q_3)(\frac{\phi}{\bar{\phi}})(R)$$

$$Q_{5OUT} = (\bar{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\frac{\phi}{\bar{\phi}})(R)$$

$$Q_{6OUT} = (\bar{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\frac{\phi}{\bar{\phi}})(R)$$

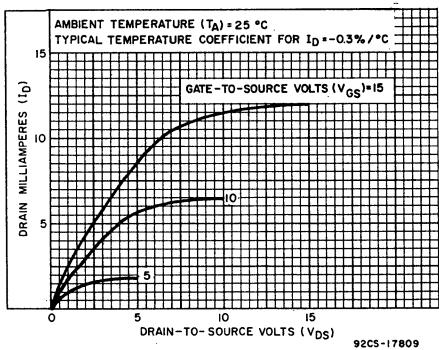
$$Q_{7OUT} = (\bar{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\frac{\phi}{\bar{\phi}})(R)$$

Fig. 1-4 — Logic block diagram (pulse shaper and 1 binary stage).

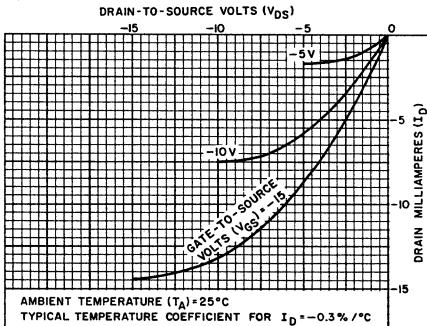
**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4024AD, CD4024AK, CD4024AT, CD4024AF											
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-55°C			25°C			125°C					
Quiescent Device Current	I <sub>L</sub>			5	-	-	5	-	0.3	5	-	-	300	μA	1-13
				10	-	-	10	-	0.5	10	-	-	600		
Quiescent Device Dissipation/Package	PD			5	-	-	25	-	1.5	25	-	-	1500	μW	-
				10	-	-	100	-	5	100	-	-	6000		
Output Voltage: Low-Level	V <sub>OL</sub>			5	-	-	0.01	-	0	0.01	-	-	0.05	V	-
				10	-	-	0.01	-	0	0.01	-	-	0.05		
High-Level	V <sub>OH</sub>			5	4.99	-	-	4.99	5	-	4.95	-	-	V	-
				10	9.99	-	-	9.99	10	-	9.95	-	-		
Noise Immunity (Any Input)	V <sub>NL</sub>			0.8	5	1.5	-	-	1.5	2.25	-	1.4	-	V	1-14
				1.0	10	3	-	-	3	4.5	-	2.9	-		
	V <sub>NH</sub>			4.2	5	1.4	-	-	1.5	2.25	-	1.5	-	V	1-15
				9.0	10	2.9	-	-	3	4.5	-	3	-		
Output Drive Current: N-Channel	I <sub>DN</sub>			0.5	5	0.31	-	-	0.25	0.5	-	0.175	-	mA	1-5 1-7
				0.5	10	0.62	-	-	0.5	1	-	0.35	-		
	I <sub>DP</sub>			4.5	5	-0.19	-	-	-0.15	-0.3	-	-0.105	-	mA	1-6 1-8
				9.5	10	-0.45	-	-	-0.35	-0.7	-	-0.25	-		
Input Current	I <sub>I</sub>			-	-	-	-	-	10	-	-	-	-	pA	-

For Output Drive Current test connections see Appendix.



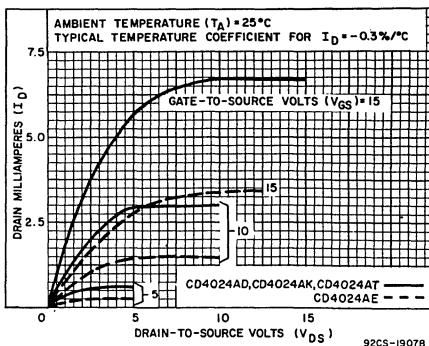
*Fig. 1-5 Typ. N-channel drain characteristics.*



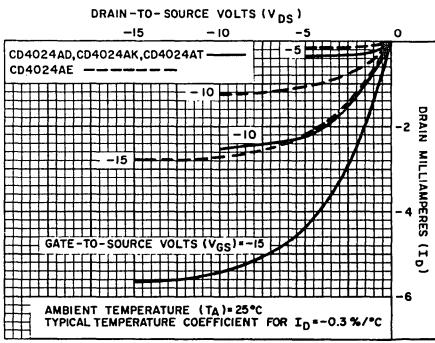
*Fig. 1-6 Typ. P-channel drain characteristics.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.			
				CD4024AE												
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-40°C			25°C			85°C						
Quiescent Device Current	I <sub>L</sub>			5	-	-	50	-	0.5	50	-	-	700	μA	1-13	
				10	-	-	100	-	1	100	-	-	1400			
Quiescent Device Dissipation/Package	PD			5	-	-	250	-	2.5	250	-	-	3500	μW	-	
				10	-	-	1000	-	10	1000	-	-	14000			
Output Voltage: Low-Level	V <sub>OL</sub>			5	-	-	0.01	-	0	0.01	-	-	0.05	V	..	
				10	-	-	0.01	-	0	0.01	-	-	0.05			
High-Level	V <sub>OH</sub>			5	4.99	-	-	4.99	5	-	4.95	-	-	V	..	
				10	9.99	-	-	9.99	10	-	9.95	-	-			
Noise Immunity (Any Input)	VNL		0.8	5	1.5	-	-	1.5	2.25	-	1.4	-	-	V	1-14	
			1.0	10	3	-	-	3	4.5	-	2.9	-	-			
	VNH		4.2	5	1.4	-	-	1.5	2.25	-	1.5	-	-	V	1-15	
			9.0	10	2.9	-	-	3	4.5	-	3	-	-			
Output Drive Current: N-Channel	I <sub>DN</sub>		0.5	5	0.15	-	-	0.12	0.5	-	0.095	-	-	mA	1-5 1-7	
			0.5	10	0.31	-	-	0.25	1	-	0.2	-	-			
P-Channel	I <sub>DP</sub>		4.5	5	-0.145	-	-	-0.12	-0.3	-	-0.095	-	-	mA	1-6 1-8	
			9.5	10	-0.31	-	-	-0.25	-0.7	-	-0.2	-	-			
Input Current	I <sub>I</sub>			-	-	-	-	10	-	-	-	-	-	pA	-	

For Output Drive Current test connections see Appendix.



*Fig. 1-7 Min. N-channel drain characteristics.*



*Fig. 1-8. Min. P-channel drain characteristics.*

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{pF}$ , and input rise and fall times = 20ns, except  $t_r^\phi$  and  $t_f^\phi$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4024AD, CD4024AK CD4024AT, CD4024AF			CD4024AE					
			V <sub>DD</sub> (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>INPUT OPERATION</b>											
Propagation Delay Time *	$t_{PHL}$ $t_{PLH}$		5	—	175	350	—	175	400	ns	1-9
			10	—	80	150	—	80	150		
Transition Time	$t_{THL}$ $t_{TLH}$		5	—	175	225	—	175	250	ns	1-10
			10	—	80	150	—	80	150		
Minimum Input-Pulse Width	$t_{WL}$ $t_{WH}$		5	—	200	330	—	200	500	ns	—
			10	—	140	125	—	140	165		
Input Pulse Rise & Fall Time	$t_r^\phi$ $t_f^\phi$		5	—	—	15	—	—	15	$\mu\text{s}$	—
			10	—	—	10	—	—	10		
Maximum Input Pulse Frequency	$f^\phi$		5	1.5	2.5	—	1	2.5	—	MHz	1-12
			10	4	7	—	3	7	—		
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	—	pF	—
<b>RESET OPERATION</b>											
Propagation Delay Time	$t_{PHL(R)}$		5	—	500	700	—	500	800	ns	—
			10	—	250	350	—	250	400		
Minimum Reset Pulse Width	$t_{WH(R)}$		5	—	375	500	—	375	600	ns	—
			10	—	200	300	—	200	350		

\* Propagation delay time is from clock input to  $Q_1$  output.

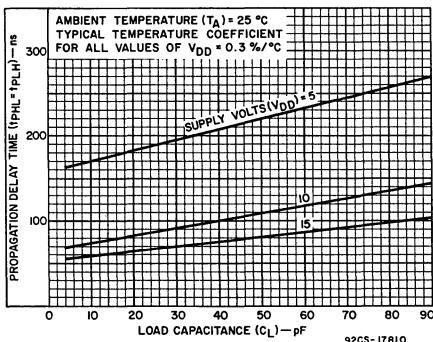


Fig. 1-9 Typ. propagation delay time vs.  $C_L$ .

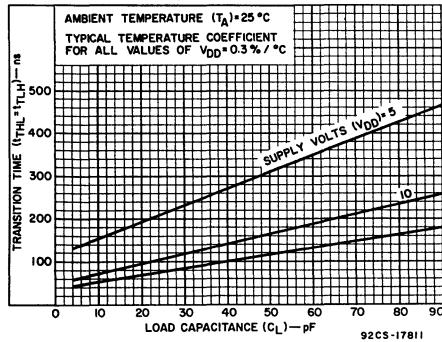


Fig. 1-10 Typ. transition time vs.  $C_L$ .

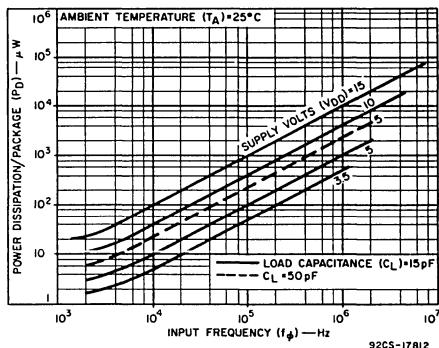


Fig.1-11 Typ. dissipation characteristics.

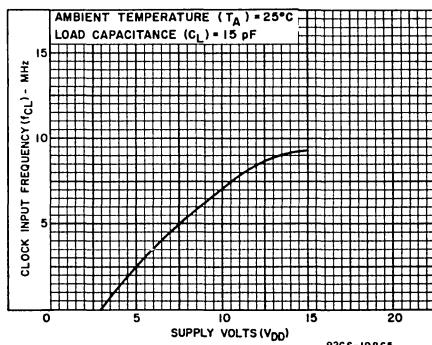
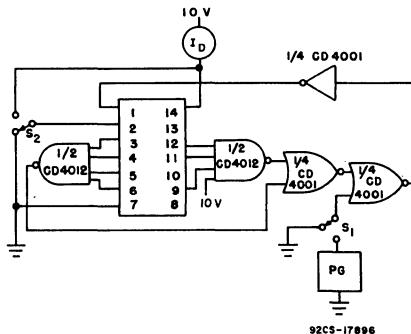
Fig.1-12 Typ. input pulse frequency vs.  $V_{DD}$ .

Fig.1-13 Quiescent device current test circuit.

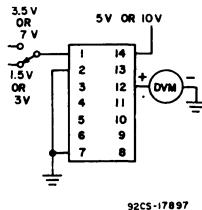


Fig.1-14 Noise Immunity test circuit.

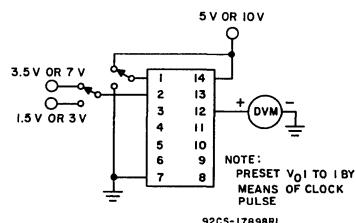


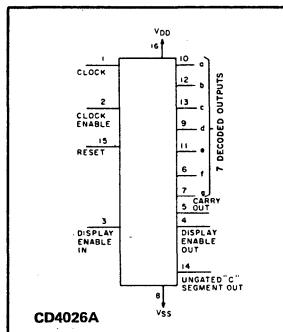
Fig.1-15 Reset noise immunity test circuit.



# Digital Integrated Circuits

Monolithic Silicon

## CD4026A, CD4033A Types



RCA CD4026A and CD4033A<sup>▲</sup> each consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are Clock, Reset, & Clock Enable; common outputs are Carry Out and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include Display Enable input and Display Enable and Ungated "C-segment" outputs. Signals peculiar to the CD4033 are Ripple-Blanking and Lamp Test inputs and a Ripple-Blanking Output.

A "high" Reset signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the Clock Enable signal is "low". Counter advancement via the clock line is inhibited when the Clock Enable signal is "high". Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (Cout) signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal number 0 to 9. The 7-segment outputs go "high" on selection in the CD4033A; in the CD4026A these outputs go "high" only when the Display Enable IN is "high".

<sup>▲</sup> Formerly developmental type TA5677.

## COS/MOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:

- Display Enable — CD4026AD, AE, AF, AK
- Ripple Blanking — CD4033AD, AE, AF, AK

### Special Features:

- Counter and 7-segment decoding in one package
- Ideal for low-power displays
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 2.5 MHz (typ.)
- Display Enable Output (CD4026A)
- "Ripple Blanking" and Lamp Test (CD4033A)



CD4033A

### Applications:

- Decade counting/7-segment decimal display
- Frequency division/7-segment decimal displays
- Clock/watches/timers (e.g.  $\div 60$ ,  $\div 60$ ,  $\div 12$  counter/display)
- Counter/display driver for meter applications

### CD4026A

When the Display Enable IN is "low" the seven decoded outputs are forced "low" regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

### CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display, consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033A associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033A in the next-lower significant

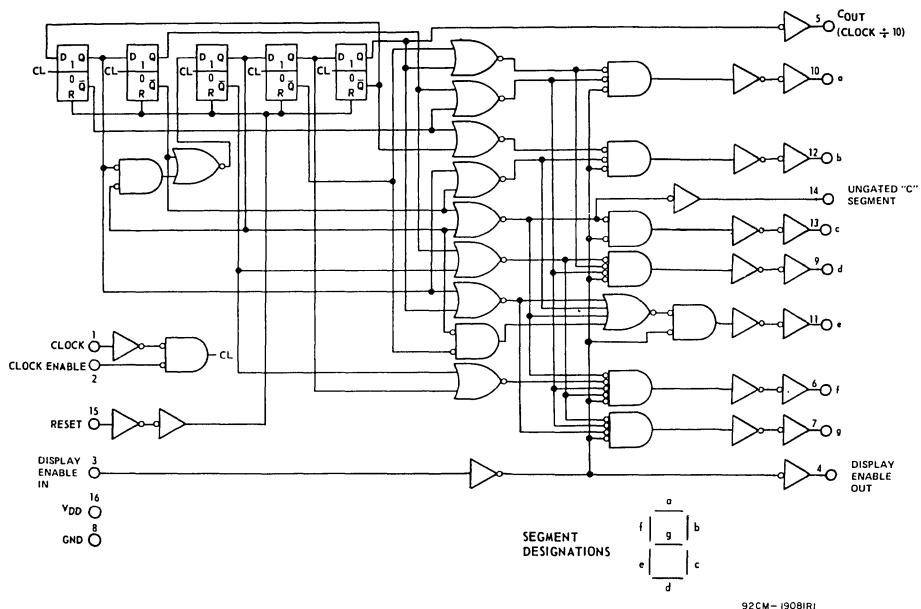


Fig.2-1 CD4026A logic diagram.

position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display

'On the fraction side of the display the RBI of the CD4033A associated with the least significant bit is connected to a "low level" voltage and the RBO of that CD4033A is connected to the RBI terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a "high level" voltage (instead of to the RBO of the next more-significant-stage). For Example: optional zero  $> 0.7346$ .

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033A associated with it to a "high-level" voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033A has a "Lamp Test" input which, when connected to a "high-level" voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the "high" state.

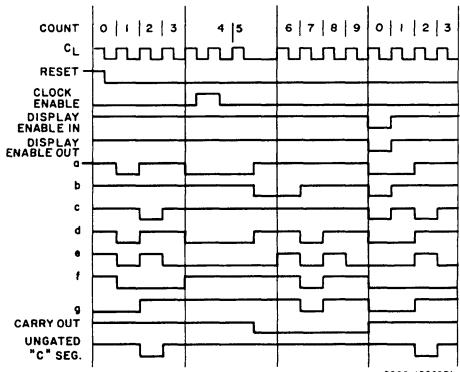


Fig.2-2 - CD4026A timing diagram.

For maximum ratings, see page 22.

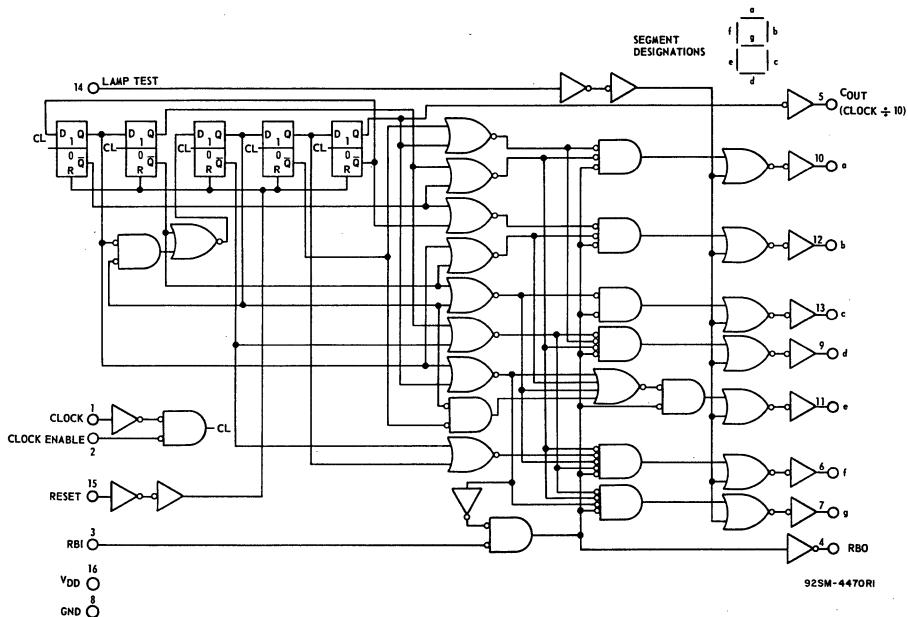


Fig.2-3 CD4033A logic diagram.

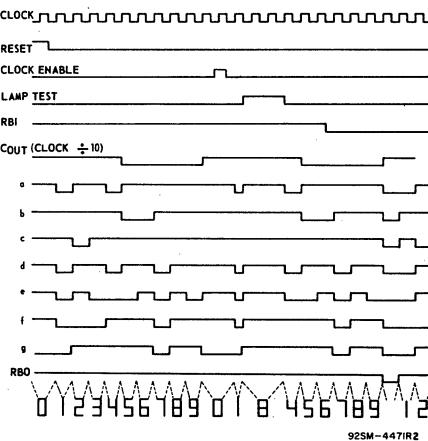


Fig.2-4 CD4033A timing diagram.

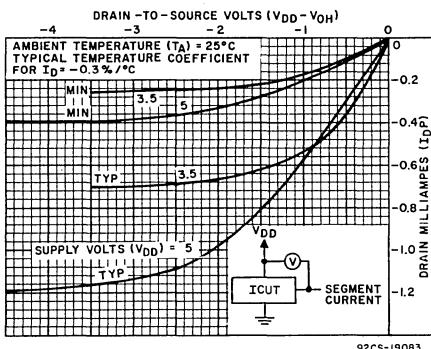


Fig.2-5 Min. & typ. P-channel segment drain characteristics @  $V_{DD} = 3.5$  & 5 V.

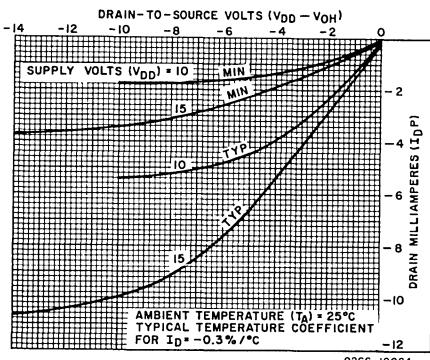


Fig.2-6 Min. & typ. P-channel segment drain characteristics @  $V_{DD} = 10$  & 15 V.

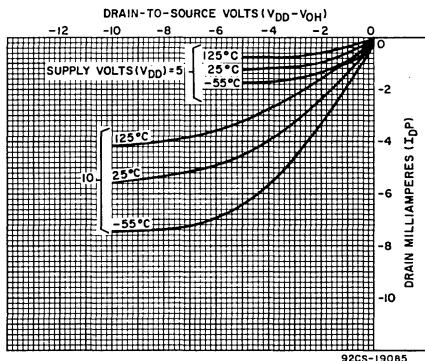


Fig.2-7 Typ. P-channel drain characteristics as a function of temp.

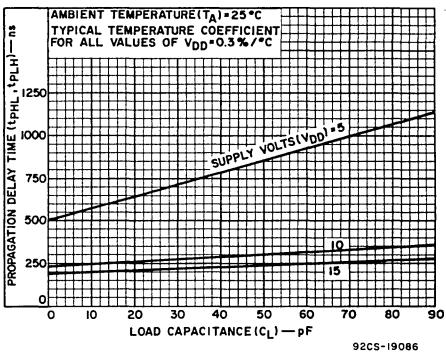


Fig.2-8 Typ. propagation delay time vs.  $C_L$  for decoded outputs.

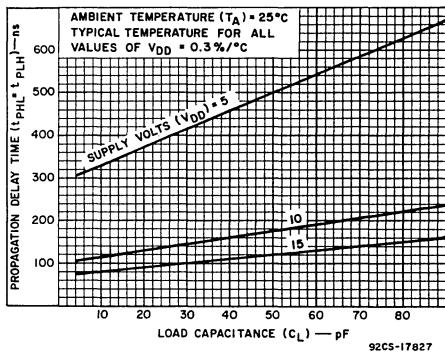


Fig.2-9 Typ. propagation delay time vs.  $C_L$  for carry outputs.

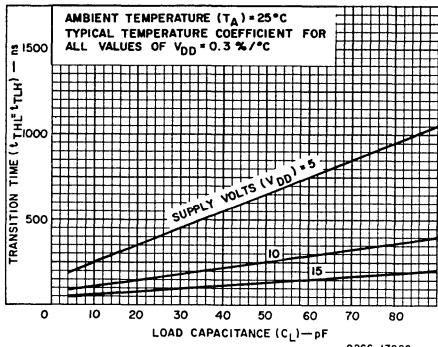


Fig.2-10 Typ. transition time vs.  $C_L$  for decoded outputs.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4026AD, CD4026AK, CD4026AF CD4033AD, CD4033AK, CD4033AF											
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C					
Quiescent Device Current	$I_L$			5	—	—	5	—	0.3	5	—	—	300	$\mu A$	2-14
			10	—	—	10	—	0.5	10	—	—	600			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	25	—	1.5	25	—	—	1500	$\mu W$	
				10	—	—	100	—	5	100	—	—	6000		
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	V	
				10	—	—	0.01	—	0	0.01	—	—	0.05		
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	V	
				10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (All Inputs)	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	V	2-15
				1.0	10	3.0	—	—	3	4.5	—	2.9	—		
	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	V	
				9.0	10	2.9	—	—	3	4.5	—	3.0	—		
Output Drive Current:	$I_{D^N}$	Decoded Outputs	0.5	5	0.15	—	—	0.12	0.24	—	0.09	—	—	mA	
			0.5	10	0.32	—	—	0.25	0.5	—	0.18	—	—		
		Carry Output	0.5	5	0.12	—	—	0.15	0.4	—	0.1	—	—		
		$I_{D^P}$	0.5	10	0.45	—	—	0.35	1	—	0.25	—	—	mA	2-5, 2-6, 2-7
			4.5	5	-0.21	—	—	-0.14	-0.28	—	-0.1	—	—		
			9.5	10	-0.45	—	—	-0.3	-0.6	—	-0.22	—	—		
		Carry Output	4.5	5	-0.12	—	—	-0.15	-0.4	—	-0.1	—	—		—
		9.5	10	-0.45	—	—	-0.35	-1	—	-0.25	—	—			
Input Current	$I_I$	Any Input		—	—	—	—	—	10	—	—	—	—	pA	

For Output Drive Current test connections see Appendix.

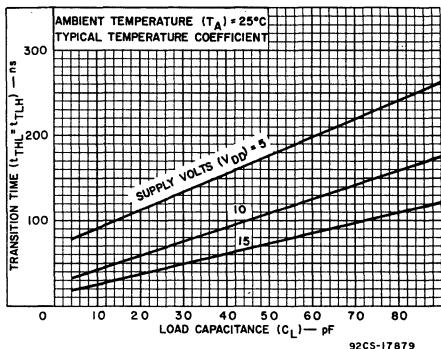


Fig. 2-11 Typ. transition time vs.  $C_L$  for carry output.

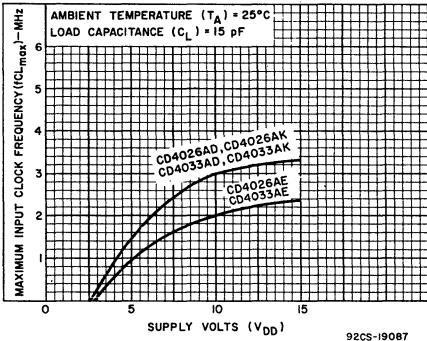


Fig. 2-12 Max. input clock frequency vs.  $V_{DD}$ .

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS			
				CD4026AE, CD4033AE												
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C						
Quiescent Device Current	$I_L$			5	—	—	50	—	0.5	50	—	700	μA	2-14		
	10	—	—	—	100	—	1	100	—	—	1400					
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	2.5	250	—	3500	μW			
				10	—	—	1000	—	10	1000	—	14000				
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	0.05	V			
				10	—	—	0.01	—	0	0.01	—	0.05				
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	V			
				10	9.99	—	—	9.99	10	—	9.95	—				
Noise Immunity (All Inputs)	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	V	2-15		
				1.0	10	3.0	—	—	3	4.5	—	2.9				
	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	V			
				9.0	10	2.9	—	—	3	4.5	—	3.0				
Output Drive Current:	$I_D$			Decoded Outputs	0.5	5	0.08	—	—	0.06	0.24	—	0.05	mA		
				N-Channel	0.5	10	0.15	—	—	0.12	0.5	—	0.1			
				Carry Output	0.5	5	0.095	—	—	0.08	0.4	—	0.06			
					0.5	10	0.3	—	—	0.25	1	—	0.2			
P-Channel	$I_D^P$			Decoded Outputs	4.5	5	-0.09	—	—	-0.07	-0.28	—	-0.06	mA	2.5, 2.6, 2.7	
					9.5	10	-0.2	—	—	-0.15	-0.6	—	-0.13			
				Carry Output	4.5	5	-0.095	—	—	-0.08	-0.4	—	-0.06	mA	—	
					9.5	10	-0.3	—	—	-0.24	-1	—	-0.2			
Input Current	$I_I$	Any Input			—	—	—	—	—	10	—	—	—	pA		

For Output Drive Current test connections see Appendix.

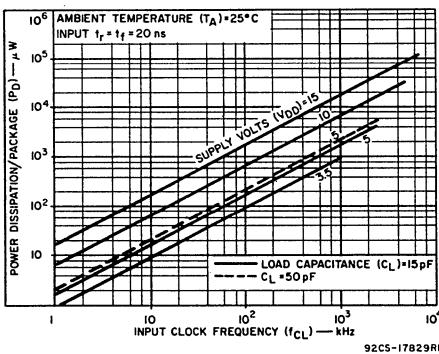


Fig.2-13 Typ. dissipation characteristics.

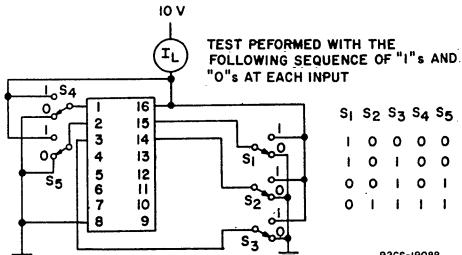


Fig.2-14 Quiescent device current test circuit.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{pF}$ , and input rise and fall times = 20ns, except  $t_{rCL}$  and  $t_{fCL}$   
 Typical Temperature Coefficient for all values of  $V_{DD}$  = 0.3%/°C. (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4026AD, AF, AK			CD4026AE CD4033AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>CLOCKED OPERATION</b>											
Propagation Delay Time: Carry Out Line	$t_{PHL}$ $t_{PLH}$		5	—	350	1000	—	350	1300	ns	2-9
			10	—	125	250	—	125	300		
Decode Out Lines	$t_{THL}$ $t_{TLH}$		5	—	600	1700	—	600	2200	ns	2-8
			10	—	250	500	—	250	700		
Transition Time: Carry Out Line	$t_{THL}$ $t_{TLH}$		5	—	100	300	—	100	350	ns	2-11
			10	—	50	150	—	50	200		
Decode Out Lines	$t_{WL}$ $t_{WH}$		5	—	300	900	—	300	1200	ns	2-10
			10	—	125	350	—	125	450		
Minimum Clock Pulse Width	$t_{WL}$ $t_{WH}$		5	—	200	330	—	200	500	ns	—
			10	—	100	170	—	100	250		
Clock Rise & Fall Time	$t_{rCL}$ $t_{fCL}$		5	—	—	15	—	—	15	$\mu\text{s}$	—
			10	—	—	15	—	—	15		
Clock Enable Set-Up Time			5	—	175	500	—	175	700	ns	—
			10	—	75	200	—	75	300		
Maximum Clock Frequency	$f_{CL}$	Measured with Respect to Carry Out Line	5	1.5	2.5	—	1	2.5	—	MHz	2-12
			10	3	5	—	2	5	—		
Input Capacitance	$C_I$	Any Input	—	—	5	—	—	5	—	pF	—
<b>RESET OPERATION</b>											
Propagation Delay Time: To Carry Out Line	$t_{PHL(R)}$		5	—	350	1000	—	350	1300	ns	—
			10	—	125	250	—	125	300		
To Decode Out Lines			5	—	550	1400	—	550	1900	ns	—
			10	—	240	500	—	240	600		
Reset Pulse Width	$t_{WH(R)}$		5	—	200	330	—	200	500	ns	—
			10	—	100	165	—	100	250		
Reset Removal Time			5	—	300	750	—	300	1000	ns	—
			10	—	100	225	—	100	275		

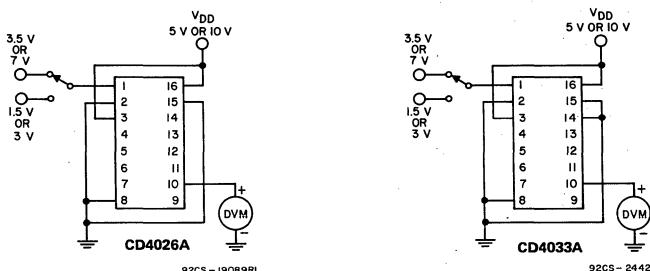
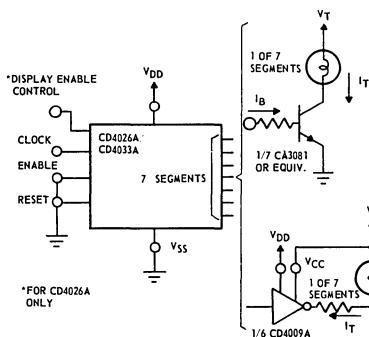


Fig.2-15 – Noise immunity test circuits.

**INTERFACING THE CD4026A AND CD4033A WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES**  
 (Refer to Application Note ICAN-6733 for detailed interfacing information)



**LOW-POWER INCANDESCENT READOUTS**

PINLITES INC- Series O and R

TUBE REQUIREMENTS:  $V_T$  (V) mA/Segment

0-03-15	1.5	8
0-04-30	3.0	8
0-06-30	3.0	8
R-R3-20	2.0	4.3
R-R4-30	3.0	4.3

**ASSUMED TRANSISTOR CHARACTERISTICS**

$$\begin{aligned} \beta_{dc} (\text{min.}) &\geq 30 \\ V_{CE(\text{sat.})} &\leq 0.50 \text{ V} \\ @V_{DD} \geq 3.5 \text{ V (min.)} \\ I_B &\geq 0.25 \text{ mA (min.)} \\ I_T &\leq 7.5 \text{ mA (min.)} \end{aligned}$$

**CD4009A**

$$\begin{aligned} @V_{DD} = 10 \text{ V (min.)} \\ V_o "O" \leq 0.6 \text{ V} \\ I_T = 8 \text{ mA (min.)} \\ @V_{DD} = 6 \text{ V (min.)} \\ V_o "O" \leq 1.0 \text{ V} \\ I_T = 5 \text{ mA (min.)} \end{aligned}$$

$$V_T \approx 1.5 \text{ V TO } 3.5 \text{ V}$$

**INCANDESCENT READOUTS**

RCA Numitron- DR2000 Series

TUBE REQUIREMENTS:

$$\begin{aligned} V_T &= 3.5 - 5.0 \text{ V} \\ I_T &= 24 \text{ mA/Segment} \end{aligned}$$

**ASSUMED TRANSISTOR CHARACTERISTICS**

$$\begin{aligned} \beta_{dc} (\text{min.}) &\geq 25 \\ V_{CE(\text{sat.})} &\leq 0.50 \text{ V} \\ @V_{DD} = 8 \text{ V (min.)} \\ I_B &= 1.0 \text{ mA (min.)} \\ I_T &= 24 \text{ mA (min.)} \end{aligned}$$

**CD4009A**

$$\begin{aligned} @V_{DD} = 10 \text{ V (min.)} \\ V_o "O" \leq 2 \text{ V} \\ I_T = 20 \text{ mA (min.)} \\ V_T \approx 3.5 \text{ V TO } 6 \text{ V} \end{aligned}$$

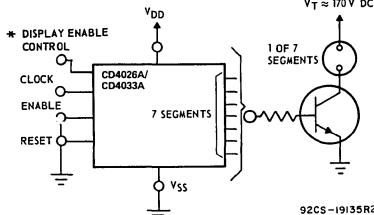
92CS-19133R2

**NEON READOUTS (NIXIE TUBE)**

1. Alco Electronics- MG19
2. Burroughs- B5971, B7971, B8971

TUBE REQUIREMENTS  $V_T$  (Vdc) mA/Segment

Alco MG19 .....	180	..... 0.5
Burroughs B5971 .....	170	..... 3
" B7971, B8971.....	170	..... 6



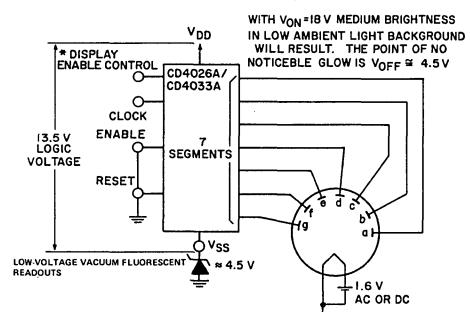
**TRANSISTOR CHARACTERISTICS**

Leakage with transistor cutoff  $\leq 0.05 \text{ mA}$   
 $V_{(BR)} \text{ CER} \cdots > V_T$

$$\beta_{dc(\text{min.})} \geq 30$$

▲ (Trademark) Burroughs Corp.

**LOW-VOLTAGE VACUUM FLUORESCENT READOUTS**



1. Tung-Sol DIGIVAC S/G<sup>t</sup>-Type DT1704A or DT1705C

2. Nippon Electric (NEC)-Type DG12E or LD915

TUBE REQUIREMENTS: 100 to 300  $\mu\text{A}/\text{seg}$ -ment at tube voltages of 12V to 25V depending on required brightness. Filament requirement 45mA at 1.6V, AC or DC.

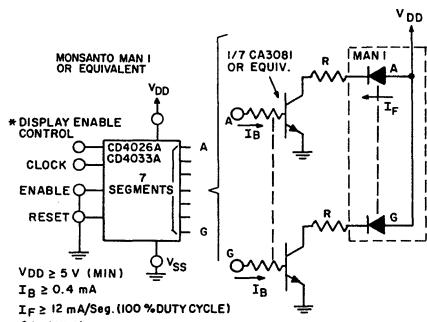
92CS-19132R2

## INTERFACING THE CD4026A AND CD4033A WITH COMMERCIALLY AVAILABLE 7-SEGMENT DISPLAY DEVICES

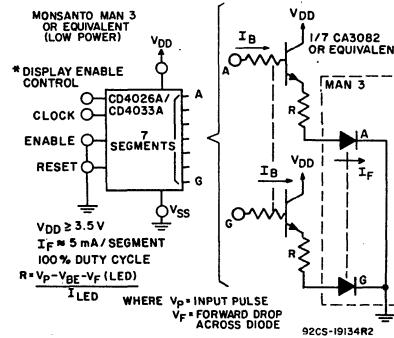
(Refer to Application Note ICAN-6733 for detailed interfacing information)

(cont'd.)

## LIGHT EMITTING DIODE DISPLAYS



$$\begin{aligned} V_{DD} &\geq 5 \text{ V (MIN)} \\ I_B &\geq 0.4 \text{ mA} \\ I_F &\geq 12 \text{ mA/Seg. (100 \% DUTY CYCLE)} \\ \beta_{dc} (\text{MIN}) &\geq 30 \\ V_{CE} (\text{SAT}) &\leq 0.5 \text{ V} \\ R &= \frac{V_{DD} - V_{CE(sat)} - V_F(\text{LED})}{I_{LED}} \end{aligned}$$

WHERE  $V_F$  = FORWARD DROP ACROSS DIODE

$$\begin{aligned} V_{DD} &\geq 3.5 \text{ V} \\ I_B &\approx 5 \text{ mA/SEGMENT} \\ 100 \% \text{ DUTY CYCLE} \\ R &= \frac{V_p - V_{BE} - V_F}{I_{LED}} \end{aligned}$$

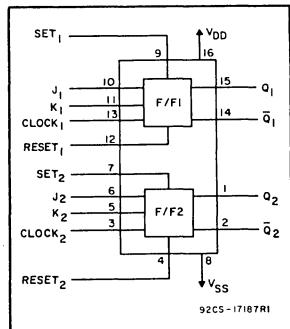
92CS-19134R2



# Digital Integrated Circuits

Monolithic Silicon

## CD4027AD, CD4027AE, CD4027AK



RCA CD4027AA is a single monolithic chip integrated circuit containing two identical complementary-symmetry "J-K" master-slave flip-flops. Each flip-flop has provisions for individual "J", "K", "Set", "Reset", and "Clock" input signals. Buffered "Q" and "Q-bar" signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA CD4013A dual "D"-type flip-flop.

▲ Formerly developmental type TA5872.

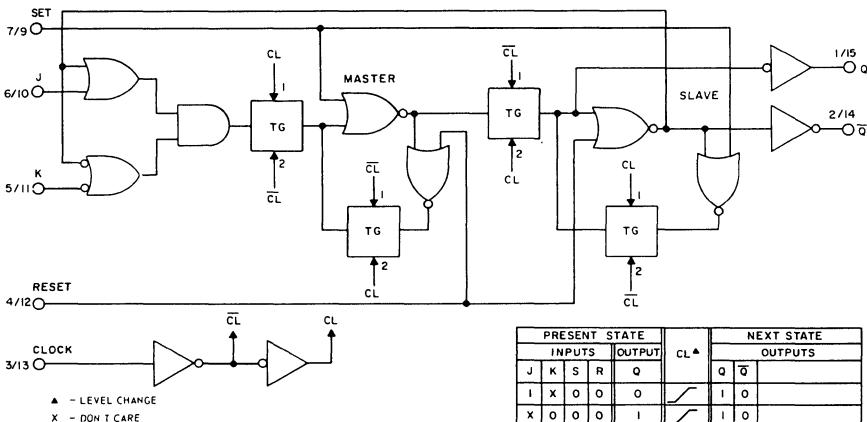


Fig.3-1 Logic diagram & truth table for one of two identical J-K flip flops.

92CM-17188R2

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS
				CD4027AD, CD4027AK								
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C		
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
	5	—	—	1	—	0.005	1	—	—	60	μA	
Quiescent Device Dissipation/Package	$P_D$	10	—	—	2	—	0.005	2	—	—	120	μW
		5	—	—	5	—	0.025	5	—	—	300	—
Output Voltage: Low-Level	$V_{OL}$	10	—	—	20	—	0.05	20	—	—	1200	—
		5	—	—	0.01	—	0	0.01	—	—	0.05	V
High-Level	$V_{OH}$	10	—	—	0.01	—	0	0.01	—	—	0.05	V
		5	4.99	—	—	4.99	5	—	4.95	—	—	—
Noise Immunity (Any Input)	$V_{NL}$	10	9.99	—	—	9.99	10	—	9.95	—	—	—
		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—
	$V_{NH}$	1.0	10	3.0	—	—	3	4.5	—	2.9	—	—
		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—
Output Drive Current:	$I_{DN}$	$V_O = 0.5V$	5	0.63	—	—	0.5	1	—	0.33	—	—
			10	1.25	—	—	1	2.5	—	0.7	—	—
P-Channel	$I_{DP}$	$V_O = 4.5V$	5	-0.31	—	—	-0.25	-0.5	—	-0.175	—	—
			10	-0.8	—	—	-0.65	-1.3	—	-0.45	—	—
Input Current	$I_I$	Any Input	—	—	—	—	—	10	—	—	—	pA

For Output Drive Current test connections see Appendix.

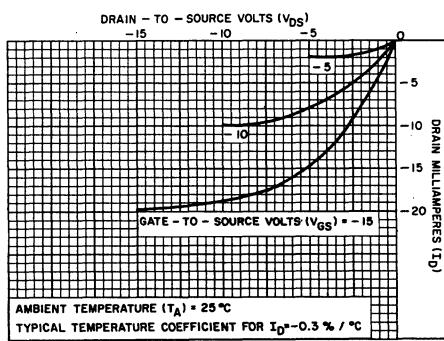
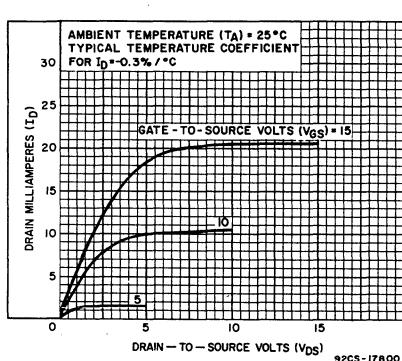


Fig.3-2 Typ. N-channel drain characteristics.

Fig.3-3 Typ. P-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS												CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.								
			CD4027AE																				
			-40°C			25°C			85°C														
Quiescent Device Current	$I_L$		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				$\mu A$	3-12							
			5	—	—	10	—	0.01	10	—	—	140											
Quiescent Device Dissipation/Package	$P_D$		10	—	—	20	—	0.05	20	—	—	280				$\mu W$							
			5	—	—	50	—	0.05	50	—	—	700											
Output Voltage: Low-Level	$V_{OL}$		10	—	—	200	—	0.5	200	—	—	2800				$V$							
			5	—	—	0.01	—	0	0.01	—	—	0.05											
High-Level	$V_{OH}$		10	4.99	—	—	4.99	5	—	4.95	—	—	—				$V$						
			10	9.99	—	—	9.99	10	—	9.95	—	—	—										
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—				$V$	3-13				
			1.0	10	3.0	—	—	3	4.5	—	2.9	—	—	—									
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—									
			9.0	10	2.9	—	—	3	4.5	—	3.0	—	—	—									
Output Drive Current:	$I_{DN}$	$V_O = 0.5V$	5	0.3	—	—	0.3	1	—	0.24	—	—	—				$mA$	3-2, 3-4					
			10	0.72	—	—	0.6	2.5	—	0.5	—	—	—										
P-Channel	$I_{DP}$	$V_O = 4.5V$	5	-0.17	—	—	-0.14	-0.5	—	-0.063	—	—	—				$mA$	3-3, 3-5					
			10	-0.4	—	—	-0.33	-1.3	—	-0.27	—	—	—										
Input Current	$I_I$	Any Input	—	—	—	—	—	10	—	—	—	—	—	$pA$	—	—	—	—					

For Output Drive Current test connections see Appendix.

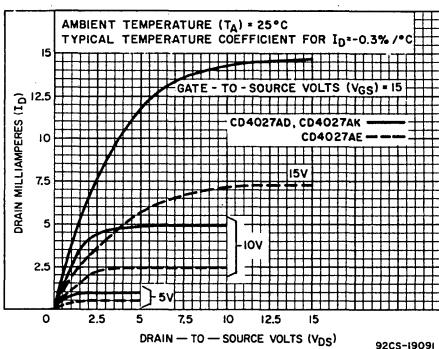


Fig.3-4 Min. N-channel drain characteristics.

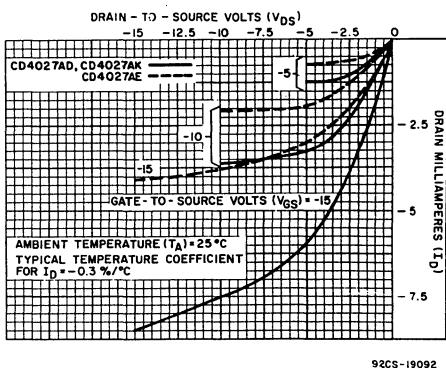
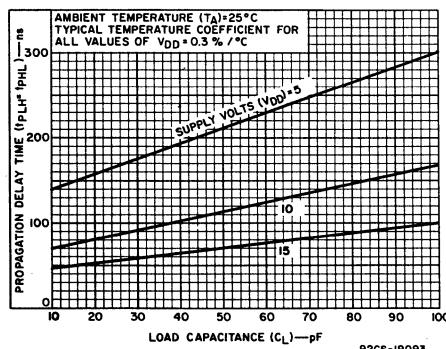
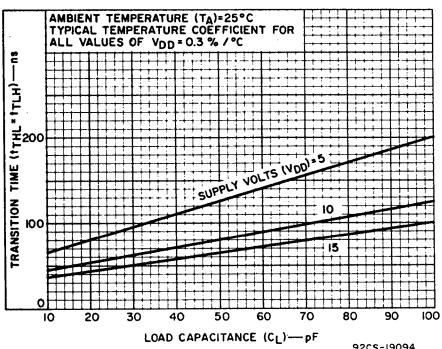


Fig.3-5 Min. P-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{pF}$ , and input rise and fall times = 20ns, except  $t_rCL$  and  $t_fCL$ .  
 Typical Temperature Coefficient for all values of  $V_{DD}$  =  $0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4027AD, CD4027AK			CD4027AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time	$t_{PHL}$ , $t_{PLH}$		5	—	150	300	—	150	400	ns	3-7
			10	—	75	110	—	75	150		
Transition Time	$t_{THL}$ , $t_{TLH}$		5	—	75	125	—	75	250	ns	3-8
			10	—	50	70	—	50	140		
Minimum Clock Pulse Width	$t_{WL}$ , $t_{WH}$		5	—	165	330	—	165	500	ns	—
			10	—	65	110	—	65	165		
Clock Rise & Fall Time	$*t_{rCL}$ , $t_{fCL}$		5	—	—	15	—	—	15	$\mu\text{s}$	—
			10	—	—	5	—	—	5		
Set-Up Time			5	—	70	150	—	70	200	ns	—
			10	—	25	50	—	25	75		
Maximum Clock Frequency (toggle mode)	$f_{CL}$		5	1.5	3	—	1	3	—	MHz	3-9
			10	4.5	8	—	3	8	—		
Input Capacitance	$C_I$		—	—	5	—	—	5	—	pF	—
<b>SET &amp; RESET OPERATION</b>											
Propagation Delay Time	$t_{PHL(R)}$ , $t_{PLH(S)}$		5	—	175	225	—	175	350	ns	—
			10	—	75	110	—	75	150		
Minimum Set and Reset Pulse Widths	$t_{WH(S)}$ , $t_{WL(R)}$		5	—	125	200	—	125	300	ns	—
			10	—	50	80	—	50	120		

- If more than one unit is cascaded in a parallel clocked operation,  $t_rCL$  should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

Fig.3-6 Typ. propagation delay time vs.  $C_L$ .Fig.3-7 Typ. transition time vs.  $C_L$ .

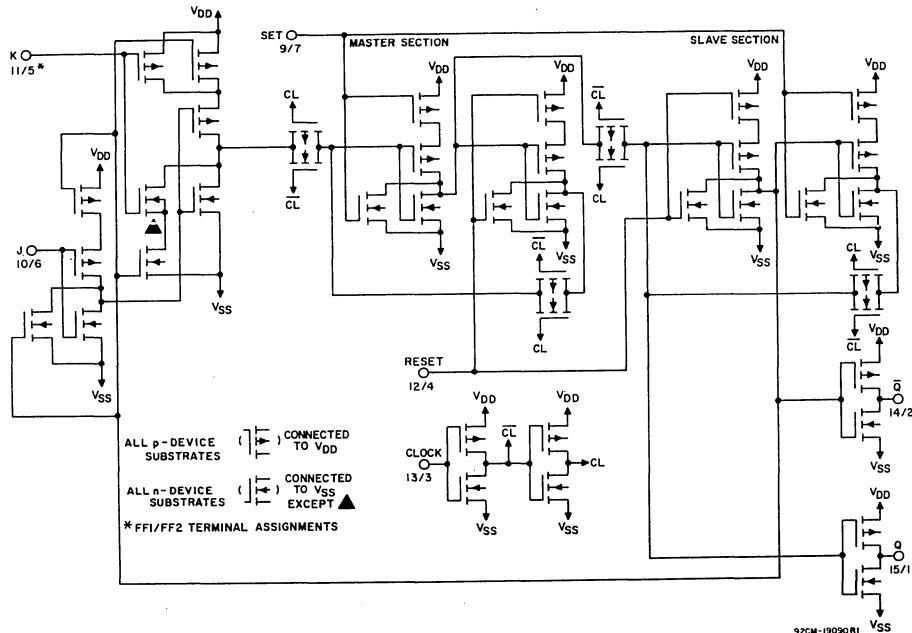


Fig.3-8 Schematic diagram for one of two identical J-K flip flops.

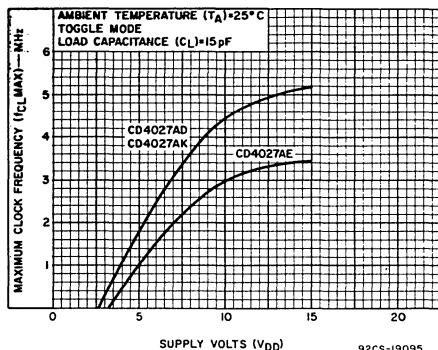


Fig.3-9 Max. clock frequency vs. supply voltage.

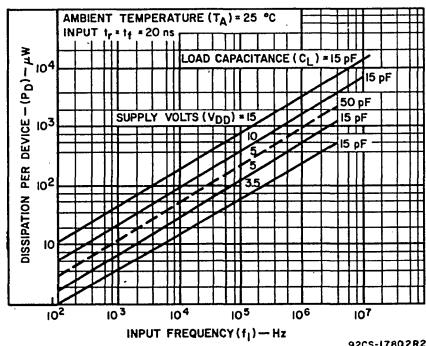


Fig.3-10 Typ. dissipation characteristics.

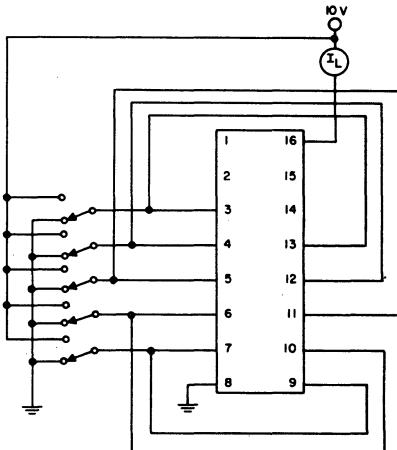
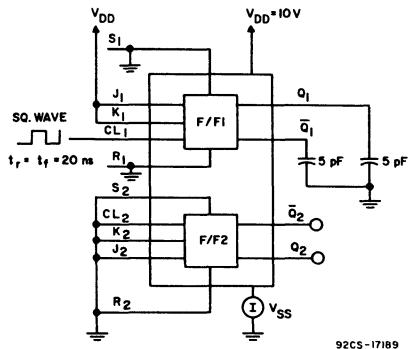


Fig. 3-12 - Quiescent device current test circuit.

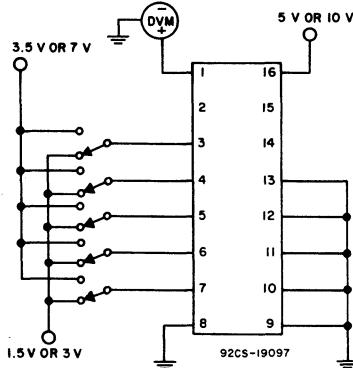
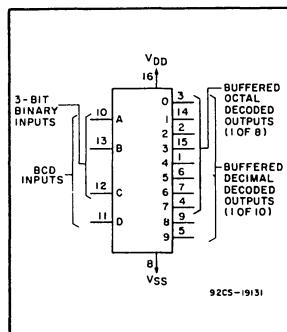


Fig. 3-13 - Noise-immunity test circuit.



# Digital Integrated Circuits

Monolithic Silicon

**CD4028AD, CD4028AF  
CD4028AE, CD4028AK**


## COS/MOS

### BCD-to-Decimal Decoder

#### Special Features:

- BCD to decimal decoding or binary to octal decoding
- High decoded output drive capability . . . . . 8 mA (typ.) sink or source
- "Positive logic" inputs and outputs . . . . . decoded outputs go "high" on selection
- Medium speed operation . . . . . t<sub>THL</sub>, t<sub>T LH</sub> = 30 ns (typ.) @ V<sub>DD</sub> = 10 V

#### Applications:

- Code conversion
- Indicator-tube decoder
- Address decoding—memory selection control

RCA CD4028AA types are BCD to decimal or binary to octal decoders consisting of pulse shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D results in a "high" level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in

▲ Formerly developmental type TA5873.

TABLE I — TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	1	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	1	0	0	0	0
0	1	1	1	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	0	0	0	0	1

WHERE 1 = HIGH LEVEL  
0 = LOW LEVEL

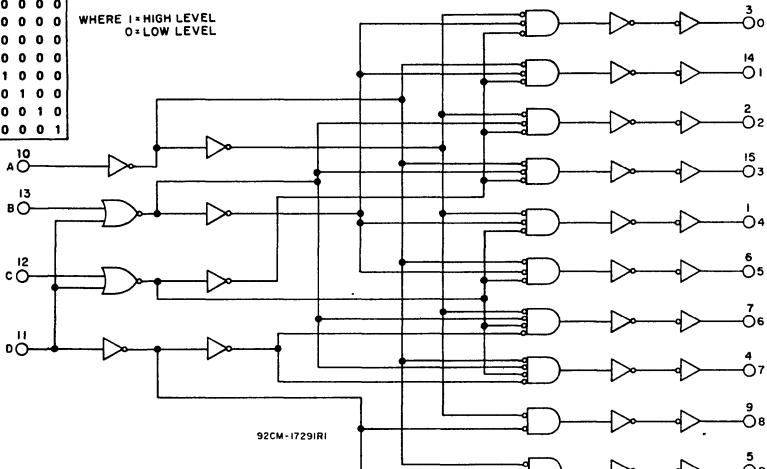
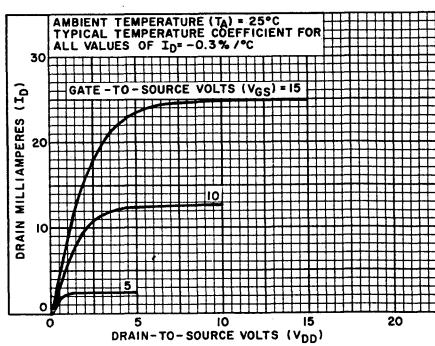


Fig.4-1 Logic diagram.

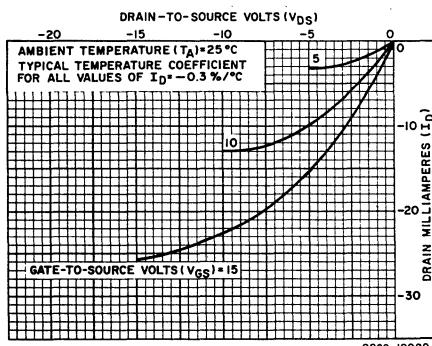
**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
			CD4028AD, CD4028AK, CD4028AF													
			$V_O$ Volts		$V_{DD}$ Volts		-55°C			25°C			125°C			
Quiescent Device Current	$I_L$		5	-	--		5	-	0.5	5	-	-	300	$\mu A$	4-8	
			10	-	-		10	-	1	10	-	-	600			
Quiescent Device Dissipation/Package	$P_D$		5	-	-		25	-	2.5	25	-	-	1500	$\mu W$		
			10	-	-		100	-	10	100	-	-	6000			
Output Voltage: Low-Level	$V_{OL}$		5	-	-		0.01	-	0	0.01	-	-	0.05	V		
			10	-	-		0.01	-	0	0.01	-	-	0.05			
High-Level	$V_{OH}$		5	4.99	-		4.99	5	-	4.95	-	-	-	V		
			10	9.99	-		9.99	10	-	9.95	-	-	-			
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	-	-	1.5	2.25	-	1.4	-	-	V	4-9	
			1	10	3.0	-	-	3	4.5	-	2.9	-	-			
	$V_{NH}$		4.2	5	1.4	-	-	1.5	2.25	-	1.5	-	-	V	4-9	
			9	10	2.9	-	-	3	4.5	-	3.0	-	-			
Output Drive Current:	$I_{DN}$		$V_O = 0.5$ V	5	0.75	-	-	0.6	1.2	-	0.45	-	-	mA	4-2	
			$V_O = 0.5$ V	10	1.5	-	-	1.2	2.4	-	0.9	-	-			
	$I_{DP}$		$V_O = 4.5$ V	5	-0.7	-	-	-0.45	-0.9	-	-0.32	-	-	mA	4-3	
			$V_O = 9.5$ V	10	-1.4	-	-	-0.95	-1.9	-	-0.65	-	-			
Input Current	$I_I$	Any Input		-	-	-	-	-	10	-	-	-	-	pA		

For Output Drive Current test connections see Appendix.



92CS-19098



92CS-19099

Fig.4-2 Typ. N-channel drain characteristics.

Fig.4-3 Typ. P-channel drain characteristics.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4028AE											
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C					
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		$\mu A$	4-8
	5	—	—	—	50	—	—	5	50	—	—	700			
Quiescent Device Dissipation/Package	$P_D$	10	—	—	—	100	—	—	10	100	—	—	1400		
		5	—	—	—	250	—	—	25	250	—	—	3500		
Output Voltage: Low-Level	$V_{OL}$	10	—	—	—	1000	—	—	100	1000	—	—	14,000		
		5	—	—	—	0.01	—	—	0	0.01	—	—	0.05		
High Level	$V_{OH}$	10	—	—	—	0.01	—	—	0	0.01	—	—	0.05		
		5	4.99	—	—	4.99	5	—	4.95	—	—	—	—		
Noise Immunity (Any Input)	$V_{NL}$	10	9.99	—	—	9.99	10	—	9.95	—	—	—	—		4-9
		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—		
Output Drive Current:	$I_{DN}$	1	10	3.0	—	—	3	4.5	—	2.9	—	—	—		4-2
		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—		
		9	10	2.9	—	—	3	4.5	—	3.0	—	—	—		
		$V_O = 0.5\text{ V}$	5	0.35	—	—	0.3	1.2	—	0.25	—	—	—		
P-Channel	$I_{DP}$	$V_O = 0.5\text{ V}$	10	0.7	—	—	0.6	2.4	—	0.5	—	—	—		4-3
		$V_O = 4.5\text{ V}$	5	-0.32	—	—	-0.22	-0.9	—	-0.18	—	—	—		
		$V_O = 9.5\text{ V}$	10	-0.65	—	—	-0.48	-1.9	—	-0.4	—	—	—		
		Any Input	—	—	—	—	-10	—	—	—	—	—	pA		

For Output Drive Current test connections see Appendix.

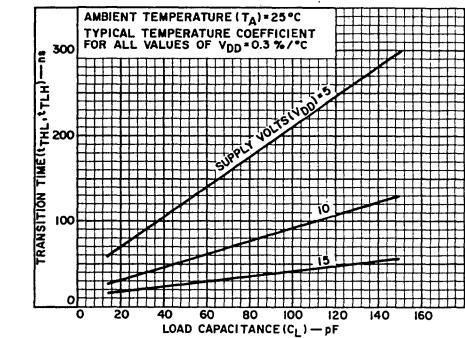
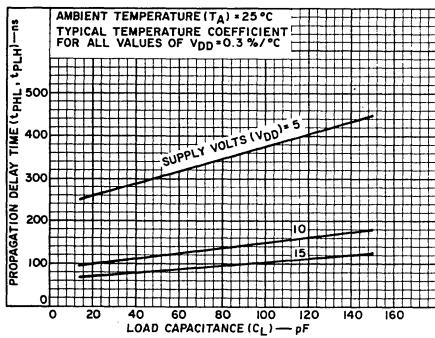


Fig.4-4 Typ. propagation delay time vs.  $C_L$ .

Fig.4-5 Typ. transition time vs.  $C_L$ .

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{ pF}$ , and all input rise and fall times = 20ns

Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\text{ }^\circ\text{C}$  (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS		
			CD4028AD CD4028 AF			CD4028AE						
			Min.	Typ.	Max.	Min.	Typ.	Max.				
Propagation Delay Time	$t_{PHL}$ $t_{PLH}$		5	—	250	480	—	250	700	ns	4-6	
			10	—	100	180	—	100	290			
Transition Time	$t_{THL}$ $t_{TLH}$		5	—	60	150	—	60	300	ns	4-5	
			10	—	30	75	—	30	150			
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—	

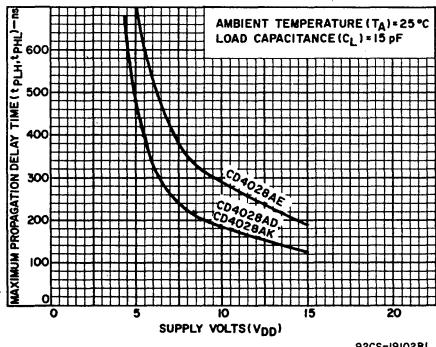


Fig.4-6 Max. propagation delay time vs.  $V_{DD}$ .

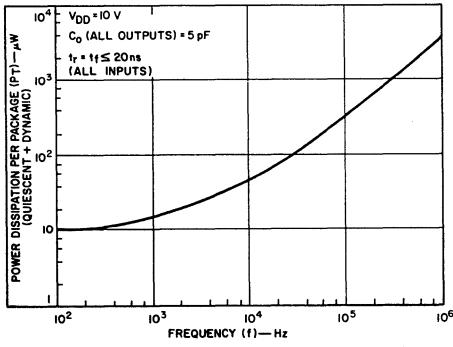


Fig.4-7 Dissipation vs. input frequency.

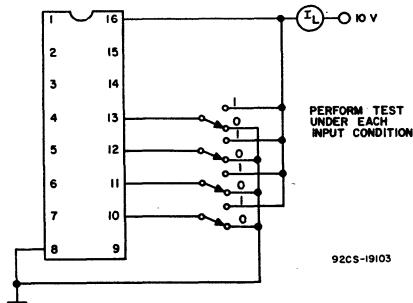


Fig.4-8 Quiescent device current test circuit.

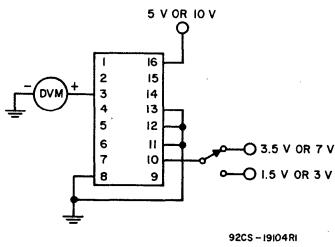


Fig.4-9 Noise-immunity test circuit.

## TYPICAL APPLICATIONS

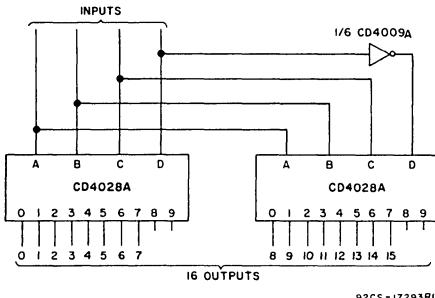


Fig.4-10 Code conversion circuit.

The circuit shown in Fig.4-10 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028A to select a particular output. For example: in order to get a "high" on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

TABLE 2 – CODE CONVERSION CHART.

INPUTS	INPUT CODES										OUTPUT NUMBER	
	Hexa Decimal					Decimal						
	D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	GRAY	HEXA	DECIMAL		
0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0	0 0 0 0	1 1 1 1	3 3 3 3	11 11 11 11	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
0 0 0 1 1 1 1 1 1 1 1 1	1	1	1	1	1 1 1 1	2 2 2 2	4 4 4 4	12 12 12 12	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
0 0 1 0 2 3 2 3 2 3 2 3	2	3	2	3	0 1 0 1	0 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
0 0 1 1 3 2 3 2 3 2 3 2	3	2	3	2	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
0 1 0 0 4 7 1 4 4 7 1 4	4	7	1	4	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
0 1 0 1 5 6 2 5 6 2 5 6	5	6	2	5	3 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
0 1 1 0 6 4 3 1 4 0 6 4	6	4	3	1	4 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
0 1 1 1 7 5 4 2 5 0 7 5	7	5	4	2	5 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 0 0 0 8 15 5 15 8 15 5	8	15	5	2	6 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 0 0 1 9 14 6 14 9 14 6	9	14	6	5	5 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 0 1 0 10 12 7 9 6 10 12	10	12	7	9	6 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 0 1 1 11 13 8 8 5 11 13	11	13	8	8	5 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 1 0 0 12 8 8 5 6 12 8 8	12	8	8	5	6 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 1 0 1 13 9 6 7 7 13 9 6	13	9	6	7	7 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 1 1 0 14 17 8 8 8 14 17 8	14	17	8	8	8 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 0		
1 1 1 1 15 10 7 9 9 15 10 7	15	10	7	9	9 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0		

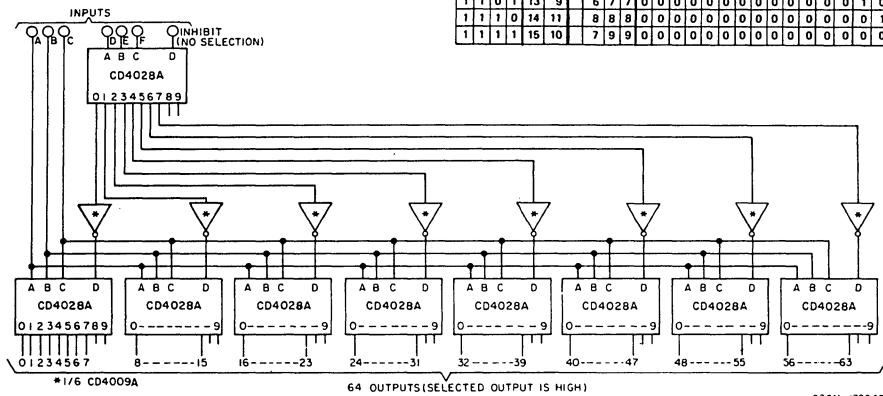
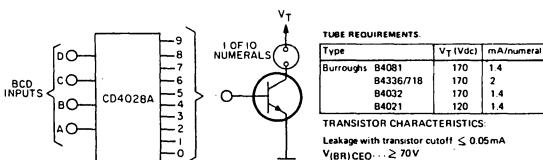


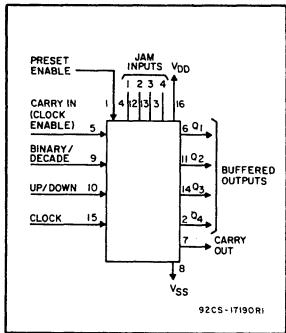
Fig.4-11 6-bit binary to 1 of 64 address decoder.



▲ (Trademark) Burrough Corp.

92CS - 17295RI

Fig.4-12 Neon readout (Nixie Tube▲) display application.

**CD4029AD, CD4029AE, CD4029AK**


## COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

### Special Features:

- Medium speed operation . . . 5 MHz (typ.) @  $C_L = 15 \text{ pF}$  and  $V_{DD} - V_{SS} = 10 \text{ V}$
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Up/Down decade counting
- Magnitude and sign generation
- Difference counting

RCA CD4029AA types consist of a four-stage binary or BCD-decade up/down counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Binary/Decade, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry Out signal are provided as outputs.

A "high" preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the clock. A "low" on each Jam line, when the Preset-Enable signal is "high", resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the Carry-In and Preset Enable signals are "low". Advancement is inhibited when the Carry-In or Preset Enable signals are "high". The carry-out signal is normally "high" and goes "low" when the counter

reaches its maximum count in the "Up" mode or the minimum count in the "Down" mode provided the Carry-In signal is "low". The Carry-In signal in the "low" state can thus be considered a "Clock Enable". The carry-in terminal must be connected to  $V_{SS}$  when not in use.

Binary counting is accomplished when the Binary/Decade input is "high"; the counter counts in the Decade mode when the Binary/Decade input is "low". The counter counts "Up" when the Up/Down input is "high", and "Down" when the Up/Down input is "low". Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 5-12. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

▲ Formerly developmental type TA5925.

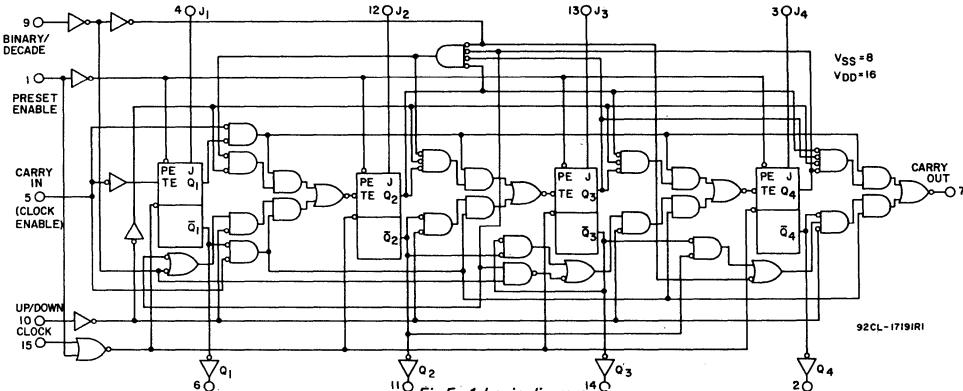


Fig.5-1 Logic diagram.

## Truth Tables

TRUTH TABLE FOR F-F No.1

J	CL	PE	T	E	J	Q	$\bar{Q}$
X	X	0	0	0	0	1	0
L	I	1	X	0	Q	0	1
X	X	0	1	1	0	0	1
L	0	1	X	0	Q	0	NC
J	X	1	X	0	Q	0	NC

NC - NO CHANGE

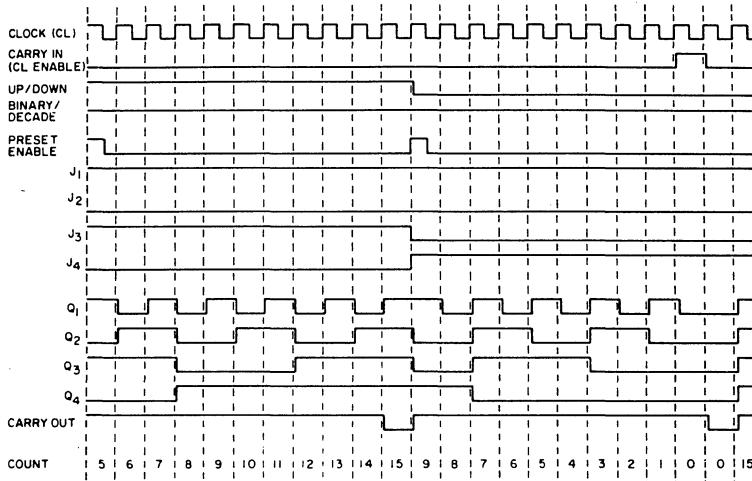
TE - TOGGLE ENABLE

X - DON'T CARE

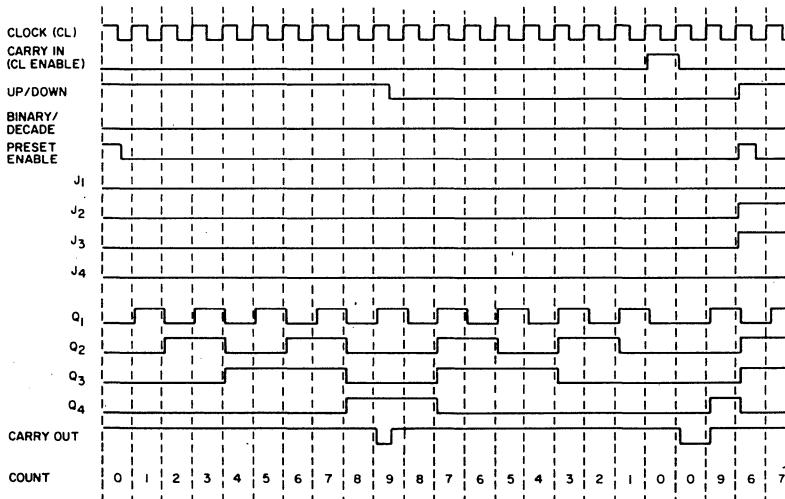
TRUTH TABLE FOR F-F's 2,3,4

PE	J	CL	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1	0
L	0	I	X	0	Q	0
X	X	0	1	1	0	1
L	I	I	X	0	Q	NC
J	X	I	X	Q	0	NC

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	I 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	I 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	I 0	JAM IN NO JAM
CARRY IN (CI) (CLOCK ENABLE)	I 0	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION
		ADVANCE COUNTER AT POS. CLOCK TRANSITION



92CM-17192



92CM-17193RI

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4029AD, CD4029AK										
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C				
Quiescent Device Current	$I_L$		5	—	—	5	—	0.3	5	—	—	300	$\mu A$	5-10
			10	—	—	10	—	0.5	10	—	—	600		
Quiescent Device Dissipation/Package	$P_D$		5	—	—	25	—	1.5	25	—	—	1500	$\mu W$	—
			10	—	—	100	—	5	100	—	—	6000		
Output Voltage: Low-Level	$V_{OL}$		5	—	—	0.01	—	—	0.01	—	—	0.05	$V$	—
			10	—	—	0.01	—	—	0.01	—	—	0.05		
High-Level	$V_{OH}$		5	4.99	—	—	4.99	5	—	4.95	—	—	$V$	—
			10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	$V$	5-11
			1.0	10	3.0	—	—	3	4.5	—	2.9	—		
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	$V$	—
			9.0	10	2.9	—	—	3	4.5	—	3.0	—		
Output Drive Current: N-Channel	$I_{DN}$		Q Outputs	0.5	5	0.5	—	—	0.4	0.8	—	0.28	$mA$	—
			Q Outputs	0.5	10	0.74	—	—	0.6	1.2	—	0.42		
			Carry Output	0.5	5	0.1	—	—	0.08	0.16	—	0.06	$mA$	—
			Carry Output	0.5	10	0.4	—	—	0.32	0.64	—	0.22		
P-Channel	$I_{DP}$		Q Outputs	4.5	5	-0.18	—	—	-0.12	-0.24	—	-0.08	$mA$	—
			Q Outputs	9.5	10	-0.3	—	—	-0.2	-0.4	—	-0.14		
			Carry Output	4.5	5	-0.09	—	—	-0.06	-0.12	—	-0.04	$mA$	—
			Carry Output	9.5	10	-0.15	—	—	-0.1	-0.2	—	-0.07		
Input Current	$I_I$	Any Input	—	—	—	—	—	10	—	—	—	—	$pA$	—

For Output Drive Current test connections see Appendix.

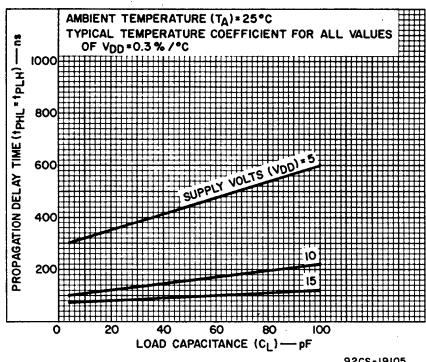


Fig.5-4 Typ. propagation delay time vs.  $C_L$  for  $Q$  outputs.

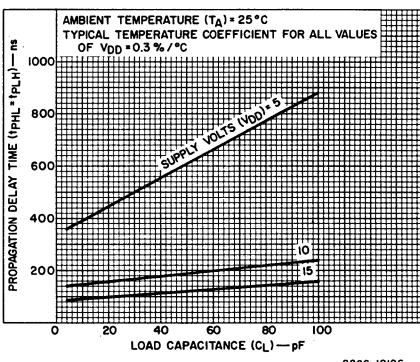


Fig.5-5 Typ. propagation delay time vs.  $C_L$  for carry output.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_O$ Volts	$V_{DD}$ Volts	LIMITS								UNITS	CHARAC- TERIS- TIC CURVES & TEST CIRCUITS Fig. No.			
				CD4029AE												
				-40°C			25°C			85°C						
Quiescent Device Current	$I_L$			5	—	—	50	—	0.5	50	—	—	700	$\mu A$	5-10	
				10	—	—	100	—	1	100	—	—	1400			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	2.5	250	—	—	3500	$\mu W$	—	
				10	—	—	1000	—	10	1000	—	—	14000			
Output Voltage: Low-Level	$V_{OL}$			5	—	—	0.01	—	—	0.01	—	—	0.05	$V$	—	
				10	—	—	0.01	—	—	0.01	—	—	0.05			
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	$V$	—	
				10	9.99	—	—	9.99	10	—	9.95	—	—			
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	$V$	5-11	
			1.0	10	3.0	—	—	3	4.5	—	2.9	—	—			
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	$V$	—	
			9.0	10	2.9	—	—	3	4.5	—	3.0	—	—			
Output Drive Current: N-Channel	$I_D^N$	Q Outputs	0.5	5	0.24	—	—	0.2	0.8	—	0.16	—	—	$mA$	—	
			0.5	10	0.36	—	—	0.3	1.2	—	0.24	—	—			
		Carry Output	0.5	5	0.05	—	—	0.04	0.16	—	0.03	—	—	$mA$	—	
		Carry Output	0.5	10	0.19	—	—	0.16	0.64	—	0.13	—	—			
P-Channel	$I_D^P$	Q Outputs	4.5	5	-0.07	—	—	-0.06	-0.24	—	-0.05	—	—	$mA$	—	
			9.5	10	-0.14	—	—	-0.1	-0.4	—	-0.08	—	—			
		Carry Output	4.5	5	-0.04	—	—	-0.03	-0.12	—	-0.02	—	—	$mA$	—	
		Carry Output	9.5	10	-0.07	—	—	-0.05	-0.2	—	-0.04	—	—			
Input Current	$I_I$	Any Input	—	—	—	—	—	10	—	—	—	—	—	$pA$	—	

For Output Drive Current test connections see Appendix.

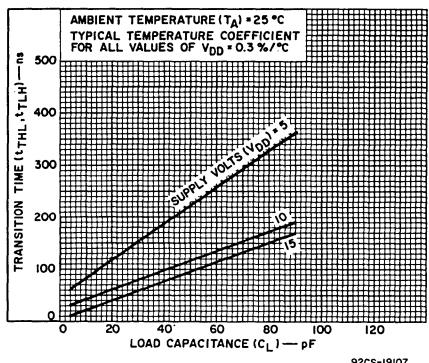


Fig.5-6 Typ. transition time vs.  $C_L$  for  $Q$  outputs.

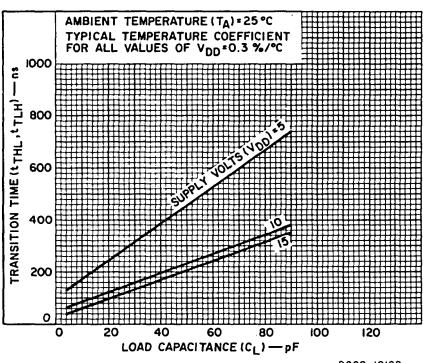


Fig.5-7 Typ. transition time vs.  $C_L$  for carry output.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = \text{OV}$ ,  $C_L = 15\text{ pF}$ , and input rise and fall times = 20ns, except  $t_rCL$  and  $t_fCL$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS		
			CD4029AD, CD4029AK			CD4029AE								
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.					
<b>CLOCKED OPERATION</b>														
Propagation Delay Time: Q Outputs	$t_{PHL}, t_{PLH}$		5	—	325	650	—	325	1300	ns	5-4			
			10	—	115	230	—	115	460					
Carry Output	$t_{THL}, t_{TLH}$		5	—	425	850	—	425	1700	ns	5-5			
			10	—	150	300	—	150	600					
Transition Time: Q Outputs	$t_{THL}, t_{TLH}$		5	—	100	200	—	100	400	ns	5-6			
			10	—	50	100	—	50	200					
Carry Output	$t_{THL}, t_{TLH}$		5	—	200	400	—	200	800	ns	5-7			
			10	—	100	200	—	100	400					
Minimum Clock Pulse Width	$t_{WL}, t_{WH}$		5	—	200	340	—	200	500	ns	—			
			10	—	100	170	—	100	250					
Clock Rise & Fall Time	$t_rCL, ** t_fCL$		5	—	—	15	—	—	15	$\mu\text{s}$	—			
			10	—	—	15	—	—	15					
Set-Up Times*	$t_{SHL}, t_{SLH}$		5	—	325	650	—	325	1300	ns	—			
			10	—	115	230	—	115	460					
Maximum Clock Frequency	$f_{CL}$		5	1.5	2.5	—	1	2.5	—	MHz	5-8			
			10	3	5	—	2	5	—					
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—	—		
<b>PRESET ENABLE</b>														
Propagation Delay Time: Q Outputs	$t_{PHL}, t_{PLH}$		5	—	325	650	—	325	1300	ns	—			
			10	—	115	230	—	115	460					
Carry Output	$t_{PLH}$		5	—	425	850	—	425	1700	ns	—			
			10	—	150	300	—	150	600					
Minimum Preset Enable Pulse Width	$t_{WH}$		5	—	115	330	—	115	660	ns	—			
			10	—	80	160	—	80	320					
Minimum Preset Enable Removal Time	$t_{removal}$		5	—	325	650	—	325	1300	ns	—			
			10	—	115	230	—	115	460					
<b>CARRY INPUT</b>														
Propagation Delay Time: Carry Output	$t_{PHL}, t_{PLH}$		5	—	175	350	—	175	700	ns	—			
			10	—	50	100	—	50	200					

\*From Up/Down, Binary/Decade or Carry Input Control Inputs to Clock Input.

\*\*If more than one unit is cascaded in the parallel clocked application,  $t_fCL$  should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

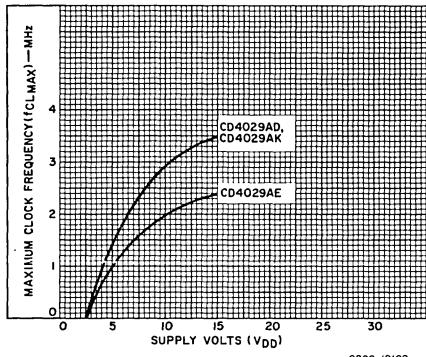
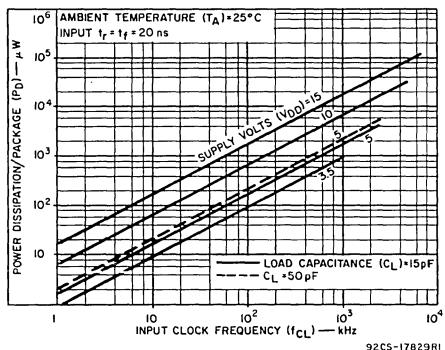
Fig.5-8 Max. clock frequency vs.  $V_{DD}$ .

Fig.5-9 Typ. dissipation characteristics.

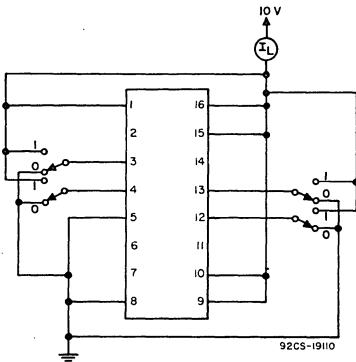


Fig.5-10 Quiescent device current test circuit.

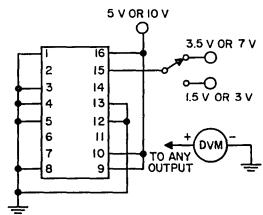
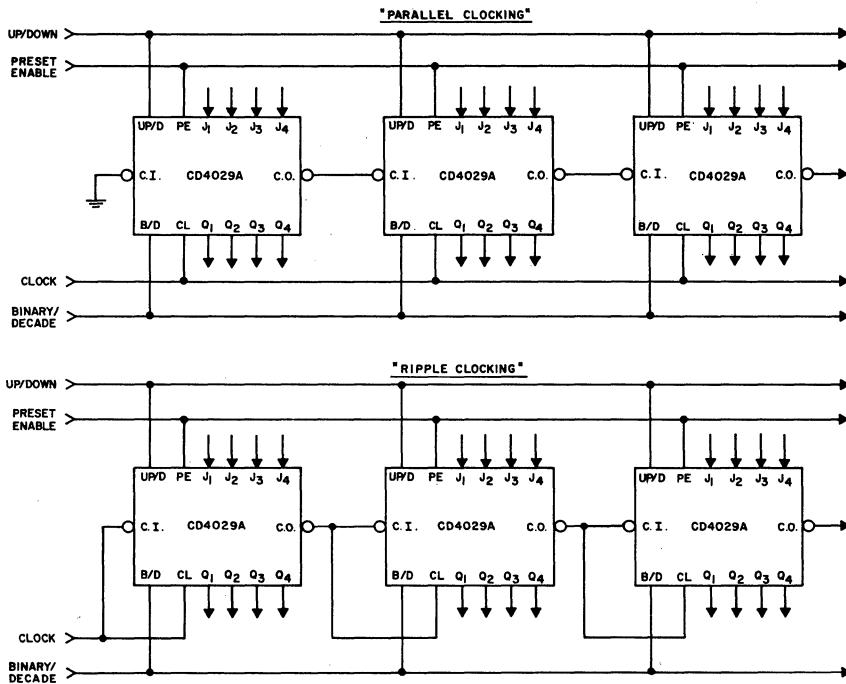


Fig.5-11 Noise-immunity test circuit.



The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be "high".

92CL-I7194R2

Fig.5-12 Cascading counter packages.

The CD4029A "Clock" and "Up/Down" inputs are used directly in most applications. In applications where "Clock Up" and "Clock Down" inputs are provided, conversion to the CD4029A "Clock" and "Up/Down" inputs can easily be realized by use of the circuit shown below.

CD4029A changes count on positive transitions of "Clock Up" or "Clock Down" inputs. For the gate configuration shown below, when counting "up" the "Clock Down" input must be maintained "high" and conversely when counting "down" the "Clock Up" input must be maintained "high".

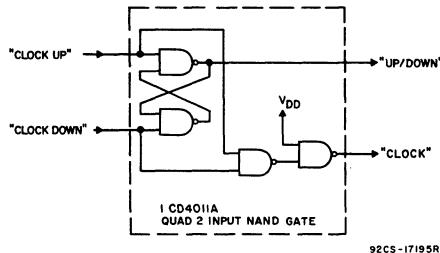


Fig.5-13 Conversion of "clock up", "clock down" input signals to "clock" and "up/down" input signals.

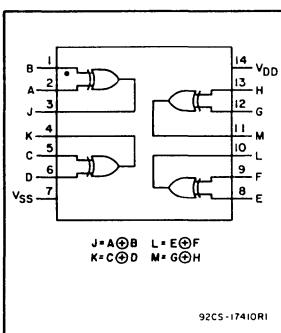


# Digital Integrated Circuits

Monolithic Silicon

CD4030AD, CD4030AF

CD4030AE, CD4030AK



RCA CD4030A types each contains four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four N-channel and four P-channel enhancement-type transistors.

All inputs and outputs are protected against electrostatic effects.

▲ Formerly developmental type TA5940.

TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL  
"0" = LOW LEVEL

Fig. 6-1 Schematic diagram for 1 of 4 identical exclusive-OR gates.

## TYPICAL APPLICATIONS

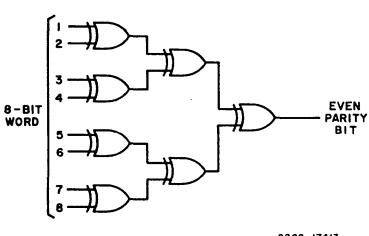


Fig. 6-2a Even-parity-bit generator (1-3/4 x CD4030A).

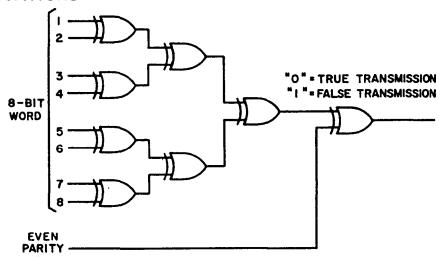


Fig. 6-2b Even-parity checker (2 x CD4030A).

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.					
				CD4030AD, CD4030AK, CD4030AF													
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C							
Quiescent Device Current	$I_L$			5	—	0.5	—	0.005	0.5	—	—	30	$\mu A$	6-11			
				10	—	1	—	0.01	1	—	—	60					
Quiescent Device Dissipation/Package	$P_D$			5	—	2.5	—	0.025	2.5	—	—	150	$\mu W$				
				10	—	10	—	0.1	10	—	—	600					
Output Voltage: Low-Level	$V_{OL}$			5	—	0.01	—	0	0.01	—	—	0.05	V				
				10	—	0.01	—	0	0.01	—	—	0.05					
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	V				
				10	9.99	—	—	9.99	10	—	9.95	—					
Noise Immunity (All Inputs)	$V_{NL}$	0.95	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	6-12			
		2.9	10	3.0	—	—	3	4.5	—	2.9	—	—					
	$V_{NH}$	3.6	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V				
		7.2	10	2.9	—	—	3	4.5	—	3.0	—	—					
Output Drive Current:	$I_{DN}$	0.5	5	0.75	—	—	0.6	1.2	—	0.45	—	—	mA	6-3			
		0.5	10	1.5	—	—	1.2	2.4	—	0.9	—	—					
P-Channel		4.5	5	-0.45	—	—	-0.3	-0.6	—	-0.21	—	—	mA	6-4			
		9.5	10	-0.95	—	—	-0.65	-1.3	—	-0.45	—	—					
Input Current	$I_I$	$V_I = OV$ or $V_I = V_{DD}$	—	—	—	—	10	—	—	—	—	—	pA	—			

For Output Drive Current test connections see Appendix.

**TYPICAL APPLICATIONS (Cont'd)**

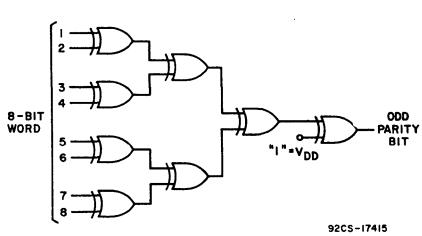


Fig.6-2c Odd-parity-bit generator (2 x CD4030A).

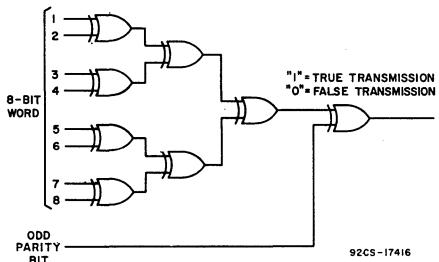


Fig.6-2d Odd-parity checker (2 x CD4030A)..

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_1 \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4030AE								
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			UNITS		
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	$\mu A$		
	5	—	—	5	—	0.05	5	—	—	70		
Quiescent Device Dissipation/Package	$P_D$	10	—	—	10	—	0.1	10	—	—	140	$\mu W$
		5	—	—	25	—	0.25	25	—	—	350	
Output Voltage: Low-Level	$V_{OL}$	10	—	—	100	—	1	100	—	—	1400	$\mu V$
		5	—	—	0.01	—	0	0.01	—	—	0.05	
High-Level	$V_{OH}$	10	—	—	0.01	—	0	0.01	—	—	0.05	$\mu V$
		5	4.99	—	—	4.99	5	—	4.95	—	—	
Noise Immunity (All Inputs)	$V_{NL}$	10	—	—	9.99	—	9.99	10	—	9.95	—	$\mu V$
		5	—	—	9.99	—	9.99	10	—	9.95	—	
	$V_{NH}$	2.9	10	3.0	—	—	3	4.5	—	2.9	—	$\mu V$
		3.6	5	1.4	—	—	1.5	2.25	—	1.5	—	
	$I_{DN}$	7.2	10	2.9	—	—	3	4.5	—	3.0	—	$mA$
		0.5	5	0.35	—	—	0.3	1.2	—	0.25	—	
Output Drive Current: N-Channel	$I_{DP}$	0.5	10	0.7	—	—	0.6	2.4	—	0.5	—	$mA$
		4.5	5	-0.21	—	—	-0.15	-0.6	—	-0.12	—	
P-Channel	$I_{DN}$	9.5	10	-0.45	—	—	-0.32	-1.3	—	-0.25	—	$mA$
		4.5	5	-0.21	—	—	-0.15	-0.6	—	-0.12	—	
Input Current	$I_I$	$V_I = OV$ or $V_I = V_{DD}$		—	—	—	—	10	—	—	—	pA

For Output Drive Current test connections see Appendix.

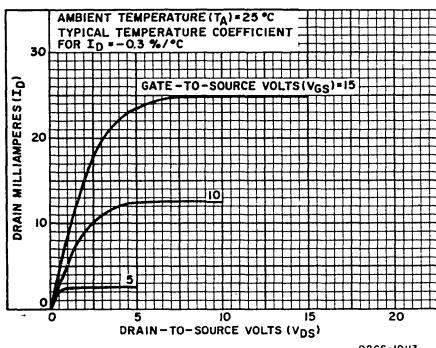


Fig.6-3 Typ. N-channel drain characteristics.

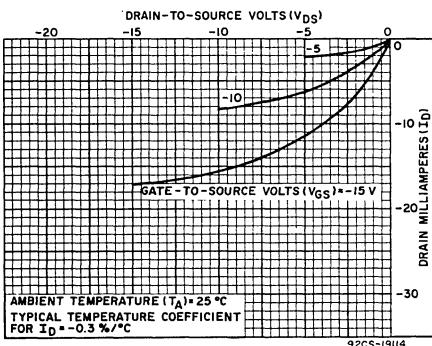
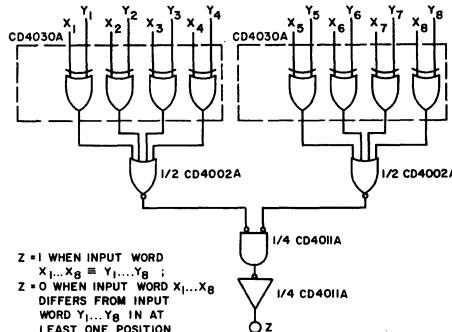


Fig.6-4 Typ. P-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = \text{OV}$ ,  $C_L = 15\text{pF}$ , and all input rise and fall times = 20ns

Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\text{/}^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	
			CD4030AD, AK, AF			CD4030AE					
			V <sub>DD</sub> (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time	$t_{PHL}$ , $t_{PLH}$		5	100	200		100	300		ns	6-7 6-9
			10	40	100		40	150			
Transition Time: High-to-Low Level	$t_{THL}$		5	70	150		70	300		ns	6-8
			10	25	75		25	150			
Low-to-High Level	$t_{TLH}$		5	80	150		80	300		ns	6-8
			10	30	75		30	150			
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—



92CS-17417R2

Fig.6-5 8-bit comparator.

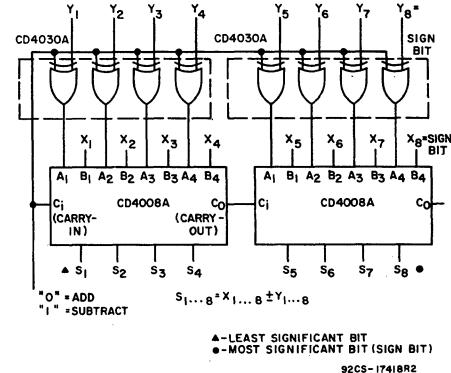


Fig.6-6 8-bit two's complement adder-subtractor.

TABLE I - TWO'S COMPLEMENT NUMBERS AND THEIR EQUIVALENT DECIMAL VALUES.

$x_8$	$x_7$	$x_6$	$x_5$	$x_4$	$x_3$	$x_2$	$x_1$		$x_8$	$x_7$	$x_6$	$x_5$	$x_4$	$x_3$	$x_2$	$x_1$	
0	0	0	0	0	0	0	0	= 0	1	1	1	1	1	1	1	1	= -1
0	0	0	0	0	0	0	1	= 1	1	1	1	1	1	1	1	0	= -2
0	0	0	0	0	0	1	0	= 2	1	1	1	1	1	1	0	1	= -3
0	0	0	0	0	0	1	1	= 3	1	1	1	1	1	1	0	0	= -4
...	...	...	...	...	...	...	...	...	1	1	1	1	1	1	0	1	= -5
...	...	...	...	...	...	...	...	...	1	1	1	1	1	1	1	0	...
0	1	1	1	1	1	1	0	= 126	1	0	0	0	0	0	0	1	= -127
0	1	1	1	1	1	1	1	= 127	1	0	0	0	0	0	0	0	= -128

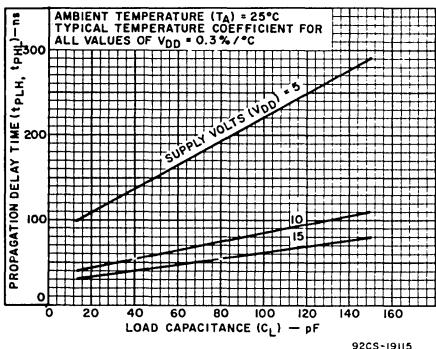
The Two's complement adder - subtractor can add or subtract any two of the numbers in Table I. For example:

a)  $+2 =$

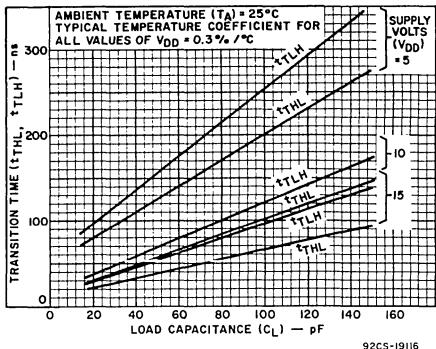
SIGN BIT	0	0	0	0	0	1	0	2 +
y	1	1	1	1	0	1	1	- 5 +
c <sub>i</sub>								+
s	0	1	1	1	1	0	1	- 3

b)  $-2 =$

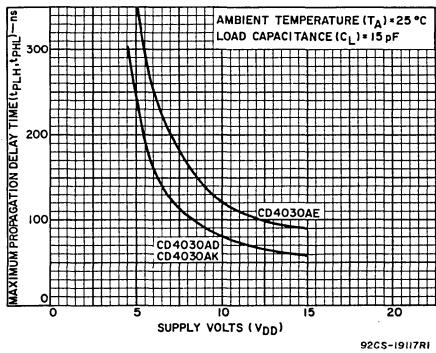
SIGN BIT	1	1	1	1	1	1	0	- 2 +
y	1	1	1	1	0	1	1	- 5 +
c <sub>i</sub>	0	0	0	0	1	0	0	+
s	1	1	1	1	1	0	1	- 3



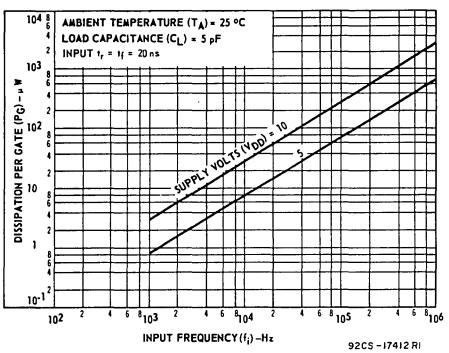
*Fig.6-7 Typ. propagation delay time vs.  $C_L$ .*



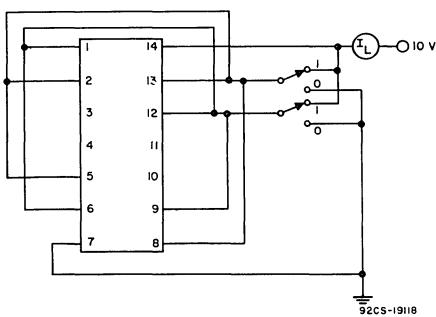
*Fig. 6-8 Typ. transition time vs.  $C_L$ .*



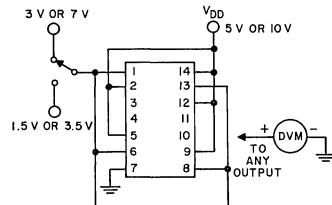
*Fig. 6-9 Max. propagation delay time vs.  $V_{DD}$ .*



*Fig. 6-10 Dissipation vs. input frequency.*



*Fig.6–11 Quiescent device current test circuit.*

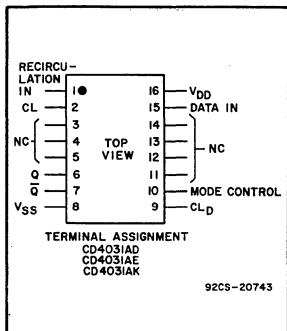


*Fig.6-12 Noise-immunity test circuit.*



# Digital Integrated Circuits

Monolithic Silicon

**CD4031AD CD4031AE  
CD4031AK**


## COS/MOS 64-Stage Static Shift Register

### Applications:

For use in digital equipment where low-power dissipation, low package count, and/or high noise immunity are primary design requirements.

- Serial shift registers
- Time delay circuits

RCA CD4031A\* is a 64-stage static shift register in which each stage is a D-type, master-slave flip-flop.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 2 Megahertz can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the "low" or "high" state. The CD4031A has a mode control input that, when in the "high" state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high speed operation. Alternatively, a delayed clock output ( $CL_D$ ) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements.

Data ( $Q$ ) and Data ( $\bar{Q}$ ) outputs are provided from the 64th register stage. The Data ( $Q$ ) output is capable of driving one TTL or DTL load.

\*Formerly Dev. No. TA5989.

### MAXIMUM RATINGS, Absolute Maximum Values:

Storage-Temperature Range . . . . .	-65°C to +150°C
Operating-Temperature Range . . . . .	-55°C to +125°C
Ceramic packages . . . . .	-55°C to +125°C
Plastic package . . . . .	-40°C to +85°C
DC Supply Voltage Range ( $V_{DD} - V_{SS}$ ) . . . . .	-0.5 to +15 V
Device Dissipation (per package) . . . . .	200 mW
All Inputs . . . . .	$V_{SS} \leq V_I \leq V_{DD}$
Recommended DC Supply . . . . .	$3 \text{ to } 15 \text{ V}$
Voltage Range ( $V_{DD} - V_{SS}$ ) . . . . .	$V_{DD} \text{ to } V_{SS}$
Recommended Input Voltage Swing . . . . .	

### Features:

- Fully static operation: DC to 4 MHz @  $V_{DD} - V_{SS} = 10\text{V}$
- Operation from a single 3 to 15 V positive or negative power supply
- High noise immunity
- Microwatt quiescent power dissipation:  $10 \mu\text{W}$  (typ.) for ceramic packages;  $100 \mu\text{W}$  (typ.) for plastic packages
- Full military operating temperature range: -55°C to +125°C (Ceramic Pkg.)
- Single phase clocking requirements
- Protection against electrostatic effects on all inputs
- Data compatible with TTL-DTL
- Recirculation capability
- Two cascading modes:  
    Direct clocking for high-speed operation  
    Delayed clocking for reduced clock drive requirements

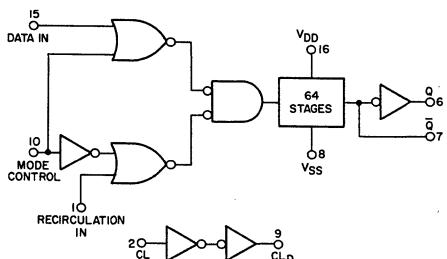


Fig. 1—Functional diagram.

92CS-19745

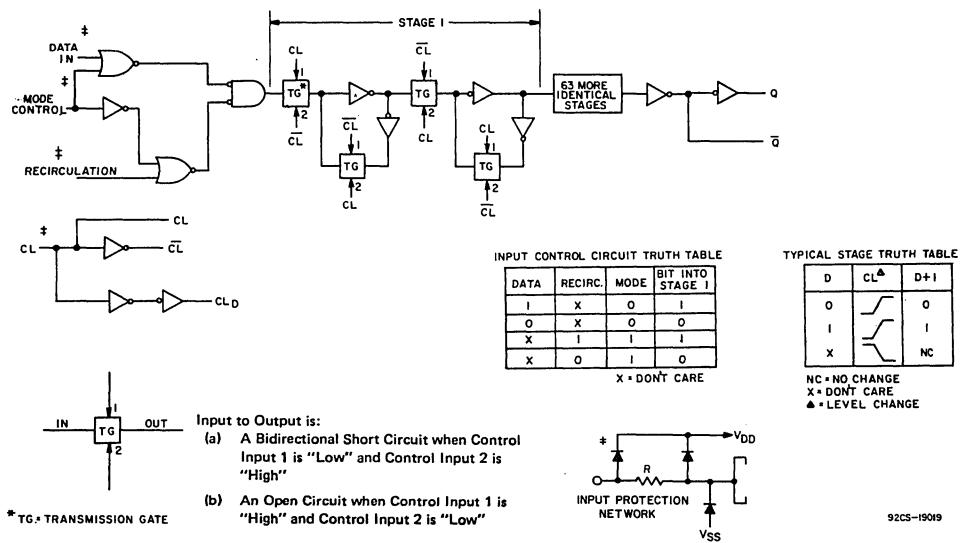


Fig. 2—CD4031A logic diagram and truth tables.

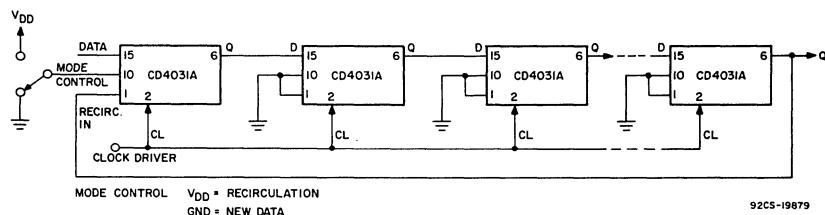


Fig. 3—Cascading using direct clocking for high speed operation (see clock rise &amp; fall time requirement).

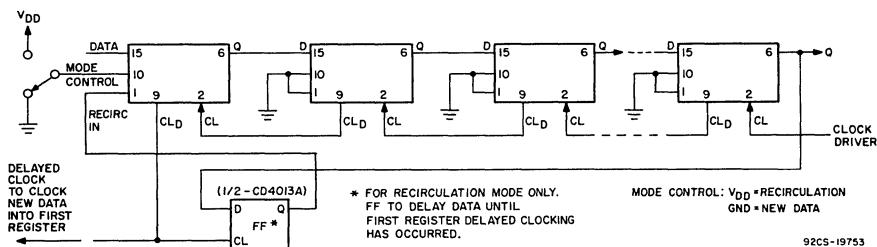


Fig. 4—Cascading using delayed clocking for reduced clock drive requirements.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			CD4031AD, CD4031AK									CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS	
		$V_D$ Volts	$V_{DD}$ Volts	-55°C			25°C			125°C						
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Device Current	$I_L$			5	—	10	—	0.5	10	—	—	600	$\mu A$	13		
				10	—	25	—	1	25	—	—	1500				
Quiescent Device Dissipation/Package	$P_D$			5	—	50	—	2.5	50	—	—	3000	$\mu W$	..		
				10	—	250	—	10	250	—	—	15000				
Output Voltage: Low-Level	$V_{OL}$			5	—	0.01	—	0	0.01	—	—	0.05	V	..		
				10	—	0.01	—	0	0.01	—	—	0.05				
High-Level	$V_{OH}$			5	4.99	—	4.99	5	—	4.95	—	—	V	..		
				10	9.99	—	9.99	10	—	9.95	—	—				
Noise Immunity (All Inputs)	$V_{NL}$			0.8	5	1.5	—	1.5	2.25	—	1.4	—	V	..		
				1.0	10	3	—	3	4.5	—	2.9	—				
For Definition See Appendix *	$V_{NH}$			4.2	5	1.4	—	1.5	2.25	—	1.5	—	V	..		
				9.0	10	2.9	—	3	4.5	—	3	—				
Output Drive Current: N-Channel	$I_{DN}$	Q	0.4	4.5	1.6	—	—	1.3	2.6	—	0.91	—	mA	..		
			0.5	10	5	9.6	—	4	8	—	3.2	5.6				
			0.5	5	0.11	—	—	0.09	0.18	—	0.06	—				
			0.5	10	0.24	—	—	0.2	0.4	—	0.14	—				
		$\bar{Q}$	0.5	5	0.48	—	—	0.4	0.8	—	0.28	—				
			0.5	10	1.5	—	—	1.2	2.4	—	0.84	—				
		$CL_D$	4.5	5	-0.4	—	—	-0.32	-0.64	—	-0.22	—		mA	..	
			9.5	10	-0.85	—	—	-0.70	-1.4	—	-0.49	—				
			4.5	5	-0.11	—	—	-0.09	-0.18	—	-0.06	—				
			9.5	10	-0.24	—	—	-0.20	-0.4	—	-0.14	—				
P-Channel	$I_{DP}$	$\bar{Q}$	4.5	5	-0.48	—	—	-0.40	-0.8	—	-0.28	—	mA	..		
			9.5	10	-1.0	—	—	-0.80	-1.6	—	-0.56	—				
		$CL_D$	4.5	5	-0.48	—	—	-0.40	-0.8	—	-0.28	—				
			9.5	10	-1.0	—	—	-0.80	-1.6	—	-0.56	—				
Input Current	$I_I$	Any Input			—	—	—	10	—	—	—	—	pA	—		

\* For "Q" and " $\bar{Q}$ " outputs use MSI Outputs Limits; for  $CL_D$  output use Gate Output Limits.

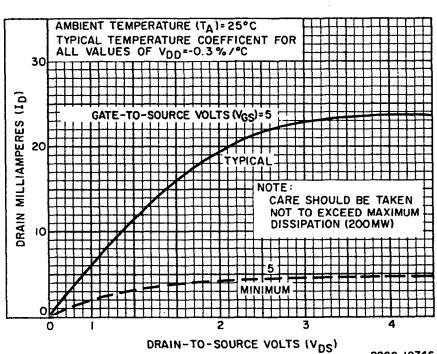


Fig. 5—Typical & minimum N-channel drain characteristics for Q output.

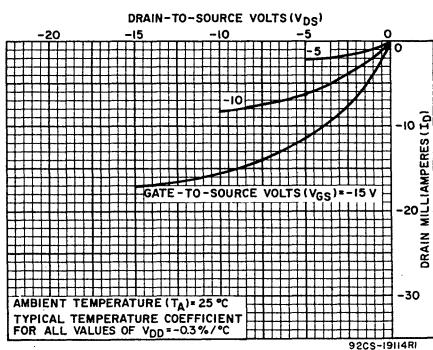
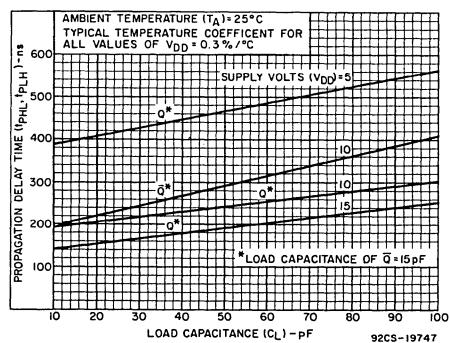


Fig. 6—Typical P-channel drain characteristics for Q output.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4031AE								CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS	
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C				
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	$I_L$			5 10	- -	50 100	- --	1 2	50 100	- -	700 1400	μA	13	
Quiescent Device Dissipation/Package	$P_D$			5 10	- -	250 1000	- -	5 20	250 1000	- -	3500 14000	μW	-	
Output Voltage: Low-Level	$V_{OL}$			5 10	- -	0.01 0.01	- -	0 0	0.01 0.01	- -	0.05 0.05	V	-	
High-Level	$V_{OH}$			5 10	4.99 9.99	- -	4.99 9.99	5 10	- -	4.95 9.95	- -	V	-	
Noise Immunity (All Inputs)	$V_{NL}$	0.8 1.0	5 10	1.5 3	- -	- -	1.5 3	2.25 4.5	- -	1.4 2.9	- -	V	14	
For Definition See Appendix *	$V_{NH}$	4.2 9.0	5 10	1.4 2.9	- -	- -	1.5 3	2.25 4.5	- -	1.5 3	- -	V		
Output Drive Current: N-Channel	$I_{DN}$	Q 0.4 0.5	4.5 10 5	1.6 9.6	- -	- 4	1.3 8	2.6 3.2	- -	1.05 6.4	- -	mA	5	
		Q 0.5 0.5	5 10	0.05 0.12	- -	- -	0.045 0.1	0.18 0.4	- -	0.037 0.08	- -			
		CLD 0.5 0.5	5 10	0.24 0.75	- -	- -	0.2 0.6	0.8 2.4	- -	0.16 0.5	- -			
P-Channel	$I_{DP}$	Q 4.5 9.5	5 10	-0.20 -0.42	- -	- -	-0.16 -0.35	-0.64 -1.4	- -	-0.13 -0.29	- -	mA	6	
		Q 4.5 9.5	5 10	-0.05 -0.12	- -	- -	-0.045 -0.10	-0.18 -0.4	- -	-0.037 -0.08	- -			
		CLD 4.5 9.5	5 10	-0.24 -0.5	- -	- -	-0.20 -0.40	-0.8 -1.6	- -	-0.16 -0.32	- -			
Input Current	$I_I$	Any Input	-	-	-	-	10	-	-	-	-	pA	--	

\* For "Q" and "Q̄" outputs use MSI Outputs Limits; for CLD output use Gate Output Limits.



\* LOAD CAPACITANCE OF  $\bar{Q} \geq 15$  pF

Fig. 7—Typical propagation delay time vs.  $C_L$  for data outputs.

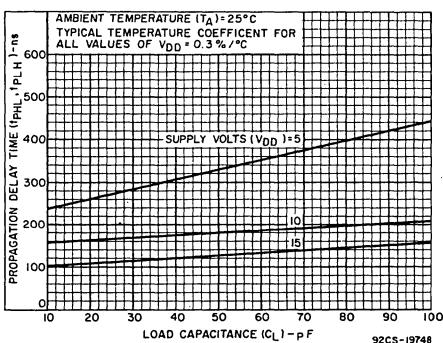


Fig. 8—Typical propagation delay vs.  $C_L$  for delayed clock output.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{ pF}$  (unless otherwise specified), and input rise and fall times = 20 ns, except  $t_{fCL}$  and  $t_{fCL}$ .

Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

Characteristics	Symbols	Test Conditions		Limits						Units	Characteristic Curves and Test Circuits		
			$V_{DD}$ Volts	CD4031AD, CD4031AK,			CD4031AE						
				Min.	Typ.	Max.	Min.	Typ.	Max.				
Propagation Delay Clock to Data Output Q & $\bar{Q}^*$	$t_{PHL}$		$C_L = 60\text{ pF}$	5	400	800	400	1600	1600	ns	7		
				10	200	400	200	800	800				
Clock to $C_{LD}$	$t_{PLH}$			5	400	800	400	1600	1600	ns	8		
				10	200	400	200	800	800				
Transition Time: Q Output	$t_{THL}$		$C_L = 60\text{ pF}$	5	75	150	75	300	300	ns	9		
				10	30	60	30	120	120				
$\bar{Q}$ Output	$t_{TLH}$			5	300	600	300	1200	1200	ns	10		
				10	150	300	150	600	600				
$C_{LD}$ Output			$C_L = 60\text{ pF}$	5	200	400	200	800	800	ns	10		
				10	100	200	100	400	400				
Clock Rise & Fall Time**	$t_{fCL}$ , $t_{fCL}$			5		2		2	2	$\mu\text{s}$			
				10		1		1	1				
Set-Up Time	$t_{SHL}$ , $t_{SLH}$			5	200	400	200	800	800	ns			
				10	50	100	50	200	200				
Data Overhang Time	$t_{DO}$			5	0	0		0	0	ns			
				10	20	50	20	50	50				
Maximum Clock*** Frequency	$f_{CL}$			5	0.8	2	0.4	2	2	MHz	11		
				10	2	4	1	4	4				
Input Capacitance: Clock	$C_I$					60		60	60	pF			
						5		5	5				

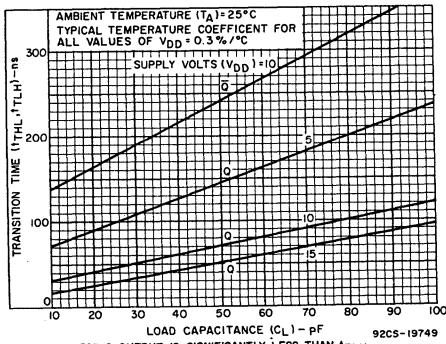
\*Capacitive loading on  $\bar{Q}$  output affects propagation delay of Q output. These limits apply for  $\bar{Q}$  load  $C_L \leq 15\text{ pF}$ .

\*\*If more than one unit is cascaded in the parallel clocked application,  $t_{fCL}$  should be made less than or equal to the sum of the propagation delay at 15pF and the transition time of the output driving stage.

\*\*\*Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature —  $f_{max} = \frac{1}{(n-1) C_{LD} \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$  where  $n$  = number of packages

b) Not Using Delayed Clock —  $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$



NOTE:  $t_{THL}$  FOR Q OUTPUT IS SIGNIFICANTLY LESS THAN  $t_{TLH}$

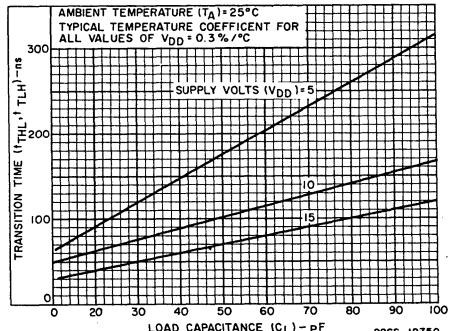
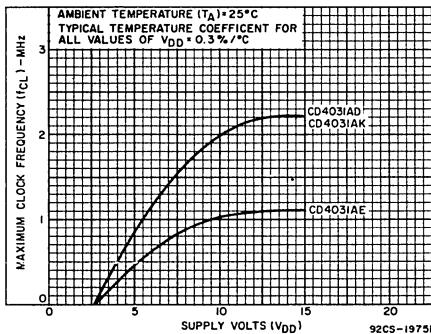
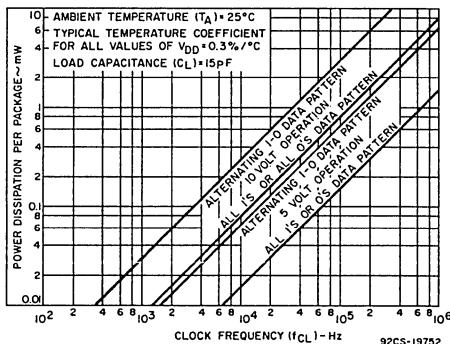


Fig. 9—Typical transition time vs.  $C_L$  for data outputs.

Fig. 10—Typical transition time vs.  $C_L$  for delayed clock output.

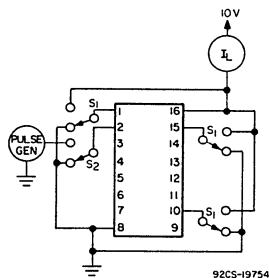


*Fig. 11—Maximum clock frequency vs.  
 $V_{DD}$ .*



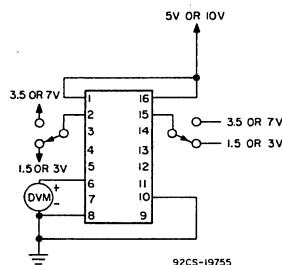
*Fig. 12—Typical power dissipation vs. frequency.*

## TEST CIRCUITS



WITH  $S_1$  AT GROUND, CLOCK UNIT 64 TIMES BY CONNECTING  $S_2$  TO PULSE GENERATOR. RETURN  $S_2$  TO GND AND MEASURE LEAKAGE CURRENT. REPEAT WITH  $S_1$  AT  $V_{DD}$ .

*Fig. 13—Quiescent device current.*



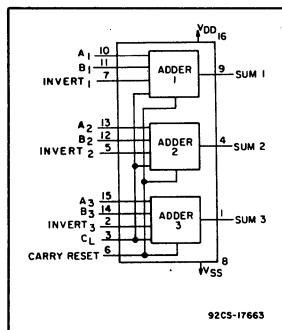
*Fig. 14—Noise immunity.*



# Digital Integrated Circuits

Monolithic Silicon

## CD4032A, CD4038A Types



### COS/MOS Triple Serial Adder

Positive Logic Adder — CD4032AD, CD4032AE, CD4032AK  
Negative Logic Adder— CD4038AD, CD4038AE, CD4038AK

#### Special Features:

- Invert inputs on all adders for sum complementing applications
- Fully static operation. ....dc to 5 MHz (typ.)
- Buffered outputs
- Single-phase clocking
- Microwatt quiescent power dissipation. ....5  $\mu$ W (typ.)

RCA CD4032A▲ and CD4038A types consist of three serial adder circuits with common clock and carry-reset inputs. Each adder has provisions for two serial data input signals and an invert command signal which, when a logical "1" complements the sum. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032A or at the negative going clock for the CD4038A, thus, for spike free operation the input data transitions should occur as soon as possible after the triggering edge.

The carry is reset to a logical "0" at the end of each word by applying a logical "1" signal to a carry-reset input one

#### Applications:

- Serial arithmetic units
- Digital correlators
- Digital datalink computers
- Flight control computers
- Digital servo control systems

bit-position before the application of the first bit of the next word Fig. 7-2 and 7-4 shows definitive waveforms for all input and output signals.

▲ Formerly developmental type TA5963.

For maximum ratings, see page 22.

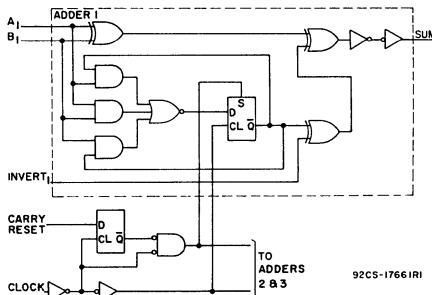


Fig.7-1 CD4032A logic diagram of one of three serial adders.

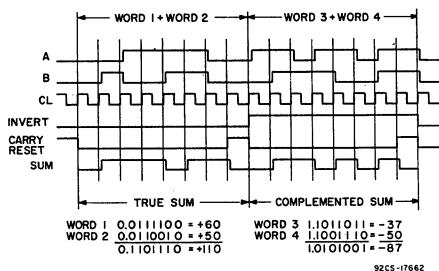


Fig.7-2 CD4032A timing diagram.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4032AD, CD4032AK CD4038AD, CD4038AK								
		$V_o$ Volts	$V_{DD}$ Volts	-55°C		25°C		125°C				
Quiescent Device Current	$I_L$			5	-	-	5	-	0.3	5	-	300 $\mu A$ 7-8, 7-10
				10	-	-	10	-	0.5	10	-	600
Quiescent Device Dissipation/Package	$P_D$			5	-	--	25	-	1.5	25	-	1500 $\mu W$
				10	-	-	100	-	5	100	-	6000
Output Voltage: Low-Level	$V_{OL}$			5	-	-	0.01	-	0	0.01	-	0.05 $V$
				10	-	-	0.01	-	0	0.01	-	0.05
High-Level	$V_{OH}$			5	4.99	-	-	4.99	5	-	4.95	-
				10	9.99	-	-	9.99	10	-	9.95	-
Noise Immunity (All Inputs)	$V_{NL}$			0.8	5	1.5	-	-	1.5	2.25	-	1.4 $V$ 7-9, 7-11
				1.0	10	3.0	-	-	3	4.5	-	2.9
	$V_{NH}$			4.2	5	1.4	-	-	1.5	2.25	-	1.5
				9.0	10	2.9	-	-	3	4.5	-	3.0
Output Drive Current: N-Channel	$I_{DN}$	$V_O = 0.5V$	5	0.6	-	-	0.5	0.9	-	0.3	-	- mA
			10	0.75	-	-	0.7	2.4	-	0.6	-	-
P-Channel	$I_{DP}$	$V_O = 4.5V$	5	-0.21	-	-	-0.15	-0.4	-	-0.075	-	- mA
			10	-0.7	-	-	-0.55	-1.2	-	-0.35	-	-
Input Current	$I_I$			-	-	-	-	10	-	-	-	pA -

For Output Drive Current test connections see Appendix.

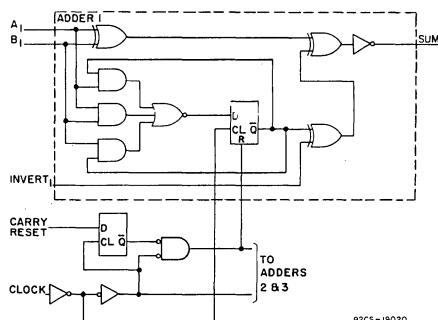


Fig.7-3 CD4038A logic diagram of one of three serial adders.

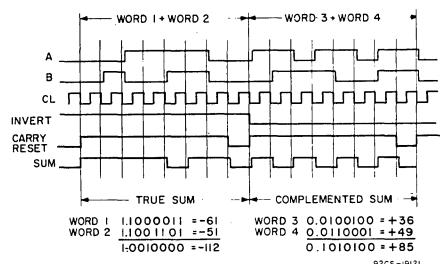


Fig.7-4 CD4038A timing diagram.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4032AE CD4038AE												
			-40°C			25°C			85°C						
			$V_O$ Volts	$V_{DD}$ Volts		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Device Current	$I_L$		5	—	—	50	—	0.5	50	—	—	700	$\mu A$	7-8, 7-10	
			10	—	—	100	—	1	100	—	—	1400			
Quiescent Device Dissipation/Package	$P_D$		5	—	—	250	—	2.5	250	—	—	3500	$\mu W$		
			10	—	—	1000	—	10	1000	—	—	14000			
Output Voltage: Low-Level	$V_{OL}$		5	—	—	0.01	—	0	0.01	—	—	0.05	$V$		
			10	—	—	0.01	—	0	0.01	—	—	0.05			
High-Level	$V_{OH}$		5	4.99	—	—	4.99	5	—	4.95	—	—	$V$		
			10	9.99	—	—	9.99	10	—	9.95	—	—			
Noise Immunity (All Inputs)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	$V$	7-9, 7-11	
			1.0	10	3.0	—	—	3	4.5	—	2.9	—			
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	$V$		
			9.0	10	2.9	—	—	3	4.5	—	3.0	—			
Output Drive Current: N-Channel	$I_{DN}$	$V_O = 0.5V$	5	0.25	—	—	0.2	0.9	—	0.14	—	—	$mA$	—	
		$V_O = 0.5V$	10	0.6	—	—	0.5	2.4	—	0.4	—	—			
	$I_{DP}$	$V_O = 4.5V$	5	-0.14	—	—	-0.1	-0.4	—	-0.095	—	—	$mA$	—	
		$V_O = 9.5V$	10	-0.3	—	—	-0.27	-1.2	—	-0.22	—	—			
Input Current	$I_I$		—	—	—	—	—	10	—	—	—	—	$pA$	—	

For Output Drive Current test connections see Appendix.

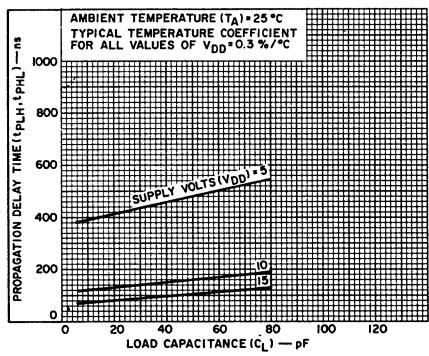


Fig. 7-5 Typ. propagation delay time vs.  $C_L$  for A,B, or invert inputs to sum outputs.

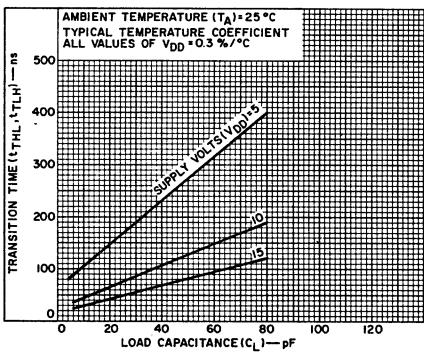


Fig. 7-6 Typ. transition time vs.  $C_L$  for sum outputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{ pF}$ , and input rise and fall times = 20ns, except  
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)  $t_{fCL}$  and  $t_{rCL}$ .

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4032AD, CD4032AK CD4038AD, CD4038AK			CD4032AE CD4038AE					
			V <sub>DD</sub> (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time: A, B, or Invert Inputs to Sum Outputs	$t_{PHL}$ , $t_{PLH}$		5	—	400	1100	—	400	1400	ns	7-5
			10	—	125	250	—	125	300		
Clock Input to Sum Outputs	$t_{THL}$ , $t_{TLH}$		5	—	800	2200	—	800	2400	ns	—
			10	—	250	500	—	250	600		
Transition Time (Sum Outputs)	$t_{rCL}$ , $t_{fCL}$		5	—	125	375	—	125	425	ns	7-6
			10	—	50	150	—	50	200		
Clock Rise & Fall Time	$^{**}t_{rCL}$ , $t_{fCL}$		5	—	—	15	—	—	15	$\mu\text{s}$	—
			10	—	—	15	—	—	15		
Input Set-Up Times*			5	$t_{rCL}$	—	—	$t_{rCL}$	—	—	—	—
			10		—	—		—	—		
Maximum Clock Frequency	$f_{CL}$		5	1.5	2.5	—	1	2.5	—	MHz	—
			10	3	5	—	2	5	—		
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	—	pF	—

\*This characteristic refers to the minimum time required for the A, B, or Reset Inputs to change state following a positive clock transition (CD4032A) or negative transition (CD4038A).

\*\*If more than one unit is cascaded  $t_{rCL}$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

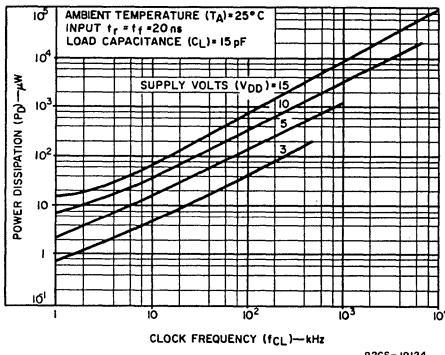


Fig. 7-7 Typ. dissipation characteristics.

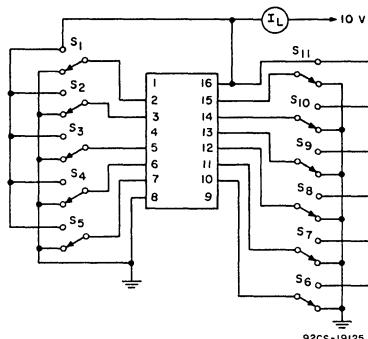


Fig. 7-8 Quiescent device current test circuit CD4032A.

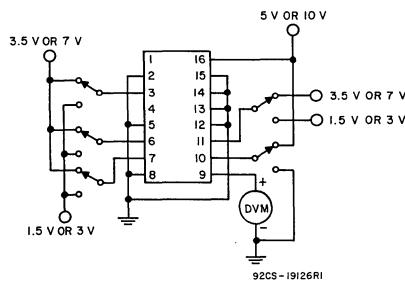


Fig.7-9 Noise-immunity test circuit-CD4032A.

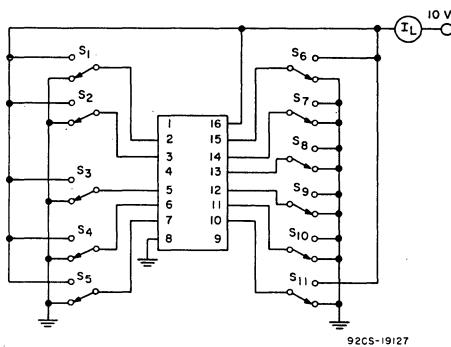


Fig.7-10 Quiescent device current test circuit-CD4038A.

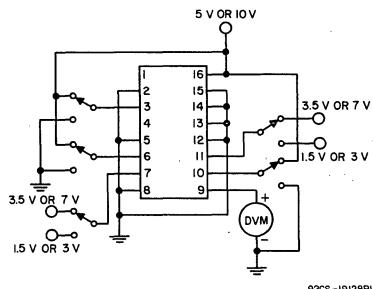


Fig.7-11 Noise-immunity test circuit-CD4038A.



# Digital Integrated Circuits

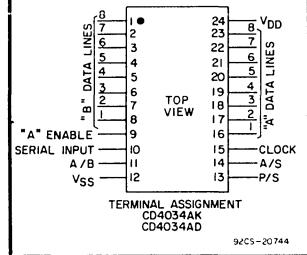
Monolithic Silicon

**CD4034AK****CD4034AD**

## COS/MOS MSI 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

### Special Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines
- Data recirculation for register storage
- Multipackage register expansion
- Fully static operation DC-to-5 MHz (typ.) at  $V_{DD}-V_{SS} = 10$  V



RCA CD4034A is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

- 1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single phase clock (CL), "A"-data enable (AE), Asynchronous/synchronous (A/S), "A" bus to "B" bus/"B" bus to "A" bus (A/B), and parallel/serial (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight "A" data lines are inputs (outputs) and the "B" data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for serial data is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

### PARALLEL OPERATION

A "high" P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is "low". If the A/S input is "high" this transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is "high" the A data lines are inputs (and B data lines are outputs); a "low" A/B signal reverses the direction of data flow.

### Applications:

- Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

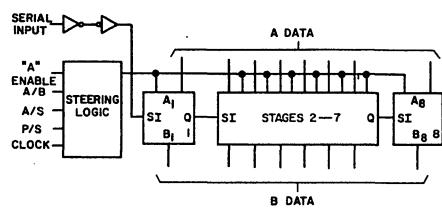


Fig. 1—Functional diagram.

The AE input is an additional feature which allows many registers to feed data to a common bus. The "A" Data lines are enabled only when this signal is "high".

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal "high" and the AE signal "low".

### SERIAL OPERATION

A "low" P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is "high") or the A lines (when A/B is "low" and the AE signal is "high").

Register expansion can be accomplished by simply cascading CD4034A packages.

The CD4034A is supplied in two different packages; the CD4034AK in a 24-lead flat pack, and the CD4034AD in a 24-lead ceramic dual-in-line package.

### MAXIMUM RATINGS, Absolute-Maximum Values:

Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
Operating Temperature Range	-55 to +125	$^{\circ}\text{C}$
DC Supply Voltage Range ( $\text{V}_{\text{DD}} - \text{V}_{\text{SS}}$ )	0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
All Inputs	$\text{V}_{\text{SS}} \leq \text{V}_i \leq \text{V}_{\text{DD}}$	
Recommended DC Supply Voltage ( $\text{V}_{\text{DD}} - \text{V}_{\text{SS}}$ )	3 to 15	V

### STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . . $\text{V}_{\text{SS}} \leq \text{V}_i \leq \text{V}_{\text{DD}}$ ) (Recommended DC Supply Voltage ( $\text{V}_{\text{DD}} - \text{V}_{\text{SS}}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
			CD4034AD, CD4034AK													
			-55°C			25°C			125°C							
Quiescent Device Current	$I_L$		5	—	—	5	—	0.3	5	—	—	300	$\mu\text{A}$	9		
			10	—	—	10	—	0.5	10	—	—	600				
Quiescent Device Dissipation/Package	$P_D$		5	—	—	25	—	1.5	25	—	—	1500	$\mu\text{W}$	8		
			10	—	—	100	—	5	100	—	—	6000				
Output Voltage: Low-Level	$V_{OL}$		5	—	—	0.01	—	—	0.01	—	—	0.05	$\text{V}$	—		
			10	—	—	0.01	—	—	0.01	—	—	0.05				
High-Level	$V_{OH}$		5	4.99	—	—	4.99	5	—	4.95	—	—	$\text{V}$	—		
			10	9.99	—	—	9.99	10	—	9.95	—	—				
Noise Immunity (All Inputs)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	$\text{V}$	10		
			1.0	10	3	—	—	3	4.5	—	2.9	—				
For Definition See Appendix	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—				
			9.0	10	2.9	—	—	3	4.5	—	3.0	—				
Output Drive Current: N-Channel	$I_{DN}$		0.5	5	0.124	—	—	0.1	0.20	—	0.07	—	$\text{mA}$	—		
			0.5	10	0.31	—	—	0.25	0.50	—	0.175	—				
P-Channel	$I_{DP}$		4.5	5	-0.075	—	—	-0.05	-0.10	—	-0.035	—	$\text{mA}$	—		
			9.5	10	-0.188	—	—	-0.125	-0.25	—	-0.088	—				
Input Current	$I_I$		—	—	—	—	—	10	—	—	—	—	$\text{pA}$	—		

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  and  $C_L = 15 \text{ pF}$ Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CD4034AD, CD4034AK			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS	
			$V_{DD}$ Volts	Min.	Typ.			
Propagation Delay Time	$t_{PHL}$		5	—	600	1200	ns	—
	$t_{PLH}$		10	—	240	480		
Transition Time	$t_{THL}$		5	—	250	750	ns	—
	$t_{TLH}$		10	—	100	300		
Minimum Clock Pulse Width	$t_{WL}$		5	—	200	400	ns	—
	$t_{WH}$		10	—	100	175		
Minimum High-Level AE, P/S, A/S Pulse Width	$t_{WH}$		5	—	240	480	ns	—
			10	—	85	195		
Clock Rise and Fall Time	$*t_{rCL}$ , $t_{fCL}$		5	—	—	15	$\mu\text{s}$	—
			10	—	—	15		
Set-Up Time	—		5	—	250	500	ns	—
			10	—	100	200		
Maximum Clock Frequency	$f_{CL}$		5	1.5	2.5	—	MHz	7
			10	3.0	5	—		
Input Capacitance	$C_I$	Any Input		—	5	—	pF	—

\* If more than one unit is cascaded,  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay at 15 pF (see chart above) and the transition time of the output driving stage for the estimated capacitive load.

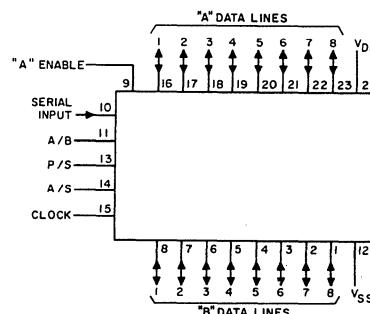


Fig.2—Functional and terminal assignment diagram for CD4034AK and CD4034AD.

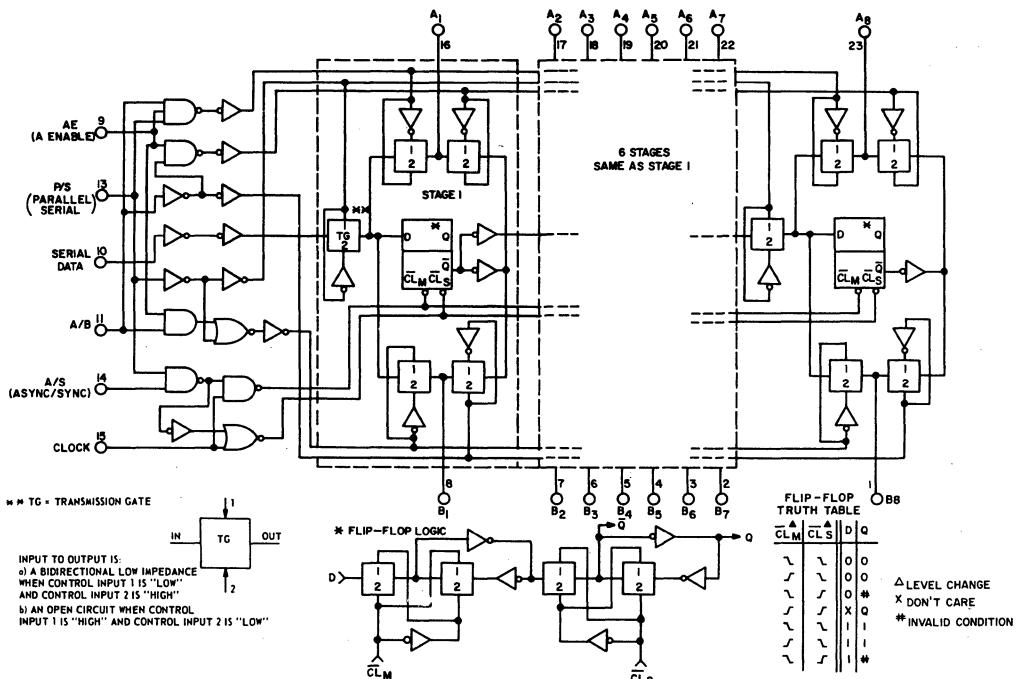


Fig.3—Logic diagram.

Table I Truth Table for Register Input-Levels and the Resulting Register Operation (L = Low Level, H = High Level, X = Don't Care)

"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

\* Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

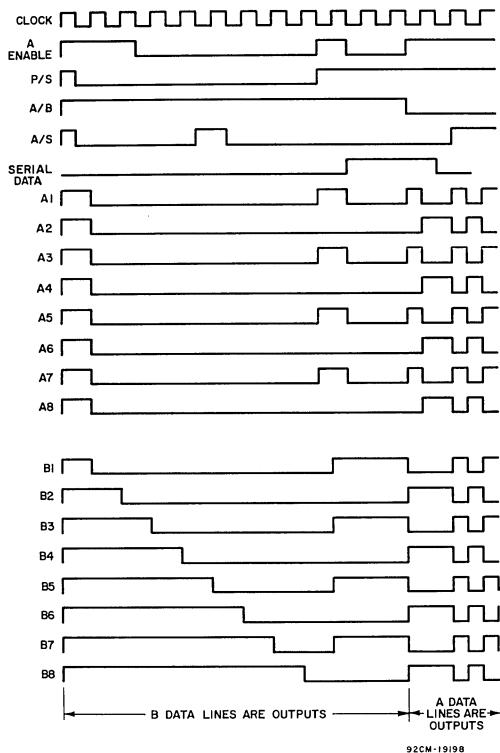


Fig.4—Timing diagram.

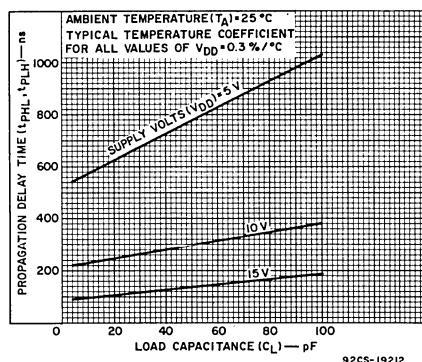
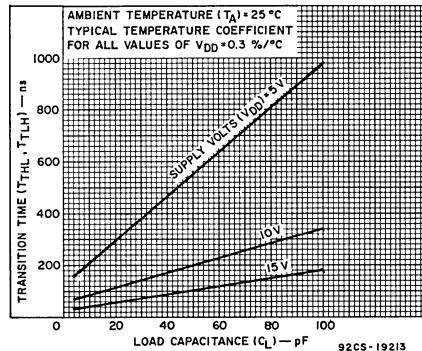
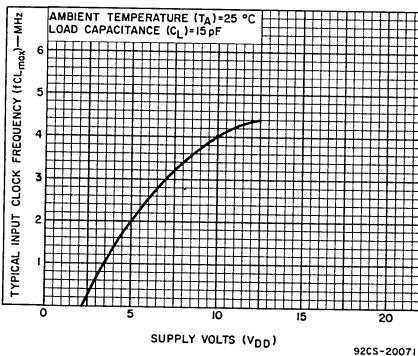
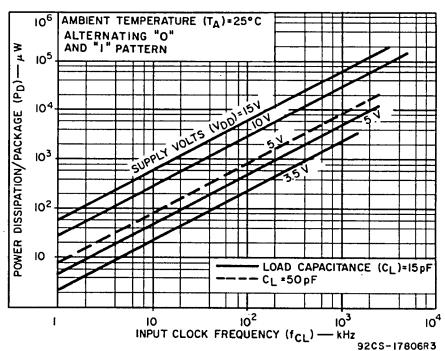
Fig.5—Typ. propagation delay time vs.  $C_L$ .Fig.6—Typ. transition time vs.  $C_L$ .Fig.7—Typ. input frequency vs.  $V_{DD}$ .

Fig.8—Typ. dissipation characteristics.

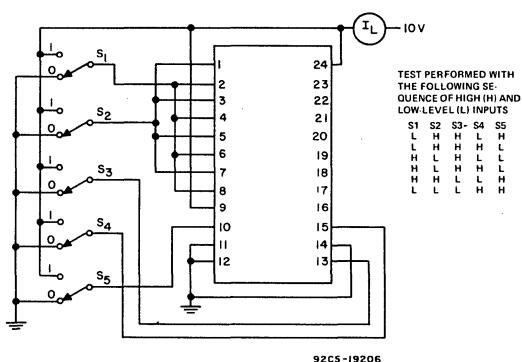


Fig.9—Quiescent device current test circuit.

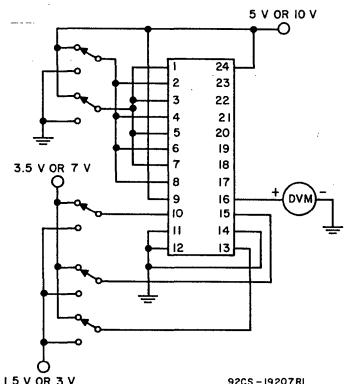


Fig.10—Noise immunity test circuit.

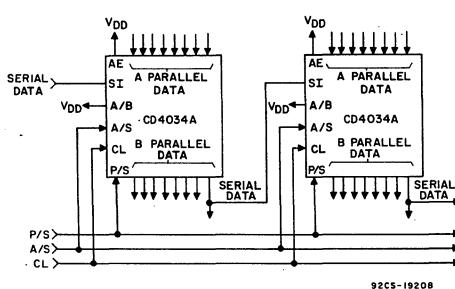


Fig.11—16-Bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.

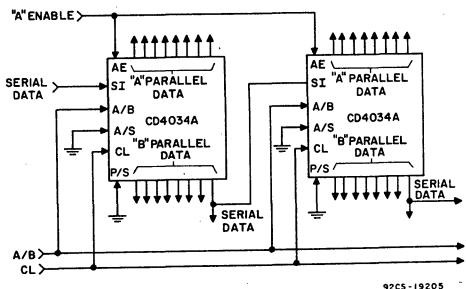


Fig.12—16-Bit serial in/gated parallel out register.

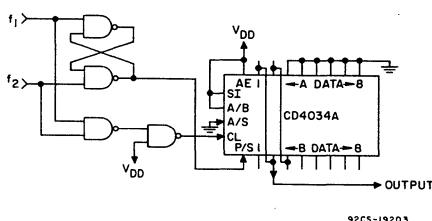
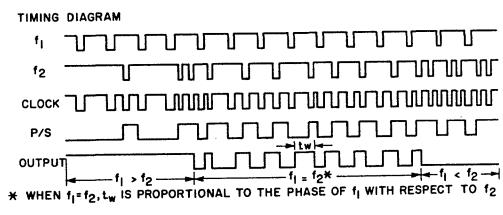
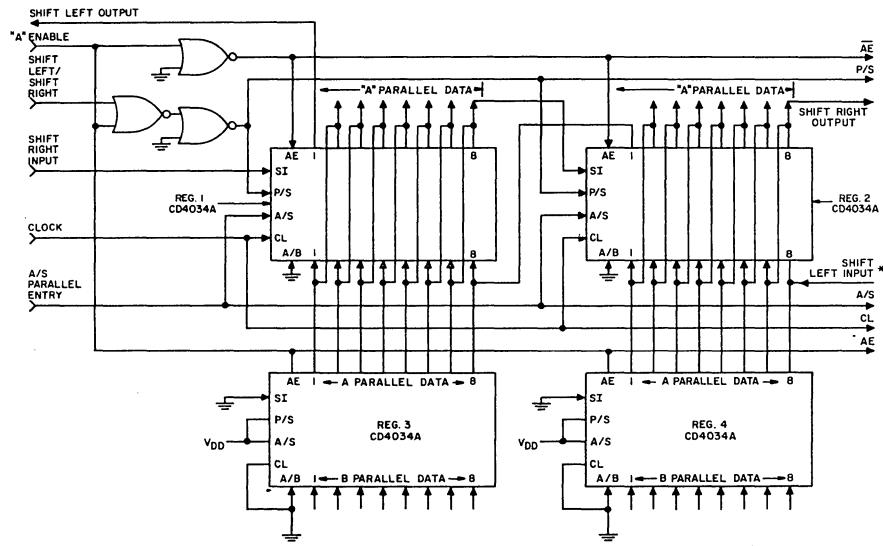


Fig.13—Frequency and phase comparator.





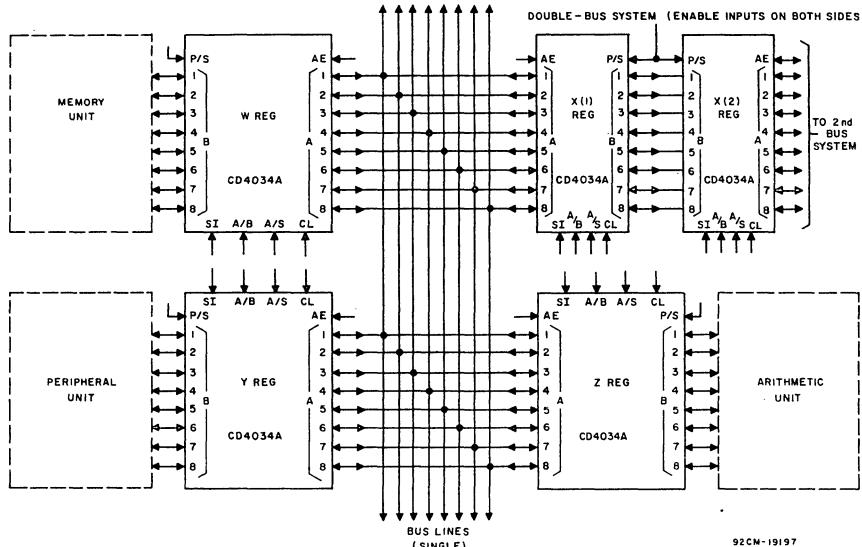
A "High" ("Low") on the shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data

into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

\*Shift left input must be disabled during parallel entry.

Fig. 14 - Shift right/shift left with parallel inputs.



The "A" enable (AE) and A/B signals control all combinations of transfer between the registers and bus systems.

Fig. 15 - Single- and double-bus systems.

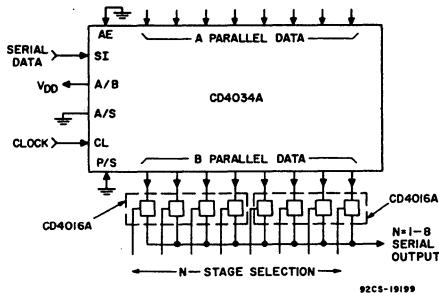


Fig. 16—N-stage shift register with fixed serial output line.

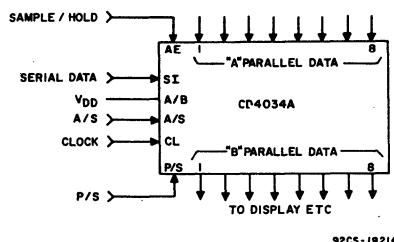
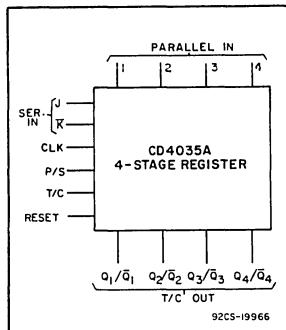


Fig. 17—Sample and hold register—serial/parallel in—parallel out.



Monolithic Silicon  
**CD4035AD**  
**CD4035AE**  
**CD4035AK**



## COS/MOS 4-Stage Parallel In/ Parallel Out Shift Register

with J-K Serial Inputs and True/  
Complement Outputs

### APPLICATIONS:

- Sequence generation, control circuits, code conversion
- Counters, Registers, Arithmetic-Unit Registers, Shift Left – Shift Right Registers, Serial-to-Parallel/Parallel-to-Serial conversions.

RCA-CD4035A\* is a four-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via J-K logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is "high".

In the parallel or serial mode information is transferred on positive clock transitions.

When the True/Complement control is "high", the True contents of the register are available at the output terminals. When the True/Complement control is "low", the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the clock signal.

J-K input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With J-K inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

CD4035A types are supplied in the 16-lead flat pack, and in both the 16-lead ceramic and plastic dual-in-line packages.

### FEATURES:

- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J-K inputs on first stage
- Asynchronous True/Complement control on all outputs
- Reset control
- Static flip-flop operation; Master-slave configuration
- Buffered outputs
- Low-Power Dissipation – 5  $\mu$ W typ. (ceramic)
- High speed – to 5 MHz

### MAXIMUM RATINGS, Absolute-Maximum Values:

Storage-Temperature Range .....	-65° to +150	°C
Operating Temperature Range:		
Ceramic Package Types .....	-55° to +125	°C
Plastic Package Types .....	-40° to +85	°C
DC Supply-Voltage Range		
(V <sub>DD</sub> – V <sub>SS</sub> ) .....	-0.5 V to +15	V
Device Dissipation (Per Pkg.) .....	200	mW
All Inputs .....	$V_{SS} \leq V_i \leq V_{DD}$	
Recommended		
DC Supply Voltage (V <sub>DD</sub> – V <sub>SS</sub> ). . . . .	3 to 15	V
Recommended		
Input Voltage Swing .....	$V_{DD}$ to $V_{SS}$	

\*Formerly developmental type TA5876

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
					CD4035AD, CD4035AK									
					$-55^\circ C$			$25^\circ C$						
Quiescent Device Current	$I_L$	$V_O$ Volts	$V_{DD}$ Volts		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
		5	—	—	5	—	5	0.3	5	—	—	300		
		10	—	—	10	—	10	0.5	10	—	—	600	$\mu A$ 11	
Quiescent Device Dissipation Package	$P_D$			5	—	—	25	—	1.5	25	—	—	1500	
		10	—	—	100	—	5	100	—	—	6000	$\mu W$ 4		
Output Voltage Low Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	
		10	—	—	0.01	—	0	0.01	—	—	0.05	V —		
High Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	V —	
		10	9.99	—	—	9.99	10	—	9.95	—	—	V —		
Noise Immunity (All Inputs)	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	
		1	10	3	—	—	3	4.5	—	2.9	—	—	V —	
<i>For definition, see Appendix</i>	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	
				9	10	2.9	—	—	3	4.5	—	3	—	
Output Drive Current: N Channel	$I_{DN}$			0.5	5	0.62	—	—	0.50	1	—	0.35	—	
				0.5	10	1.55	—	—	1.25	2.5	—	0.87	—	
P Channel	$I_{DP}$			4.5	5	-0.31	—	—	-0.25	-0.5	—	-0.17	—	
				9.5	10	-0.81	—	—	-0.65	-1.3	—	-0.45	—	
Input Current	$I_I$			—	—	—	—	—	10	—	—	—	pA —	

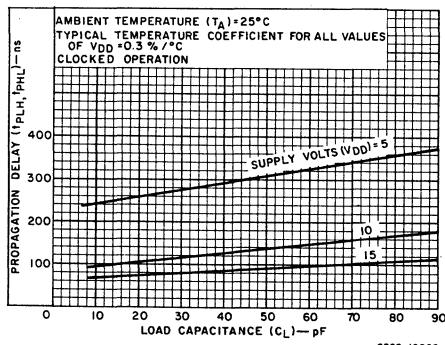


Fig. 1—Typical Propagation Delay Time vs. Load Capacitance.

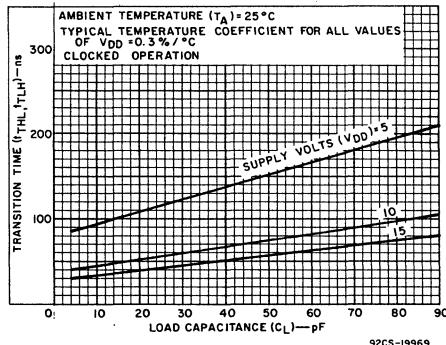


Fig. 2—Typical Transition Time vs. Load Capacitance.

STATIC ELECTRICAL CHARACTERISTICS (All inputs  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS												UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4035AE															
			$V_O$ Volts	$V_{DD}$ Volts	$-40^\circ C$			$25^\circ C$			$85^\circ C$							
Quiescent Device Current	$I_L$				5	—	—	50	—	0.5	50	—	—	700	$\mu A$	11		
					10	—	—	100	—	1	100	—	—	1400				
Quiescent Device Dissipation Package	$P_D$				5	—	—	250	—	2.5	250	—	—	3500	$\mu W$	4		
					10	—	—	1000	—	10	1000	—	—	14000				
Output Voltage Low Level	$V_{OL}$				5	—	—	0.01	—	0	0.01	—	—	0.05	$V$	—		
					10	—	—	0.01	—	0	0.01	—	—	0.05				
High Level	$V_{OH}$				5	4.99	—	—	4.99	5	—	4.95	—	—	$V$	—		
					10	9.99	—	—	9.99	10	—	9.95	—	—				
Noise Immunity (All Inputs)	$V_{NL}$				0.8	5	1.5	—	1.5	2.25	—	1.4	—	—	$V$	12		
					1	10	3	—	3	4.5	—	2.9	—	—				
For Definition See Appendix	$V_{NH}$				4.2	5	1.4	—	1.5	2.25	—	1.5	—	—	$V$	12		
					9	10	2.9	—	3	4.5	—	3	—	—				
Output Drive Current: N Channel	$I_{DN}$				0.5	5	0.43	—	0.35	1	—	0.24	—	—	$mA$	—		
					0.5	10	1.05	—	0.85	2.5	—	0.59	—	—				
P Channel	$I_{DP}$				4.5	5	-0.2	—	-0.18	-0.5	—	-0.12	—	—	$mA$	—		
					9.5	10	-0.56	—	-0.45	-0.31	—	-0.31	—	—				
Input Current	$I_I$						—	—	—	10	—	—	—	—	$pA$	—		

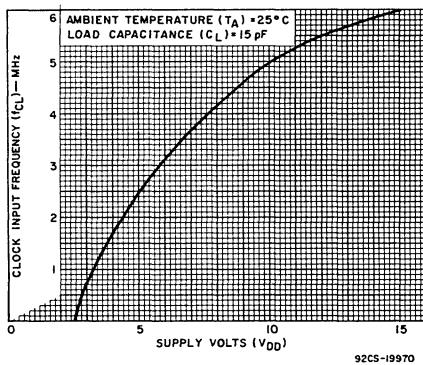
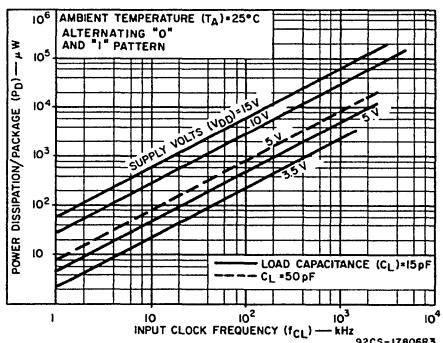
Fig. 3—Typical clock input frequency vs.  $V_{DD}$ .

Fig. 4—Typical dissipation characteristics.

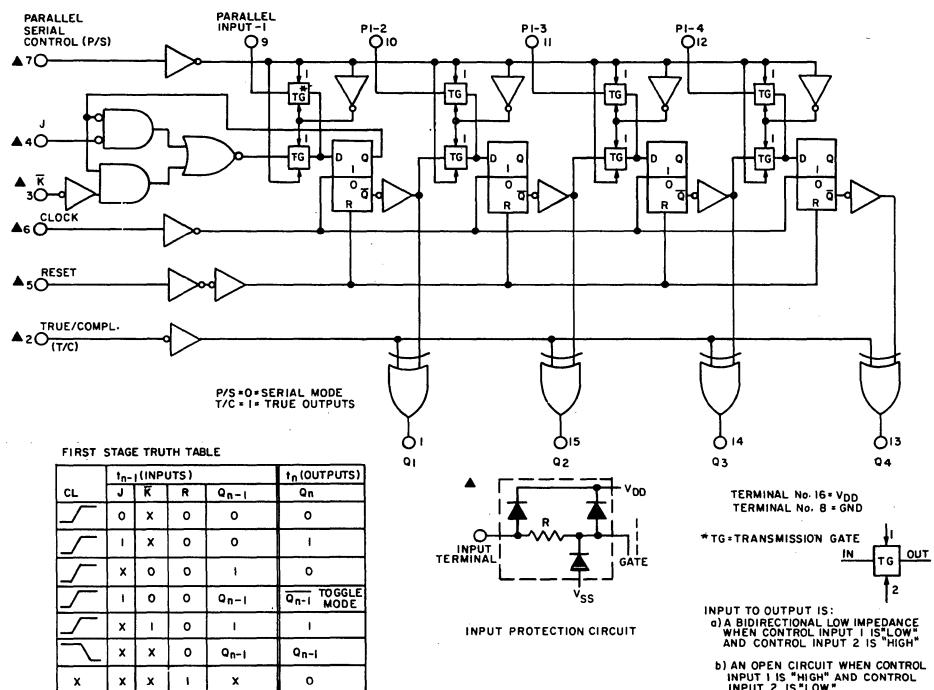


Fig. 5—Logic Block Diagram.

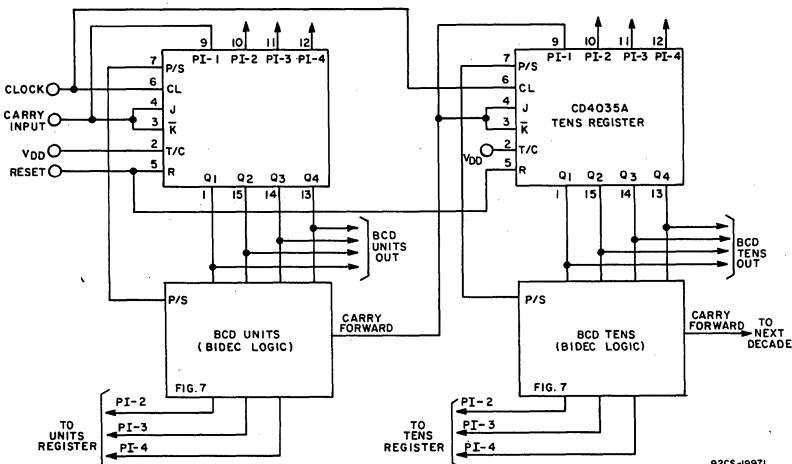


Fig. 6—Binary-to-BCD Converter.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ C$  and  $C_L = 15 \text{ pF}$   
 Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ C$  (See Appendix for Waveforms)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4035AD, CD4035AK			CD4035AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
<b>CLOCKED OPERATION</b>											
Propagation Delay Time:	$t_{PLH}, t_{PHL}$		5	—	250	500	—	250	700	ns	1
			10	—	100	200	—	100	300	ns	
Transition Time:	$t_{THL}, t_{TLH}$		5	—	100	200	—	100	300	ns	2
			10	—	50	100	—	50	150	ns	
Minimum Clock Pulse Duration	$t_{WL}, t_{WH}$		5	—	200	335	—	200	500	ns	—
Clock Rise & Fall Time	$t_{rCL}^*, t_{fCL}$		10	—	100	165	—	100	250	ns	—
Setup Time: <u>J/K Lines</u>			5	—	250	500	—	250	750	ns	—
			10	—	100	200	—	100	250	ns	
Parallel-In Lines			5	—	100	350	—	100	500	ns	—
			10	—	50	80	—	50	100	ns	
Maximum Clock Frequency	$f_{CL}$		5	1.5	2.5	—	1	2.5	—	MHz	3
			10	3	5	—	2	5	—		
Input Capacitance	$C_I$	Any Input	—	5	—	—	5	—	pF	—	—
<b>RESET OPERATION</b>											—
Propagation Delay Time:	$t_{PHL}, t_{PLH}$		5	—	250	500	—	250	700	ns	—
			10	—	100	200	—	100	300	ns	
Minimum Reset Pulse Duration	$t_{WL}, t_{WH}$		5	—	200	400	—	200	500	ns	—
			10	—	100	175	—	100	200	ns	

\* If more than one unit is cascaded  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

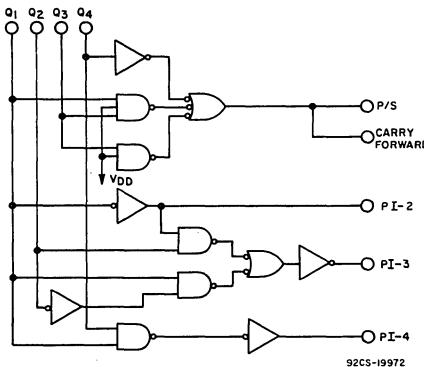


Fig. 7-BIDEC Logic.

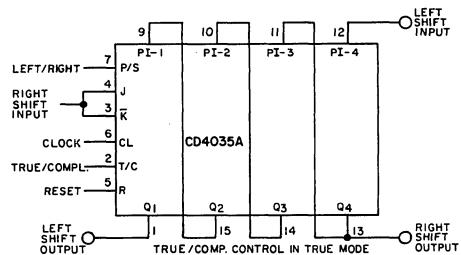


Fig. 8-Shift Left/Shift Right Register.

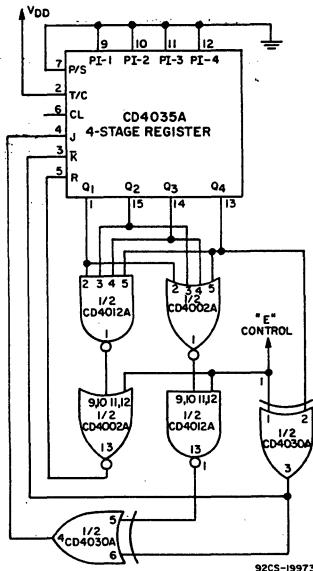
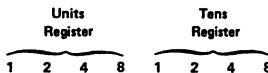


Fig. 9(a)—Double Sequence Generator.

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E)

Control = E =	0				1			
	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>
A	B	C	D	A	B	C	D	
0	0	0	0	0	15	1	1	1
1	1	0	0	0	14	0	1	1
2	0	1	0	0	13	1	0	1
5	1	0	1	0	10	0	1	0
10	0	1	0	1	5	1	0	1
4	0	0	1	0	11	1	1	0
9	1	0	0	1	6	0	1	0
3	1	1	0	0	12	0	0	1
6	0	1	1	0	9	1	0	1
13	1	0	1	1	2	0	1	0
11	1	1	0	1	4	0	0	1
7	1	1	1	0	8	0	0	1
14	0	1	1	1	1	1	0	0
12	0	0	1	1	3	1	1	0
8	0	0	0	1	7	1	1	0

Fig. 9(b)—State Sequences.



LSB	MSB
58	= 0 1 0 1 1 1
Shift	
Shift	
Shift	0 1 0 1 1 1
Add* 3 to Units Decade & Shift	0 1 0 1 1 1 (1 1)
Shift	0 1 0 0 1 0 1
Add* 3 to Units Decade & Shift	0 1 0 0 1 0 1 (1 1)
	0 0 0 1 1 0 1 0
* From Left to Right	8                        5

Fig. 10—Example of Binary-to-BCD Conversion.

Using Couleur's Technique (BIDEC)<sup>▲</sup>, a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035A, with the correct conversion logic, can also be used as a BCD-to-binary converter.

▲ The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, Pages 313-316.

## TEST CIRCUITS

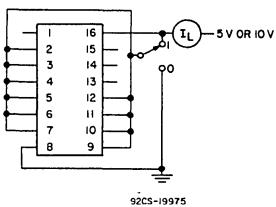


Fig. 11—Quiescent device current.

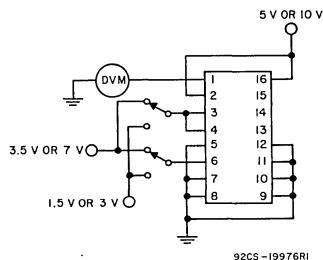
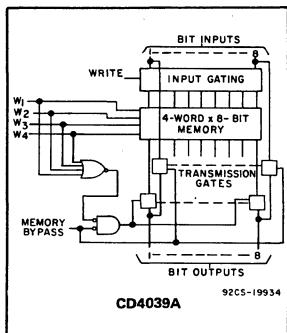


Fig. 12—Noise immunity.



# Digital Integrated Circuits

Monolithic Silicon

**CD4036AD CD4039AD  
CD4036AK CD4039AK**


## COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

Binary Addressing

CD4036AD, CD4036AK

Direct Word-Line Addressing

CD4039AD, CD4039AK

*Special Features:*

- COS/MOS logic compatibility at all input and output terminals
- Memory bit expansion
- Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines
- Memory bypass capability for all bits
- Buffering on all outputs
- CD4036A- on-chip binary address decoding, separate READ INHIBIT and WRITE controls
- Access Time—200 ns(Typ) at V<sub>DD</sub>=10 V
- CD4039A-Direct word-line addressing

RCA type CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (See Fig.15). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (See Fig.4).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary

*Applications:*

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- Channel Preset Memory in digital frequency-synthesizer circuits
- General-purpose and scratch-pad memory in COS/MOS and other low-power systems.

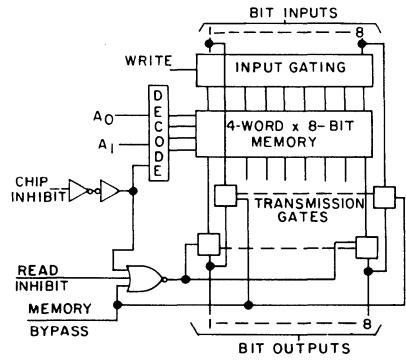


Fig.1 — CD4036A — Logic block diagram.

ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-Oring multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig.5).

These devices will be supplied in two different 24-lead ceramic packages; the CD4036AK and CD4039AK in the flat-pack, and the CD4036AD and CD4039AD in the dual-in-line package.

#### MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range .....	-65 to +150	°C
Operating Temperature Range ...	-55 to +125	°C
DC Supply Voltage Range		
(V <sub>DD</sub> - V <sub>SS</sub> ). ....	-0.5 to +15	V
Device Dissipation (Per Pkg.) ....	200	mW
All Inputs .....	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	
Recommended DC Supply Voltage		
(V <sub>DD</sub> - V <sub>SS</sub> ). ....	3 to 15	V
Lead Temperature (During soldering)		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case		
for 10 seconds max. ....	265	°C

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... V<sub>SS</sub> ≤ V<sub>I</sub> ≤ V<sub>DD</sub>)  
(Recommended DC Supply Voltage (V<sub>DD</sub> - V<sub>SS</sub>). .... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS										CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS			
			CD4036AD, CD4036AK CD4039AD, CD4039AK														
			V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-55°C			25°C			125°C						
Quiescent Device Current	I <sub>L</sub>				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
		5	—	—	5	—	0.5	5	—	—	300	—	μA	11, 12			
Quiescent Device Dissipation/Package	PD		10	—	—	10	—	1	10	—	—	600	—	μW	—		
			5	—	—	25	—	2.5	25	—	—	1500	—	—	—		
Output Voltage: Low-Level	V <sub>OL</sub>		10	—	—	100	—	10	100	—	—	6000	—	V	—		
			5	—	—	0.01	—	0	0.01	—	—	0.05	—	—	—		
High-Level	V <sub>OH</sub>		10	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—		
			5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	V	—	
Noise Immunity (All inputs except bit inputs when in memory bypass mode.)	V <sub>NL</sub>		10	9.99	—	—	9.99	10	—	9.95	—	—	—	—	V	13	
			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—	—		
	V <sub>NH</sub>		1.0	10	3	—	—	3	4.5	—	2.9	—	—	—	—		
			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—	—		
Output Drive Current: N-Channel	I <sub>DN</sub>	Normal Read Modes	9.0	10	2.9	—	—	3	4.5	—	3	—	—	—	—	V	13
			0.5	5	0.12	—	—	0.10	0.20	—	0.07	—	—	—	—	mA	
P-Channel	I <sub>DP</sub>		0.5	10	0.30	—	—	0.25	0.50	—	0.17	—	—	—	—	mA	6
			4.5	5	-0.12	—	—	-0.10	-0.20	—	-0.07	—	—	—	—	mA	
Output Drive Current: N-Channel	I <sub>DN</sub>	Memory Bypass Mode	9.5	10	-0.30	—	—	-0.25	-0.50	—	-0.17	—	—	—	—	mA	7
			0.5	5	0.04	—	—	0.03	0.06	—	0.02	—	—	—	—	mA	
P-Channel	I <sub>DP</sub>	Memory Bypass Mode	0.5	10	0.09	—	—	0.075	0.15	—	0.05	—	—	—	—	mA	—
			4.5	5	-0.04	—	—	-0.03	-0.06	—	-0.02	—	—	—	—	mA	
Input Current	I <sub>I</sub>		—	—	—	—	—	—	—	10	—	—	—	—	pA	—	

<sup>+</sup>Bit inputs driven from low-impedance driver.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  and  $C_L = 15 \text{ pF}$ Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{^oC}$ 

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	$V_{DD}$ Volts	CD4036AD, CD4036AK CD4039AD, CD4039AK			UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS
				Min.	Typ.	Max.		
Read Delay Time: (Access time) Read Inhibit (RI)	$t_{RD}$	OUTPUT TIED THROUGH $100 \text{ k}\Omega$ TO $V_{SS}$ FOR DATA OUTPUT "HIGH" AND TO $V_{DD}$ FOR DATA OUTPUT "LOW"	5	—	375	750	ns Note 4	4,5
			10	—	150	300		
			5	—	500	1000	ns Note 4	4,5
			10	—	200	400		
			5	—	375	750	ns	4,5
			10	—	150	300		
			5	—	500	1000	ns	4,5,8
			10	—	200	400		
Write Set-up Time <sup>2</sup>	$t_{WS}$		5	250	125	—	ns	4,5
			10	100	50	—		
Write Removal Time <sup>3</sup>	$t_{WR}$		5	0	0	—	ns	4,5
			10	0	0	—		
Write Pulse Duration	$t_W$		5	150	75	—	ns	4,5
			10	60	30	—		
Data Set-up Time <sup>5</sup>	$t_{DS}$		5	—	0	$0^*$	ns	4,5
			10	—	0	$0^*$		
Data Overlap Time <sup>6</sup>	$t_{DO}$		5	100●	50	—	ns	4,5
			10	40●	20	—		
Output Transition Time	$t_{THL},$ $t_{TLH}$		5	—	200	400	ns	9
			10	—	100	200		
Input Capacitance	$C_I$	Any Input		—	5	—	pF	—

1. For CD4036A only, remove  $100-\text{k}\Omega$  test condition and write all 1's in word one, and all 0's in word two, or vice-versa.

2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.

3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.

4. Values for CD4036AD &amp; 4036AK only.

5. The time that DATA signal must be present before the WRITE pulse removal.

\* Max. indicates satisfactory operation if  $t_{DS}$  equals or exceeds this value.

6. The time that DATA signal must remain present after the WRITE pulse removal.

● Min. indicates satisfactory operation if  $t_{DO}$  equals or exceeds this value.

Write (Pin 2)	Read Inhibit (Pin 21)	Memory Bypass (Pin 11)	Chip Inhibit (Pin 22)	Operating Mode
X	X	L	H	Chip Inhibited (Outputs float)
X	X	H	H	Input/Output Shunted to output; No Reading from Memory;
L	X	H	L	Information in Memory Undisturbed
H	X	H	L	Input/Output Shunted to output; No Reading from Memory; Write Data into Addressed Word
L	L	L	L	Read Data from Addressed Word Write Deactivated
L	H	L	L	Read/Write Deactivated (Outputs float)
H	L	L	L	Read from Memory while Writing Data into Addressed Word
H	H	L	L	Write Data into Addressed Word Read Deactivated (outputs float)

Fig.2 – Operating-mode truth table.

A1 Pin 1	A0 Pin 23	Addressed Word
L	L	Word 1
L	H	Word 2
H	L	Word 3
H	H	Word 4

L = Low-Level Voltage,  
H = High-Level Voltage

Fig.3 – Address truth table.

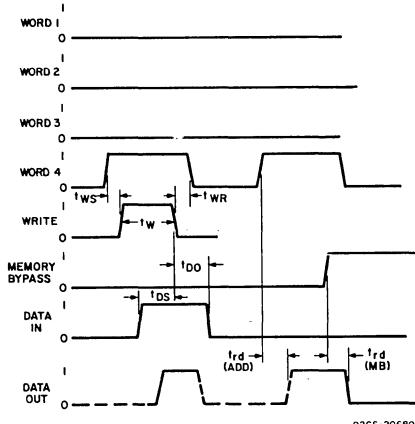
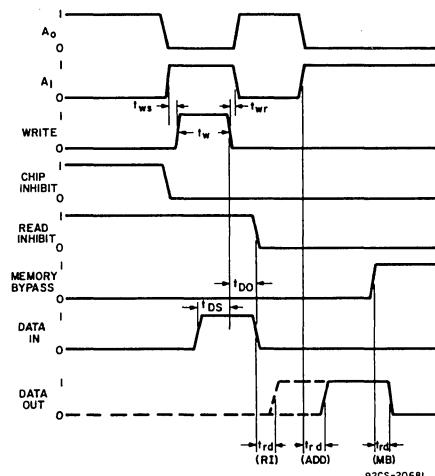


Fig.5—CD4039A Timing Diagram.

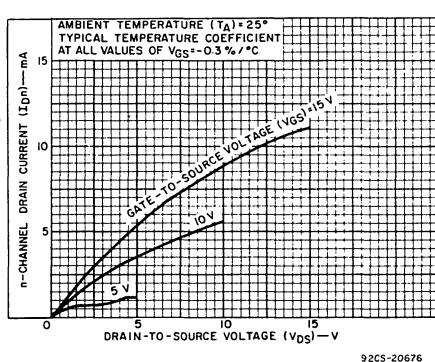


Fig.6—Typical n-channel drain characteristics.

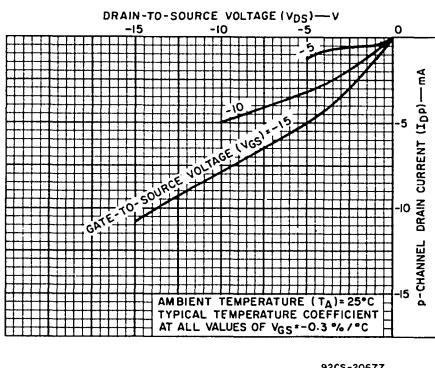
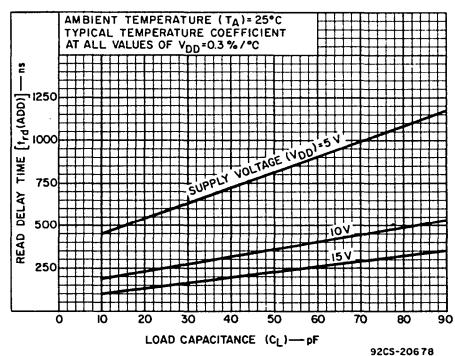
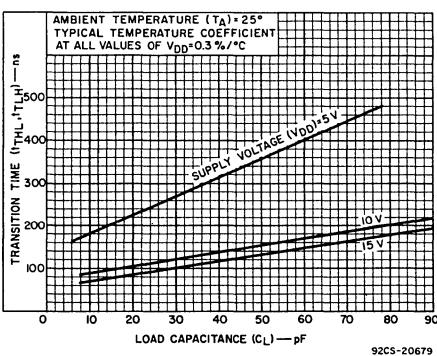


Fig.7—Typical p-channel drain characteristics.

Fig.8—Typical read delay time vs.  $C_L$ .Fig.9—Typical transition time vs.  $C_L$ .

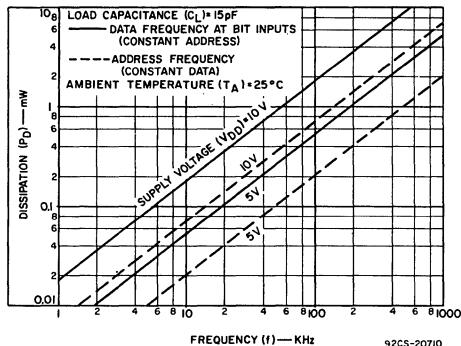


Fig.10—Typical power dissipation vs. frequency.

## TEST CIRCUITS

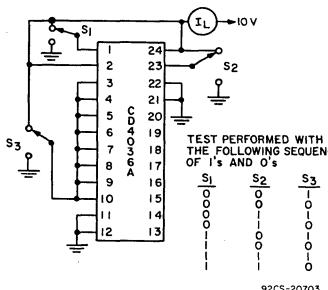


Fig.11—Quiescent current (CD4036A).

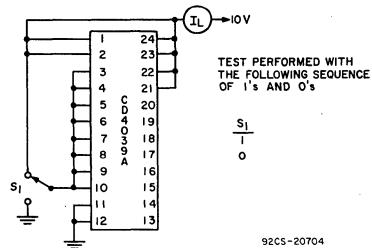


Fig.12—Quiescent current (CD4039A).

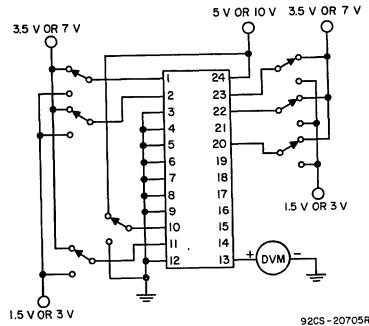
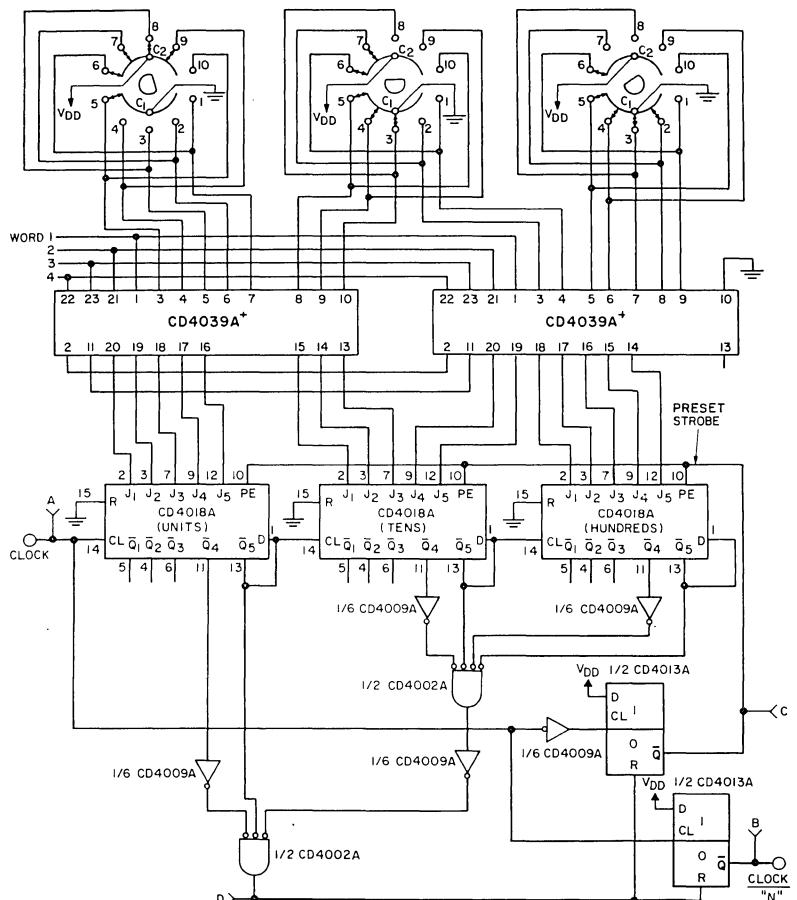


Fig.13—Noise immunity.



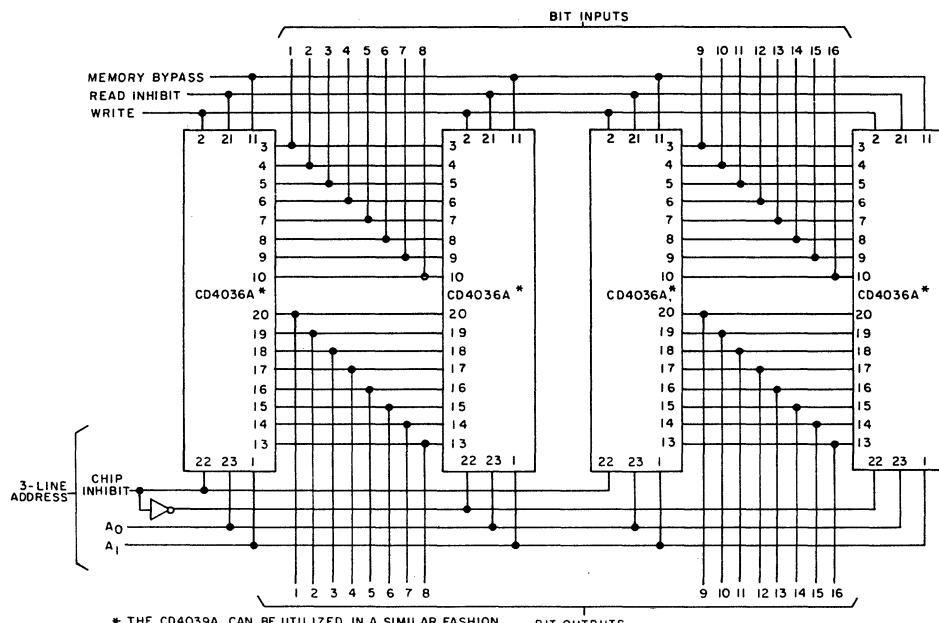
+ The CD4036A CAN BE UTILIZED IN A SIMILAR FASHION.

SEE APP. NOTE ICAN-6498 - "DESIGN OF FIXED AND PROGRAMMABLE COUNTERS USING THE RCA CD4018A COS/MOS PRESETTABLE DIVIDE-BY-'N' COUNTER" AND ICAN-6716, "LOW POWER DIGITAL FREQUENCY SYNTHESIZERS UTILIZING COS/MOS IC'S".

Fig.14—Three-decade programmable  $\div N$  counter with 4-channel preset memory settings for frequency synthesizers.

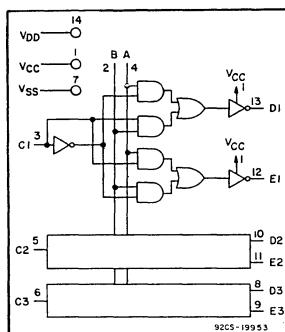
The divide-by-N counter system shown in Fig.14 is programmable from 2 to 999. Four counter-preset words, selected by means of the rotary switches, can be stored in the CD4039A devices and can be read into each CD4018A by

simply addressing the proper word. Note that the CD4029A (see Bulletin File No. 503) Presettable Up/Down Counter with BCD decade counting can also be used to perform the basic counting function.



92CM-19938

Fig.15—General-purpose memory storage — 8 words x 16 bits (RAM or ROM).



RCA CD4037A consists of three AND-OR pairs driven by common control signals A and B.

Each circuit has a data input (C), and two output terminals (D and E) that provide outputs in accordance with the truth table shown in Fig. 2. The circuit is useful for coding or decoding signals for split-phase (Bi-phase) communication systems, magnetic recording, and plated wire and core memory systems. A separate V<sub>CC</sub> terminal is provided to allow level conversion to any voltage from 3 volts to V<sub>DD</sub>.

CD4037AD is supplied in a 14-lead ceramic dual-in-line package, CD4037AE in a 14-lead plastic dual-in-line package, CD4037AF in a 16-lead dual-in-line ceramic frit-seal package, and CD4037AK in a 14-lead ceramic flat package.

## COS/MOS Triple AND-OR Bi-Phase Pairs

### Applications:

For use in digital equipment where low-power dissipation, low package count, and/or high noise immunity are primary design requirements.

- Split-Phase (Bi-Phase) Communication Systems.
- Disc, Drum, and Tape Digital Recording Systems.
- Plated Wire and Core Memory Systems.
- High-to-low logic level converter.

### Features:

- Outputs compatible with low-power TTL systems.
- High current sink and source (1.6 mA typ.) capability at V<sub>DD</sub> = V<sub>CC</sub> = 10 V and V<sub>DS</sub> = 0.5 V.
- Input protection against electrostatic effects.
- Microwatt quiescent power dissipation: P<sub>D</sub> = 0.5  $\mu$ W/ceramic pkg. (typ.), P<sub>D</sub> = 2  $\mu$ W/plastic pkg. (typ.) at V<sub>DD</sub> = 10 V

### MAXIMUM RATINGS, Absolute-Maximum Values:

Storage Temperature Range ..... -65°C to +150 °C

Operating Temperature Range:

Ceramic Package Types ..... -55°C to +125 °C

Plastic Package Types ..... -40°C to +85 °C

DC Supply Voltage Range (V<sub>DD</sub> - V<sub>SS</sub>) ..... -0.5 V to +15 V

Dissipation:

Per Package ..... 200 mW

Per Output ..... 100 mW

All Inputs ..... V<sub>SS</sub> ≤ V<sub>I</sub> ≤ V<sub>DD</sub>

For V<sub>CC</sub> ..... 3 < V<sub>CC</sub> ≤ V<sub>DD</sub>

Recommended DC Supply Voltage

(V<sub>DD</sub> - V<sub>SS</sub>) ..... 3 to 15 V

**CAUTION: V<sub>CC</sub> VOLTAGE LEVEL MUST BE EQUAL TO OR LESS POSITIVE THAN V<sub>DD</sub>**

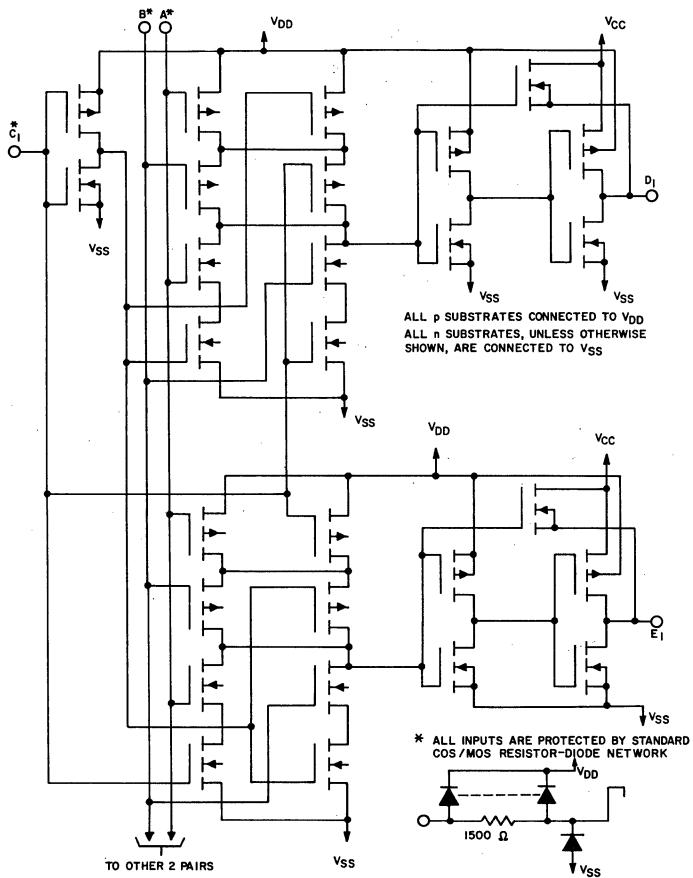


Fig.1—Schematic diagram of one AND-OR-Bi-Phase Pair.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS												CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.
					CD4037AD, CD4037AF, CD4037AK												
					-55°C			25°C			125°C						
Quiescent Device Current	$I_L$		5		5	—	—	5	—	0.03	5	—	—	300	—	$\mu A$	9
				10	—	—	—	10	—	0.05	10	—	—	600	—		
Quiescent Device Dissipation/Package	$P_D$		5		5	—	—	25	—	0.15	25	—	—	1500	—	$\mu W$	—
Output Voltage: Low-Level	$V_{OL}$		5		5	—	—	0.01	—	0	0.01	—	—	0.05	—	$V$	—
				10	—	—	—	0.01	—	0	0.01	—	—	0.05	—		
High-Level	$V_{OH}$		5	5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	$V$	—
				10	10	9.99	—	—	9.99	10	—	9.95	—	—	—		
Noise Immunity (All Inputs) For Definition, See Appendix	$V_{NIL}$ $V_{NIH}$	0.8 1.0 4.2 9.0	5 10 5 10	5 10 5 10	5 10 3 2.9	— — — —	— — — —	1.5 3 1.5 3	2.25 4.5 2.25 4.5	— — — —	1.4 2.9 1.5 3	— — — —	—	—	$V$	10	
Output Drive Current: N-Channel	$I_{DN}$	0.5 0.5	5 10	5 10	0.85 1.3	— —	— —	0.7 1.1	1.2 2	— —	0.45 0.7	— —	—	—	mA	—	
	$I_{DP}$	4.5 9.5	5 10	5 10	-0.65 -0.9	— —	— —	-0.55 -0.75	-1 -1.6	— —	-0.35 -0.45	— —	—	—	mA	—	
Input Current	$I_I$				—	—	—	—	10	—	—	—	—	—	pA	—	

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS												CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.
					CD4037AE												
					-40°C			25°C			85°C						
Quiescent Device Current	$I_L$		5		5	—	—	50	—	0.1	50	—	—	700	—	$\mu A$	9
				10	—	—	—	100	—	0.2	100	—	—	1400	—		
Quiescent Device Dissipation/Package	$P_D$		5		5	—	—	250	—	0.5	250	—	—	3500	—	$\mu W$	—
				10	—	—	—	1000	—	2	1000	—	—	14000	—		
Output Voltage: Low-Level	$V_{OL}$		5		5	—	—	0.01	—	0	0.01	—	—	—	—	$V$	—
				10	—	—	—	0.01	—	0	0.01	—	—	—	—		
High-Level	$V_{OH}$		5	5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	$V$	—
				10	10	9.99	—	—	9.99	10	—	9.95	—	—	—		
Noise Immunity (All Inputs) For Definition, See Appendix	$V_{NIL}$ $V_{NIH}$	0.8 1.0 4.2 9.0	5 10 5 10	5 10 5 10	5 10 3 2.9	— — — —	— — — —	1.5 3 1.5 3	2.25 4.5 2.25 4.5	— — — —	1.4 2.9 1.5 3	— — — —	—	—	$V$	10	
Output Drive Current: N-Channel	$I_{DN}$	0.5 0.5	5 10	5 10	0.4 0.65	— —	— —	0.35 0.55	0.7 1.1	— —	0.3 0.45	— —	—	—	mA	—	
	$I_{DP}$	4.5 9.5	5 10	5 10	-0.35 -0.5	— —	— —	-0.3 -0.4	-0.55 -0.75	— —	-0.2 -0.3	— —	—	—	mA	—	
Input Current	$I_I$				—	—	—	—	10	—	—	—	—	—	pA	—	

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and  $V_{CC} = 5 \text{ V}$

Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4037AD, CD4037AK, CD4037AF			CD4037AE						
			Min.	Typ.	Max.	Min.	Typ.	Max.				
Propagation Delay Time: A and B Inputs	$t_{PHL}$	$V_{DD}$ (Volts)	5	—	225	450	—	325	650	ns	6, 8	
	$t_{PLH}$		10	—	75	150	—	100	200			
C Inputs	$t_{PHL}$	$V_{DD}$ (Volts)	5	—	250	500	—	350	700	ns		
	$t_{PLH}$		10	—	75	150	—	100	200			
	$t_{PHL}$	$V_{DD}$ (Volts)	5	—	225	450	—	325	650	ns		
	$t_{PLH}$		10	—	90	180	—	125	250			
Transition Time: High-to-Low Level	$t_{THL}$	$V_{DD}$ (Volts)	5	—	40	80	—	60	120	ns	4, 8	
	$t_{TLH}$		10	—	15	30	—	20	40			
Input Capacitance	$C_I$	Any Input	5	—	—	—	5	—	pF	—	—	
			10	—	60	120	—	90	180			

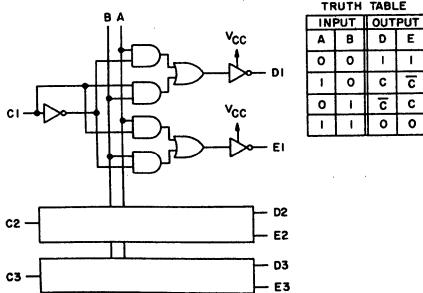


Fig.2—Logic diagram and truth table.

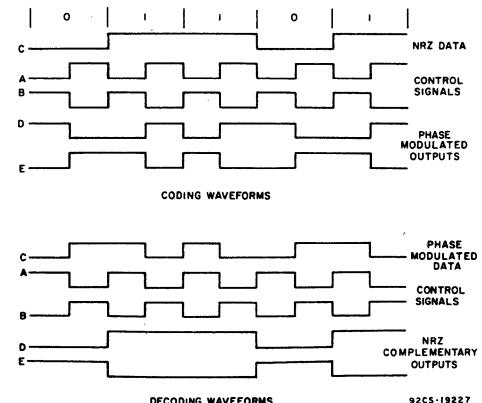


Fig.3—Coding and decoding waveforms.

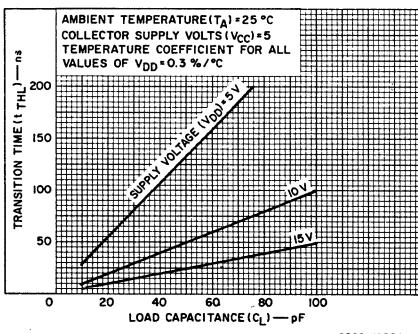


Fig.4—Typical transition time vs  $C_L$ .

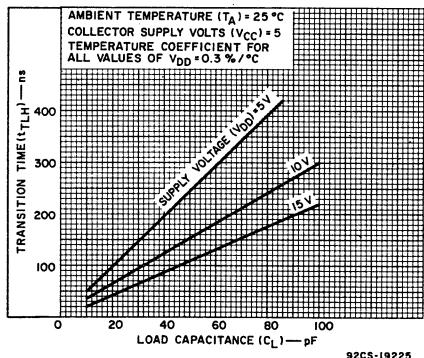


Fig.5—Typical transition time vs  $C_L$ .

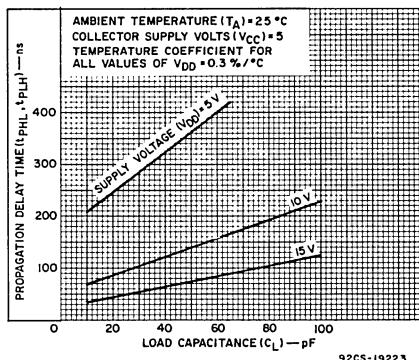
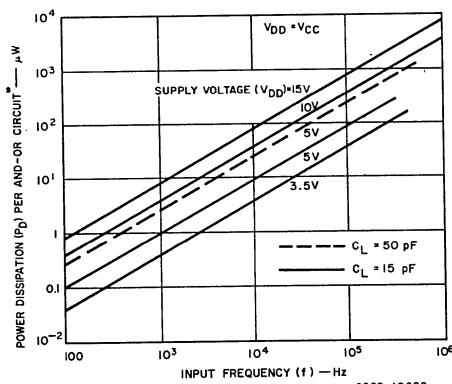
Fig.6—Typical propagation delay time vs  $C_L$ .

Fig.7—Typical dissipation characteristics.

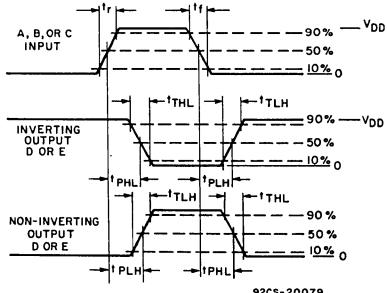


Fig.8—Waveforms for measurement of dynamic characteristics.

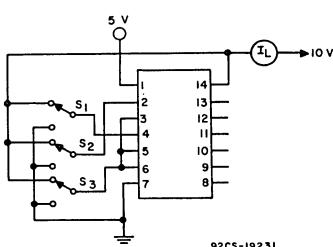
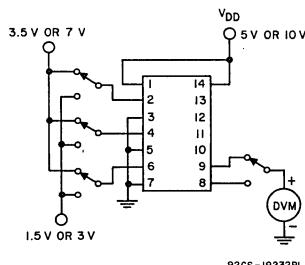


Fig.9—Quiescent device current.

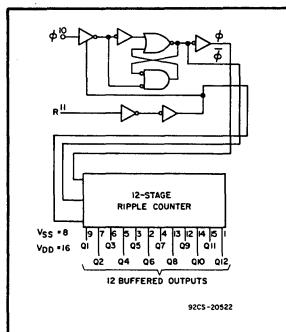
Fig.10—Noise immunity (at  $T_A = 25^\circ\text{C}$ ).

**RCA**  
Solid State  
Division

# Digital Integrated Circuits

Monolithic Silicon

**CD4040AD CD4040AE**  
**CD4040AF CD4040AK**



## COS/MOS 12-Stage Ripple-Carry Binary Counter/Divider

### Features:

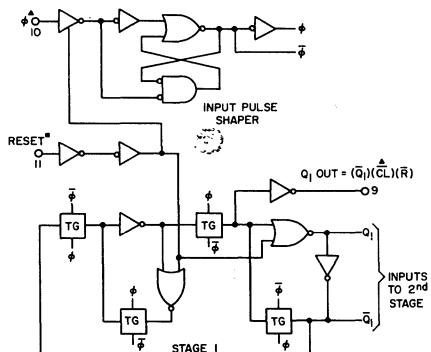
- Medium-speed operation . . . . . 5-MHz (typ.) input pulse rate at  $V_{DD}-V_{SS} = 10$  V
- Low "high"- and "low"- level output impedance . . . . . 750 Ω (typ.) at  $V_{DD}-V_{SS} = 10$  V and  $V_{DS} = 0.5$  V
- Common reset
- Fully static operation
- All 12 buffered outputs available
- Low-power TTL compatible

RCA-CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

The CD4040A is supplied in a 16-lead dual-in-line ceramic welded-seal package (CD4040AD), a 16-lead dual-in-line plastic package (CD4040AE), a 16-lead dual-in-line ceramic frit-seal package (CD4040AF), or a 16-lead flat pack (CD4040AK).

### Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Control counters



92CM-20748RI

Fig. 1 — Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

### MAXIMUM RATINGS, Absolute-Maximum Values:

Storage-Temperature Range . . . . .  $-65$  to  $+150$  °C

Operating-Temperature Range:

Ceramic-Package Types . . . . .  $-55$  to  $+125$  °C

Plastic-Package Types . . . . .  $-40$  to  $+85$  °C

DC Supply-Voltage Range:

$(V_{DD} - V_{SS})$  . . . . .  $-0.5$  to  $+15$  V

Device Dissipation (Per Package) . . . . . 200 mW

All Inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$

Recommended

DC Supply-Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V

Recommended

Input-Voltage Swing . . . . .  $V_{DD}$  to  $V_{SS}$

Lead Temperature (During Soldering)

At distance  $1/16'' \pm 1/32''$  (1.59 ± 0.79 mm)  
from case for 10 s max. . . . . +265°C

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS
				CD4040AD, CD4040AK, CD4040AF										
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-55°C			25°C			125°C				
Quiescent Device Current	I <sub>L</sub>		5	—	—	15	—	0.5	15	—	—	900	μA	13
			10	—	—	25	—	1	25	—	—	1500		
Quiescent Device Dissipation Package	P <sub>D</sub>		5	—	—	75	—	2.5	75	—	—	4500	μW	13
			10	—	—	250	—	10	250	—	—	15000		
Output Voltage: Low Level	V <sub>OL</sub>	Fanout of 50	5	—	—	0.01	—	0	0.01	—	—	0.05	V	
			10	—	—	0.01	—	0	0.01	—	—	0.05		
High Level	V <sub>OH</sub>	COS/MOS Inputs	5	4.99	—	—	4.99	5	—	4.95	—	—	V	
			10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (All Inputs)	V <sub>NL</sub>		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	V	11,12
			1	10	3	—	—	3	4.5	—	2.9	—		
	V <sub>NH</sub>		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—		
			9	10	2.9	—	—	3	4.5	—	3	—		
Output Drive Current: n-Channel	I <sub>DN</sub>		0.5	5	0.22	—	—	0.145	0.36	—	0.102	—	mA	2,4
			0.5	10	0.44	—	—	0.4	0.75	—	0.250	—		
p-Channel	I <sub>DP</sub>		4.5	5	-0.15	—	—	-0.1	-0.25	—	-0.07	—	mA	3,5
			9.5	10	-0.3	—	—	-0.25	-0.5	—	0.175	—		
Input Current	I <sub>I</sub>	Any Input	—	—	—	—	—	10	—	—	—	—	pA	

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS
				CD4040AE										
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-40°C			25°C			85°C				
Quiescent Device Current	I <sub>L</sub>		5	—	—	50	—	1	50	—	—	700	μA	13
			10	—	—	100	—	2	100	—	—	1400		
Quiescent Device Dissipation Package	P <sub>D</sub>		5	—	—	250	—	5	250	—	—	3500	μW	13
			10	—	—	1000	—	20	1000	—	—	14000		
Output Voltage: Low Level	V <sub>OL</sub>	Fanout of 50	5	—	—	0.01	—	0	0.01	—	—	0.05	V	
			10	—	—	0.01	—	0	0.01	—	—	0.05		
High Level	V <sub>OH</sub>	COS/MOS Inputs	5	4.99	—	—	4.99	5	—	4.95	—	—	V	
			10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (All Inputs)	V <sub>NL</sub>		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	V	11,12
			1	10	3	—	—	3	4.5	—	2.9	—		
	V <sub>NH</sub>		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—		
			9	10	2.9	—	—	3	4.5	—	3	—		
Output Drive Current (Q, Q̄ Outputs): n-Channel	I <sub>DN</sub>		0.5	5	0.21	—	—	0.08	0.36	—	0.056	—	mA	2,4
			0.5	10	0.42	—	—	0.2	0.75	—	0.14	—		
p-Channel	I <sub>DP</sub>		4.5	5	-0.145	—	—	-0.06	-0.25	—	-0.4	—	mA	3,5
			9.5	10	-0.29	—	—	-0.15	-0.5	—	-0.1	—		
Input Current	I <sub>I</sub>	Any Input	—	—	—	—	—	10	—	—	—	—	pA	

**DYNAMIC ELECTRICAL CHARACTERISTICS, At  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0V$ ,  $C_L = 15 \mu\text{F}$  (unless otherwise specified), and input rise and fall times = 20 ns, except  $t_rCL$  and  $t_fCL$ . Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{^{\circ}C}$ .**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	CD4040AK, AD, AF			CD4040AE			UNITS	NOTE
			V <sub>DD</sub>	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
<i>Input-Pulse Operation</i>										
Propagation Delay Time	$t_{PHL}$ , $t_{PLH}$		5 10	— —	450 225 450	900	— —	450 225	950 475	ns
Transition Time	$t_{THL}$ , $t_{TLH}$		5 10	— —	150 75 150	300	— —	150 75	350 175	ns
Min. Input-Pulse Width	$t_{WL}$ , $t_{WH}$	$f = 100\text{KHz}$	5 10	— —	200 75	400 110	— —	200 75	500 125	ns
Input-Pulse Rise & Fall Time	$t_{r\phi}$ , $t_{f\phi}$		5 10	— —	— —	15 7.5	— —	— —	15 7.5	$\mu\text{s}$
Max. Input-Pulse Frequency	$f_\phi$		5 10	1 3.5	1.75 5	— —	0.9 3.25	1.75 5	— —	MHz
Input Capacitance	$C_I$	Any input		—	5	—	—	5	—	pF
<i>Reset Operation</i>										
Propagation Delay Time	$t_{PHL}$		5 10	— —	500 250	1000 500	— —	500 250	1250 600	ns
Minimum Reset Pulse Width	$t_{WH}$		5 10	— —	500 250	1000 500	— —	500 250	1250 600	ns

## NOTES:

1. Measured from the 50% level of the negative clock edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.

2. Maximum input rise or fall time for functional operation.  
3. Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12.).

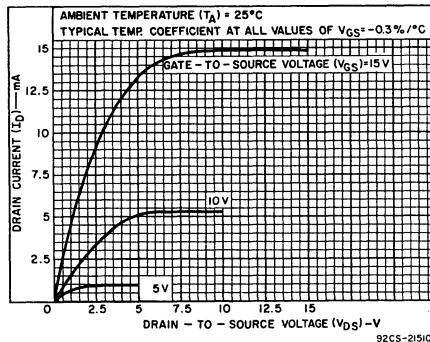


Fig.2 – Typical n-channel drain characteristics.

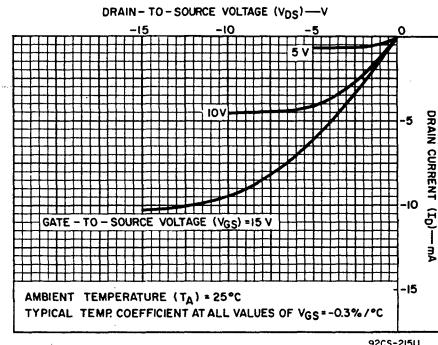


Fig.3 – Typical p-channel drain characteristics.

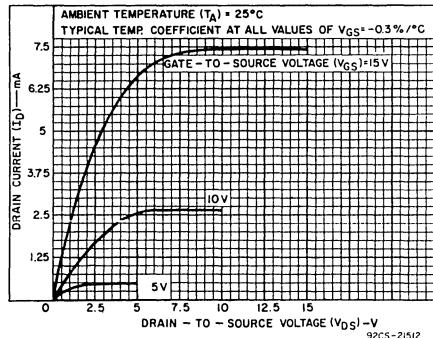


Fig.4 – Minimum n-channel drain characteristics.

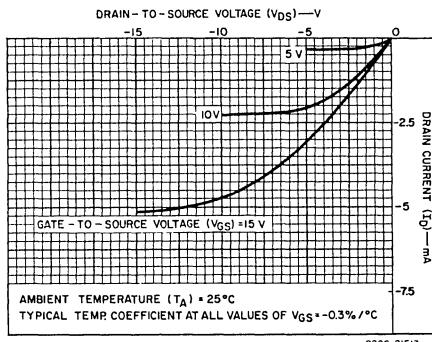


Fig.5 – Minimum p-channel drain characteristics.

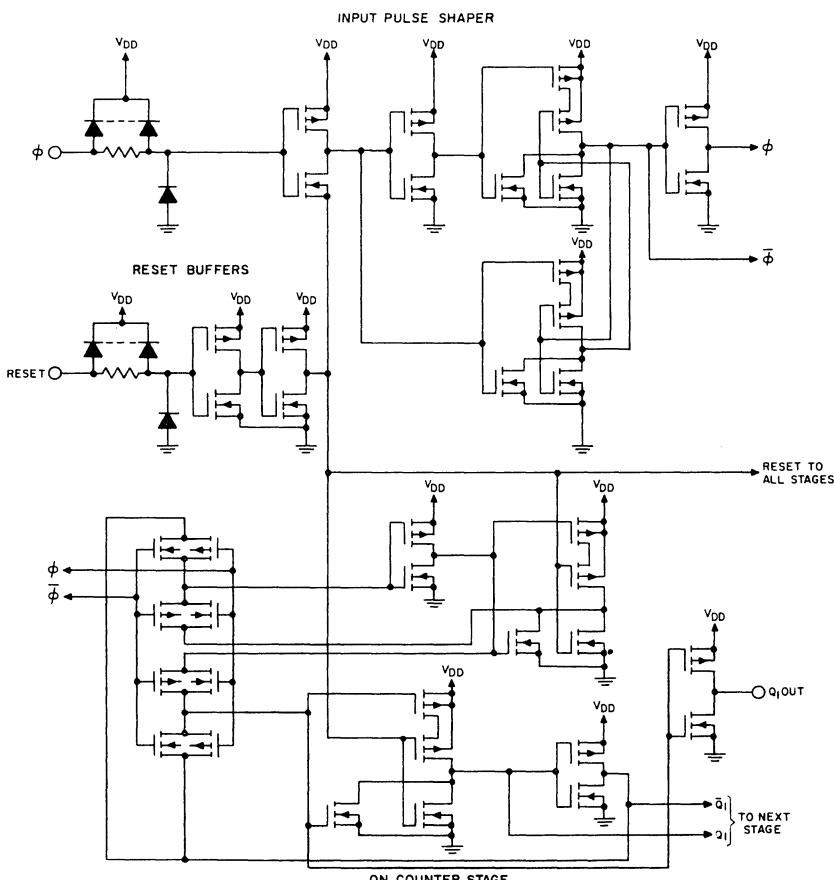


Fig.6 – Schematic diagram of input shaping, reset buffers, and one counter stage of CD4040A.

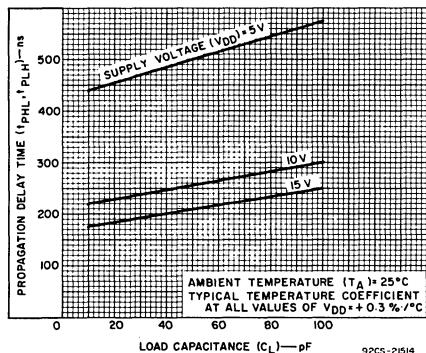


Fig. 7 – Typical propagation delay time vs. load capacitance (per stage.)

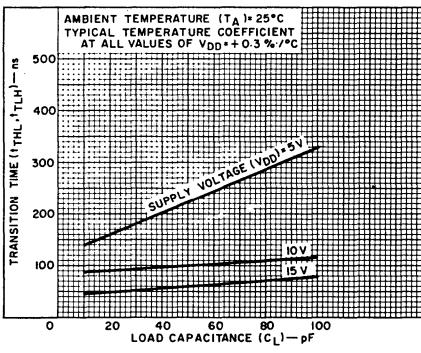


Fig. 8 – Typical transition time vs. load capacitance.

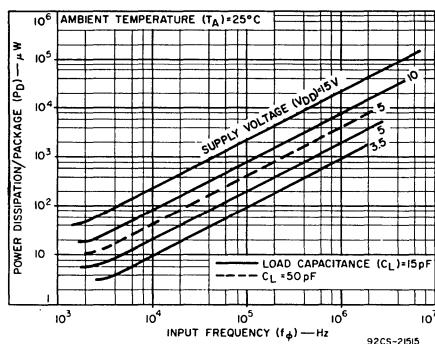


Fig. 9 – Typical dissipation characteristics.

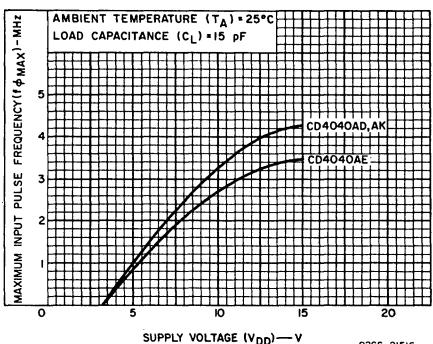


Fig. 10 – Maximum input-pulse frequency vs. supply voltage.

## TEST CIRCUITS

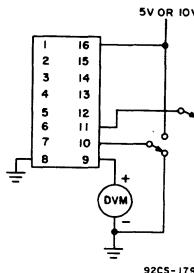


Fig. 11 – Reset-noise-immunity test circuit.

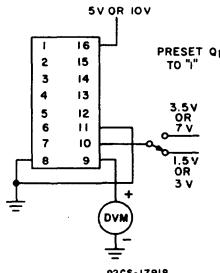


Fig. 12 – Input-pulse noise-immunity test circuit.

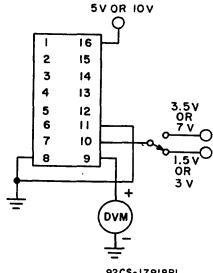


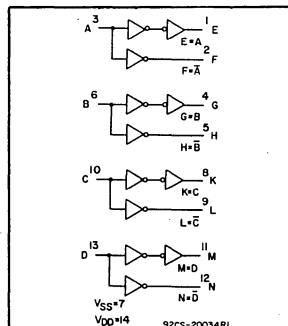
Fig. 13 – Quiescent-device-dissipation test circuit.

**RCA**  
Solid State  
Division

# Digital Integrated Circuits

Monolithic Silicon

## CD4041AD, CD4041AE, CD4041AK



RCA COS/MOS type CD4041A\* is a Quad True/Complement Buffer consisting of n- and p- channel units having low-channel resistance and high-current (sourcing and sinking) capability. The CD4041A is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

The CD4041A is supplied in a 14-lead dual-in-line ceramic package (CD4041AD), a 14-lead dual-in-line plastic package (CD4041AE), or a 14-lead flat pack (CD4041AK).

\*Formerly Dev. No. TA6031

### MAXIMUM RATINGS, Absolute-Maximum Values:

Storage Temperature Range .....	-65°C to +150	°C
Operating Temperature Range:		
Ceramic Package Types .....	-55°C to +125	°C
Plastic Package Types .....	-40°C to +85	°C
DC Supply Voltage Range		
(V <sub>DD</sub> - V <sub>SS</sub> ) .....	-0.5 V to +15	V
Device Dissipation (Per Pkg.) .....	200	mW
Average Dissipation Per Output .....	100	mW
Allowable Input Rise and Fall Time vs Supply and Frequency .....	See Fig. 17	
All Inputs .....	V <sub>SS</sub> < V <sub>I</sub> < V <sub>DD</sub>	
Recommended		
DC Supply Voltage (V <sub>DD</sub> - V <sub>SS</sub> ) ..	3 to 15	V
Input Voltage Swing .....	V <sub>DD</sub> to V <sub>SS</sub>	

## COS/MOS Quad True/Complement Buffer

### APPLICATIONS

- High Current Source/Sink Driver
- COS/MOS-to-DTL/TTL Converter
- Display Driver
- MOS Clock Driver
- Resistor Network Driver (Ladder or Weighted R)
- Buffer
- Transmission Line Driver

### Special Features

#### True Output

- High Current Source and Sink Capability  
8 mA (typ.) @ V<sub>DS</sub> = 0.5 V, V<sub>DD</sub> = 10 V  
3.2 mA (typ.) @ V<sub>DS</sub> = 0.4 V, V<sub>DD</sub> = 5 V (two TTL loads)

#### Complement Output

- Medium Current Source and Sink Capability  
3.6 mA (typ.) @ V<sub>DS</sub> = 0.5 V, V<sub>DD</sub> = 10 V  
1.6 mA (typ.) @ V<sub>DS</sub> = 0.5 V, V<sub>DD</sub> = 5 V

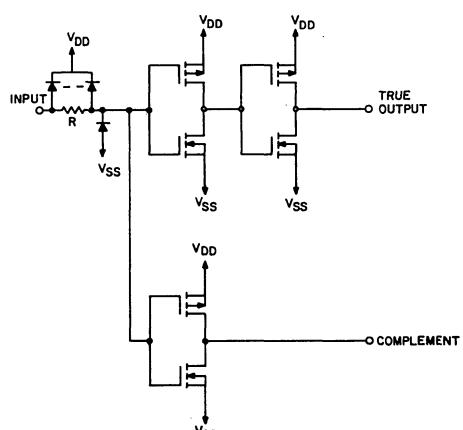
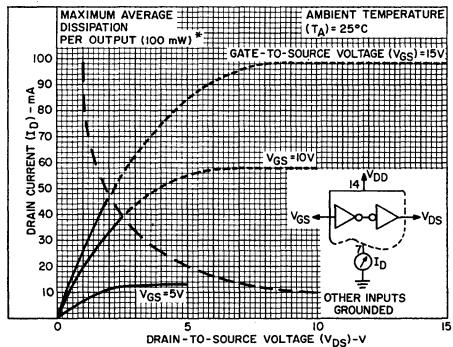


Fig. 1—CD4041A schematic diagram.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	CHARAC. TERISTIC CURVES & TEST CIRCUITS Fig. No.				
				CD4041AD, CD4041AK											
		$V_O$ Volts	$V_{DD}$ Volts	-55°C		25°C		125°C							
Quiescent Device Current	$I_L$			Min.	Max.	Min.	Typ.	Max.	Min.	Max.					
	Inputs to Ground or $V_{DD}$		5	-	1	-	0.005	1	-	60	$\mu A$	19			
Quiescent Device Dissipation/Package			$P_D$	10	-	2	-	0.005	2	-	120	$\mu W$			
Output Voltage: Low-Level	$V_{OL}$	Fan-out of 50 COS/MOS Inputs		5	-	0.01	-	0	0.01	-	0.05	V	10, 11		
				10	-	0.01	-	0	0.01	-	0.05	V			
High-Level	$V_{OH}$			5	4.99	-	4.99	5	-	4.95	-	V	10, 11		
				10	9.99	-	9.99	10	-	9.95	-	V			
Noise Immunity ● (All Inputs) <i>For definition, see Appendix</i>	$V_{NL}$			0.95	5	1.5	-	1.5	2.25	-	1.4	V	20		
				2.9	10	3	-	3	4.5	-	2.9	V			
	$V_{NH}$			3.6	5	1.4	-	1.5	2.25	-	1.5	V	20		
				7.2	10	2.9	-	3	4.5	-	3	V			
Output Drive Current: N-Channel	$I_{DN}$		True Output	0.4	5	2.1	-	1.6	3.2	-	1.2	-	2, 6,		
				0.5	10	6.25	-	5	10	-	3.5	-			
	$I_{DN}$			0.5	5	1	-	0.8	1.6	-	0.55	-	4, 8,		
				0.5	10	2.5	-	2	4	-	1.4	-			
P-Channel	$I_{DP}$		True Output	4.5	5	-1.75	-	-1.4	-2.8	-	-1	-	3, 7,		
				9.5	10	-5	-	-4	-8	-	-2.8	-			
	$I_{DP}$			4.5	5	-0.75	-	-0.6	-1.2	-	-0.4	-	5, 9,		
				9.5	10	-2.25	-	-1.8	-3.6	-	-1.25	-			
Input Current	$I_I$	Any Input		-	-	--	10	-	-	-	-	pA			

● Values shown are for true output.



\*SEE FIG. 17 FOR TRANSITION TIME LIMITATIONS

92CS-20036

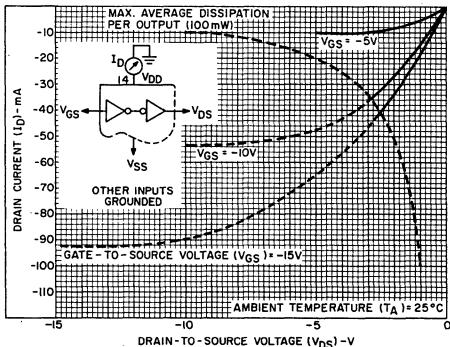


Fig. 2—Typical n-channel drain characteristics—true output.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS								CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
			CD4041AE											
			$V_O$ Volts		$V_{DD}$ Volts		-40°C		25°C		85°C			
Quiescent Device Current	$I_L$	Inputs to Ground or $V_{DD}$		5	-	10	--	0.01	10	-	140	$\mu A$	19	
				10	-	20	--	0.02	20	-	280			
Quiescent Device Dissipation/Package	$P_D$			5	-	50	--	0.05	50	-	700	$\mu W$		
				10	-	200	--	0.2	200	-	2800			
Output Voltage: Low-Level	$V_{OL}$	Fan-out of 50 COS/MOS Inputs		5	-	0.01	-	0	0.01	--	0.05	V	10, 11	
				10	-	0.01	-	0	0.01	--	0.05			
High-Level	$V_{OH}$			5	4.99	-	4.99	5	--	4.95	-	V	10, 11	
				10	9.99	-	9.99	10	--	9.95	-			
Noise Immunity ● (All Inputs) <i>For definition, see Appendix</i>	$V_{NL}$		0.95	5	1.5	-	1.5	2.25	-	1.4	-	V	20	
			2.9	10	3	-	3	4.5	-	2.9	-			
	$V_{NH}$		3.6	5	1.4	-	1.5	2.25	-	1.5	-	V	20	
			7.2	10	2.9	-	3	4.5	-	3	-			
Output Drive Current:	$I_{DN}$	True Output	0.4	5	1	-	0.8	3.2	-	0.7	-	mA	2, 6,	
			0.5	10	3	-	2.5	10	-	2.2	-			
		Complement Output	0.5	5	0.5	-	0.4	1.6	-	0.35	-	mA	4, 8,	
			0.5	10	1.2	-	1	4	-	0.9	-			
P-Channel	$I_{DP}$	True Output	4.5	5	-0.85	-	-0.7	-2.8	--	-0.6	-	mA	3, 7,	
			9.5	10	-2.4	-	-2	-8	-	-1.8	-			
		Complement Output	4.5	5	-0.35	--	-0.3	-1.2	-	-0.27	-	mA	5, 9,	
			9.5	10	-1.1	-	-0.9	-3.6	-	-0.8	-			
Input Current	$I_I$	Any Input	-	-	-	-	10	--	--	--	--	pA		

● Values shown are for true output.

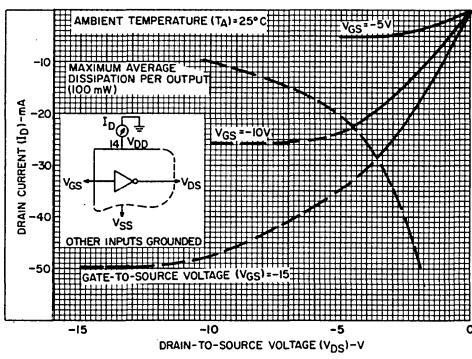
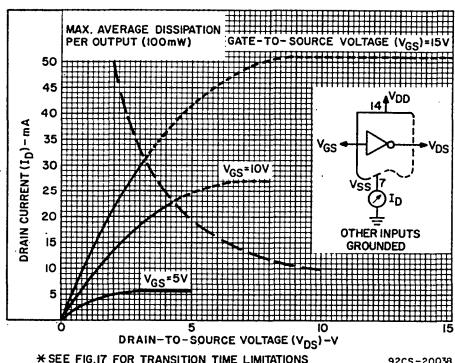


Fig. 4—Typical n-channel drain characteristics-complement output.

Fig. 5—Typical p-channel drain characteristics-complement output.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  and  $C_L = 15\text{pF}$ Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{C}$ 

(See Appendix for Waveforms)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			$V_{DD}$ (Volts)	CD4041AD, CD4041AK			CD4041AE				
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>	True Output	5	—	65	115	—	65	140	ns	—
		Complement Output	10	—	40	75	—	40	100		
	t <sub>PLH</sub>	True Output	5	—	55	100	—	55	125	ns	—
		Complement Output	10	—	30	45	—	30	65		
Low-to-High Level	t <sub>PLH</sub>	True Output	5	—	75	125	—	75	150	ns	14
		Complement Output	10	—	45	75	—	45	100		
	t <sub>THL</sub>	True Output	5	—	45	100	—	45	125	ns	15
		Complement Output	10	—	25	40	—	25	60		
Transition Time: High-to-Low Level	t <sub>THL</sub>	True Output	5	—	20	40	—	20	60	ns	12
		Complement Output	10	—	13	25	—	13	40		
	t <sub>TLH</sub>	True Output	5	—	40	60	—	40	80	ns	13
		Complement Output	10	—	25	40	—	25	50		
Input Capacitance	C <sub>I</sub>	Any Input	—	—	5	—	—	5	—	pF	—

DYNAMIC ELECTRICAL CHARACTERISTICS (Driving TTL,DTL) AT  $T_A = 25^\circ\text{C}$ ,  $V_{DD}-V_{SS} = 5\text{V}$ ,  $C_L = 15\text{pF}$  (True Output)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES Fig. No.	
			Driving TTL,DTL	CD4041AD CD4041AK			CD4041AE				
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Propagation Delay Time: High-To-Low Level	t <sub>PHL</sub>	$R_L = 2\text{k}\Omega$	Med. Power	—	75	150	—	75	175	ns	—
		$R_L = 20\text{k}\Omega$	Low Power	—	75	150	—	75	175		
	t <sub>PLH</sub>	$R_L = 2\text{k}\Omega$	Med. Power	—	85	175	—	85	200	ns	—
		$R_L = 20\text{k}\Omega$	Low Power	—	85	175	—	85	200		
Transition Time	t <sub>THL</sub> = t <sub>TLH</sub>	$R_L = 2\text{k}\Omega$	Med. Power	—	20	50	—	20	75	ns	—
		$R_L = 20\text{k}\Omega$	Low Power	—	20	50	—	20	75		

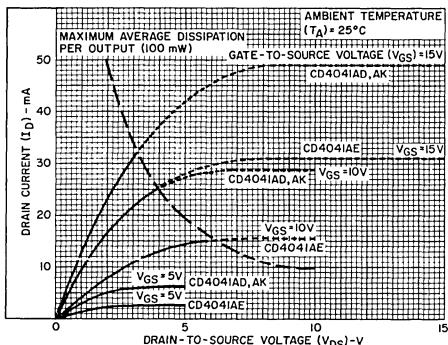


Fig. 6—Minimum n-channel drain characteristics—true output.

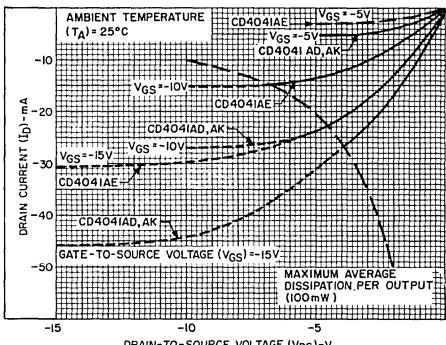


Fig. 7—Minimum p-channel drain characteristics—true output.

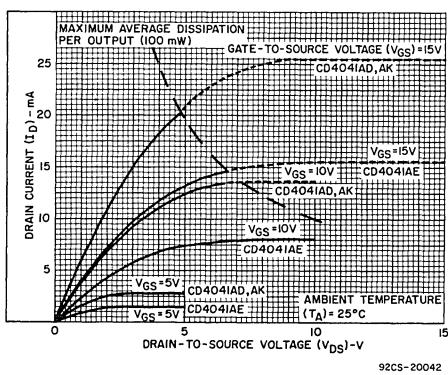


Fig. 8—Minimum n-channel drain characteristics—complement output.

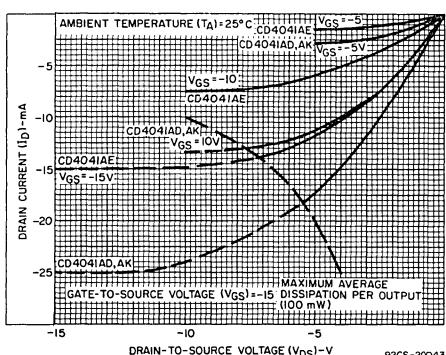


Fig. 9—Minimum p-channel drain characteristics—complement output.

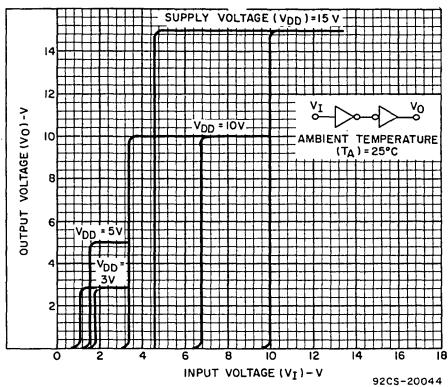


Fig. 10—Minimum and maximum transfer characteristics—true output.

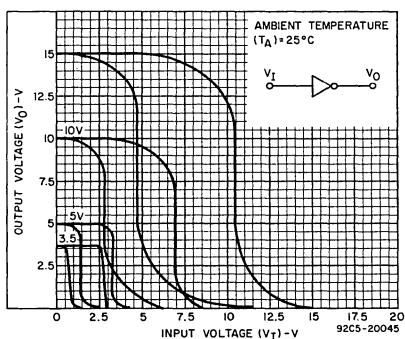


Fig. 11—Minimum and maximum transfer characteristics—complement output.

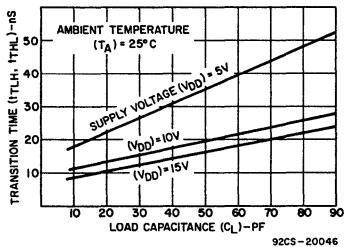


Fig. 12—Typical transition time vs.  
 $C_L$ -true output.

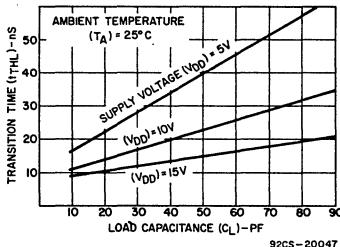


Fig. 13—Typical high-to-low level  
transition time vs.  $C_L$ -complement output.

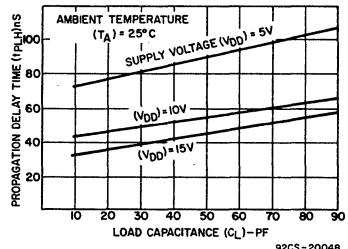


Fig. 14—Typical low-to-high level  
propagation delay time vs.  
 $C_L$ -true output.

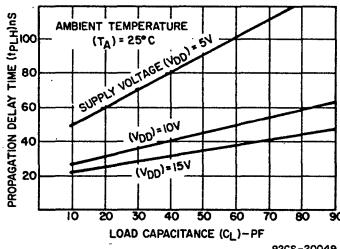


Fig. 15—Typical low-to-high level  
propagation delay time vs.  
 $C_L$ -complement output.

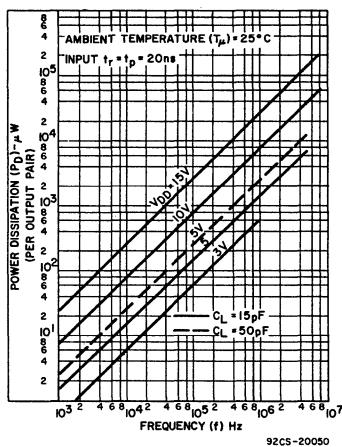


Fig. 16—Typical power dissipation vs.  
frequency per output pair.

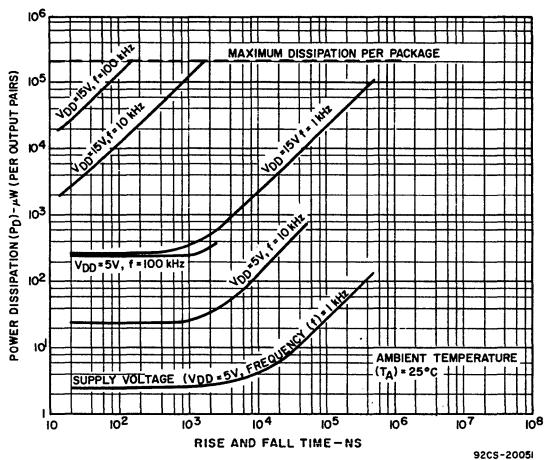


Fig. 17—Typical power dissipation vs.  
input rise and fall time per  
output pair.

## TYPICAL APPLICATIONS

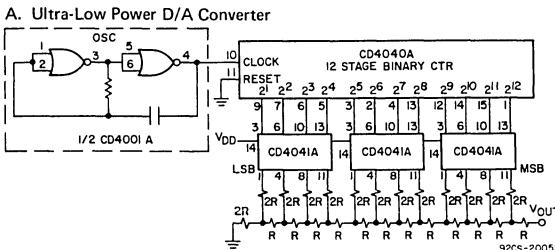


Fig. 18—D/A converter block diagram.

For resolution and accuracy of  $\pm 1/2$  least significant bit (LSB), choose the values for R (shown in Table I) where R equals the value of the external ladder resistor plus the switch source impedance.

These values have been tabulated for  $V_{DD} = 5V$  and  $V_{SS} = 0V$ . For different supply (reference) voltages, the switch source impedance must be computed and added to the value of R shown in Table I.

TABLE I. RESISTANCE VALUES AT  $V_{DD}-V_{SS} = 5V$ ,  $T_A = 25^\circ C$ 

RESOLUTION	ACCURACY OF 1/2 LSB	$R_{min}$ ( $\Omega$ )
4 bit	$\pm 3.25\%$ of full scale	3.5 k
6 bit	$\pm 0.8\%$ of full scale	14 k
8 bit	$\pm 0.2\%$ of full scale	56 k
10 bit	$\pm 0.05\%$ of full scale	224 k
12 bit	$\pm 0.0125\%$ of full scale	896 k

TABLE II. ON RESISTANCE VALUES AT  $V_{DS} = 0.1V$ ,  $T_A = 25^\circ C$ 

$V_{DD}-V_{SS}$ (Volts)	$R_N$ ( $\Omega$ )	$R_P$ ( $\Omega$ )
5	$175 \pm 50$	$200 \pm 75$
10	$75 \pm 25$	$90 \pm 30$

## B. Transmission Line Driver

Drive 100 pF load at 75 ns delay (typ.)  $V_{DD}-V_{SS} = 10V$

## C. CD4031A (64-Stage Static Shift Register) Clock Driver (80pF Load)

$t_r = t_f = 40$  ns (typ.),  $V_{DD}-V_{SS} = 10V$

## TEST CIRCUITS

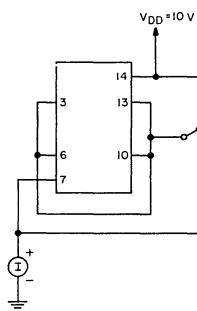


Fig. 19—Quiescent device current.

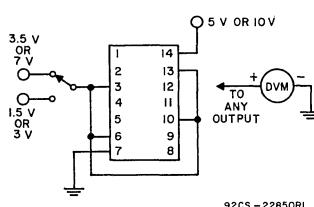
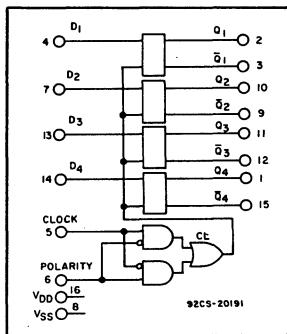


Fig. 20—Noise immunity.



# Digital Integrated Circuits

Monolithic Silicon

**CD4042AD, CD4042AE  
CD4042AF, CD4042AK**


RCA-CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the N- and P-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs  $Q$  and  $\bar{Q}$  during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

CD4042A types are supplied in 16-lead ceramic flat-packs, plastic dual-in-line packages, and both welded-seal and frit-seal ceramic dual-in-line packages.

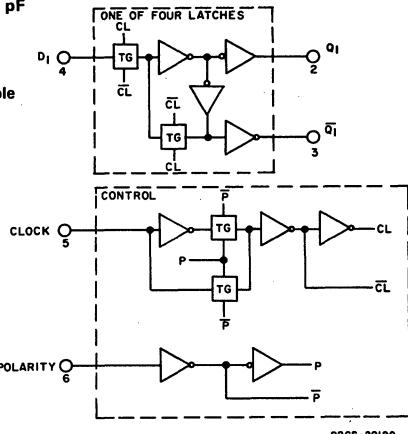
## COS/MOS Quad Clocked "D" Latch

### Special Features:

- Medium Speed Operation ...  
 $t_{PHL} = t_{PLH} = 50 \text{ ns (typ)}$  at  $V_{DD} = 10 \text{ V}$  and  $C_L = 15 \text{ pF}$
- Clock Polarity Control
- $Q$  and  $\bar{Q}$  Outputs
- Common Clock
- Low Power TTL Compatible

### Applications:

- Buffer Storage
- Holding Register
- General Digital Logic



CLOCK	POLARITY	Q
0	0	D
—	0	LATCH
1	1	D
—	1	LATCH

Fig.1—Logic block diagram & truth table.

### MAXIMUM RATINGS, Absolute-Maximum Values:

Storage Temperature Range: . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

Operating Temperature Range:

Ceramic Package Types . . . . .  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Plastic Package Types . . . . .  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

DC Supply Voltage Range

$(V_{DD} - V_{SS})$  . . . . .  $-0.5 \text{ V}$  to  $+15 \text{ V}$

Device Dissipation (Per Pkg.) . . . . .  $200 \text{ mW}$

All Inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$

Recommended DC Supply Voltage

$(V_{DD} - V_{SS})$  . . . . . 3 to 15  $\text{V}$

Recommended Input Voltage Swing . . . . .  $V_{DD}$  to  $V_{SS}$

Lead Temperature (During Soldering):

At distance  $1/16 \pm 1/32 \text{ in.}$  ( $1.59 \pm 0.79 \text{ mm}$ )

from case for 10s max. . . . .  $+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS								UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4042AD, CD4042AK, CD4042A											
			-55°C		25°C		125°C							
		$V_{DD}$ Volts	Min.	Max.	Min.	Typ.	Max.	Min.	Max.					
Quiescent Device Current	$I_L$	Inputs to Ground or $V_{DD}$	5	—	1	—	0.005	1	—	60	$\mu A$	8		
			10	—	2	—	0.005	2	—	120				
Quiescent Device Dissipation/Package	$P_D$	5	—	5	—	0.025	5	—	300	$\mu W$	—			
			10	—	20	—	0.05	20	—	1200				
Output Voltage: Low-Level	$V_{OL}$	Fan-out of 50 COS/MOS Inputs	5	—	0.01	—	0	0.01	—	0.05	V	—		
			10	—	0.01	—	0	0.01	—	0.05				
High-Level	$V_{OH}$	5	4.99	—	4.99	5	—	4.95	—	—	V	—		
			10	9.99	—	9.99	10	—	9.95	—				
Noise Immunity ♦ (All Inputs) For Definition, See Application	$V_{NL}$	$V_O = 0.95V$	5	1.5	—	1.5	2.25	—	1.4	—	V	9		
		$V_O = 2.9V$	10	3	—	3	4.5	—	2.9	—				
	$V_{NH}$	$V_O = 3.6 V$	5	1.4	—	1.5	2.25	—	1.5	—	V	—		
		$V_O = 7.2V$	10	2.9	—	3	4.5	—	3	—				
Output Drive Current: N-Channel	$I_{DN}$	$V_O = 0.5V$	5	0.5	—	0.4	1	—	0.27	—	mA	2, 4		
		$V_O = 0.5V$	10	1.25	—	1	2	—	0.7	—				
P-Channel	$I_{DP}$	$V_O = 4.5V$	5	-0.45	—	-0.35	-1	—	-0.25	—	mA	3, 5		
		$V_O = 9.5V$	10	-1.15	—	-0.9	-2	—	-0.6	—				
Input Current	$I_I$	Any Input	—	—	—	—	10	—	—	..	pA	—		

♦ For inverter output only.

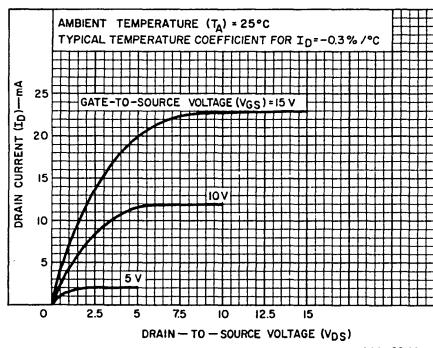


Fig.2—Typ. n-channel drain characteristics.

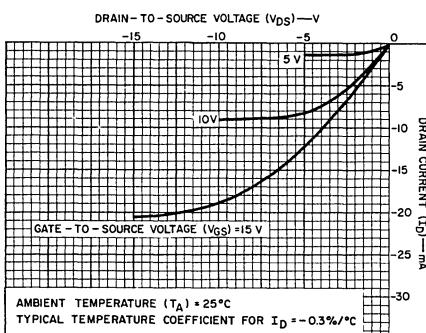
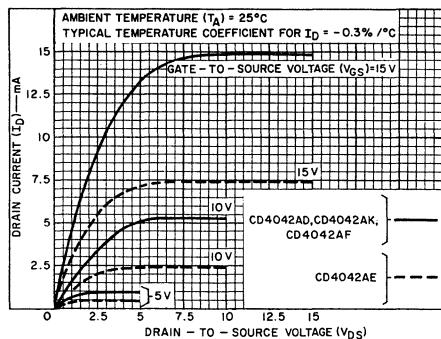


Fig.3—Typ. p-channel drain characteristics.

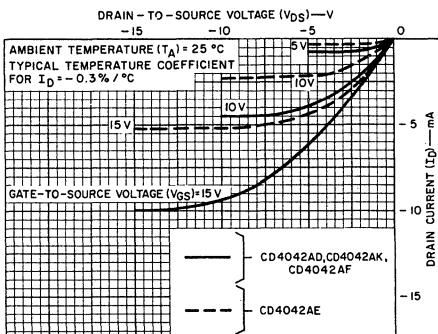
STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS								CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS		
			CD4042AE											
			V <sub>DD</sub> Volts	-40°C		25°C		85°C						
Quiescent Device Current	I <sub>L</sub>	Inputs to Ground or V <sub>DD</sub>		Min.	Max.	Min.	Typ.	Max.	Min.	Max.				
		5	—	10	—	0.01	10	—	140	μA	8			
Quiescent Device Dissipation/Package	P <sub>D</sub>	Fan-out of 50 COS/MOS Inputs	10	—	20	—	0.02	20	—	280	μW	—		
			5	—	50	—	0.05	50	—	700	—	—		
Output Voltage: Low-Level	V <sub>OL</sub>	Fan-out of 50 COS/MOS Inputs	10	—	200	—	0.2	200	—	2800	—	—		
			5	—	0.01	—	0	0.01	—	0.05	V	—		
High-Level	V <sub>OH</sub>	Fan-out of 50 COS/MOS Inputs	10	—	0.01	—	0	0.01	—	0.05	V	—		
			5	4.99	—	4.99	5	—	4.95	—	V	—		
Noise Immunity ♦ (All Inputs)	V <sub>NL</sub>	V <sub>O</sub> = 0.95V	5	1.5	—	1.5	2.25	—	1.4	—	V	—		
			10	3	—	3	4.5	—	2.9	—	V	9		
	V <sub>NH</sub>	V <sub>O</sub> = 3.6 V	5	1.4	—	1.5	2.25	—	1.5	—	V	—		
			10	2.9	—	3	4.5	—	3	—	V	—		
Output Drive Current: N-Channel	I <sub>DN</sub>	V <sub>O</sub> = 0.5V	5	0.24	—	0.2	1	—	0.18	—	mA	2, 4		
			10	0.6	—	0.5	2	—	0.45	—	mA	—		
P-Channel	I <sub>DP</sub>	V <sub>O</sub> = 4.5V	5	-0.2	—	-0.175	-1	—	-0.15	—	mA	—		
			10	-0.34	—	-0.45	-2	—	-0.4	—	mA	3, 5		
Input Current	I <sub>I</sub>	Any Input	—	—	—	—	10	—	—	—	pA	—		

♦ For inverter output only.



92CS-201B8



92CS-201B9

Fig.4—Min. n-channel drain characteristics.

Fig.5—Min. p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{pF}$ , and input rise and fall times = 20 ns.  
 Typical Temperature Coefficient for all values of  $V_{DD}$  =  $0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)  
 except  $t_{fCL}$  and  $t_{fCL}$ .

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4042AD, CD4042AK CD4042AF			CD4042AE						
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.			
			5	—	150	300	—	150	400	ns	—	
Propagation Delay Time	$t_{PHL}$ , $t_{PLH}$			10	—	75	125	—	75			
				5	—	100	200	—	100			
Transition Time	$t_{THL}$ , $t_{TLH}$			10	—	50	100	—	50			
				5	—	175	250	—	175			
Minimum Clock Pulse Width	$t_{WL}$ , $t_{WH}$			10	—	50	75	—	50			
				5	—	—	15	—	15			
Clock Rise & Fall Time	$t_{fCL}$ , $t_{fCL}$			10	—	—	5	—	5			
				5	—	50	100	—	50			
Set-Up Time				10	—	25	50	—	25			
				5	—	—	50	—	125			
Input Capacitance	$C_1$		—	—	5	—	—	5	—	pF	—	

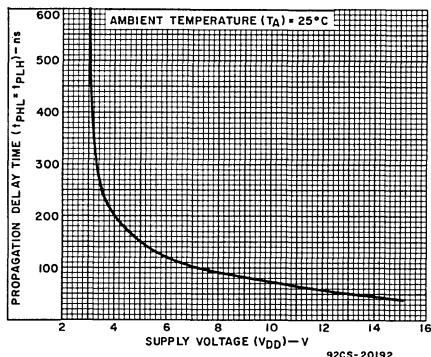
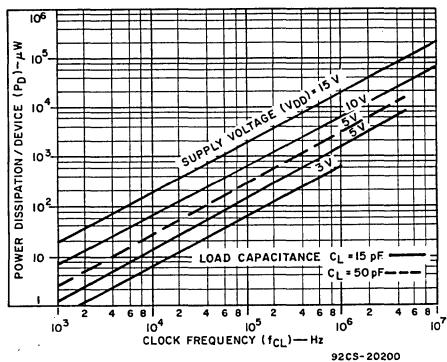
Fig.6—Typical propagation delay time vs.  $V_{DD}$ .

Fig.7—Typical dissipation characteristics.

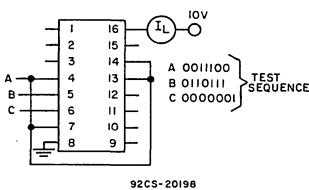


Fig.8 — Quiescent device current.

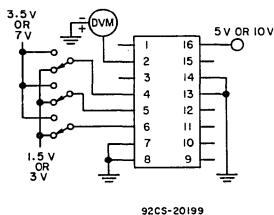


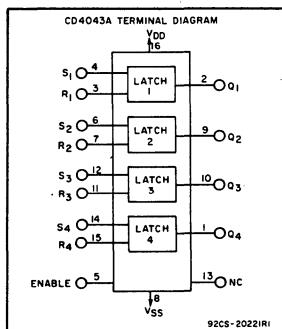
Fig.9 — Noise Immunity



# Digital Integrated Circuits

Monolithic Silicon

## CD4043AD, CD4043AE, CD4043AK, CD4044AD, CD4044AE, CD4044AK



### COS/MOS Quad 3-State R/S Latches

Quad NOR R/S Latch – CD4043A  
Quad NAND R/S Latch - CD4044A

#### Special Features:

- Medium Speed Operation
- 3-Level Outputs with Common Output Enable
- Separate Set and Reset Inputs for Each Latch
- Low Power TTL Compatible
- NOR and NAND Configurations

#### Applications:

- Holding Register in Multi-Register System
- Four Bits of Independent Storage with Output Enable
- Strobed Register
- General Digital Logic

RCA-CD4043A types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044A types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are gated through transmission gates controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE input connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the

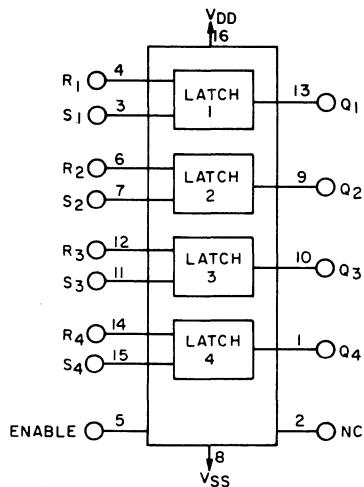
latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs. The logic operation of the latches is summarized in the truth table below shown in Fig.1.

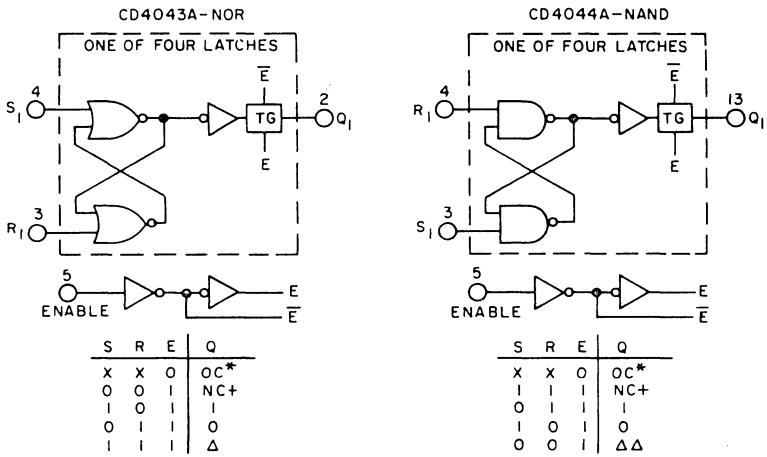
The CD4043A and CD4044A are supplied in 16-lead dual-in-line ceramic packages (CD4043AD and CD4044AD), 16-lead ceramic flat packs (CD4043AK and CD4044AK), and 16-lead dual-in-line plastic packages (CD4043AE, CD4044AE).

#### MAXIMUM RATINGS, Absolute-Maximum Values:

Storage Temperature Range: . . . . .	-65°C to +150	°C
Operating Temperature Range: . . . . .		
Ceramic Package Types . . . . .	-55°C to +125	°C
Plastic Package Types . . . . .	-40°C to +85	°C
DC Supply Voltage Range . . . . .		
(V <sub>DD</sub> - V <sub>SS</sub> ) . . . . .	-0.5 V to +15	V
Device Dissipation (Per Pkg.) . . . . .	200	mW
All Inputs . . . . .	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	
Recommended DC Supply Voltage . . . . .		
(V <sub>DD</sub> - V <sub>SS</sub> ) . . . . .	3 to 15	V
Recommended Input Voltage Swing . . . . .	V <sub>DD</sub> to V <sub>SS</sub>	
Lead Temperature (During Soldering: . . . . .		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max. . . . .	+265	°C

#### CD4044A TERMINAL DIAGRAM





92CS-2021I

Fig.1 – Logic diagrams &amp; truth tables.

92CS-2021I

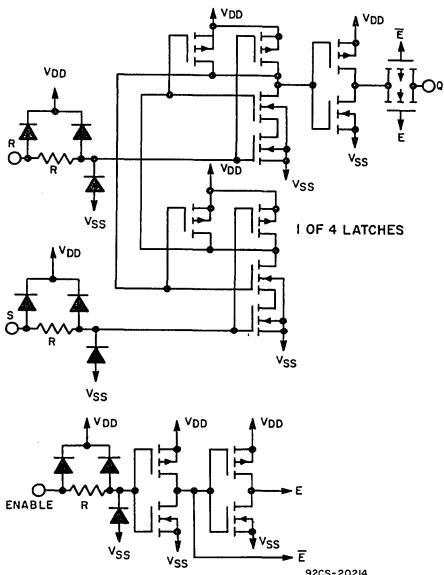
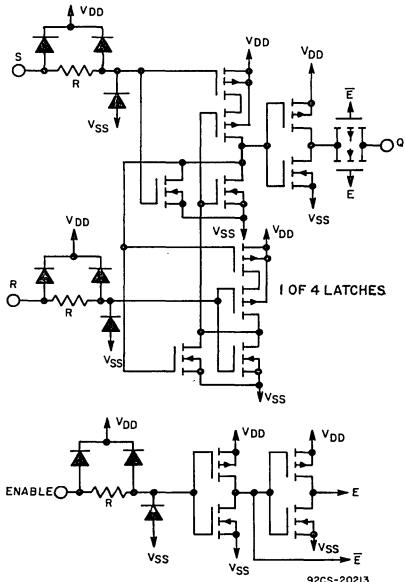
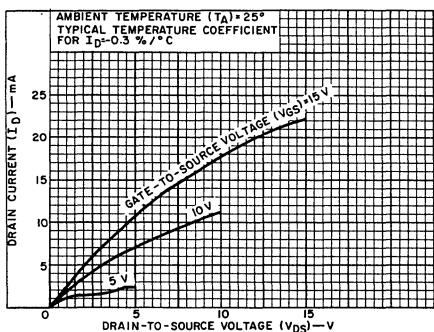


Fig.2–Schematic diagram—CD4043A.

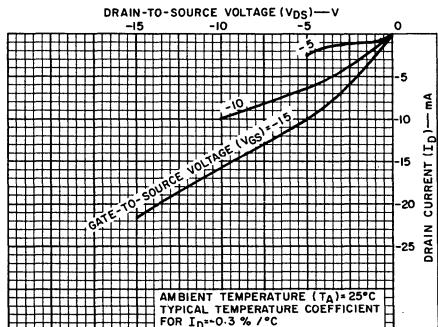
Fig.3–Schematic diagram—CD4044A.

**STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No		
			CD4043AD, CD4043AK, CD4044AD, CD4044AK											
			$-55^{\circ}\text{C}$		$25^{\circ}\text{C}$		$125^{\circ}\text{C}$							
Quiescent Device Current	$I_L$	Inputs to Ground or $V_{DD}$	5	—	1	—	0.005	1	—	60	$\mu\text{A}$	11		
			10	—	2	—	0.005	2	—	120				
Quiescent Device Dissipation/Package	$P_D$	5	—	5	—	0.025	5	—	300	$\mu\text{W}$	—			
			10	—	20	—	0.05	20	—	1200				
Output Voltage: Low-Level	$V_{OL}$	Fan-out of 50 COS/MOS Inputs	5	—	0.01	—	0	0.01	—	0.05	$\text{V}$	—		
			10	—	0.01	—	0	0.01	—	0.05				
High-Level	$V_{OH}$	5	4.99	—	4.99	5	—	4.95	—	9.95	$\text{V}$	—		
			10	9.99	—	9.99	10	—	9.95	—				
Noise Immunity (All Inputs)	$V_{NL}$	$V_O = 0.95\text{V}$	5	1.5	—	1.5	2.25	—	1.4	—	$\text{V}$	12		
			10	3	—	3	4.5	—	2.9	—				
<i>For definition, see Appendix</i>	$V_{NH}$	$V_O = 3.6\text{V}$	5	1.4	—	1.5	2.25	—	1.5	—	$\text{V}$	—		
			10	2.9	—	3	4.5	—	3	—				
Output Drive Current: N-Channel	$I_{DN}$	$V_O = 0.5\text{V}$	5	0.25	—	0.2	0.5	—	0.14	—	$\text{mA}$	4,6		
			10	0.61	—	0.5	1	—	0.35	—				
P-Channel	$I_{DP}$	$V_O = 4.5\text{V}$	5	-0.22	—	-0.175	-0.5	—	-0.12	—	$\text{mA}$	5,7		
			10	-0.5	—	-0.4	-1	—	-0.28	—				
Input Current	$I_I$	Any Input	—	—	—	—	10	—	—	—	$\mu\text{A}$	—		



92CS-20215



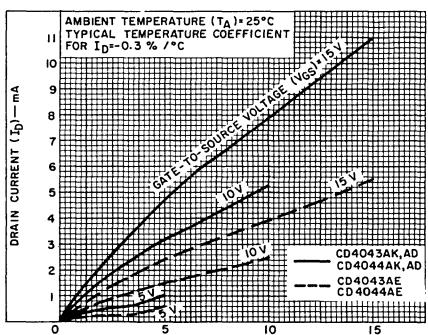
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Fig.4—Typ. n-channel drain characteristics.

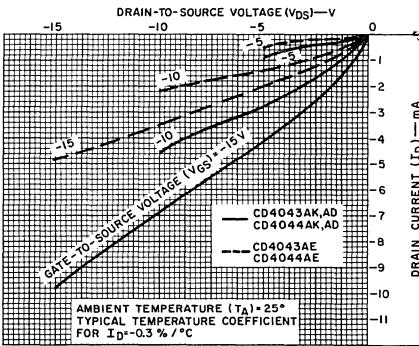
Fig.5—Typ. p-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS (All inputs ..... V<sub>SS</sub> ≤ V<sub>I</sub> ≤ V<sub>DD</sub>)  
 (Recommended DC Supply Voltage (V<sub>DD</sub> - V<sub>SS</sub>) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS								CHARACTERISTIC CURVES & TEST CIRCUITS Fig No	
			CD4043AE, CD4044AE									
			V <sub>DD</sub> Volts		-40°C		25°C		85°C			
Quiescent Device Current	I <sub>L</sub>	Inputs to Ground or V <sub>DD</sub>	5	—	10	—	0.01	10	—	140	μA	11
			10	—	20	—	0.02	20	—	280		
Quiescent Device Dissipation/Package	P <sub>D</sub>	V <sub>DD</sub>	5	—	50	—	0.05	50	—	700	μW	—
			10	—	200	—	0.2	200	—	2800		
Output Voltage: Low-Level	V <sub>OL</sub>	Fan-out of 50 COS/MOS Inputs	5	—	0.01	—	0	0.01	—	0.05	V	—
			10	—	0.01	—	0	0.01	—	0.05		
High-Level	V <sub>OH</sub>	V <sub>O</sub> = 0.95V	5	4.99	—	4.99	5	—	4.95	—	V	—
			10	9.99	—	9.99	10	—	9.95	—		
Noise Immunity (All Inputs) For Definition See Appendix	V <sub>NL</sub>	V <sub>O</sub> = 2.9V	5	1.5	—	1.5	2.25	—	1.4	—	V	12
			10	3	—	3	4.5	—	2.9	—		
	V <sub>NH</sub>	V <sub>O</sub> = 3.6V	5	1.4	—	1.5	2.25	—	1.5	—	V	—
			10	2.9	—	3	4.5	—	3	—		
Output Drive Current N-Channel	I <sub>DN</sub>	V <sub>O</sub> = 0.5V	5	0.12	—	0.1	0.5	—	0.09	—	mA	4, 6,
		V <sub>O</sub> = 0.5V	10	0.3	—	0.25	1	—	0.22	—		
P-Channel	I <sub>DP</sub>	V <sub>O</sub> = 4.5V	5	-0.11	—	-0.09	-0.5	—	-0.08	—	mA	5, 7,
		V <sub>O</sub> = 9.5V	10	-0.24	—	-0.2	-1	—	-0.18	—		
Input Current	I <sub>I</sub>	Any Input	—	—	—	—	10	—	—	—	pA	—



92CS-20217



92CS-20218

Fig. 6—Min. n-channel drain characteristics.

Fig. 7—Min. p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 15\text{pF}$ , and input rise and fall times = 20 ns, except  $t_rCL$  and  $t_fCL$ .

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARAC-TERISTIC CURVES	
			CD4043AD, CD4043AK CD4044AD, CD4044AK			CD4043AE, CD4044AE					
			V <sub>DD</sub> (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time	$t_{PHL}$ , $t_{PLH}$		5	—	175	350	—	175	400	ns	8
			10	—	75	175	—	75	200		
Transition Time	$t_{THL}$ , $t_{TLH}$		5	—	100	200	—	100	250	ns	9
			10	—	50	100	—	50	125		
Minimum Set and Reset Pulse Width	$t_{WH(S)}$ , $t_{WH(R)}$		5	—	80	200	—	80	225	ns	—
Input Capacitance	$C_I$		10	—	40	100	—	40	110	pF	—

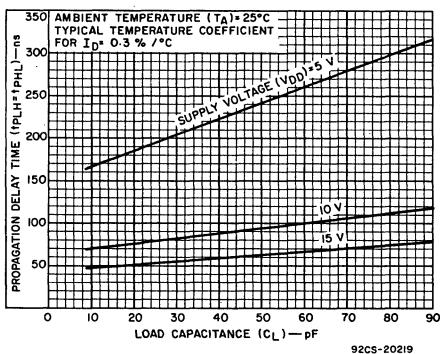


Fig.8—Typ. propagation delay time vs.  $C_L$ .

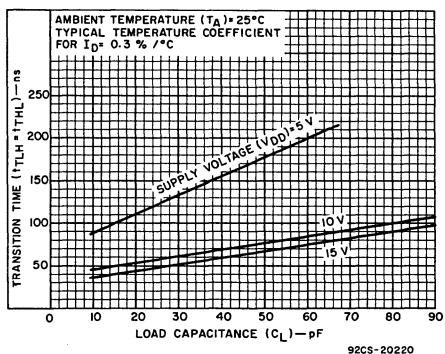


Fig.9—Typ. transition time vs.  $C_L$ .

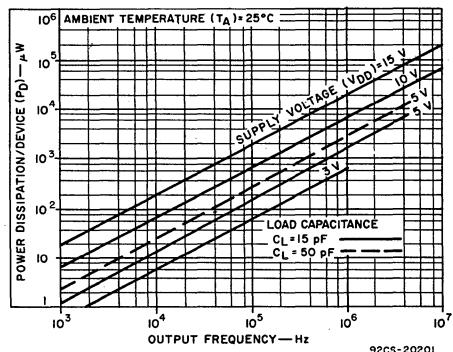


Fig.10—Typ. dissipation characteristics.

## TEST CIRCUITS

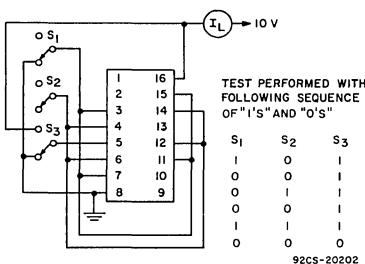


Fig. 11—Quiescent current.

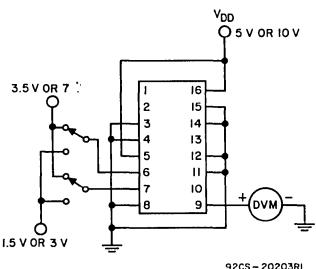


Fig. 12—Noise immunity.

## TYPICAL APPLICATIONS

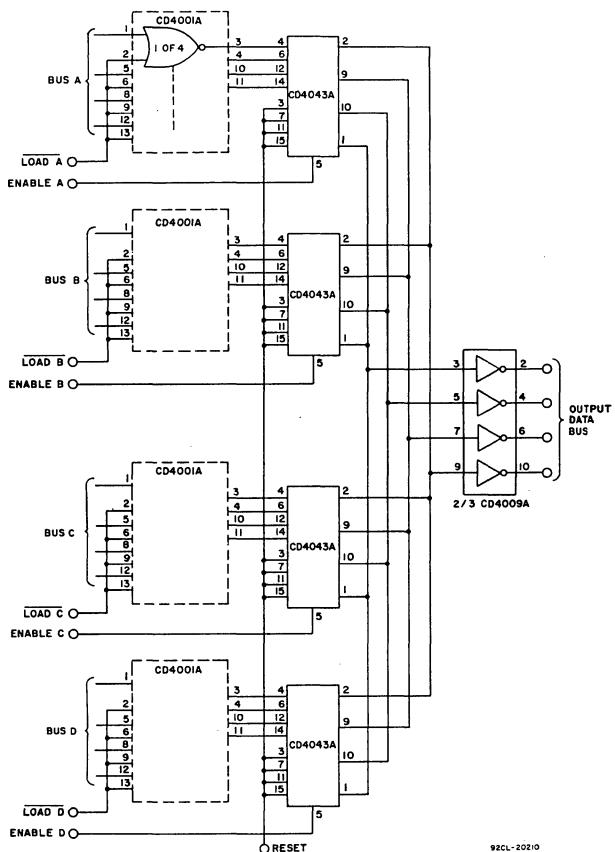
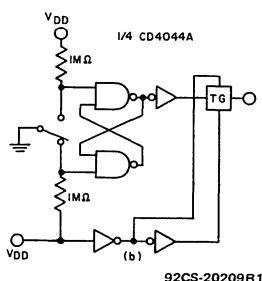
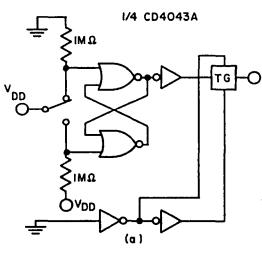


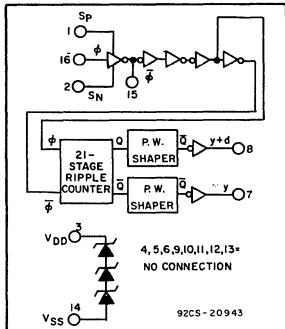
Fig. 13—Switch bounce eliminator.

Fig. 14—Multiple bus storage.



# Digital Integrated Circuits

Monolithic Silicon

**CD4045AK CD4045AE CD4045AD**


## COS/MOS 21-Stage Counter

### Applications:

- Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
- Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.
- Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.

RCA-CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip flops, two inverter output drivers, three 5.5 V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. This device may be operated over a 3 to 15 V supply voltage range. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired.

A crystal oscillator circuit can be made less sensitive to voltage supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective

### Features:

- Operation from 3 to 15 volts
- Microwatt quiescent dissipation . . . . .  
2.5  $\mu$ W (typ.) @ V<sub>DD</sub> = 5V; 10  $\mu$ W (typ.) @ V<sub>DD</sub> = 10V
- Very-low operating dissipation . . . . .  
1 mW (typ.); @ V<sub>DD</sub> = 5 V, f<sub>φ</sub> = 1 MHz
- Output drivers with sink or source capability. . . . .  
7 mA (typ.) @ V<sub>O</sub> = 0.5 V, V<sub>DD</sub> = 5 V (sink)  
5 mA (typ.) @ V<sub>O</sub> = 4.5 V, V<sub>DD</sub> = 5 V (source)
- Medium speed (typ.). . . . . f<sub>φ</sub> = 5 MHz @ V<sub>DD</sub> = 5 V  
f<sub>φ</sub> = 10 MHz @ V<sub>DD</sub> = 10 V
- 16.5 V zener diode transient protection  
on chip for automotive use

substrates (Sp to V<sub>DD</sub>, SN to V<sub>SS</sub>). See Fig. 1.

CD4045A types are supplied in a 16-lead flat pack, and in both 16-lead ceramic and plastic dual-in-line packages.

### Maximum Ratings, Absolute-Maximum Values:

Storage-Temperature Range . . . . . -65°C to +150°C

Operating-Temperature Range:

Ceramic packages . . . . . -55°C to +125°C

Plastic package . . . . . -40°C to + 85°C

DC Supply Voltage Range (V<sub>DD</sub> - V<sub>SS</sub>) . . . . . -0.5 to +15 V

Device Dissipation:

(per package, including zener diodes) . . . . . 200 mW

All Inputs . . . . . V<sub>SS</sub> ≤ V<sub>I</sub> ≤ V<sub>DD</sub>

Recommended DC Supply

Voltage Range (V<sub>DD</sub> - V<sub>SS</sub>) . . . . . 3 to 15 V

Recommended Input Voltage Swing . . . . . V<sub>DD</sub> to V<sub>SS</sub>

Peak Zener Diode Current

(decay  $\tau$  = 80 ms) . . . . . 150 mA

### Lead Temperature (During soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)  
from case for 10 seconds max. . . . . 265 °C

**NOTE 1:** To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150  $\Omega$  current-limiting resistor must be placed in series with the power supply for V<sub>DD</sub> > 13 V.

**NOTE 2:** Observe power supply terminal connections. V<sub>DD</sub> is terminal No.3 and V<sub>SS</sub> is terminal No.14 (not 16 and 8 respectively, as in all other CD4000A Series 16-lead devices).

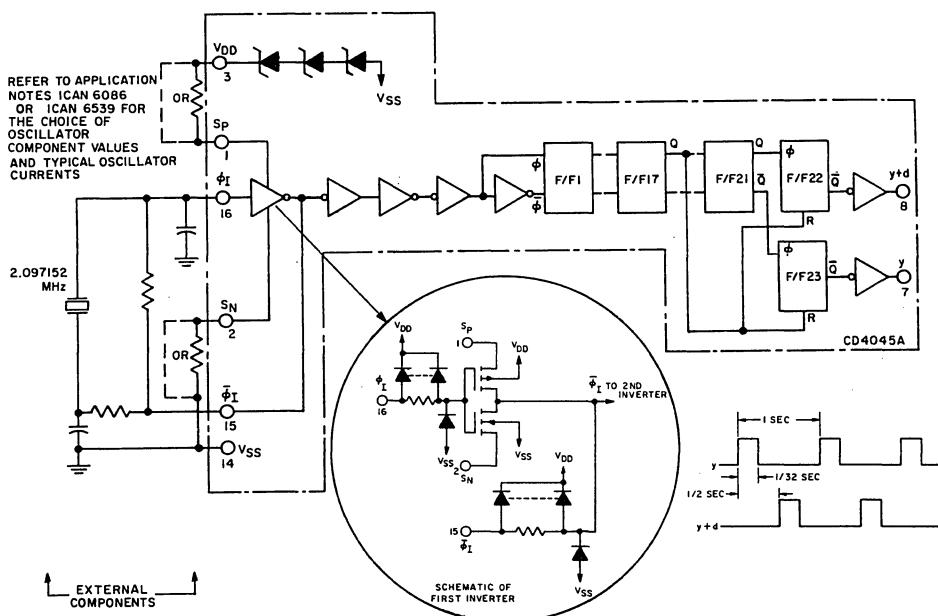


Fig. 1—CD4045A and outboard components in a typical 21-stage counter application.

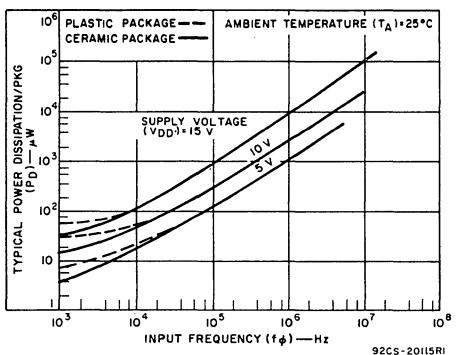


Fig. 2—Typical dissipation vs input frequency (21 counting stages).

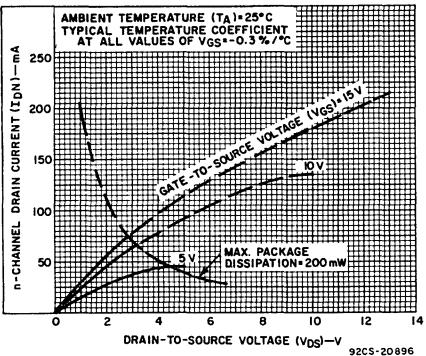


Fig. 3—Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS								UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4045AD, CD4045AK											
			$-55^\circ\text{C}$		$25^\circ\text{C}$		$125^\circ\text{C}$							
Quiescent Device Current	$I_L$		5	—	15	—	0.5	15	—	900	$\mu\text{A}$	11		
			10	—	25	—	1	25	—	1500				
Quiescent Device Dissipation/Package	$P_D$		5	—	0.075	—	0.0025	0.075	—	4.5	$\text{mW}$			
			10	—	0.25	—	0.01	0.25	—	15				
Output Voltage: Low-Level	$V_{OL}$	Driving COS/MOS	5	—	0.01	—	0	0.01	—	0.05	$\text{V}$			
			10	—	0.01	—	0	0.01	—	0.05				
High-Level	$V_{OH}$		5	4.99	—	4.99	5	—	4.95	—	$\text{V}$	12		
			10	9.99	—	9.99	10	—	9.95	—				
Noise Immunity (All Inputs)	$V_{NL}$		5	1.5	—	1.5	2.25	—	1.4	—	$\text{V}$	12		
			10	3	—	3	4.5	—	2.9	—				
	$V_{NH}$		5	1.4	—	1.5	2.25	—	1.5	—				
			10	2.9	—	3	4.5	—	3	—				
Output Drive Current N-Channel	$I_{DN}$		0.5	5	4.4	—	3.5	7	—	2.5	$\text{mA}$			
			0.5	10	6.9	—	5.5	11	—	3.9				
P-Channel	$I_{DP}$		4.5	5	-3.1	—	-2.5	-5	—	-1.8	$\text{mA}$			
			9.5	10	-5.6	—	-4.5	-9	—	-3.2				
Input Current	$I_I$		—	—	—	—	10	—	—	—	$\text{pA}$			
Zener Breakdown Voltage	$V_{(BR)Z}$	$I = 100 \mu\text{A}$	13.3	17.8	13.5	16.5	18	13.7	18.2	V		7		

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS								UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.		
			CD4045AE											
			$-40^\circ\text{C}$		$25^\circ\text{C}$		$85^\circ\text{C}$							
Quiescent Device Current	$I_L$		5	—	50	—	1	50	—	700	$\mu\text{A}$	11		
			10	—	100	—	2	100	—	1400				
Quiescent Device Dissipation/Package	$P_D$		5	—	0.25	—	0.005	0.25	—	3.5	$\text{mW}$			
			10	—	1	—	0.02	1	—	14				
Output Voltage: Low-Level	$V_{OL}$	Driving COS/MOS	5	—	0.01	—	0	0.01	—	0.05	$\text{V}$			
			10	—	0.01	—	0	0.01	—	0.05				
High-Level	$V_{OH}$		5	4.99	—	4.99	5	—	4.95	—	$\text{V}$	12		
			10	9.99	—	9.99	10	—	9.95	—				
Noise Immunity (All Inputs)	$V_{NL}$		5	1.5	—	1.5	2.25	—	1.4	—	$\text{V}$	12		
			10	3	—	3	4.5	—	2.9	—				
	$V_{NH}$		5	1.4	—	1.5	2.25	—	1.5	—				
			10	2.9	—	3	4.5	—	3	—				
Output Drive Current N-Channel	$I_{DN}$		0.5	5	2.2	—	1.8	7	—	1.3	$\text{mA}$			
			0.5	10	3.5	—	2.8	11	—	2.0				
P-Channel	$I_{DP}$		4.5	5	-1.6	—	-1.3	-5	—	-0.9	$\text{mA}$			
			9.5	10	-2.8	—	-2.3	-9	—	-1.6				
Input Current	$I_I$		—	—	—	—	10	—	—	—	$\text{pA}$			
Zener Breakdown Voltage	$V_{(BR)Z}$	$I = 100 \mu\text{A}$	13.3	17.8	13.5	16.5	18	13.6	18.1	V		7		

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns, except  $t_{r\phi}$  and  $t_{f\phi}$ .  
 Typical Temperature Coefficient for all values of  $V_{DD}$  =  $0.3\%/\text{ }^\circ\text{C}$ .

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4045AD, CD4045AK			CD4045AE					
			$V_{DD}$ (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time $\phi_I$ to $y$ or $y+d$ out	$t_{PHL}$ $t_{PLH}$		5	2.2	4.4	5.5	2.2	5.5	5.5	$\mu\text{s}$	8
	$t_{THL}$ $t_{TLH}$		10	1.2	2.4	3.3	1.2	3.3	3.3		
Transition Time	$t_{WHL}$ $t_{WH}$		5	450	800	900	450	900	900	$\text{ns}$	9
	$t_{WLH}$ $t_{WH}$		10	375	650	750	375	750	750		
Minimum Input-Pulse Width	$t_{WHL}$ $t_{WH}$		5	100	115	140	100	140	140	$\text{ns}$	
	$t_{WLH}$ $t_{WH}$		10	50	60	75	50	75	75		
Input Pulse Rise & Fall Time	$t_{r\phi}$ $t_{f\phi}$		5		15		15		15	$\mu\text{s}$	
	$t_{r\phi}$ $t_{f\phi}$		10		10		10		10		
Maximum Input-Pulse Frequency	$f_{m\phi}$		5	4.4	5	5	3.5	5	5	$\text{MHz}$	10
	$f_{m\phi}$		10	8.5	10	10	6.5	10	10		
Input Capacitance	$C_I$	Any Input		5			5		5	$\text{pF}$	

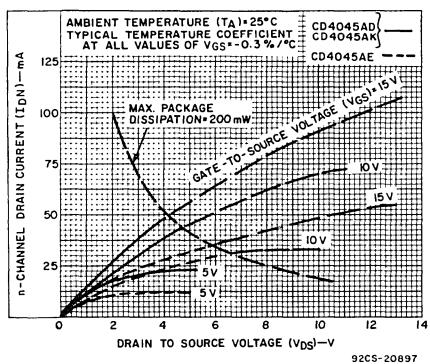


Fig. 4—Minimum n-channel drain characteristics.

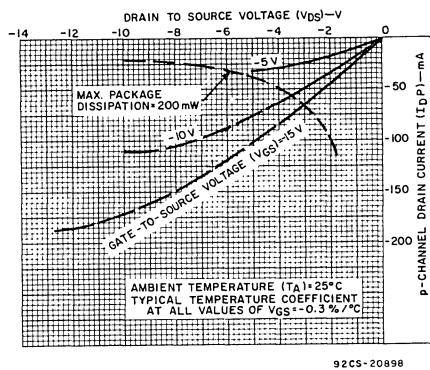


Fig. 5—Typical p-channel drain characteristics.

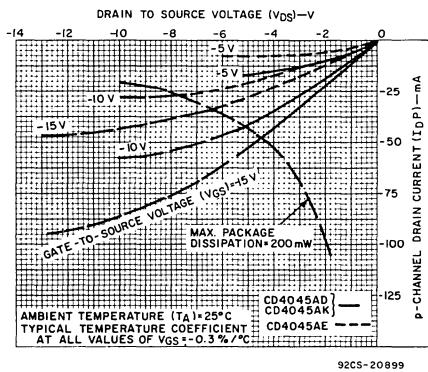


Fig. 6—Minimum p-channel drain characteristics.

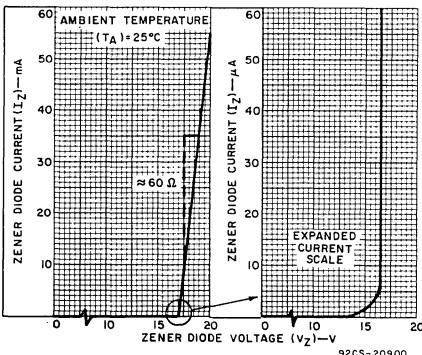


Fig. 7—Typical zener diode characteristics.

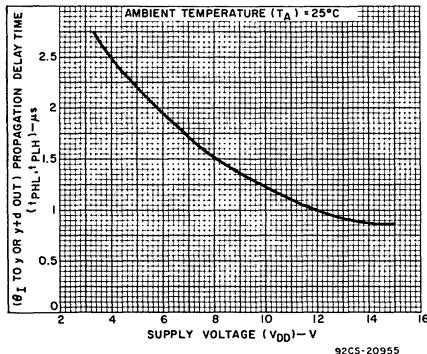
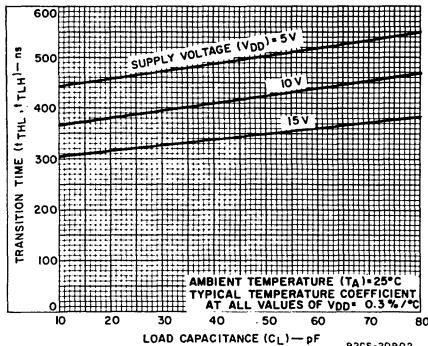
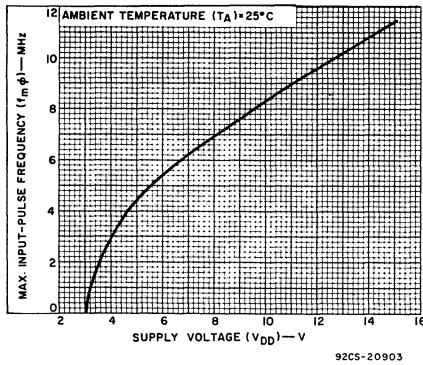
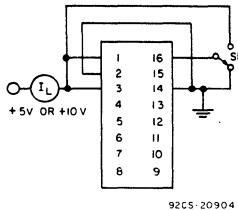
Fig. 8—Typical propagation delay ( $t_{\phi_1}$  to  $y$  or  $y+d$  out) vs  $V_{DD}$ .Fig. 9—Typical transition time vs  $C_L$ .Fig. 10—Minimum  $f_{m\phi}$  vs  $V_{DD}$  for CD4045AD and CD4045AK.

Fig. 11—Quiescent device current test circuit.

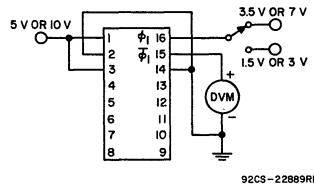
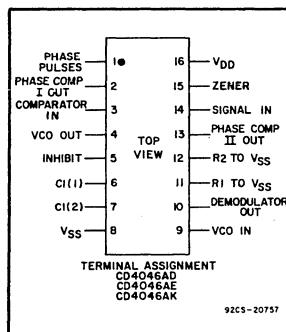


Fig. 12—Noise immunity test circuit.



# COS/MOS Micropower Phase-Locked Loop

#### *Features:*



The RCA-CD4046A COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary. The CD4046A is supplied in a 16-lead dual-in-line ceramic package (CD4046AD), a 16-lead dual-in-line plastic package (CD4046AE), and a 16-lead flat pack (CD4046AK). It is also available in chip form (CD4046AH).

## VCO Section

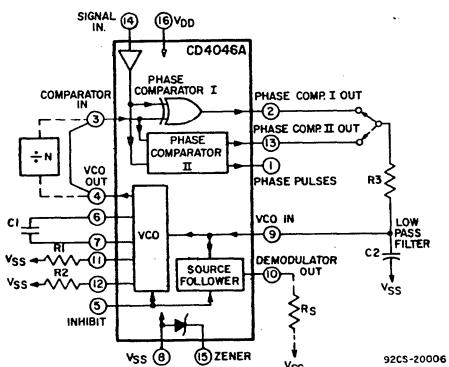
The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ( $10^2\Omega$ ) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor ( $R_S$ ) of  $10\text{k}\Omega$  or more should be connected from this terminal to  $V_{SS}$ . If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024A, CD4018A, CD4020A, CD4022A, or CD4029A. One or more CD4018A (Presettable Divide-by-N Counter) or CD4029A (Presettable Up/Down Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micro-power low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

- Source-follower output of VCO control input  
(Demod. output)
  - Zener diode to assist supply regulation

### *Applications:*

- FM demodulator and modulator
  - Frequency synthesis and multiplication
  - Frequency discriminator
  - Data synchronization
  - Voltage-to-frequency conversion
  - Tone decoding
  - FSK – Modems
  - Signal conditioning

(See ICAN-6101 for application information and circuit details)



*Fig. 1 – COS/MOS phase-locked loop block diagram*

### Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0"  $\leq$  30% ( $V_{DD}$ - $V_{SS}$ ), logic "1"  $\geq$  70% ( $V_{DD}$ - $V_{SS}$ )]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to  $V_{DD}/2$ . The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency ( $f_0$ ).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ( $2f_c$ ).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ( $2f_L$ ). The capture range is  $\leq$  the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response charac-

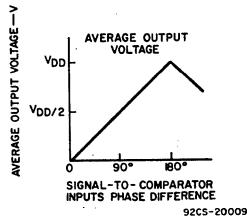


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

teristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of  $f_0$  is shown in Fig. 3.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to  $V_{DD}$  or down to  $V_{SS}$ , respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The

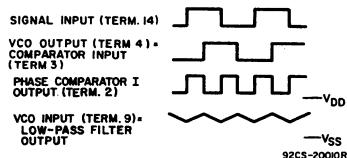
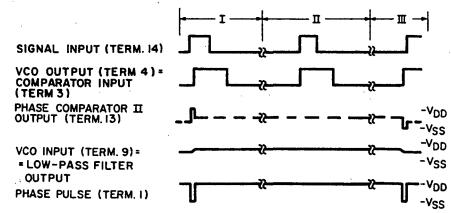


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of  $f_0$ .

duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.



NOTE: DASHED LINE IS AN OPEN-CIRCUIT CONDITION  
Fig.4 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

**DESIGN INFORMATION**

This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10 \text{ k}\Omega \leq R_1, R_2, R_S \leq 1 \text{ M}\Omega$

$C_1 \geq 100 \text{ pF at } V_{DD} \geq 5 \text{ V}$

$C_1 \geq 50 \text{ pF at } V_{DD} \geq 10 \text{ V}$

In addition to the given design information refer to Fig. 5 for  $R_1$ ,  $R_2$ , and  $C_1$  component selections.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, $f_0$		VCO in PLL system will adjust to lowest operating frequency, $f_{min}$	
Frequency Lock Range, $2f_L$	$2f_L = \text{full VCO frequency range}$ $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	$\frac{1}{\pi\sqrt{\frac{2\pi f_L}{T_1}}}$ $T_1 = R_3 C_2$	(1),(2)		
Loop Filter Component Selection	 $f_C = f_L$	For $2f_C$ , see Ref. (2)  $92CS-2190I$		
Phase Angle between Signal and Comparator	$90^\circ$ at center frequency ( $f_0$ ), approximating $0^\circ$ and $180^\circ$ at ends of lock range ( $2f_L$ )		Always $0^\circ$ in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	<ul style="list-style-type: none"> <li>- Given: <math>f_0</math></li> <li>- Use <math>f_0</math> with Fig.5a to determine <math>R_1</math> and <math>C_1</math></li> </ul>	<ul style="list-style-type: none"> <li>- Given: <math>f_0</math> and <math>f_L</math></li> <li>- Calculate <math>f_{min}</math> from the equation</li> <math display="block">f_{min} = f_0 - f_L</math> <li>- Use <math>f_{min}</math> with Fig. 5b to determine <math>R_2</math> and <math>C_1</math></li> <li>- Calculate <math>\frac{f_{max}}{f_{min}}</math> from the equation</li> <math display="block">\frac{f_{max}}{f_{min}} = \frac{f_0 + f_L}{f_0 - f_L}</math> <li>- Use <math>f_{min}</math> with Fig.5c to determine ratio <math>R_2/R_1</math> to obtain <math>R_1</math></li> </ul>	<ul style="list-style-type: none"> <li>- Given: <math>f_{max}</math></li> <li>- Calculate <math>f_0</math> from the equation</li> <math display="block">f_0 = \frac{f_{max}}{2}</math> <li>- Use <math>f_0</math> with Fig.5a to determine <math>R_1</math> and <math>C_1</math></li> </ul>	<ul style="list-style-type: none"> <li>- Given: <math>f_{min}</math> &amp; <math>f_{max}</math></li> <li>- Use <math>f_{min}</math> with Fig.5b to determine <math>R_2</math> and <math>C_1</math></li> <li>- Calculate <math>\frac{f_{max}}{f_{min}}</math></li> <li>- Use <math>f_{min}</math> with Fig.5c to determine ratio <math>R_2/R_1</math> to obtain <math>R_1</math></li> </ul>

For further information, see

(1) F. Gardner, "Phase-Lock Techniques", John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniatirized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.			
				CD4046AD, CD4046AK CD4046AE							
		MIN.	TYP.	MAX.							
<b>VCO Section</b>											
Operating Supply Voltage	V <sub>DD</sub> -V <sub>SS</sub>	As fixed oscillator only			3	—	15	V			
		Phase-lock-loop operation			5	—	15				
Operating Power Dissipation	P <sub>D</sub>	$f_0 = 10 \text{ kHz}$ $R_1 = 1 \text{ M}\Omega$ $R_2 = \infty$ $V_{COIN} = \frac{V_{DD}}{2}$	5	—	70	—	μW	6a			
			10	—	600	—					
			15	—	2400	—					
Maximum Operating Frequency	f <sub>MAX</sub>	$R_1 = 10 \text{ k}\Omega$ $R_2 = \infty$ $C_1 = 100 \text{ pF}$ $C_1 = 50 \text{ pF}$ $V_{COIN} = V_{DD}$	5	0.25	0.5	—	MHz	—			
			10	0.6	1.2	—					
			15	—	1.5	—					
Center Frequency and	f <sub>0</sub>	Programmable with external components R <sub>1</sub> , R <sub>2</sub> , and C <sub>1</sub>						See Design Info.			
Frequency Range	f <sub>MAX</sub> -f <sub>MIN</sub>										
Linearity	—	$V_{COIN} = 2.5 \text{ V} \pm 0.3 \text{ V}, R_1 > 10 \text{ k}\Omega$ $= 5 \text{ V} \pm 2.5 \text{ V}, R_1 > 400 \text{ k}\Omega$ $= 7.5 \text{ V} \pm 5 \text{ V}, R_1 = 1 \text{ M}\Omega$	5	—	1	—	%	8a,b			
			10	—	1	—					
			15	—	1	—					
Temperature-Frequency Stability : No Frequency Offset <u>f<sub>MIN</sub> = 0</u>	—	$\%/\text{^oC} \propto \frac{1}{f \cdot V_{DD}}$ $R_2 = \infty$	5	—	0.12-0.24	—	%/ $^\circ\text{C}$	—			
			10	—	0.04-0.08	—					
			15	—	0.015-0.03	—					
Frequency Offset <u>f<sub>MIN</sub> ≠ 0</u>	—	$\%/\text{^oC} \propto \frac{1}{f \cdot V_{DD}}$	5	—	0.06-0.12	—	%/ $^\circ\text{C}$	—			
			10	—	0.05-0.1	—					
			15	—	0.03-0.06	—					
Input Resistance of VCO <sub>IN</sub> (Term 9)	R <sub>I</sub>	Driving COS/MOS-Type Load (e.g. Term 3 Phase Comparator Input)			5,10,15	—	10 <sup>12</sup>	—	Ω	—	
VCO Output Voltage (Term 4) Low Level	V <sub>OL</sub>				5,10,15	—	—	0.01	V	—	
High Level	V <sub>OH</sub>				5	4.99	—	—			
					10	9.99	—	—			
					15	14.99	—	—			
VCO Output Duty Cycle		$t_{THL} - t_{TLH}$	V <sub>O</sub> VOLTS	5,10,15	—	50	—	%	—		
VCO Output Transition Times				5	—	75	150	ns	—		
				10	—	50	100				
				15	—	40	—				
VCO Output Drive Current: n-Channel (Sink)	I <sub>DN</sub>	$R_S > 10 \text{ k}\Omega$ $V_{COIN} = 2.5 \pm 0.3 \text{ V}$ $= 5 \pm 2.5 \text{ V}$ $= 7.5 \pm 5 \text{ V}$			0.5	5	0.43	0.86	mA	—	
p-Channel (Source)	I <sub>DP</sub>				0.5	10	1.3	2.6			
					4.5	5	-0.3	-0.6			
					9.5	10	-0.9	-1.8			
Source-Follower Output : (Demodulated Output):					5,10	—	1.5	2.2	V	—	
Offset Voltage (V <sub>COIN</sub> -V <sub>DEM</sub> )	—				15	—	1.5	—			
Linearity	—	$R_S > 50 \text{ k}\Omega$ $I_Z = 50 \mu\text{A}$	I <sub>Z</sub> = 50 μA	5	—	0.1	—	%	—		
Zener Diode Voltage CD4046AD, CD4046AK	V <sub>Z</sub>			10	—	0.6	—				
CD4046AE				15	—	0.8	—				
Zener Dynamic Resistance	R <sub>Z</sub>	$I_Z = 1 \text{ mA}$			—	100	—	Ω	—		

ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS FIG. NO.		
			CD4046AD, CD4046AK CD4046AE						
			MIN.	TYP.	MAX.				
<b>PHASE COMPARATOR Section</b>									
Operating Supply Voltage	$V_{DD}-V_{SS}$	Amplifier Operation	—	5	—	15	V		
		Comparators only	—	3	—	15	—		
Total Quiescent Device Current:									
Term. 14 Open	$I_L$	Term. 15 open Term. 5 at $V_{DD}$ Terms. 3 & 9 at $V_{SS}$	5	—	25	55	$\mu\text{A}$		
Term. 14 at $V_{SS}$ or $V_{DD}$			10	—	200	410			
			5	—	5	15			
			10	—	25	60			
Term. 14 (SIGNAL IN) Input Impedance	$Z_{14}$		5	1	2	—	$\text{m}\Omega$		
			10	0.2	0.4	—	—		
			15	—	0.2	—	—		
AC-Coupled Signal Input Voltage Sensitivity			5	—	200	400	mV		
			10	—	400	800			
			15	—	700	—			
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity: Low Level			5	1.5	2.25	—	V		
			10	3	4.5	—			
			15	4.5	6.75	—			
High Level			5	—	2.75	3.5			
			10	—	5.5	7			
			15	—	8.25	—			
Output Drive Current:									
n-Channel (Sink)	$I_{DN}$	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	mA		
			0.5	10	1.3	2.5			
p-Channel (Source)	$I_{DP}$	Phase Pulses	0.5	5	0.23	0.47			
			0.5	10	0.7	1.4			
		Phase Comparator I & II Term. 2 & 13	4.5	5	-0.3	-0.6			
			9.5	10	-0.9	-1.8			
		Phase Pulses	4.5	5	-0.08	-0.16			
			9.5	10	-0.25	-0.5			

**MAXIMUM RATINGS, Absolute-Maximum Values:**Storage Temperature Range . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$ 

Operating Temperature Range:

Ceramic Package Types . . . . .  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ Plastic Package Types . . . . .  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ 

DC Supply Voltage Range

 $(V_{DD} - V_{SS})$  . . . . .  $-0.5 \text{ V}$  to  $+15 \text{ V}$ Device Dissipation (Per Pkg.) . . . . .  $200 \text{ mW}$ All Inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ 

Lead Temperature (During soldering):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$  mm)  
from case for 10 seconds max. . . . .  $265^\circ\text{C}$

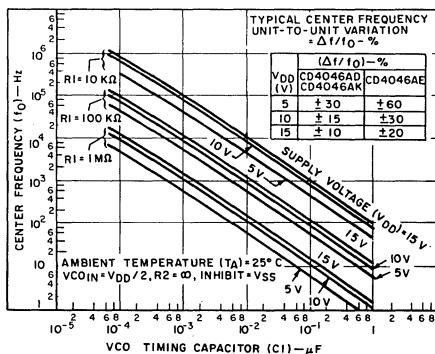


Fig. 5(a) — Typical center frequency vs  $C_1$  for  $R_1 = 10\text{ k}\Omega$ , and  $1\text{ M}\Omega$ .

**NOTE:** Lower frequency values are obtainable if larger values of  $C_1$  than shown in Figs. 5(a) and 5(b) are used.

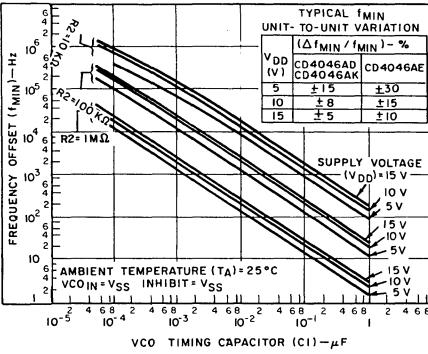


Fig. 5(b) — Typical frequency offset vs  $C_1$  for  $R_2 = 10\text{ k}\Omega$ ,  $100\text{ k}\Omega$ , and  $1\text{ M}\Omega$ .

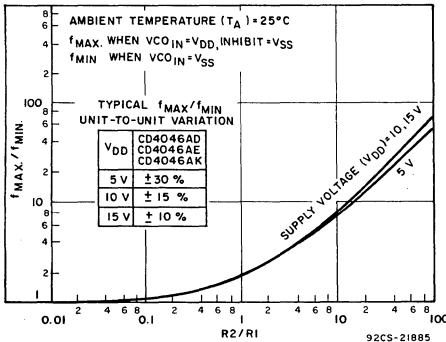


Fig. 5(c) — Typical  $f_{max}/f_{min}$  vs  $R_2/R_1$ .

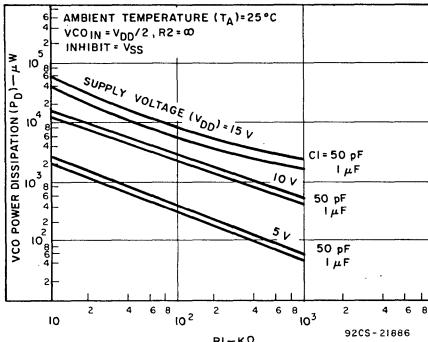


Fig. 6(a) — Typical VCO power dissipation at center frequency vs  $R_1$ .

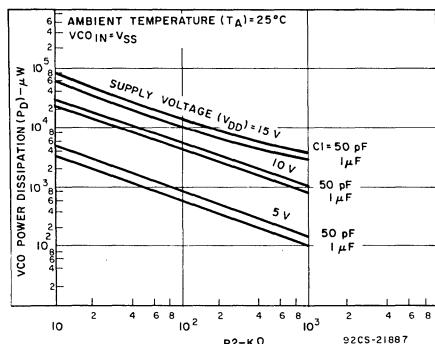


Fig. 6(b) — Typical VCO power dissipation at  $f_{min}$  vs  $R_2$ .

**NOTE:** To obtain approximate total power dissipation of PLL system for no-signal input

$$P_D (\text{Total}) = P_D (f_0) + P_D (f_{MIN}) + P_D (R_S) - \text{Phase Comparator I}$$

$$P_D (\text{Total}) = P_D (f_{MIN}) - \text{Phase Comparator II}$$

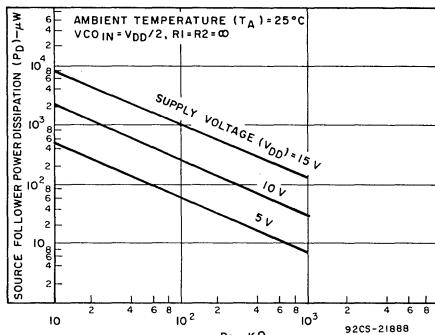


Fig. 6(c) — Typical source follower power dissipation vs  $R_S$ .

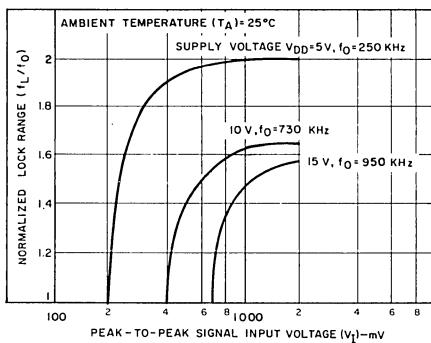
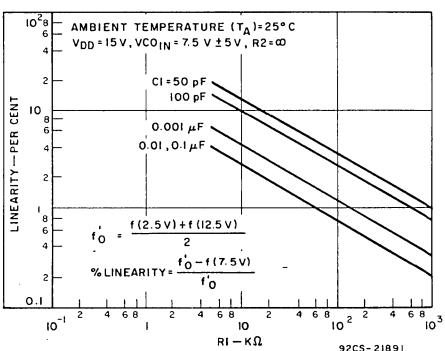
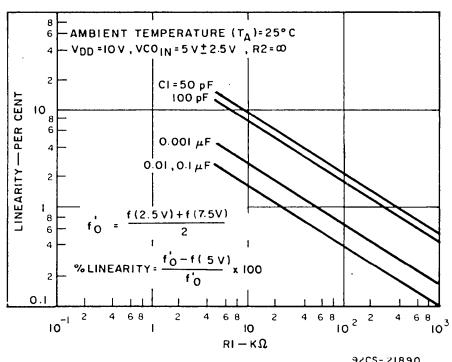


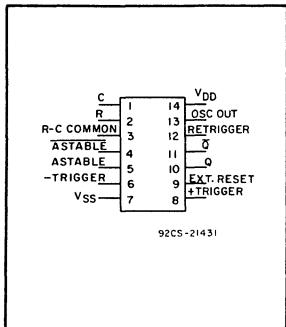
Fig.7 – Typical lock range vs signal input amplitude.

Fig.8(a) and (b) – Typical VCO linearity vs  $R1$  and  $C1$ .



# Digital Integrated Circuits

Monolithic Silicon

**CD4047AD CD4047AE CD4047AK**


## COS/MOS Low-Power Monostable/Astable Multivibrator

### Special Features:

- Low power consumption: special COS/MOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

### Monostable Multivibrator Features:

- Positive- or negative-edge trigger
- Output pulse width independent of trigger pulse duration

RCA-CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action having retriggering and external counting options.

Inputs include +Trigger, -Trigger, Astable, Astable, Retrigger, and External Reset. Buffered outputs are Q,  $\bar{Q}$ , and Oscillator. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the Astable input. The period of the square wave at the Q and  $\bar{Q}$  outputs in this mode of operation is a function of the external components employed. "True" input pulses on the Astable input or "Complement" pulses on the  $\bar{Q}$  terminal allow the circuit to be used as a gatable multivibrator. An output whose period is half of that which appears at the Q terminal is available at the Oscillator Output terminal. However, a 50% duty cycle is not guaranteed at this output.

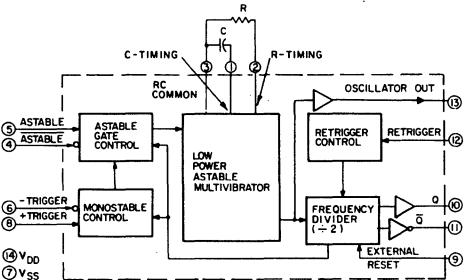


Fig.1 — CD4047A logic block diagram.

- Retriggerable option for pulse width expansion
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

### Astable Multivibrator Features:

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available
- Good astable frequency stability:  
frequency deviation =  $\pm 2\% + 0.03\%/\text{°C}$  @ 100 kHz\*  
 $= \pm 0.5\% + 0.015\%/\text{°C}$  @ 10 kHz\*

### COS/MOS Features:

- Microwatt quiescent power dissipation:  $0.5 \mu\text{W}$  (Typ)
- High noise immunity: 45% of supply voltage (Typ)
- Wide operating-temperature range: ceramic package types,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ ; plastic package types,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

### Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- |  |  |
|--|--|
| <ul style="list-style-type: none"> <li>■ Frequency discriminators</li> <li>■ Timing circuits</li> <li>■ Time-delay applications</li> </ul> | <ul style="list-style-type: none"> <li>■ Envelope detection</li> <li>■ Frequency multiplication</li> <li>■ Frequency division</li> </ul> |
|--|--|

\* Circuits "trimmed" to frequency;  $V_{DD} = 10 \text{ V} \pm 10\%$ .

A high level should be applied to the external reset whenever V<sub>DD</sub> is applied or removed. In the monostable mode positive-edge triggering is accomplished by application of a leading-edge pulse to the "+Trigger" input and a low level to the "-Trigger" input. For negative-edge triggering a trailing-edge pulse is applied to the "-Trigger" and a high level is applied to the "+Trigger". Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the "Retrigger" and "+Trigger" inputs. In this mode the output pulse remains "high" as long as the input pulse period is shorter than the period determined by the RC components.

An external countdown option can be implemented by coupling "Q" to an external "N" counter (e.g. CD4017A) and resetting the counter with the trigger pulse. The counter output pulse is fed back to the Astable input and has a duration equal to N times the period of the multivibrator.

A high level on the External Reset input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time.

This device is supplied in a 14-lead flat pack (CD4047AK), a 14-lead dual-in-line ceramic package (CD4047AD), or a 14-lead dual-in-line plastic package (CD4047AE). It is also available in chip form (CD4047AH).

#### MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage-Temperature Range	. . . . .	-65 to +150	°C
Operating-Temperature Range:			
Ceramic Package Types	. . . . .	-55 to +125	°C
Plastic Package Types	. . . . .	-40 to +85	°C
DC Supply-Voltage Range			
(V <sub>DD</sub> - V <sub>SS</sub> )	. . . . .	-0.5 to +15	V
Device Dissipation (Per Pkg.)	. . . . .	200	mW
All Inputs <sup>t</sup>	. . . . .	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	V
Recommended			
DC Supply Voltage			
(V <sub>DD</sub> - V <sub>SS</sub> )	. . . . .	3 to 15	V
Recommended			
Input Voltage Swing	. . . . .	V <sub>DD</sub> to V <sub>SS</sub>	V

<sup>t</sup> In normal operation of the CD4047A, signals at terminal 3 may go above V<sub>DD</sub> or below V<sub>SS</sub>; therefore a different gate-oxide protection circuit is used that is only 30 per cent as effective as the static-discharge protection at other terminals in the device. Additional care in following the guidance of ICAN-6000 is advised for this device.

#### CD4047A FUNCTIONAL TERMINAL CONNECTIONS

NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3 &  
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V <sub>DD</sub>	TO V <sub>SS</sub>	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4, 5, 6, 14	7, 8, 9, 12	—	10, 11, 13	t <sub>A</sub> (10,11)=4.40 RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t <sub>A</sub> (13)=2.20 RC
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator:					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown*	14	5, 6, 7, 8, 9, 12	—	10, 11	t <sub>M</sub> (10,11)=2.48 RC

\* Input Pulse to Reset of External Counting Chip  
External Counting Chip Output to Terminal 4

▲ See Text.

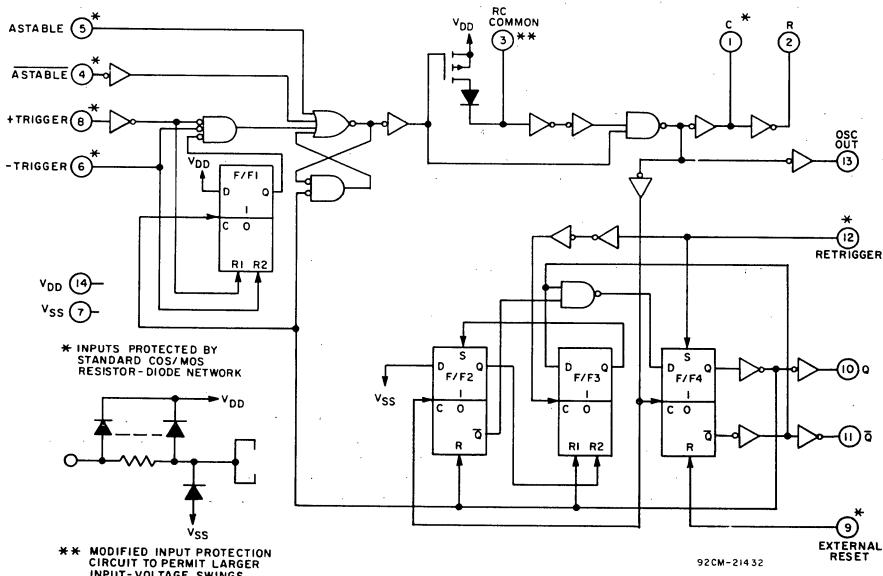
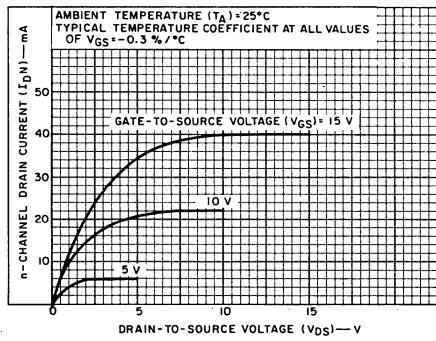
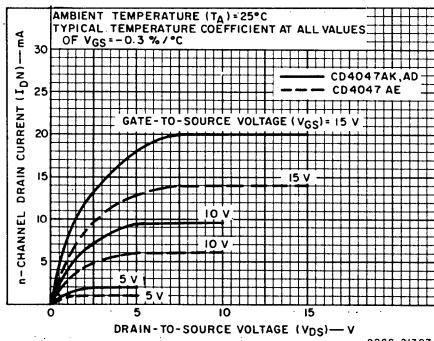


Fig.2 – CD4047A logic diagram.

Fig.3 – Typical n-channel drain characteristics for Q and  $\bar{Q}$  buffers.Fig.4 – Minimum n-channel drain characteristics for Q and  $\bar{Q}$  buffers.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4047AD, CD4047AK											
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-55°C			25°C			125°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>			5	—	—	5	—	0.03	5	—	—	300	μA	33
				10	—	—	10	—	0.05	10	—	—	600		
Quiescent Device Dissipation Package	P <sub>D</sub>			5	—	—	25	—	0.15	25	—	—	1500	μW	
				10	—	—	100	—	0.5	100	—	—	6000		
Output Voltage Low Level	V <sub>OL</sub>			5	—	—	0.01	—	0	0.01	—	—	0.05	V	
				10	—	—	0.01	—	0	0.01	—	—	0.05		
High Level	V <sub>OH</sub>			5	4.99	—	—	4.99	5	—	4.95	—	—	V	
				10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (All Inputs)	V <sub>NL</sub>	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	34	
		9	10	3	—	—	3	4.5	—	2.9	—	—			
	V <sub>NH</sub>	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V		
		1	10	2.9	—	—	3	4.5	—	3	—	—			
Output Drive Current (O, $\bar{Q}$ Outputs) N-Channel	I <sub>DN</sub>	0.5 V	5	0.5	—	—	0.4	0.8	—	0.28	—	—	mA	3, 4	
		0.5 V	10	1.25	—	—	1	2	—	0.7	—	—			
P-Channel		4.5 V	5	-0.5	—	—	-0.4	-0.8	—	-0.28	—	—	mA	5, 6	
		9.5 V	10	-1.25	—	—	-1	-2	—	-0.7	—	—			
Input Current	I <sub>I</sub>	Any Input		—	—	—	10	—	—	—	—	—	pA		

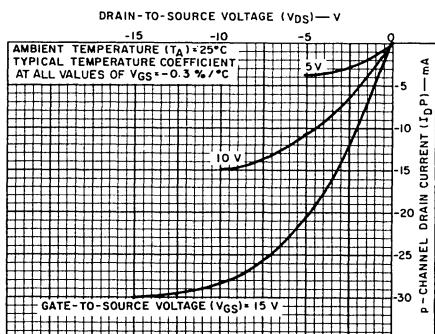


Fig.5 – Typical p-channel drain characteristics for Q and  $\bar{Q}$  buffers.

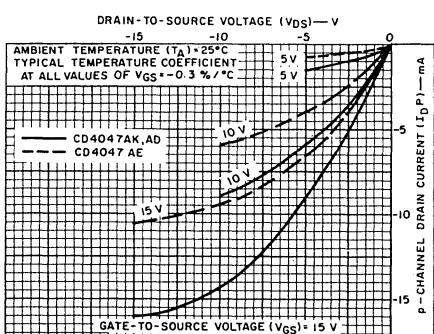


Fig. 6 – Minimum  $p$ -channel drain characteristics for  $\overline{Q}$  and  $Q$  buffers

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	UNITS	
				CD4047AE								
		$V_O$ Volts	$V_{DD}$ Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
Quiescent Device Current	$I_L$			5	—	50	—	0.1	50	—	—	700 $\mu A$
				10	—	100	—	0.2	100	—	—	1400 $\mu A$
Quiescent Device Dissipation Package	$P_D$			5	—	250	—	0.5	250	—	—	3500 $\mu W$
				10	—	1000	—	2	1000	—	—	14000 $\mu W$
Output Voltage Low Level	$V_{OL}$			5	—	0.01	—	0	0.01	—	—	0.05 V
				10	—	0.01	—	0	0.01	—	—	0.05 V
High Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—
				10	9.99	—	—	9.99	10	—	9.95	—
Noise Immunity (All Inputs)	$V_{NL}$	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	V
		9	10	3	—	—	3	4.5	—	2.9	—	V
		0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	V
		1	10	2.9	—	—	3	4.5	—	3	—	V
Output Drive Current ( $Q$ , $\bar{Q}$ Outputs) N-Channel	$I_{DN}$	0.5 V	5	0.34	—	—	0.28	0.8	—	0.23	—	mA
		0.5 V	10	0.85	—	—	0.7	2	—	0.6	—	mA
P-Channel	$I_{DP}$	4.5 V	5	-0.34	—	—	-0.28	-0.8	—	-0.23	—	mA
		9.5 V	10	-0.85	—	—	-0.7	-2	—	-0.6	—	mA
Input Current	$I_I$	Any Input		—	—	—	—	10	—	—	—	pA

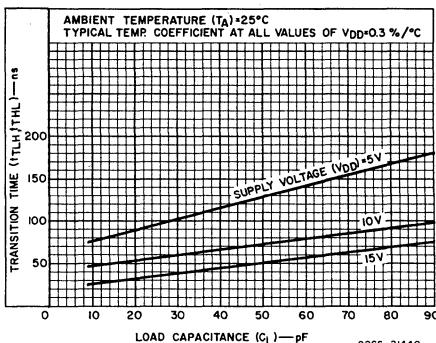
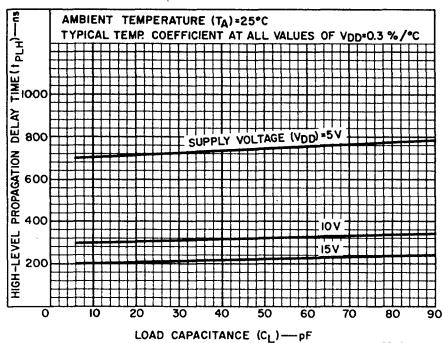


Fig.7 — Typical low-to-high level propagation delay time vs. load capacitance for  $Q$  and  $\bar{Q}$  buffers.

Fig.8 — Typical transition time vs. load capacitance for  $Q$  and  $\bar{Q}$  buffers.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$ ,  $C_L = 15 \text{ pF}$ Typical Temperature Coefficient at all values of  $V_{DD} = 0.3\%/\text{ }^\circ\text{C}$ 

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS	
			$V_{DD}$ (Volts)	CD4047AK CD4047AD			CD4047AE			
				MIN.	TYP.	MAX.	MIN.	TYP.		
Propagation Delay Time: Astable, Astable to Osc. Out			5	—	200	400	—	200	550	ns
			10	—	100	200	—	100	275	
			5	—	550	900	—	550	1200	
			10	—	250	500	—	250	650	
			5	—	700	1200	—	700	1600	
			10	—	300	600	—	300	800	
			5	—	300	600	—	300	800	
			10	—	175	300	—	175	400	
			5	—	300	600	—	300	800	
			10	—	125	250	—	125	350	
Transition Time: $Q, \bar{Q}$			5	—	75	125	—	75	150	ns
			10	—	45	75	—	45	100	
			5	—	75	150	—	75	180	
			10	—	45	100	—	45	130	
* Minimum Input Pulse Duration (any input)	$t_{WL},$ $t_{WH}$		5	—	500	1000	—	500	1300	ns
			10	—	200	400	—	200	600	
+Trigger,Retrigger,-Trigger Rise & Fall Time	$t_r,$ $t_f$		5	—	—	15	—	—	15	$\mu\text{s}$
			10	—	—	5	—	—	5	
Average Input Capacitance	$C_I$	any input	—	—	5	—	—	5	—	pF

\* Input pulse widths below the minimum specified may cause malfunction of the unit.

See Application Note ICAN-6230.

## I. Astable Mode Design Information

## A. Unit-to-Unit Transfer-Voltage Variations

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage ( $V_{TR}$ ) shift (33%–67%  $V_{DD}$ ) for free-running (astable) operation.

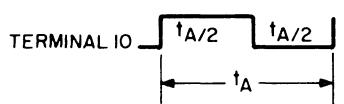
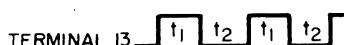


Fig.9 – Astable mode waveforms.

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$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2)$$

$$= -2RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ:  $V_{TR} = 0.5 V_{DD}$  $t_A = 4.40 RC$ Min:  $V_{TR} = 0.33 V_{DD}$  $t_A = 4.62 RC$ Max:  $V_{TR} = 0.67 V_{DD}$  $t_A = 4.62 RC$ 

thus if  $t_A = 4.40 RC$  is used, the maximum variation will be (+5.0%, -0.0%).

### B. Variations Due to $V_{DD}$ and Temperature Changes

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to  $V_{DD}$  and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

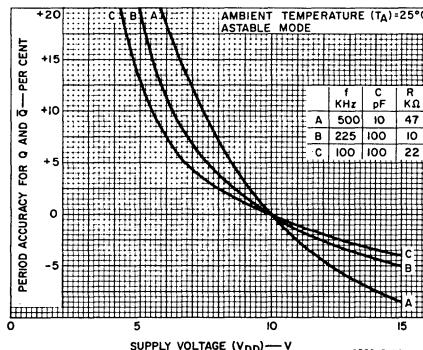


Fig.10 — Typical Q-and- $\bar{Q}$ -period accuracy vs. supply voltage (high frequency).

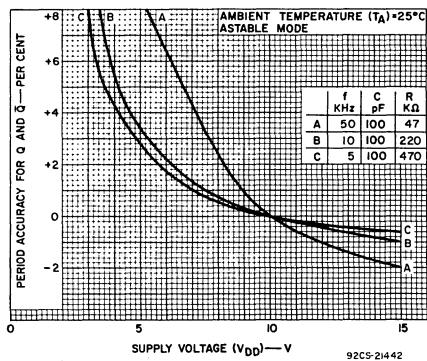


Fig.11 — Typical Q-and- $\bar{Q}$ -period accuracy vs. supply voltage (medium frequency).

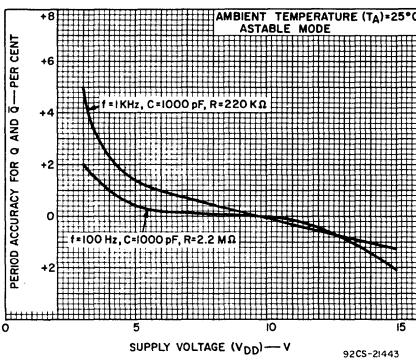


Fig.12 — Typical Q-and- $\bar{Q}$ -period accuracy vs. supply voltage (low frequency).

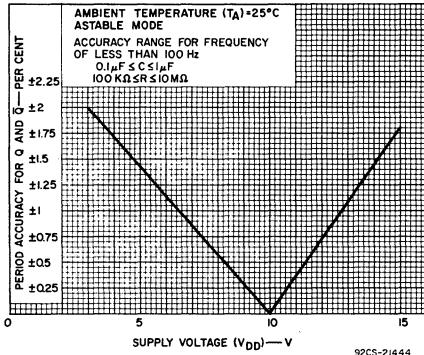


Fig.13 — Typical Q-and- $\bar{Q}$ -period accuracy vs. supply voltage (very low frequency).

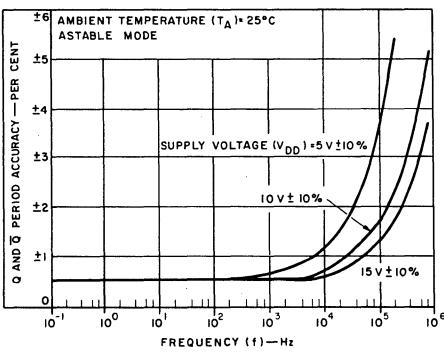


Fig.14 — Typical Q-and- $\bar{Q}$ -period accuracy vs. frequency for  $V_{DD}$  variation of ± 10% from value indicated.

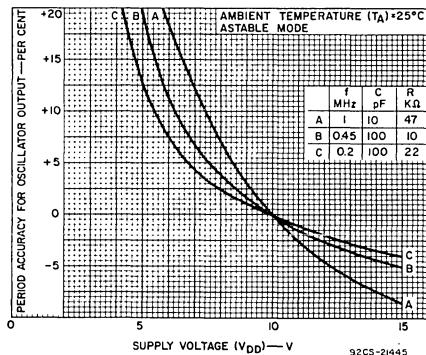


Fig. 15 — Typical oscillator-output-period accuracy vs. supply voltage (high frequency).

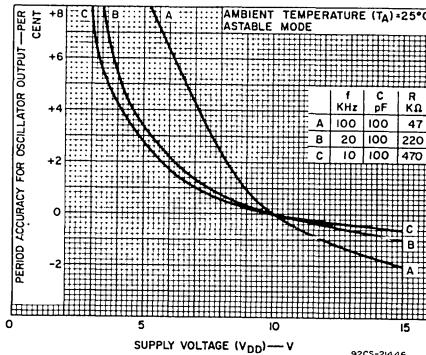


Fig. 16 — Typical oscillator-output-period accuracy vs. supply voltage (medium frequency).

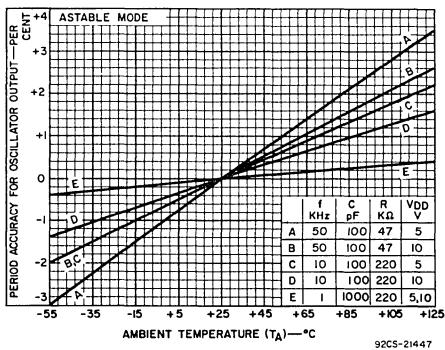


Fig. 17 — Typical Q-and- $\bar{Q}$ -period accuracy vs. temperature (medium frequency).

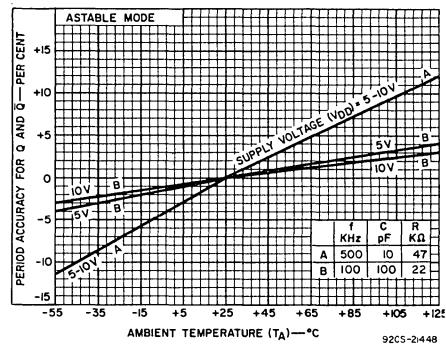


Fig. 18 — Typical Q-and- $\bar{Q}$ -period accuracy vs. temperature (high frequency).

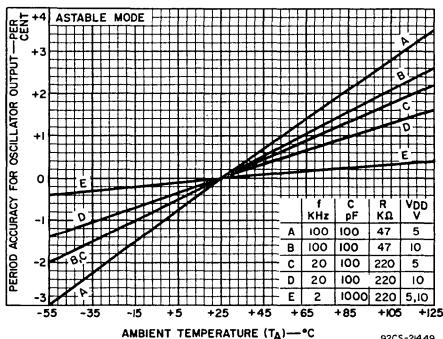


Fig. 19 — Typical oscillator-period accuracy vs. temperature (medium frequency).

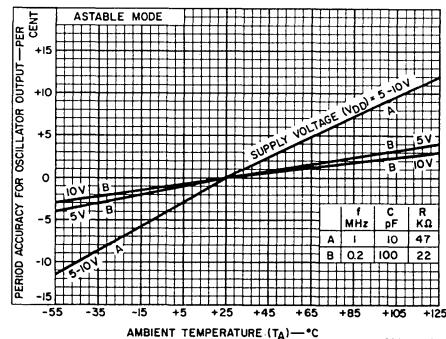


Fig. 20 — Typical oscillator-period accuracy vs. temperature (high frequency).

## II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage ( $V_{TR}$ ) shift (33% - 67%  $V_{DD}$ ) for one-shot (monostable) operation.

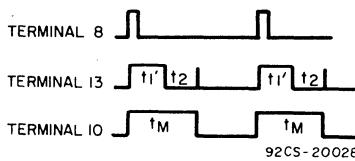


Fig.21 - Monostable waveforms.

where  $t_M$  = Monostable mode pulse width. Values for  $t_M$  are as follows:

$$\text{Typ: } V_{TR} = 0.5 V_{DD} \quad t_M = 2.48 \text{ RC}$$

$$\text{Min: } V_{TR} = 0.33 V_{DD} \quad t_M = 2.71 \text{ RC}$$

$$\text{Max. } V_{TR} = 0.67 V_{DD} \quad t_M = 2.48 \text{ RC}$$

Thus if  $t_M = 2.48 \text{ RC}$  is used, the maximum variation will be (+9.3%, -0.0%).

### Note:

In the astable mode, the first positive half cycle has a duration of  $T_M$ ; succeeding durations are  $t_A/2$ .

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to  $V_{DD}$  and temperature. These variations are presented in graphical form in Figs.22 to 27 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

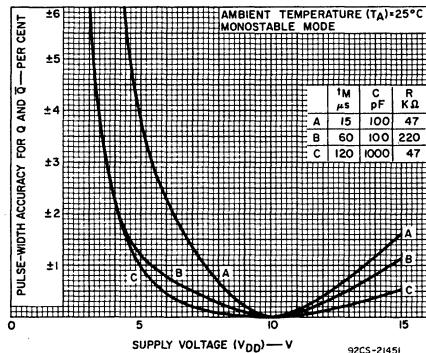


Fig.22 - Typical Q-and-Q-bar-pulse-width accuracy vs. supply voltage ( $t_M = 15, 60, 120 \mu s$ ).

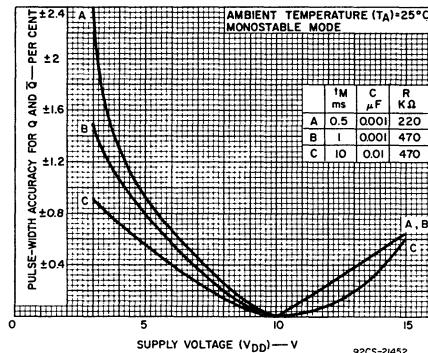


Fig.23 - Typical Q-and-Q-bar-pulse-width accuracy vs. supply voltage ( $t_M = 0.5, 1, 10 \text{ ms}$ ).

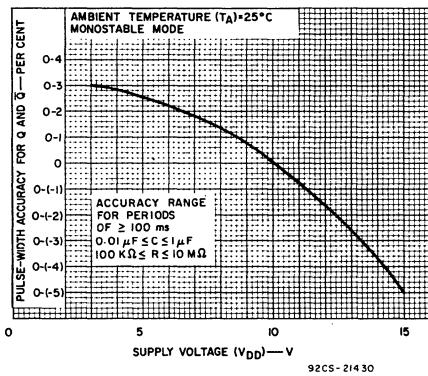


Fig.24 - Typical Q-and-Q-bar-pulse-width accuracy vs. supply voltage ( $t_M \geq 100 \text{ ms}$ ).

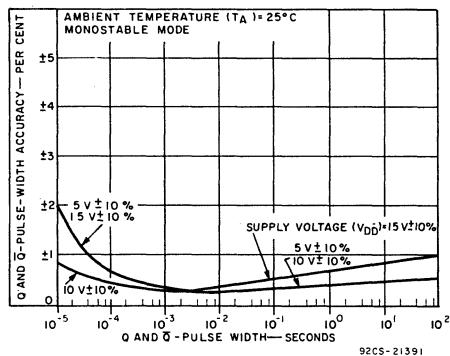


Fig.25 - Typical Q-and-Q-bar-pulse-width accuracy vs. Q and Q-bar pulse width for a variation of  $\pm 10\%$  from value indicated.

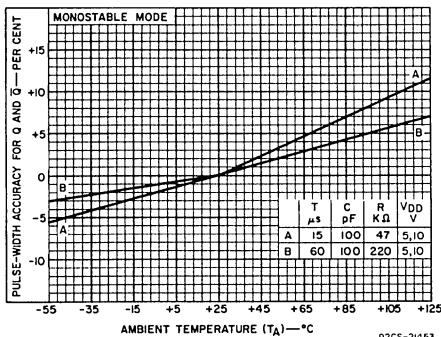


Fig.26 -- Typical Q-and- $\bar{Q}$ -pulse-width accuracy vs. temperature (high frequency).

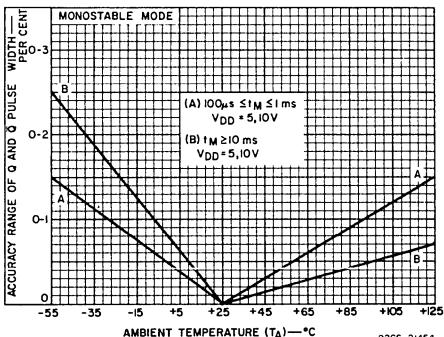


Fig.27 -- Typical Q-and- $\bar{Q}$ -pulse-width accuracy range vs. temperature.

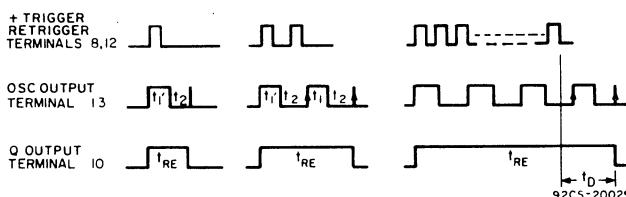


Fig.28 -- Retrigger-mode waveforms.

### III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig.28, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses,  $t_{RE} = t_1' + t_1 + 2t_2$ . For more than two pulses,  $t_{RE}$  (Q OUTPUT) terminates at some variable time  $t_D$  after the termination of the last retrigger pulse.  $t_D$  is variable because  $t_{RE}$  (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig.2).

### IV. External Counter Option

Time  $t_M$  can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig.29. The pulse

duration at the output is

$$t_{ext} = (N - 1) (t_A) + (t_M + t_A/2)$$

where  $t_{ext}$  = pulse duration of the circuitry, and N is the number of counts used.

### V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$$C \geq 100 \text{ pF, up to any practical value, for astable modes;}$$

$$C \geq 1000 \text{ pF, up to any practical value for monostable modes.}$$

$$10 \text{ k}\Omega \leq R \leq 1 \text{ M}\Omega.$$

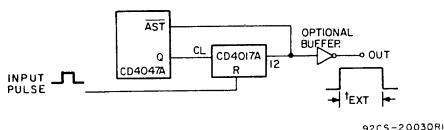


Fig.29 -- Implementation of external counter option.

## VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode:  $P = 2CV^2f$ . (Output at terminal No. 13)

$P = 4CV^2f$ . (Output at terminal Nos. 10 and 11)

$$\text{Monostable Mode: } P = \frac{(2.9CV^2)}{T} \text{ (Duty Cycle)}$$

(Output at terminal Nos. 10 and 11)

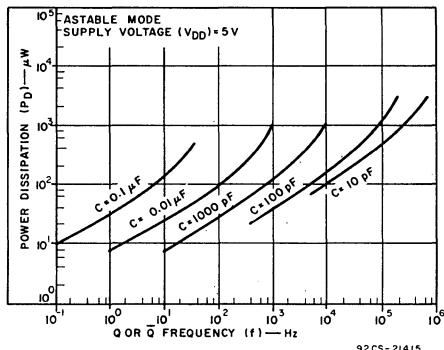


Fig.30 – Power dissipation vs. output frequency ( $V_{DD} = 5$  V).

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 30–32 for typical power consumption in astable mode.

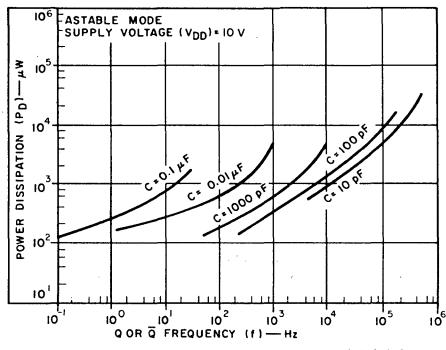


Fig.31 – Power dissipation vs. output frequency ( $V_{DD} = 10$  V).

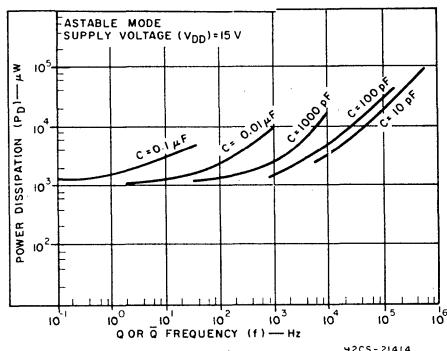


Fig.32 – Power dissipation vs. output frequency ( $V_{DD} = 15$  V).

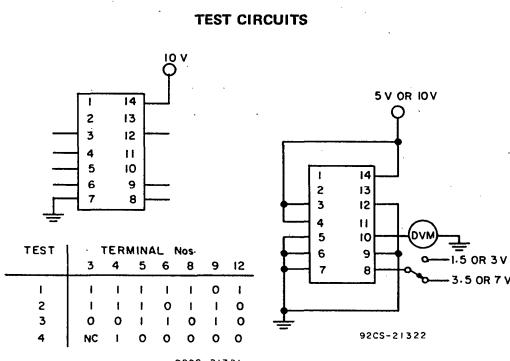


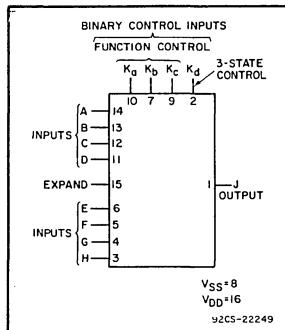
Fig.33 – Quiescent device current.

Fig.34 – Noise immunity.



# Digital Integrated Circuits

Monolithic Silicon

**CD4048AD CD4048AE CD4048AK**


## COS/MOS Multi-Function Expandable 8-Input Gate

### Special Features:

- Medium-power TTL drive capability
- Three-state output
- High-current source and sink capability  
 $9 \text{ mA} (\text{typ.}) @ V_{DS} = 0.5 \text{ V}, V_{DD} = 10 \text{ V}$
- Many logic functions available in one package

### Applications:

- Selection of up to 8 logic functions
- Digital control of logic
- General-purpose gating logic
  - Decoding
  - Encoding

RCA-CD4048A is an 8-input gate having four control inputs. Three binary control inputs —  $K_a$ ,  $K_b$ , and  $K_c$  — provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

A fourth control input —  $K_d$  — provides the user with 3-state outputs. When control input  $K_d$  is "high" the output is either a logic 1 or a logic 0 depending on the input states. When control input  $K_d$  is "low", the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 2). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to  $V_{SS}$ .

The CD4048A is supplied in a 16-lead dual-in-line ceramic package (CD4048AD), a 16-lead dual-in-line plastic package (CD4048AE), or a 16-lead flat pack (CD4048AK).

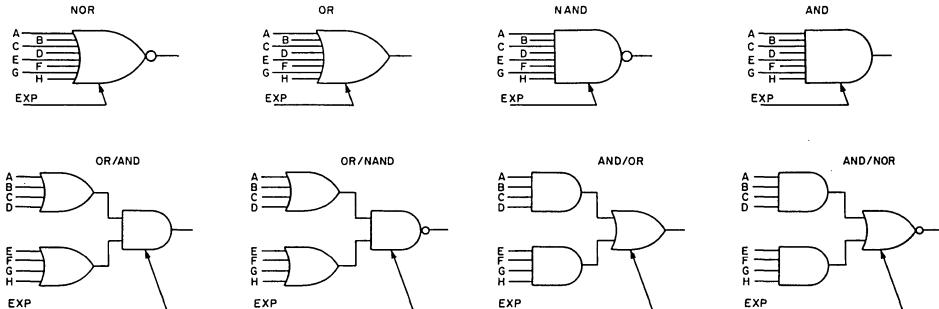


Fig. 1—Basic logic configurations.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

Storage-Temperature Range ..... -65 to +150 °C

Operating-Temperature Range:

Ceramic Package Types ..... -55 to +125 °C

Plastic Package Types ..... -40 to +85 °C

DC Supply-Voltage Range ( $V_{DD} - V_{SS}$ ) ..... -0.5 to +15 V

Device Dissipation (Per Pkg.) ..... 200 mW

All Inputs .....  $V_{SS} \leq V_I \leq V_{DD}$ 

Recommended

DC Supply Voltage ( $V_{DD} - V_{SS}$ ) ..... 3 to 15 V

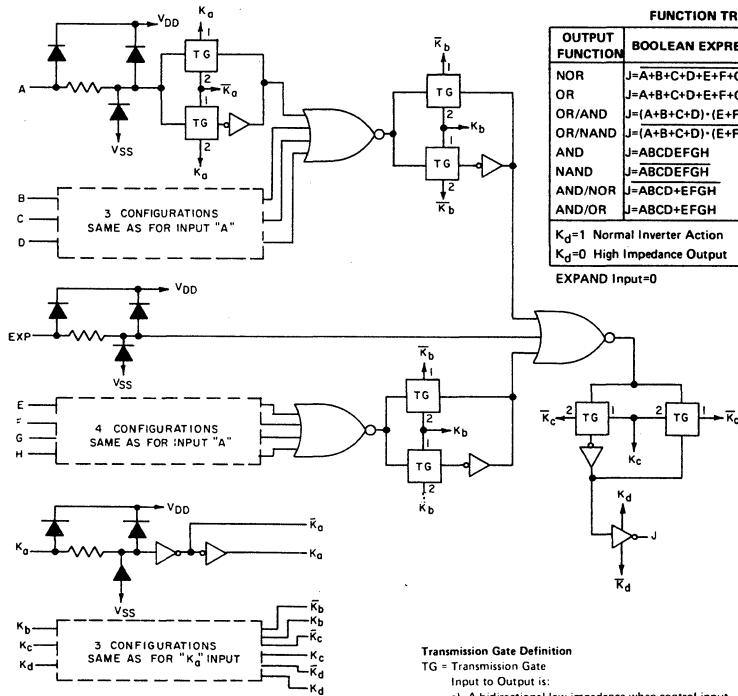
Recommended

Input Voltage Swing .....  $V_{DD}$  to  $V_{SS}$ 

Lead Temperature (During Soldering):

At distance  $1/16 \pm 1/32$  in. ( $1.59 \pm 0.79$  mm)

from case for 10 s max. ..... 265 °C



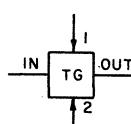
\*See Figs. 1 and 3.

## Transmission Gate Definition

TG = Transmission Gate

Input to Output is:

- a) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high"
- b) An open circuit when control input 1 is "high" and control input 2 is "low"



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Fig. 2—Logic diagram and truth table.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
				CD4048AD, CD4048AK			25°C			125°C					
		V <sub>O</sub> Volts		V <sub>DD</sub> Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	I <sub>L</sub>			5	—	—	1	—	0.005	1	—	—	60	μA	14
				10	—	—	2	—	0.01	2	—	—	120		
Quiescent Device Dissipation/Package	P <sub>D</sub>			5	—	—	5	—	0.025	5	—	—	300	μW	
				10	—	—	20	—	0.1	20	—	—	1200		
Output Voltage: Low-Level	V <sub>OL</sub>			5	—	—	0.01	—	0	0.01	—	—	0.05	V	
				10	—	—	0.01	—	0	0.01	—	—	0.05		
Output Voltage: High-Level	V <sub>OH</sub>			5	4.99	—	—	4.99	5	—	4.95	—	—	V	
				10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (All Inputs)	V <sub>NL</sub>			4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	V	13
				9	10	3	—	—	3	4.5	—	2.9	—		
For definition, see Appendix	V <sub>NH</sub>			0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	V	13
				1	10	2.9	—	—	3	4.5	—	3	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>			0.4	4.5	2	—	—	1.6	3.2	—	1.1	—	mA	5, 6
				0.5	10	5.6	—	—	4.5	9	—	3.1	—		
P-Channel (Source)	I <sub>DP</sub>			4.6	5	-2	—	—	-1.6	-3.2	—	-1.1	—	mA	7, 8
				9.5	10	-5.6	—	—	-4.5	-9	—	-3.1	—		

## Applications of Expand Input

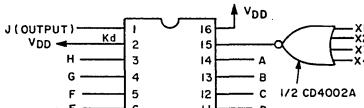


Fig. 3(a)– 12-input OR/AND gate.

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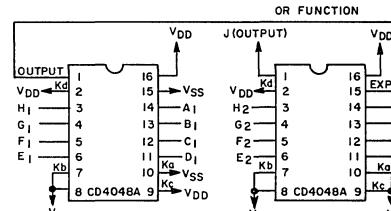


Fig. 3(b)– 16-input NOR gate.

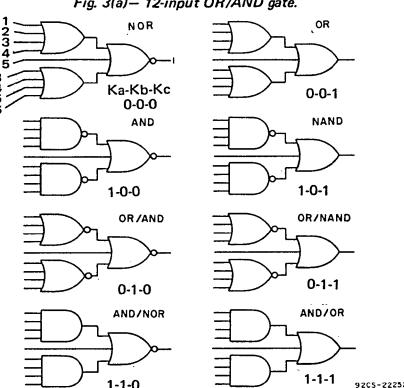


Fig. 3(c)– Actual-circuit logic configurations.

92CS-22232

## IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	J = (A+B+C+D+E+F+G+H)+(EXP)
OR	OR	J = (A+B+C+D+E+F+G+H)+(EXP)
AND	NAND	J = (ABCDEFGH)+(EXP)
NAND	NAND	J = (ABCD EFGH)+(EXP)
OR/AND	NOR	J = (A+B+C+D) · (E+F+G+H) · (EXP)
OR/NAND	NOR	J = (A+B+C+D) · (E+F+G+H) · (EXP)
AND/NOR	AND	J = (ABCD)+(EFGH)+(EXP)
AND/OR	AND	J = (ABCD)+(EFGH)+(EXP)

Note: (EXP) designates the EXPAND function (i.e.,  $X_1 \cdot X_2 \cdot \dots \cdot X_N$ ).

Fig. 3– Expansion logic and truth table.

STATIC ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.		
				CD4048AE											
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C					
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		$\mu A$	14
	5	—	—	10	—	0.01	10	—	—	140	—				
Quiescent Device Dissipation/Package	$P_D$	10	—	—	20	—	0.02	20	—	—	280	—	$\mu W$		
		5	—	—	50	—	0.05	50	—	—	700	—			
Output Voltage: Low-Level	$V_{OL}$	10	—	—	200	—	0.2	200	—	—	2800	—	V		
		5	—	—	0.01	—	0	0.01	—	—	0.05	—			
High-Level	$V_{OH}$	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V		
		10	9.99	—	—	9.99	10	—	9.95	—	—	—			
Noise Immunity (All Inputs)	$V_{NL}$	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	13	
		9	10	3	—	—	3	4.5	—	2.9	—	—			
<i>For definition see Appendix</i>	$V_{NH}$	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	13	
		1	10	2.9	—	—	3	4.5	—	3	—	—			
Output Drive Current: N-Channel (Sink)	$I_{DN}$	0.4	4.5	1.9	—	—	1.6	3.2	—	1.3	—	—	mA	5, 6	
		0.5	10	5.4	—	—	4.5	9	—	3.7	—	—			
P-Channel (Source)	$I_{DP}$	4.6	5	-1.9	—	—	-1.6	-3.2	—	-1.3	—	—	mA	7, 8	
		9.5	10	-3.8	—	—	-3.15	-9	—	-2.6	—	—			

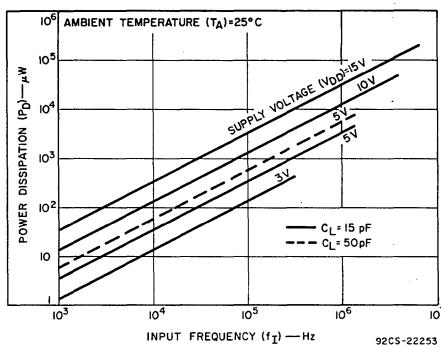


Fig. 4—Typical power dissipation as a function of input frequency.

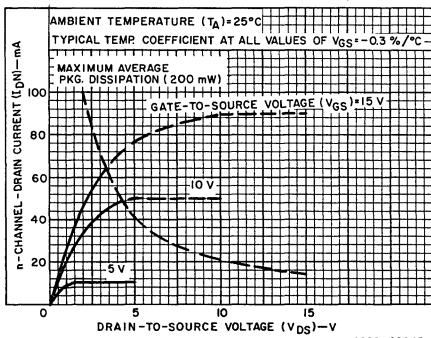


Fig. 5—Typical n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  and  $C_L = 15 \text{ pF}$  and  $50 \text{ pF}$ Typical Temperature Coefficient for all values of  $V_{DD} = 0.3\%/\text{OC}$  $C_L = 15 \text{ pF}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4048AD			CD4048AE					
			$V_{DD}$ (Volts)	MIN.	TYP.	MAX.*	MIN.	TYP.	MAX.*		
Propagation Delay Time	$t_{PLH}, t_{PHL}$		5	—	750	1300	—	750	1600	ns	15,16
			10	—	225	400	—	225	500		
Transition Time: High-to-Low Level	$t_{THL}$		5	—	90	140	—	90	170	ns	17
			10	—	30	50	—	30	65		
Low-to-High Level	$t_{TLH}$		5	—	130	250	—	130	300	ns	17
			10	—	40	60	—	40	75		
Input Capacitance	$C_I$	Any Input	—	—	5	—	—	5	—	pF	—

 $C_L = 50 \text{ pF}$ 

Propagation Delay Time	$t_{PLH}, t_{PHL}$		5	—	775	1350	—	775	1650	ns	15,16
			10	—	240	430	—	240	530		
Transition Time: High-to-Low Level	$t_{THL}$		5	—	105	170	—	105	200	ns	17
			10	—	40	70	—	40	85		
Low-to-High Level	$t_{TLH}$		5	—	145	280	—	145	330	ns	17
			10	—	50	80	—	50	95		
Input Capacitance	$C_I$	Any Input	—	—	5	—	—	5	—	pF	—

\* Max. Limits represent worst-case limits for worst-case modes of operation shown in Figs. 15, 16, and 17

DYNAMIC ELECTRICAL CHARACTERISTICS, Driving TTL at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} - V_{SS} = 5 \text{ V}$ ,  $C_L = 15 \text{ pF}$ 

CD4048AD, CD4048AK

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Driving One TTL Load	LIMITS			UNITS	TYPICAL CHARACTERISTICS CURVES Fig. No.	
			MIN.	TYP.	MAX.			
Propagation Delay Time: High-to-Low Level	$t_{PHL}$	Series 54L, 74L	—	775	—	ns	12	
		Series 54, 74	—	775	—			
	$t_{PLH}$	Series 54L, 74L	—	710	—	ns		
		Series 54, 74	—	600	—			

CD4048AE

Propagation Delay Time: High-to-Low Level	$t_{PHL}$	Series 54L, 74L	—	775	—	ns	12	
		Series 54, 74	—	775	—			
Low-to-High Level	$t_{PLH}$	Series 54L, 74L	—	710	—	ns		
		Series 54, 74	—	600	—			

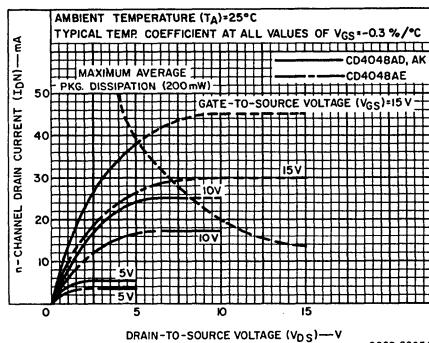
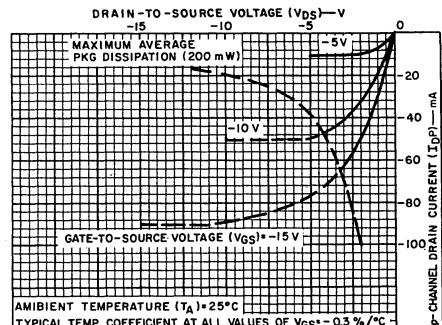
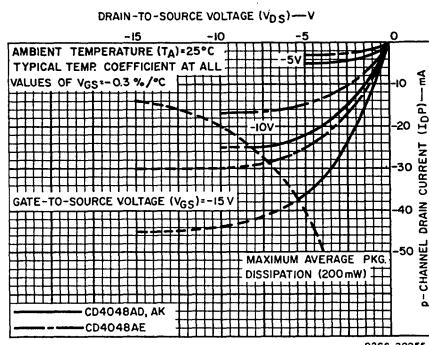
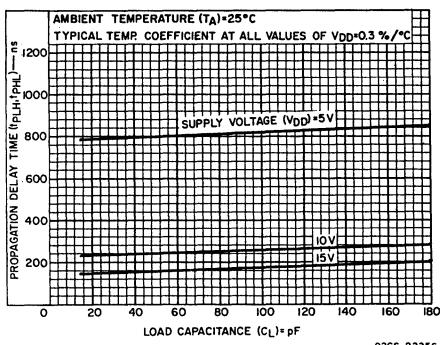
Fig. 6—Minimum *n*-channel drain characteristics.Fig. 7—Typical *p*-channel drain characteristics.Fig. 8—Minimum *p*-channel drain characteristics.

Fig. 9—Typical propagation delay time as a function of load capacitance.

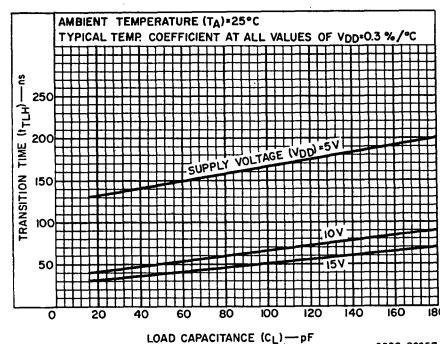


Fig. 10—Typical low-to-high level transition time as a function of load capacitance.

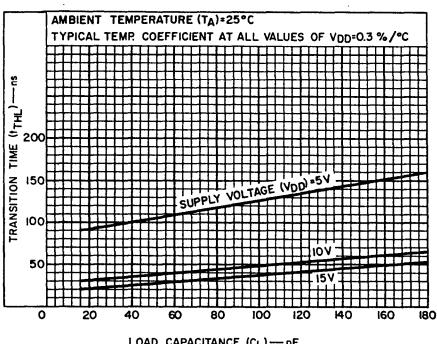


Fig. 11—Typical high-to-low level transition time as a function of load capacitance.

## TEST CIRCUITS

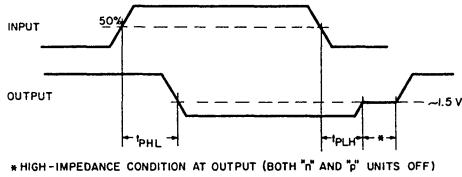
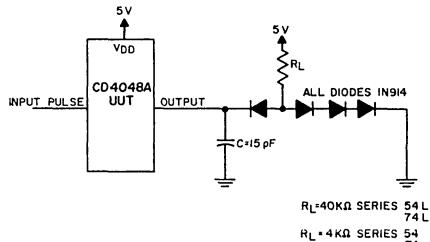


Fig. 12—Test circuit and waveforms for propagation delay time (CD4048A driving 1 TTL load).

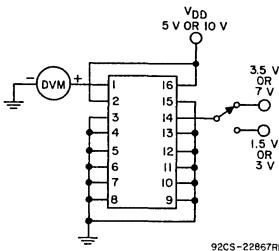
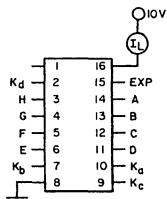


Fig. 13—Noise immunity. (can also be measured using one input; other inputs are tied to  $V_{DD}$ ).



Input Conditions For Leakage Measurements:												
K <sub>d</sub>	H	G	F	E	K <sub>b</sub>	K <sub>c</sub>	K <sub>s</sub>	D	C	B	A	EXP
(1)	0	0	0	0	0	0	0	0	0	0	0	0
(2)	1	0	0	0	0	1	1	1	0	0	0	0
(3)	0	1	1	1	0	0	0	1	1	1	1	1
(4)	1	1	1	1	1	1	1	1	1	1	1	1

92CS-22259

Fig. 14—Quiescent device current.

## TEST CIRCUITS — DYNAMIC MEASUREMENTS

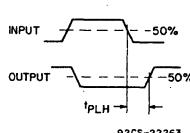
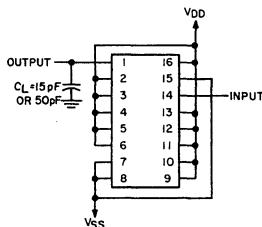


Fig. 15— $t_{PLH}$  — NAND.

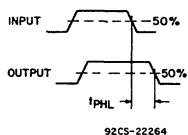
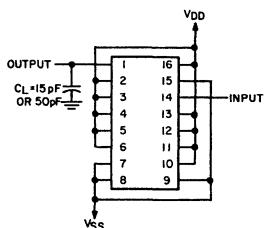


Fig. 16— $t_{PHL}$  — AND.

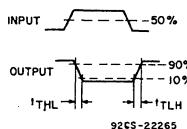
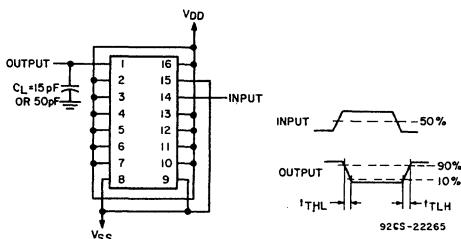


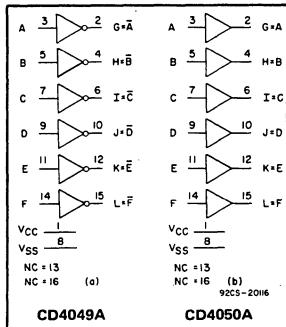
Fig. 17— $t_{THL}$ ,  $t_{TLH}$  — AND/NOR.



# Digital Integrated Circuits

Monolithic Silicon

## CD4049A, CD4050A



## COS/MOS Hex Buffer/Converters

CD4049AD  
CD4049AE  
CD4049AF  
CD4049AK

{ INVERTING  
TYPE

CD4050AAD  
CD4050AE  
CD4050AF  
CD4050AK

{ NON-INVERTING  
TYPE

### Features:

- Direct Drive to 2 TTL Loads at 5 V,  $V_{CC} = 5$  V,  $V_{OL} \leq 0.4$  V,  $I_{DN} \geq 3$  mA
- High Source and Sink Current Capability
- General COS/MOS Characteristics

### Applications:

- COS/MOS to DTL/TTL Hex Converter
- COS/MOS Current "Sink" or "Source" Driver
- COS/MOS High-to-Low Logic-Level Converter

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage ( $V_{CC}$ ). The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{CC}$  supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. ( $V_{CC} = 5$  V,  $V_{OL} \leq 0.4$  V, and  $I_{DN} \geq 3$  mA.)

Table 1 shows the range of voltage-supply levels that can be utilized for such logic level conversions. Conversion to logic-levels greater than +6 V is permitted provided that  $V_{CC} \leq V_{IH}$ . At 15 V, the maximum allowable load capacitance is 5000 pF.

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation.

The CD4049A and CD4050A are supplied in 16-lead dual inline welded-seal ceramic packages (CD4049AD and CD4050AD), 16-lead dual-in-line plastic packages (CD4049AE and CD4050AE), 16-lead dual-in-line frit-seal ceramic packages (CD4049AF and CD4050AF) and 16-lead flat packages (CD4049AK and CD4050AK).

TABLE I

FUNCTION	COS/MOS VOLTAGE RANGE (INPUT)	DTL/TTL VOLTAGE RANGE (OUTPUT)	POWER SUPPLY VOLTAGE RANGE ( $V_{CC}$ )
HEX LEVEL SHIFTER	3-15 V	3-6 V	3-6 V
HEX INVERTER HEX BUFFER	3-15 V	3-15 V	3-15 V

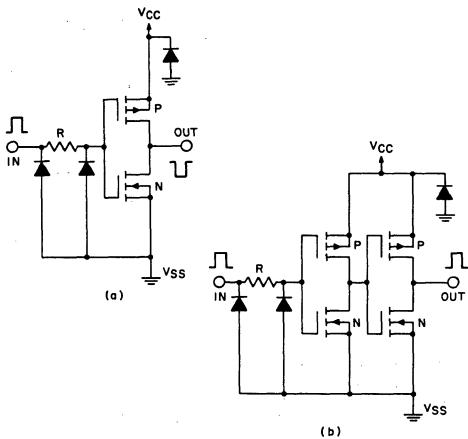


Fig.1-(a) Schematic diagram of CD4049A, 1 of 6 identical units;  
b) Schematic diagram of CD4050A, 1 of 6 identical units.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

Storage-Temperature Range . . . . .	-65 to +150	°C
Operating-Temperature Range:		
Ceramic Package Types . . . . .	-55 to +125	°C
Plastic Package Types . . . . .	-40 to +85	°C
DC Supply Voltage Range ( $V_{CC} - V_{SS}$ ) . . . . .	-0.5 to +15	V
Dissipation:		
Per Package . . . . .	200	mW
Per Buffer. . . . .	100	mW
All Inputs . . . . .	$V_{SS} \leq V_I \leq 15$	V
Recommended Minimum DC Supply Voltage ( $V_{CC} - V_{SS}$ ) . . . . .	3	V
Lead Temperature (During soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . .	265	°C

**STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . . .       $V_{SS} \leq V_I \leq 15$  V)**  
**(Recommended DC Supply Voltage ( $V_{CC} - V_{SS}$ ) . . . . .      3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS		
				CD4049AD, CD4049AK, CD4049AF				CD4050AD, CD4050AK, CD4050AF						
		$V_O$ Volts	$V_{CC}$ Volts	-55°C			25°C			125°C				
Quiescent Device Current	$I_L$			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	μA	
Quiescent Device Current	$I_L$	$V_{IH} = V_{CC}$		5	—	0.3	—	0.01	0.3	—	—	20	μA	
Quiescent Device Dissipation Package	$P_D$	$V_{IH} = V_{CC}$		10	—	0.5	—	0.01	0.5	—	—	30	μW	
Output Voltage Low-Level	$V_{OL}$			5	—	0.01	—	0	0.01	—	—	0.05	V	
High-Level	$V_{OH}$			10	—	0.01	—	0	0.01	—	—	0.05	V	
Noise Immunity (All Inputs)		$V_{OH} = 3.6$ V		5	1	—	—	1	2.25	—	0.9	—		
CD4049A		$V_{OH} = 7.2$ V		10	2	—	—	2	4.5	—	1.9	—		
CD4050A		$V_{OL} = 0.95$ V		5	1.5	—	—	1.5	2.25	—	1.4	—		
		$V_{OL} = 2.9$ V		10	3	—	—	3	4.5	—	2.9	—		
CD4050A		$V_{OH} = 7.2$ V		10	2.9	—	—	3	4.5	—	3	—	V	
CD4049A For Definition, See Appendix		$V_{OH} = 3.6$ V		5	1.4	—	—	1.5	2.25	—	1.5	—		
		$V_{OL} = 2.9$ V		10	2.9	—	—	3	4.5	—	3	—		
		$V_{OL} = 0.95$ V		5	1.4	—	—	1.5	2.25	—	1.5	—		
Output Drive Current N-CHANNEL	$I_{DN}$			0.4	4.5	3.3	—	—	2.6	5.2	—	1.8	—	
				0.4	5	3.75	—	—	3.0	6	—	2.1	—	
				0.5	10	10	—	—	8	16	—	5.6	—	
P-CHANNEL	$I_{DP}$			4.5	5	-0.62	—	—	-0.5	-1	—	-0.35	—	
				2.5	5	-1.85	—	—	-1.25	-2.5	—	-0.9	—	
				9.5	10	-1.85	—	—	-1.25	-2.5	—	-0.9	—	
Input Current	$I_I$	$V_{IH} = V_{CC}$			—	—	—	—	10	—	—	—	pA	

**STATIC ELECTRICAL CHARACTERISTICS (All Inputs . . . . . V<sub>SS</sub> ≤ V<sub>I</sub> ≤ 15 V)**  
**(Recommended DC Supply Voltage (V<sub>CC</sub> - V<sub>SS</sub>) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	
				CD4049AE, CD4050AE									
		V <sub>O</sub> Volts	V <sub>CC</sub> Volts	-40°C			25°C			85°C			
Quiescent Device Current	I <sub>L</sub>			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	V <sub>IH</sub> = V <sub>CC</sub>		5	—	3	—	0.03	3	—	—	42		
Quiescent Device Dissipation Package	P <sub>D</sub>	V <sub>IH</sub> = V <sub>CC</sub>		10	—	5	—	0.05	5	—	—	70	
				5	—	15	—	0.15	15	—	—	210	
Output Voltage Low-Level	V <sub>OL</sub>			10	—	50	—	0.5	50	—	—	700	
				5	—	0.01	—	0	0.01	—	—	0.05	
High-Level	V <sub>OH</sub>			10	—	0.01	—	0	0.01	—	—	0.05	
				5	4.99	—	—	4.99	5	—	4.95	—	
Noise Immunity (All Inputs) CD4049A	V <sub>NL</sub>	V <sub>OH</sub> = 3.6 V		10	—	—	1	2.25	—	0.9	—	—	
		V <sub>OH</sub> = 7.2 V		5	1	—	—	—	—	—	—	—	
CD4050A		V <sub>OL</sub> = 0.95 V		10	2	—	—	2	4.5	—	1.9	—	
		V <sub>OL</sub> = 2.9 V		5	1.5	—	—	1.5	2.25	—	1.4	—	
CD4050A		V <sub>OH</sub> = 7.2 V		10	3	—	—	3	4.5	—	2.9	—	
		V <sub>OH</sub> = 3.6 V		10	2.9	—	—	3	4.5	—	3	—	
CD4049A		V <sub>OL</sub> = 2.9 V		5	1.4	—	—	1.5	2.25	—	1.5	—	
		V <sub>OL</sub> = 0.95 V		10	2.9	—	—	3	4.5	—	3	—	
Output Drive Current N-CHANNEL	I <sub>DN</sub>			0.4	4.5	3.1	—	—	2.6	5.2	—	2.1	
				0.4	5	3.6	—	—	3	6.0	—	2.5	
P-CHANNEL	I <sub>DP</sub>			0.5	10	9.6	—	—	8	16	—	6.6	
				4.5	5	-0.6	—	—	-0.5	-1	—	-0.4	
Input Current	I <sub>I</sub>	V <sub>IH</sub> =V <sub>CC</sub>		2.5	5	-1.5	—	—	-1.25	-2.5	—	-1	
				9.5	10	-1.5	—	—	-1.25	-2.5	—	-1	

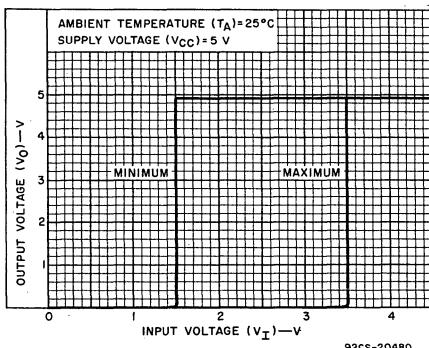
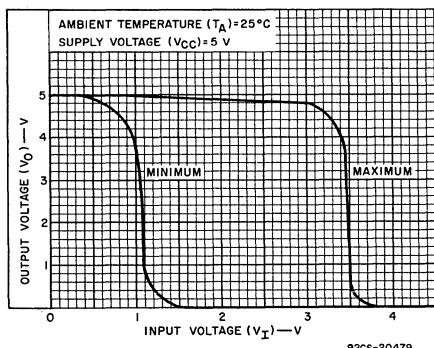


Fig.2 – Min. &amp; max. voltage transfer characteristics for CD4049A.

Fig.3 – Min. &amp; max. voltage transfer characteristics for CD4050A.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A=25^\circ\text{C}$ ,  $C_L=15 \text{ pF}$ , and input rise and fall times=20 ns  
 Typical Temperature Coefficient for all values of  $V_{CC} = 0.3\%/\text{ }^\circ\text{C}$ . (See Appendix for Waveforms)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS Fig. No.	
			CD4049AD, AE CD4049AF, AK			CD4050AD, AE CD4050AF, AK					
			V <sub>CC</sub> (Volts)	Min.	Typ.	Max.	Min.	Typ.	Max.		
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>	V <sub>IH</sub> =V <sub>CC</sub>	5 10	— —	15 10	55 30	— —	55 25	110 55	ns	10,11
Low-to-High Level	t <sub>PLH</sub>	V <sub>IH</sub> =V <sub>CC</sub>	5 10	— —	50 25	80 55	— —	75 35	140 85	ns	12,13
Transition Time: High-to-Low Level	t <sub>THL</sub>	V <sub>IH</sub> =V <sub>CC</sub>	5 10	— —	20 16	45 40	— —	20 16	45 40	ns	14
Low-to-High Level	t <sub>TLH</sub>	V <sub>IH</sub> =V <sub>CC</sub>	5 10	— —	50 30	100 60	— —	50 30	100 60	ns	15
Input Capacitance (Any Input)	C <sub>I</sub>	CD4049A CD4050A		— —	15 5	— —	— —	15 5	— —	pF	

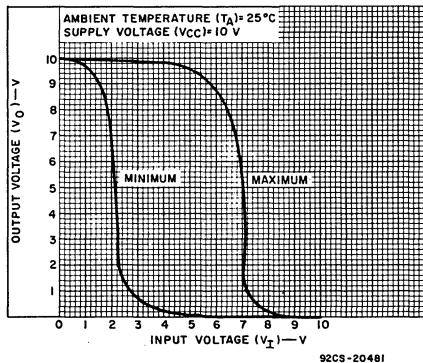


Fig.4 – Min. & max. voltage transfer characteristics for CD4049A.

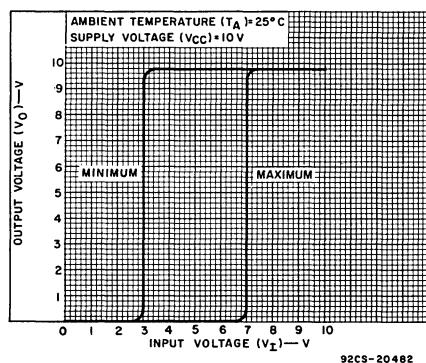


Fig.5 – Min. & max. voltage transfer characteristics for CD4050A.

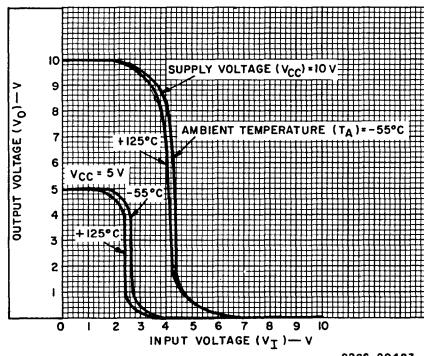


Fig.6 – Typ. voltage transfer characteristics as a function of temperature for CD4049A.

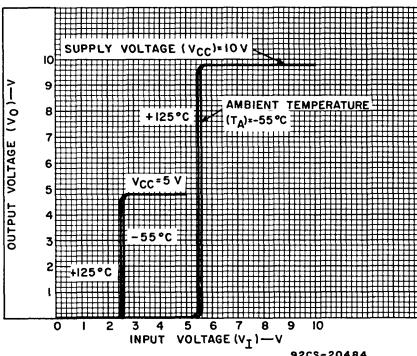


Fig.7 – Typ. voltage transfer characteristics as a function of temperature for CD4050A.

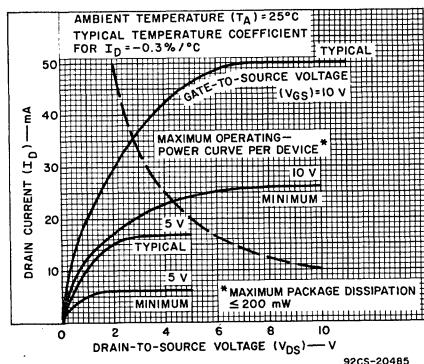


Fig.8 – Typ. & min. drain characteristics as a function of gate-to-source voltage ( $V_{GS}$ ) for CD4049A, CD4050A.

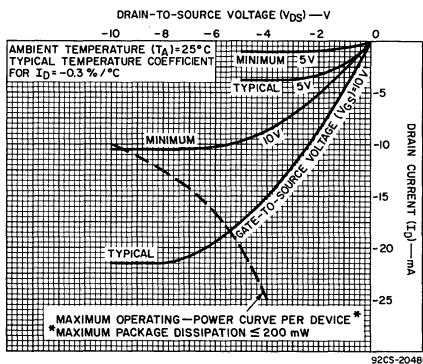


Fig.9 – Typ. & min. P-channel drain characteristics as a function of gate-to-source voltage ( $V_{GS}$ ) for CD4049A, CD4050A.

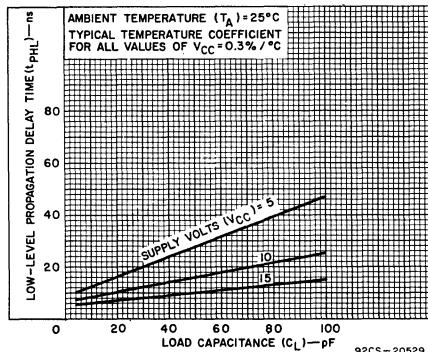


Fig.10 – Typ. high-to-low level propagation delay time vs.  $C_L$  for CD4049A.

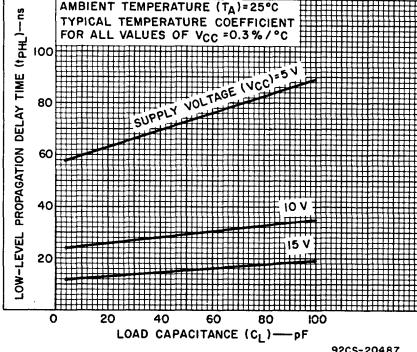


Fig.11 – Typ. high-to-low level propagation delay time vs.  $C_L$  for CD4050A.

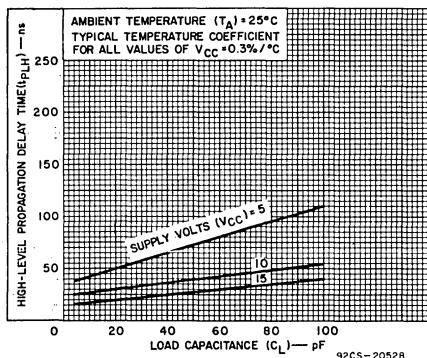


Fig.12 – Typ. low-to-high level propagation delay time vs.  $C_L$  for CD4049A.

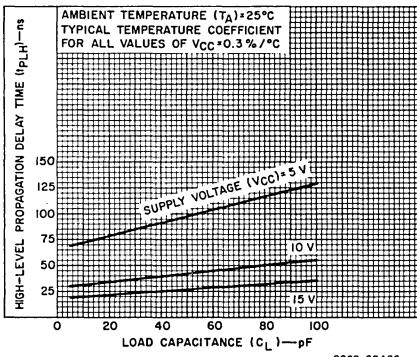


Fig.13 – Typ. low-to-high level propagation delay time vs.  $C_L$  for CD4050A.

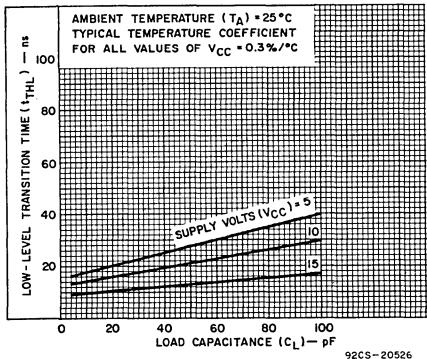


Fig.14 – Typ. high-to-low level transition time vs.  $C_L$  for CD4049A, CD4050A.

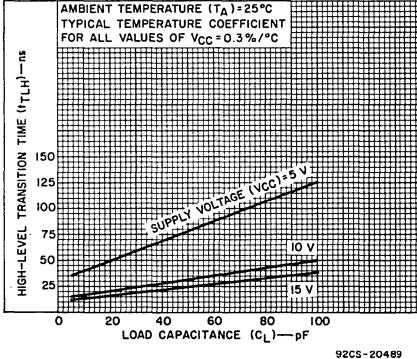


Fig.15 – Typ. low-to-high level transition time vs.  $C_L$  for CD4049A, CD4050A.

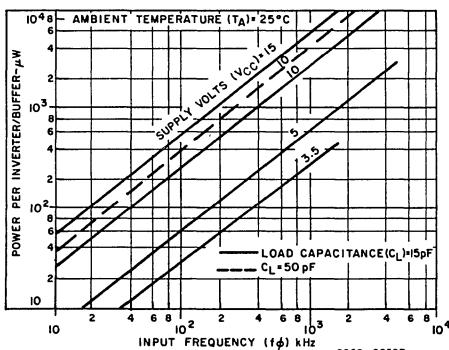


Fig.16 – Typ. dissipation characteristics for CD4049A, CD4050A.

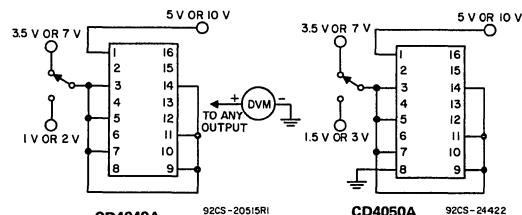


Fig.17 – Noise immunity test circuits.

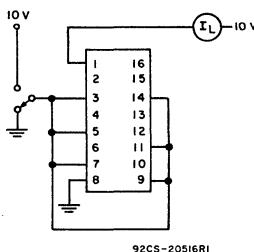


Fig.18 – Quiescent device current test circuit.

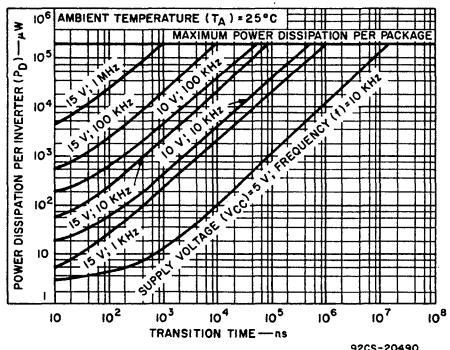


Fig.19 – Typ. power dissipation vs transition time per inverter CD4049A.

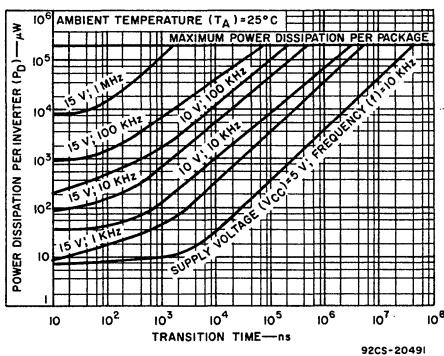


Fig.20 – Typ. power dissipation vs. transition time per inverter CD4050A.

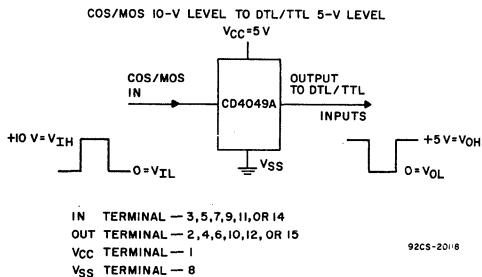


Fig.21 – Logic-level conversion application.



# Digital Integrated Circuits

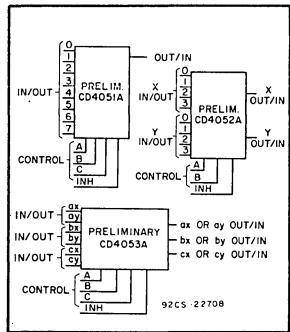
Monolithic Silicon

Preliminary CD4051AD, CD4051AE, CD4051AK

Preliminary CD4052AD, CD4052AE, CD4052AK

Preliminary CD4053AD, CD4053AE, CD4053AK

## Preliminary Data ▲



RCA COS/MOS Analog Multiplexers/Demultiplexers\*. Preliminary CD4051A, CD4052A, and CD4053A are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage current. Control of analog signals up to 15 V p-p can be achieved by digital signal amplitudes of 3 to 15 V. For example, if  $V_{DD} = +5$  V,  $V_{SS} = 0$  V, and  $V_{EE} = -5$  V, analog signals from -5 V to +5 V can be controlled by digital inputs of 0 to 5 V. The multiplexer circuits dissipate extremely low quiescent power over the full  $V_{DD} - V_{SS}$  and  $V_{DD} - V_{EE}$  supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are "OFF".

CD4051A is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052A is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053A is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

These devices are supplied in a 16-lead dual-in-line ceramic package (CD4051AD, CD4052AD, and CD4053AD), a 16-lead dual-in-line plastic package (CD4051AE, CD4052AE, and CD4053AE), or a 16-lead flat pack (CD4051AK, CD4052AK, and CD4053AK).

\* When the devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminal(s) is (are) the input(s).

## COS/MOS Analog Multiplexers/Demultiplexers

### With Logic — Level Conversion

CD4051A Single 8-Channel Multiplexer/Demultiplexeur

CD4052A Differential 4-Channel Multiplexer/Demultiplexeur

CD4053A Triple 2-Channel Multiplexer/Demultiplexeur

### Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

### Features:

- Wide range of digital and analog signal levels: digital 3 to 15 V, analog to 15 V p-p
- Low "ON" resistance:  $80\Omega$  (typ.) over entire 15 V p-p signal-input range for  $V_{DD} - V_{EE} = 15$  V
- High "OFF" resistance: input leakage  $\pm 10$  pA (typ.) @  $V_{DD} - V_{EE} = 10$  V
- Matched switch characteristics:  $\Delta R_{ON} = 5\Omega$  (typ.) for  $V_{DD} - V_{EE} = 15$  V
- Logic-level conversion for digital addressing signals of 3 to 15 V ( $V_{DD} - V_{SS} = 3$  V to 15 V) to switch analog signals to 15 V p-p ( $V_{DD} - V_{EE} = 15$  V)
- Very low quiescent power dissipation under all digital-control input and supply conditions:  $1 \mu\text{W}$  typ. @  $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10$  V
- Binary address decoding on chip

TRUTH TABLE

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051A	CD4052A	CD4053A
0	0	0	0	0	0x, 0y	cx, bx, ax
0	0	0	1	1	1x, 1y	cx, bx, ay
0	0	1	0	2	2x, 2y	cx, by, ax
0	0	1	1	3	3x, 3y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

\* = Don't care condition

**MAXIMUM RATINGS, Absolute Maximum Values**

Storage-Temperature Range	.....	-65°C to +150°C
Operating-Temperature Range	.....	.....
Ceramic Packages	.....	-55°C to +125°C
Plastic Packages	.....	-40°C to +85°C
Dissipation Per Package	.....	200 mW
DC Supply Voltages	.....	.....
V <sub>DD</sub> - V <sub>SS</sub> ; V <sub>DD</sub> - V <sub>EE</sub>	.....	-0.5 to +15 V
Digital Control Inputs	.....	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>
<b>Minimum Recommended Power Supply Voltages</b>	.....	.....
V <sub>DD</sub> - V <sub>SS</sub> ; V <sub>DD</sub> - V <sub>EE</sub>	.....	3 V
Lead Temperature (During soldering)	.....	.....
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	.....	265°C

**Operating Precautions:**

1. R<sub>L</sub> ≥ 100 Ω
2. Signal Input Current Capability < 25 mA

**OPERATING CONSIDERATIONS****1. Handling**

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces fully protect COS/MOS devices from gate-oxide failure (70 to 100 volt limit) for static discharge or signal voltage up to 1 to 2 kilovolts under most transient or low-current conditions.

Although protection against electrostatic effects is provided by built-in circuitry, the following handling precautions should be taken:

1. Soldering-iron tips and test equipment should be grounded.
2. Devices should not be inserted in non-conductive containers such as conventional plastic snow or trays.

**2. Operating****Unused Inputs**

All unused input leads must be connected to either V<sub>SS</sub> or V<sub>DD</sub>, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4009A, CD4010A, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V<sub>SS</sub> or V<sub>DD</sub>. A useful range of values for such resistors is from 0.2 to 1 megohm.

**Input Signals**

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes.

**Output Short Circuits**

Shorting of outputs to V<sub>SS</sub> or V<sub>DD</sub> can damage many of the higher-output-current COS/MOS-types, such as the CD4007A, CD4009A, and CD4010A. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

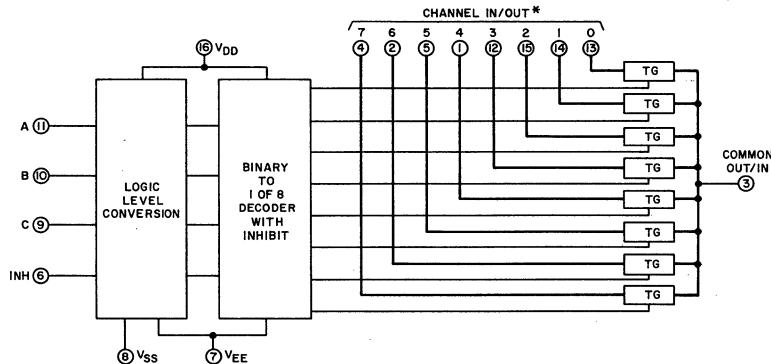


Fig. 1 – Functional diagram preliminary CD4051A.

\* See operating precautions, above.

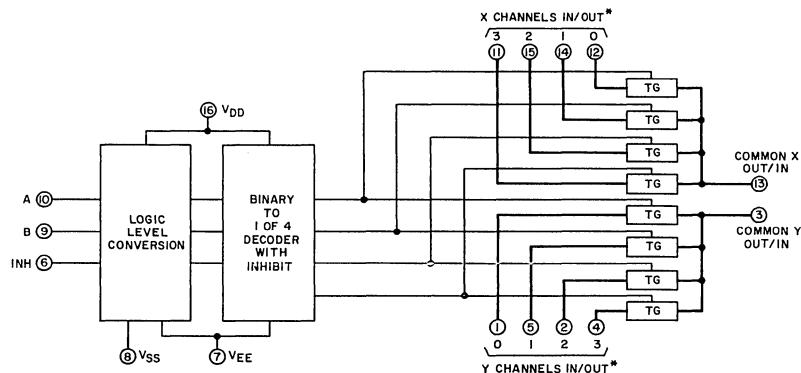


Fig. 2 – Functional diagram preliminary CD4052A.

92CS - 20086RI

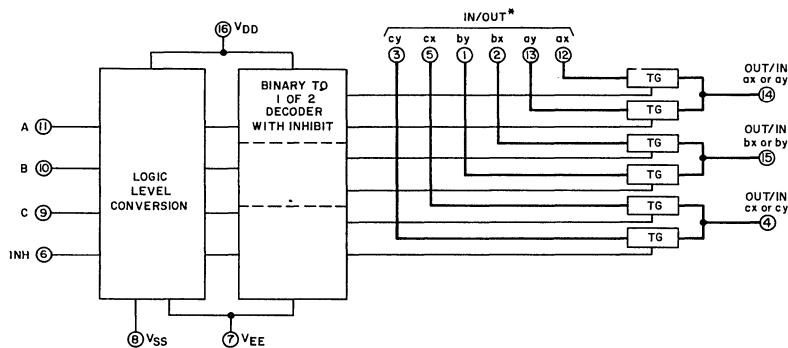


Fig. 3 – Functional diagram, preliminary CD4053A.

92CS - 20087RI

\* See operating precautions, P. 2.

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			TYPICAL VALUES	UNITS	CURVE & TEST CIRCUIT Fig. No.
		V <sub>DD</sub>	V <sub>SS</sub>	V <sub>EE</sub>			
Quiescent Device Current	I <sub>L</sub>	+10 V	0 V	0 V	0.1	μA	–
		+ 5 V	0 V NOTE 1	-5 V			
Quiescent Device Dissipation per Package	P <sub>D</sub>	+10 V	0 V	0 V	1	μW	–
		+ 5 V	0 V NOTE 1	-5 V			

NOTE 1: All digital combinations on address inputs; all analog inputs

$$V_{EE} \leq V_1 \leq V_{DD}$$

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			TYPICAL VALUES	UNITS	CURVE & TEST CIRCUIT Fig. No.	
<b>SIGNAL INPUTS (<math>V_{IS}</math>) AND OUTPUTS (<math>V_{OS}</math>)</b>								
"ON" Resistance (Peak for $V_{SS} \leq V_{IS} \leq V_{DD}$ )	$R_{ON}$	$R_L = 10 \text{ k}\Omega$ $V_{SS} = 0$	$V_{DD}$	$V_{EE}$	$V_{IS}$	80	Ω	
			+7.5 V	-7.5 V OR 0 V	—			
			+15 V	0 V	—	120		
			+5 V	-5 V OR 0 V	—			
	$\Delta R_{ON}$	(Any channel selected)	+10 V	0 V	—	270	—	
			+2.5 V	-2.5 V OR 0 V	—			
			+5 V	0 V	—	5		
			+7.5 V	-7.5 V OR 0 V	—			
Δ "ON" Resistance Between Any 2 Channels	$\Delta R_{ON}$		+15 V	-5 V	—	10	Ω	
			+5 V	-5 V OR 0 V	—			
Sine Wave Response (Distortion)		$R_L = 10 \text{ k}\Omega$ $V_{SS} = 0$ $f_{IS} = 1 \text{ kHz}$	+7.5 V +5 V +2.5 V	-7.5 V -5 V -2.5 V	5 V (p-p)▲	0.1 0.2 1	%	
OFF Channel Leakage Current: Any Channel "OFF"		$V_{SS} = 0 \text{ V}$	+5 V	(= $V_C$ ) -5 V	—	±0.01	nA	
All Channels "OFF" (Common OUT/IN)		INHIBIT +5 V $V_{SS} = 0 \text{ V}$	+5 V	(= $V_C$ ) -5 V	CD4051A CD4052A CD4053A	±0.08 ±0.04 ±0.02	11 12	
Frequency Response— Channel "ON" (Sine Wave Input)		$R_L = 1 \text{ k}\Omega$ $V_{IS} = 5 \text{ V (p-p)}$ $V_{SS} = 0 \text{ V}$	$V_C - V_{DD} = +5 \text{ V}$ , $V_{EE} = -5 \text{ V}$	$20 \log_{10} \frac{V_{OS}}{V_{IS}} = -3 \text{ dB}$	40	MHz		
Feedthrough Channel "OFF"			$V_{DD} = +5 \text{ V}$ , $V_C = V_{EE} = -5 \text{ V}$	$20 \log_{10} \frac{V_{OS}}{V_{IS}} = -40 \text{ dB}$	1	MHz		
Crosstalk Between any 2 Channels (Frequency at -40 dB)		$R_L = 1 \text{ k}\Omega$ $V_{IS} (\text{A}) = 5 \text{ V (p-p)}$ $V_{SS} = 0 \text{ V}$	$V_C(\text{A}) - V_{DD} = +5 \text{ V}$ $V_C(\text{B}) - V_{EE} = -5 \text{ V}$	$20 \log_{10} \frac{V_{OS}}{V_{IS}} = -40 \text{ dB}$	1	MHz		
Capacitance:	Input	$C_{IS}$	$V_{DD} = +5 \text{ V}$ $V_C = V_{EE} = -5 \text{ V}$ $V_{SS} = 0 \text{ V}$	CD4051A CD4052A CD4053A 0.2	5	pF		
	Output (Common) (OUT/IN)	$C_{OS}$			30			
	Feedthrough	$C_{IOS}$			18			
					10			
Propagation Delay: Signal Input-to- Signal Output	$t_{PLH}$ , $t_{PHL}$	$V_C = V_{DD} = +10 \text{ V}$ , $V_{EE} = 0 \text{ V}$ , $C_L = 15 \text{ pF}$ $V_{IS} = 10 \text{ V}^*$ , $V_{SS} = 0 \text{ V}$ ▲ Inhibit $t_r, t_f = 20 \text{ ns}$ (input signal)			10	ns		
<b>CONTROL (<math>V_C</math>) INPUTS A, B, C, AND INHIBIT</b>								
Noise Immunity (Any control input)	$V_{NL}$	$V_{IS} = V_{DD}$ thru 1 kΩ	$V_{DD} - V_{SS} = 10 \text{ V}$	$V_{DD} - V_{SS} = 5 \text{ V}$	4.5 2.25	V	—	
	$V_{NH}$	$I_{IS} = 10 \mu\text{A}$ $R_L = 1 \text{ k}\Omega$ to $V_{EE}$	$V_{DD} - V_{SS} = 10 \text{ V}$	$V_{DD} - V_{SS} = 5 \text{ V}$	4.5 2.25			
Average Input Capacitance	$C_I$	$V_{DD} = +5 \text{ V}$ $V_{SS} = 0 \text{ V}$	$V_{EE} = -5 \text{ V}$ Channel "OFF"		5	pF	—	

♦ Square wave

▲ Symmetrical about 0 volts.

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				TYPICAL VALUES	UNITS	CURVE & TEST CIRCUIT Fig. No.
<b>CONTROL (<math>V_C</math>) INPUTS A, B, C, AND INHIBIT</b>								
Turn "ON" Propagation Delay: <sup>♦</sup> Control Input-to-signal output	$t_{PLH}$ , $t_{PHL}$	$C_L = 15 \text{ pF}$ $R_L = 10 \text{ k}\Omega$ $V_{is} \leq V_{DD}$ $t_r, t_f = 20 \text{ ns}$ $V_{SS} = \text{Inhibit} = 0 \text{ V}$	$V_C$ <sup>◆</sup> 10 V 5 V +5 V to -5 V	$V_{DD}$ 10 V 5 V 5 V	$V_{EE}$ 0 V 0 V -5 V	200 400 400	ns	13
		$C_L = 15 \text{ pF}$ $R_L = 10 \text{ k}\Omega$ $V_{is} = V_{DD}$ $t_r, t_f = 20 \text{ ns}$	10 V 5 V	10 V 5 V	0 V 0 V	300 600	ns	14
Inhibit Recovery Time*	-	$V_{DD} = 10 \text{ V}$				200	ns	

♦ Time after inhibit is removed during which channel information is invalid

◆ Square wave

♦ Channel Overlap = Turn-on propagation delay, where channel overlap is defined as the duration after control signal change during which two channels may be on together.

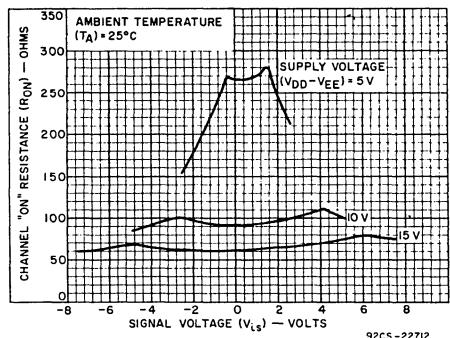
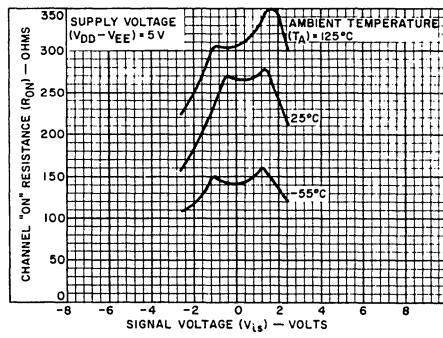
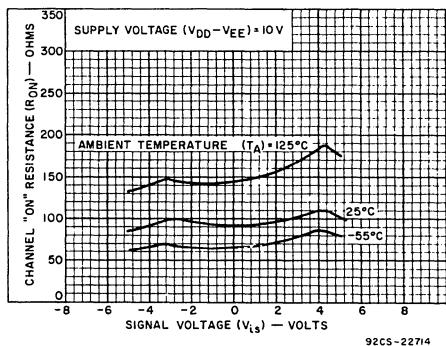
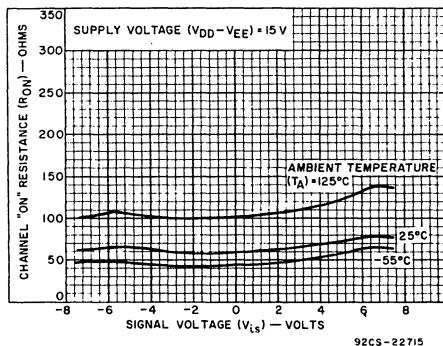
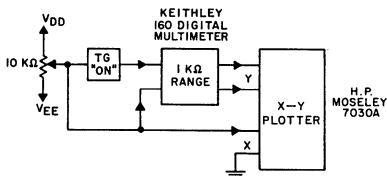


Fig. 4(a) — Typical Channel "ON" resistance vs. signal voltage for preliminary CD4051A.

Fig. 4(b) — Typical Channel "ON" resistance vs. signal voltage for preliminary CD4051A with supply voltage ( $V_{DD} - V_{EE}$ ) = 5 V.Fig. 4(c) — Typical Channel "ON" resistance vs. signal voltage for preliminary CD4051A with supply voltage ( $V_{DD} - V_{EE}$ ) = 10 V.Fig. 4(d) — Typical Channel "ON" resistance vs. signal voltage for preliminary CD4051A with supply voltage ( $V_{DD} - V_{EE}$ ) = 15 V.



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Fig. 5 – Channel "ON" resistance measurement circuit.

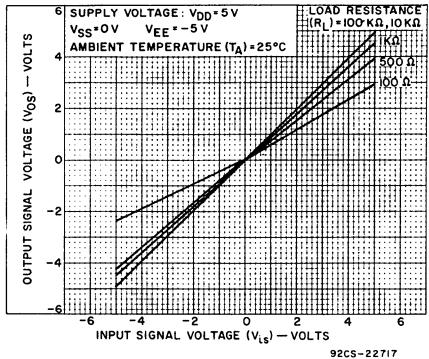


Fig. 6 – Typical "ON" characteristics for 1 of 8 channels for preliminary CD4051A.

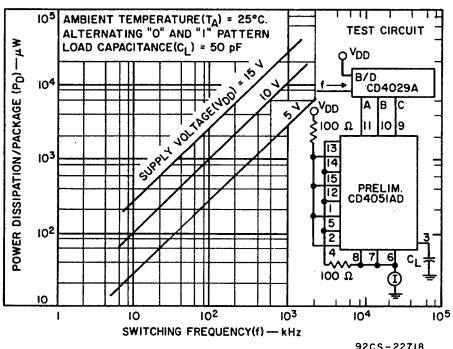


Fig. 7 – Typical dissipation (per package) vs. switching frequency for preliminary CD4051AD.

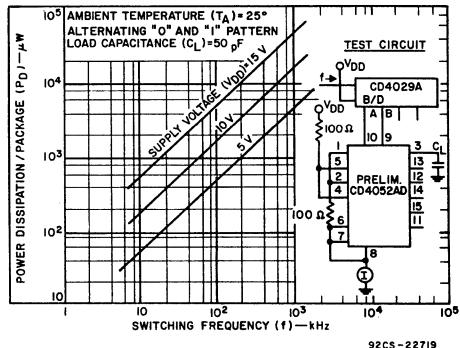


Fig. 8 – Typical dissipation (per package) vs. switching frequency for preliminary CD4052AD.

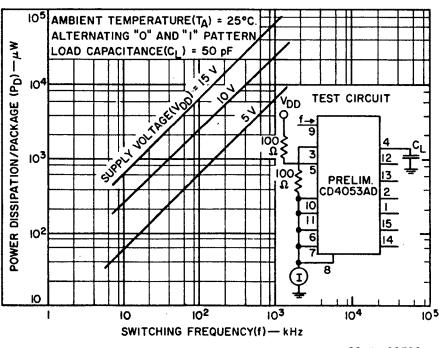
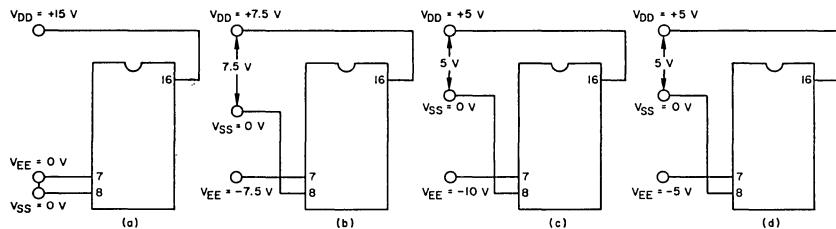
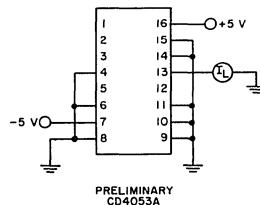
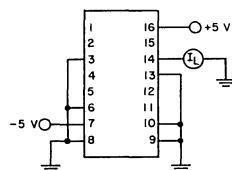
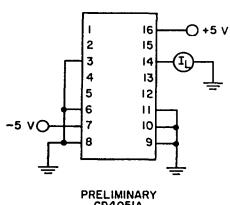


Fig. 9 – Typical dissipation (per package) vs. switching frequency for preliminary CD4053AD.



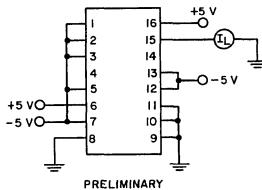
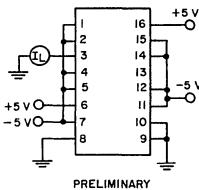
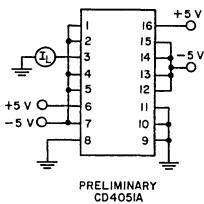
92CS-20088RI

### TEST CIRCUITS



92CS-22722

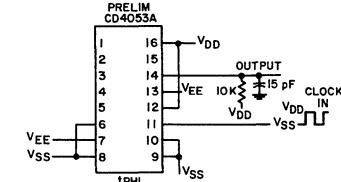
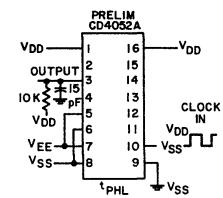
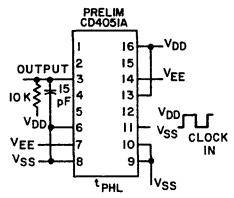
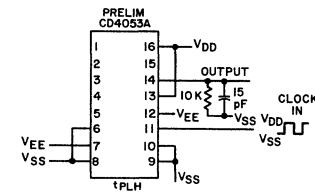
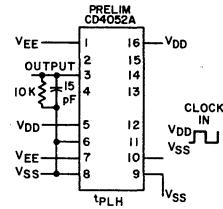
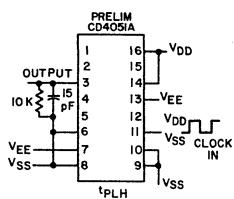
Fig. 11 – OFF channel leakage current . . . any channel off.



92CS-22723

Fig. 12 – OFF channel leakage current . . . all channels off.

## TEST CIRCUITS



92CM-22724

Fig. 13 — Turn-on propagation delay . . . control input to signal output.

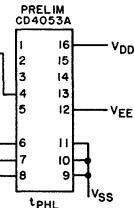
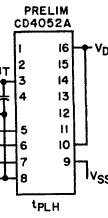
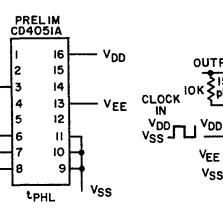
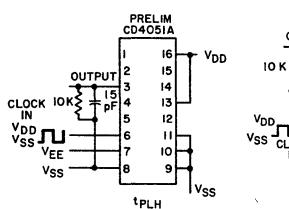


Fig. 14 — Turn-on propagation delay . . . inhibit input to signal output.

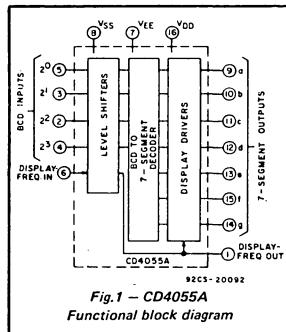
92CM-22725



# Digital Integrated Circuits

Monolithic Silicon

**CD4054AD**   **CD4054AE**   **CD4054AK**  
**CD4055AD**   **CD4055AE**   **CD4055AK**  
**CD4056AD**   **CD4056AE**   **CD4056AK**



## COS/MOS Liquid-Crystal Display Drivers

**CD4054A** – 4-Segment Display Driver

**CD4055A** – BCD to 7-Segment Decoder/Driver with  
“Display-Frequency” Output

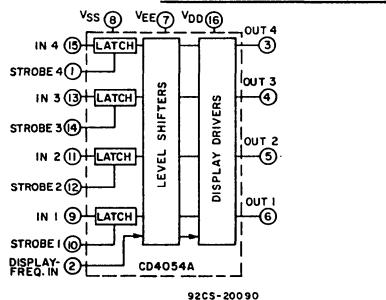
**CD4056A** – BCD to 7-Segment Decoder/Driver with  
Strobed-Latch Function

### Features:

- Operation of liquid crystals with COS/MOS circuits provides ultra-low-power displays
- Equivalent AC output drive for liquid-crystal displays – no external capacitor required
- Voltage doubling across display ( $(V_{DD} - V_{EE}) = 15$  V)  
results in effective 30 V (p-p) drive across selected display segments

RCA-CD4055A and CD4056A are Single-Digit BCD-to-7-Segment Decoder/Driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings ( $V_{DD}$  to  $V_{SS}$ ) to be the same as or different from the 7-segment output-signal swings ( $V_{DD}$  to  $V_{EE}$ ). For example, the BCD input-signal swings ( $V_{DD}$  to  $V_{SS}$ ) may be as low as 0 to  $-3$  V, whereas the output-display drive-signal swing ( $V_{DD}$  to  $V_{EE}$ ) may be from 0 to  $-15$  V.

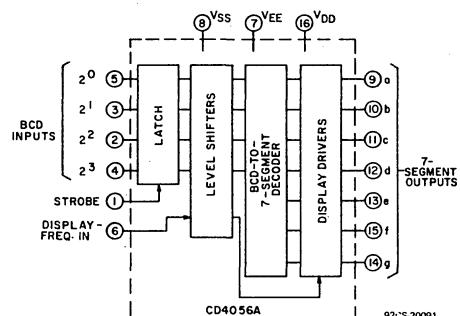
The 7-segment outputs are controlled by the “Display-Frequency” (DF) input which causes the selected segment outputs to be “low”, “high”, or a “square-wave” output (for liquid-crystal displays). When the DF input is “low” the output segments will be “high” when selected by the BCD inputs. When the DF input is “high”, the output segments will be “low” when selected by the BCD inputs. When a square wave is present at the DF input, the selected segments will have a square-wave output which is  $180^\circ$  out of phase with the DF input. Those segments which are not selected will have a



- Low- or high-output level DC drive for other types of displays
- On-chip logic – level conversion for different input- and output-level swings
- Full decoding of all input combinations: “0–9, L, H, P, A, –,” and blank positions
- Strobed-latch function – CD4054A and CD4056A
- “Display-frequency” (DF) output for liquid-crystal common-line drive signal CD4054A and CD4055A

### Applications:

- |                             |                            |
|-----------------------------|----------------------------|
| ■ General-purpose displays  | ■ Portable lab instruments |
| ■ Calculators and meters    | ■ Panel meters             |
| ■ Wall and table clocks     | ■ Auto dashboard displays  |
| ■ Industrial control panels | ■ Appliance control panels |



**Maximum Ratings, Absolute-Maximum Values:**

Storage-Temperature Range . . . . .	-65 to +150	°C	Minimum Recommended
Operating-Temperature Range: Ceramic Package Types . . . . .	-55 to +125	°C	DC Supply Voltage ( $V_{DD}$ – $V_{SS}$ ) or ( $V_{DD}$ – $V_{EE}$ ) . . . . .
Plastic Package Types . . . . .	-40 to +85	°C	Lead Temperature (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . .
DC Supply-Voltage Range ( $V_{DD}$ – $V_{SS}$ ) or ( $V_{DD}$ – $V_{EE}$ ) . . . . .	-0.5 to +15	V	265 °C
Device Dissipation (Per Pkg.) . . . . .	200	mW	$V_{SS} \leq V_I \leq V_{DD}$
All Inputs . . . . .			

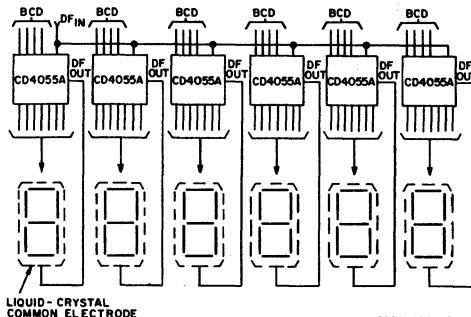


Fig.4 – Clock display:  $V_{DD} = 0$  V,  $V_{SS} = -5$  V,  $V_{EE} = -15$  V,  $DF_{IN} = 30$  Hz square wave

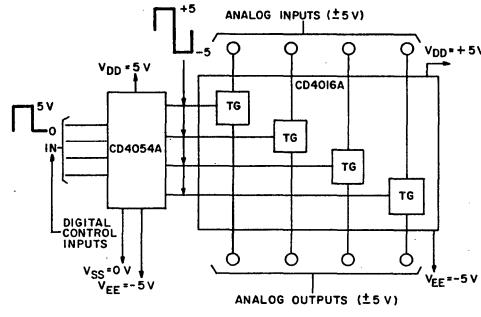


Fig.5 – Digital (0.5 V) to bidirectional analog control (+5 to –5 V) level shifter

square-wave output that is in phase with the input. The DF input square wave is required to provide equivalent ac drive to liquid-crystal displays such as RCA Dev. Nos. TA8054R, TA8054T, TA8055R, and TA8055T. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055A provides a level-shifted high amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056A provides a strobed latch function at the BCD inputs. Decoding of all input combinations on the CD4055A and CD4056A provides displays of 0 to 9 as well as “L, H, P, A, –,” and a blank position.

The CD4054A provides level shifting similar to the CD4055A and CD4056A, independently strobed latches, and common DF control on 4 signal lines. The CD4054A is intended to provide drive-signal compatibility with the CD4055A and CD4056A 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054A output line by connecting the corresponding input and strobe lines to a “low” and “high” level, respectively. The CD4054A may also be utilized for logic-level “up conversion” or “down conversion”. For example, input-signal swings ( $V_{DD}$  to  $V_{SS}$ ) from +5 to 0 V can be converted to output-signal swings

( $V_{DD}$  to  $V_{EE}$ ) of +5 to –5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a “low” level of  $V_{SS}$  to a high level of  $V_{DD}$  while the output swings from a “low” level of  $V_{EE}$  to the same “high” level of  $V_{DD}$ . Thus the input and output swings can be selected independently of each other over a 3-to-15 V range.  $V_{SS}$  may be connected to  $V_{EE}$  when no level-shift function is required.

For the CD4054A and CD4056A data is transferred from input to output by placing a “high” voltage level at the strobe input. A “low” voltage level at the strobe input latches the data input and the corresponding outputs.

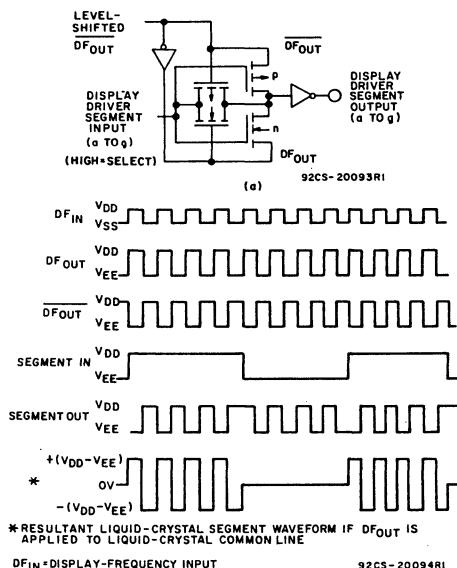
Whenever the level-shifting function is required, the CD4055A can be used by itself to drive a liquid-crystal display (Figs. 4 and 7). However, the CD4056A must be used together with a CD4054A to provide the common DF output (see Fig. 8). The capability of extending the voltage swing on the negative end can be used to advantage in the setup of Fig. 5. Fig. 6 is common to all three IC types.

These devices are available in 16-lead dual-in-line ceramic packages (“D suffix), dual-in-line plastic packages (“E” suffix), 16-lead flat packages (“K” suffix), or in chip form (“H” suffix).

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) . . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.			
				CD4054AD		CD4054AK		CD4055AD		CD4055AK						
		$V_O$	$V_{DD} - V_{SS}$	-55°C		25°C		125°C		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Device Current	$I_L$			5	10	—	—	10	—	0.5	10	—	—	100	$\mu A$	18,19,20
	15	15	—	—	20	—	1	20	—	—	—	—	200			
Quiescent Device Dissipation/Package	$P_D$	5	10	—	—	100	—	5	100	—	—	1000	—	—	$\mu W$	
		15	15	—	—	300	—	15	300	—	—	3000	—	—		
Output Voltage: Low-Level	$V_{OL}$	5	10	—	—	0.01	—	0	0.01	—	—	0.05	—	—	$V$	
		15	15	—	—	0.01	—	0	0.01	—	—	0.05	—	—		
High-Level	$V_{OH}$	5	10	9.99	—	—	9.99	10	—	9.95	—	—	—	—	$V$	
		15	15	14.99	—	—	14.99	15	—	14.95	—	—	—	—		
Noise Immunity (All Inputs)*	$V_{NL}$	1	5	10	1	—	—	1	2.25	—	1	—	—	—	$V$	15,16,17
		1.5	15	15	2	—	—	2	6.75	—	2	—	—	—		
	$V_{NH}$	9	5	10	1	—	—	1	2.25	—	1	—	—	—		
		13.5	15	15	2	—	—	2	6.75	—	2	—	—	—		
Output Drive Current: (All Outputs)																
N-Channel	$I_{DN}$	0.5	5	10	1.1	—	—	0.9	1.8	—	0.6	—	—	—	$mA$	11,12
		0.5	15	15	1.7	—	—	1.4	2.8	—	1	—	—	—		
(All Outputs) P-Channel	$I_{DP}$	9.5	5	10	-0.6	—	—	-0.45	-0.9	—	-0.3	—	—	—	$mA$	13,14
		14.5	15	15	-0.9	—	—	-0.7	-1.4	—	-0.5	—	—	—		

\* For definition, see Appendix.



\*RESULTANT LIQUID-CRYSTAL SEGMENT WAVEFORM IF DF OUT IS APPLIED TO LIQUID-CRYSTAL COMMON LINE

DF IN = DISPLAY-FREQUENCY INPUT 92CS-20094RI  
 DF OUT = LEVEL-SHIFTED DISPLAY-FREQUENCY OUTPUT

(b)

Fig.6 — Display-driver circuit for one segment line and waveforms

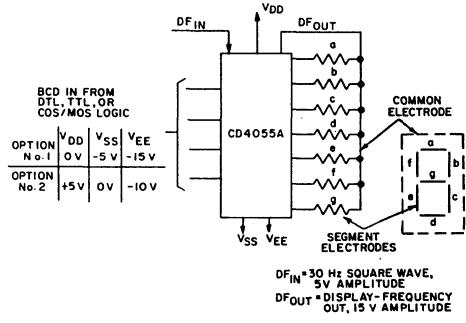


Fig.7 — Single-digit liquid-crystal display

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS						UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS  Fig. No.	
					CD4054AE CD4055AE CD4056AE								
		$V_O$	$V_{DD} - V_{SS}$	$V_{DD} - V_{EE}$	-40°C			25°C			Min.	Typ.	Max.
Quiescent Device Current	$I_L$		5	10	—	—	10	—	0.5	10			
			15	15	—	—	20	—	1	20			100
Quiescent Device Dissipation/Package	$P_D$	$V_O$	5	10	—	—	100	—	5	100			500
			15	15	—	—	300	—	15	300			1500
Output Voltage: Low-Level	$V_{OL}$	$V_O$	5	10	—	—	0.01	—	0	0.01		V	
			15	15	—	—	0.01	—	0	0.01			0.05
High-Level	$V_{OH}$	$V_O$	5	10	9.99	—	—	9.99	10	—	9.95	—	—
			15	15	14.99	—	—	14.99	15	—	14.95	—	—
Noise Immunity (All Inputs)*	$V_{NL}$	1	5	10	1	—	—	1	2.25	—	1	—	—
		1.5	15	15	2	—	—	2	6.75	—	2	—	—
	$V_{NH}$	9	5	10	1	—	—	1	2.25	—	1	—	—
		13.5	15	15	2	—	—	2	6.75	—	2	—	—
Output Drive Current: (All Outputs)	$I_{DN}$	$I_D$	0.5	5	10	0.7	—	—	0.6	1.8	—	0.5	—
			0.5	15	15	1.2	—	—	1	2.8	—	0.8	—
(All Outputs) P-Channel	$I_{DP}$	$I_D$	9.5	5	10	-0.4	—	—	-0.3	-0.9	—	-0.2	—
			14.5	15	15	-0.6	—	—	-0.5	-1.4	—	-0.4	—

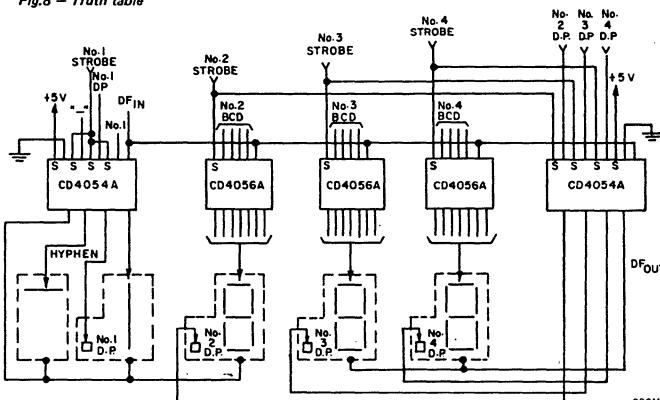
\* For definition, see Appendix.

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , and input rise and fall times = 20 ns  
 Typical Temperature Coefficient at all values of  $V_{DD}$  = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS						UNITS	CHARAC- TERISTIC CURVES  Fig. No.	
					CD4054AD,AK			CD4054AE					
		$V_{DD} - V_{SS}$	$V_{DD} - V_{EE}$	Min.	Typ.	Max.	Min.	Typ.	Max.	ns	—	—	
Propagation Delay Time (Any Input to Any Output)	$t_{PHL}, t_{PLH}$	5	10	—	450	900	—	450	1200	ns	—	—	
		15	15	—	300	600	—	300	800				
Transition Time (Any Output)	$t_{THL}, t_{TLH}$	5	10	—	40	80	—	40	110	ns	—	—	
		15	15	—	30	60	—	30	80				
Data Setup Time*	$t_s$	5	10	—	70	140	—	70	200	ns	9	9	
		15	15	—	30	60	—	30	80				
Strobe Pulse* Duration	$t_w$	5	10	—	85	170	—	85	220	ns	9	9	
		15	15	—	40	80	—	40	110				
Input Capacitance	$C_I$	Any Input			—	5	—	—	5	—	pF	—	—

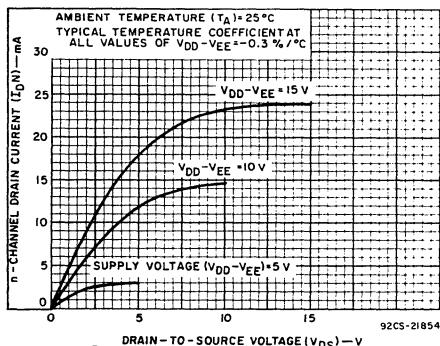
\* CD4054A and CD4056A only.

**Fig.8 – Truth table**

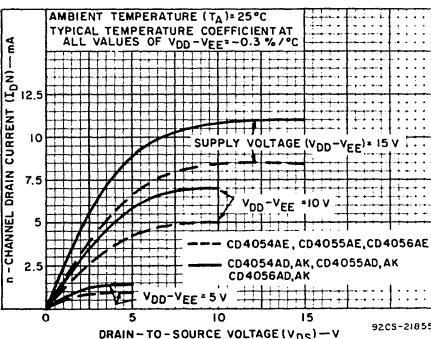


**Fig. 10 – Typical 3-1/2-digit liquid crystal display:  $V_{DD} = +5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{EE} = -10\text{ V}$ ,  $PF_{IN} = 30\text{ Hz}$  square wave**

## CHARACTERISTIC CURVES



**Fig. 11 – Typical n-channel drain characteristics**



**Fig. 12** – Minimum  $n$ -channel drain characteristics

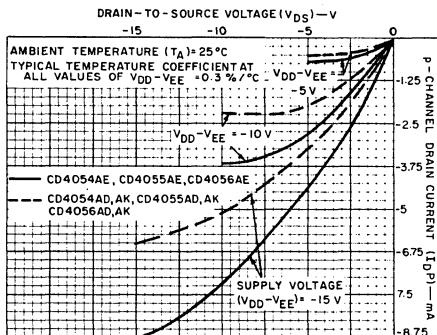


Fig.13 – Typical p-channel drain characteristics

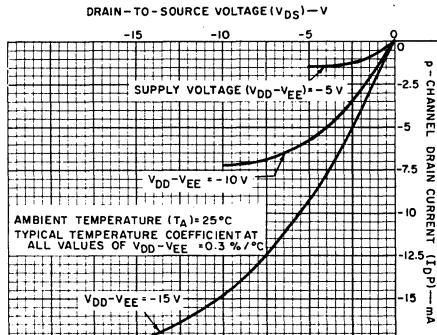


Fig.14 – Minimum p-channel drain characteristics

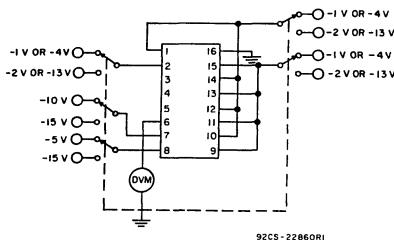


Fig.15 – Noise-immunity test circuit for CD4054A.

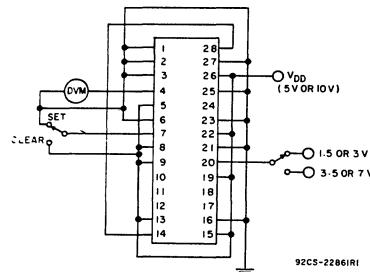


Fig.16 – Noise-immunity test circuit for CD4055A.

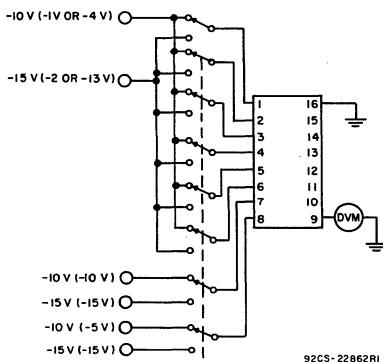


Fig.17 – Noise-immunity test circuit for CD4056A.

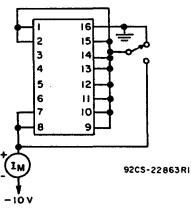


Fig.18 – Quiescent-device-current test circuit for CD4054A.

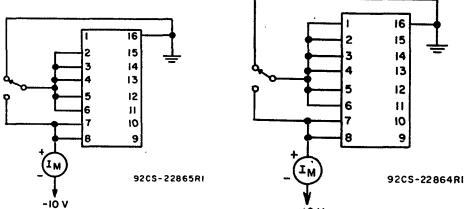


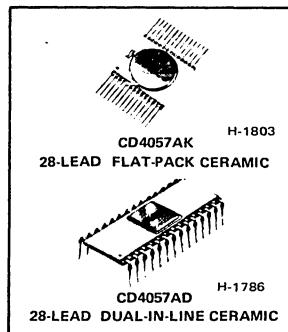
Fig.19 – Quiescent-device-current test circuit for CD4054A.

Fig.20 – Quiescent-device-current test circuit for CD4056A.



# Digital Integrated Circuits

Monolithic Silicon  
**CD4057AD**  
**CD4057AK**  
**CD4057AH**



## COS/MOS LSI 4-Bit Arithmetic Logic Unit

### Applications:

- Parallel Arithmetic Units
- Process Controllers
- Remote Data Sets
- Graphic Display Terminals

### Features:

- LSI Complexity on a Single Chip
- 16-Instruction Capability
  - Add, Subtract, Count
  - AND, OR, Exclusive-OR
  - Right, Left, or Cyclic Shifts
- Bidirectional Data Busses
- Instruction Decoding on Chip
- Fully Static Operation
- Single-Phase Clocking

RCA-CD4057A is a low-power arithmetic logic unit (ALU) designed for use in LSI computers. An arithmetic system of virtually any size can be constructed by wiring together a number of CD4057A ALU's. The CD4057A provides 4-bit arithmetic operations, time sharing of data terminals, and full functional decoding for all control lines. The distributed control system of this device provides great flexibility in system designs by allowing hard-wired connection of N units in  $4^N$  unique combinations. Four control lines provide 16 instructions which include Addition, Subtraction, Bidirectional and Cycle Shifts, Up-Down Counting, AND, OR, and Exclusive-OR logic operations.

- Easily Expandable to 8, 12, 16, . . . Bit Operation
- Conditional-Operation Controls on Chip
- Low Quiescent Device Dissipation . . .  $10 \mu\text{W}$  (typ) at  $V_{DD} = 10 \text{ V}$
- Add Time (Data In-To Sum Out) =  $375 \text{ ns}$  (typ) at  $10 \text{ V}$
- All Terminals Protected Against Static Discharge
- High Noise Immunity . . . 45% of  $V_{DD}$  (typ) Over Full Temperature Range
- Operation from Single Positive or Negative Power Supply . . .  $3 \text{ V}$  to  $15 \text{ V}$
- Full Military Temperature Range . . .  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

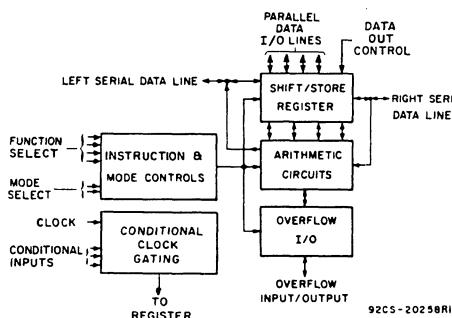


Fig. 1 – Block diagram – CD4057A.

PARALLEL DATA I	1	28	Ro 2
PARALLEL DATA 4	2	27	PARALLEL DATA 3
PARALLEL DATA 2	3	26	*V <sub>DD</sub>
NEGATIVE INDICATOR	4	25	*V <sub>SS</sub>
ZI INPUT	5	24	ZERO INDICATOR
INPUT c	6	23	"DATA OUT" CONTROL
INPUT d	7	CD4057A (TOP VIEW)	22 INPUT a
CONDITIONAL INPUT A	8		21 INPUT b
CONDITIONAL INPUT C	9		20 CLOCK
RIGHT SERIAL DATA LINE	10		19 CONDITIONAL INPUT B
BYPASS	11		18 LEFT SERIAL DATA LINE
NC	12		17 OVERFLOW INDICATOR
MODE-CONTROL INPUT LINE Ci	13		16 OVERFLOW I/O
Ro I	14		15 MODE-CONTROL INPUT LINE C2

\* NOTE: NON-STANDARD TERMINAL LOCATIONS FOR V<sub>SS</sub> AND V<sub>DD</sub>. MOST OTHER COS/MOS TYPES USE CORNER TERMINALS FOR POWER-SUPPLY CONNECTIONS

92CS-20253

Fig. 2 – Terminal assignments.

Two mode control lines allow the CD4057A to function as any 4-bit section of a larger arithmetic unit by controlling the bidirectional serial transfer of data to adjacent arithmetic arrays. By means of three "Conditional Control" lines Overflow, All Zeros, and Negative State conditions may be detected and used to establish a conditional operation. Predetermined operation of the CD4057A on a conditional basis allows greater ALU flexibility. Although especially applicable as a parallel arithmetic unit, the CD4057A also finds use in virtually any application requiring one or more of its 16 basic instructions. The CD4057A is supplied in a hermetically sealed 28-lead dual-in-line ceramic package (CD4057AD), in a flat-pack (CD4057AK), and in chip form (CD4057AH).

**MAXIMUM RATINGS, Absolute Maximum Values:**

STORAGE-TEMPERATURE RANGE .....	-65 to +150 °C
OPERATING-TEMPERATURE RANGE .....	-55 to +125 °C
DISSIPATION PER PACKAGE .....	200 mW
DC SUPPLY-VOLTAGE RANGE ( $V_{DD}$ - $V_{SS}$ ) .....	-0.5 to +15 V
ALL INPUTS .....	$V_{SS} \leq V_I \leq V_{DD}$
Lead Temperature (During soldering)	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm)	
from case for 10 seconds max. ....	265 °C

**MINIMUM RECOMMENDED**

DC SUPPLY VOLTAGE ( $V_{DD}$ - $V_{SS}$ ) .....	3 V
---	-----

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs .....  $V_{SS} \leq V_I \leq V_{DD}$ )  
(Recommended DC Supply Voltage ( $V_{DD}$  -  $V_{SS}$ ) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS						UNITS	
		$V_O$ Volts	$V_{DD}$ Volts	-55°C			25°C			UNITS	
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	$I_L$	5	—	—	3.7	—	0.5	5	—	—	μA
		10	—	—	7.5	—	1	10	—	—	300
Quiescent Device Dissipation/Package	$P_D$	5	—	—	18.5	—	2.5	2.5	—	—	750
		10	—	—	75.0	—	10	100	—	—	3000
Output Voltage: Low-Level	$V_{OL}$	5	—	—	0.01	—	—	0.01	—	—	0.05
		10	—	—	0.01	—	—	0.01	—	—	0.05
High Level	$V_{OH}$	5	4.99	—	—	4.99	5	—	4.95	—	—
		10	9.99	—	—	9.99	10	—	9.95	—	—
Noise Immunity (All Inputs)	$V_{NIL}$	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—
		1	10	3	—	—	3	4.5	—	2.9	—
For Definition See Appendix	$V_{NIH}$	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—
		9	10	2.9	—	—	3	4.5	—	3	—
Output Drive Current:											
Zero Indicator n-channel	$I_{DN}$	0.5	5	0.11	—	—	0.09	0.16	—	0.06	—
		0.5	10	0.12	—	—	0.10	0.16	—	0.07	—
p-channel	$I_{DP}$	3	5	0.04	—	—	0.03	0.06	—	0.02	—
		7	10	0.08	—	—	0.07	0.13	—	0.05	—
Negative Indicator n-channel	$I_{DN}$	0.5	5	0.11	—	—	0.09	0.30	—	0.06	—
		0.5	10	0.12	—	—	0.10	0.40	—	0.07	—
p-channel	$I_{DP}$	4.5	5	0.07	—	—	0.06	0.19	—	0.04	—
		9.5	10	0.12	—	—	0.10	0.30	—	0.07	—
Overflow Indicator n-channel	$I_{DN}$	0.5	5	0.25	—	—	0.20	0.50	—	0.14	—
		0.5	10	0.37	—	—	0.30	0.90	—	0.21	—
p-channel	$I_{DP}$	4.5	5	0.08	—	—	0.07	0.21	—	0.05	—
		9.5	10	0.12	—	—	0.10	0.38	—	0.07	—
All Other Outputs n-channel	$I_{DN}$	0.5	5	0.11	—	—	0.09	0.10	—	0.06	—
		0.5	10	0.06	—	—	0.05	0.12	—	0.03	—
p-channel	$I_{DP}$	4.5	5	0.02	—	—	0.02	0.05	—	0.01	—
		9.5	10	0.06	—	—	0.05	0.08	—	0.03	—

DYNAMIC ELECTRICAL CHARACTERISTICS, at  $T_A = 25^\circ C$  and  $C_L = 15 \mu F$ Typical Temperature Coefficient at all values of  $V_{DD} = 0.3\%/\text{ }^\circ C$ 

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS	CHARAC-TERISTIC CURVES & TEST CIRCUITS		
			$V_{DD}$ Volts	CD4057AD, CD4057AK					
				Min.	Tvp.	Max.			
Propagation Delay Time:	tPLH, tPHL		5	—	1430	3900	ns	10 a	
			10	—	375	720		10 b	
			5	—	915	2550		10 a	
			10	—	310	840		10 b	
			5	—	950	2580			
			10	—	265	720			
			5	—	485	1320			
			10	—	175	480			
ZI Input -to- ZI Output	tPLH		5	—	1980	5400			
			10	—	750	2040			
	tPHL		5	—	265	720			
			10	—	110	300			
Transition Time:	tTLH		5	—	3700	10350	ns	12	
			10	—	1650	4500			
	tTHL		5	—	420	1140			
			10	—	220	600			
	tTLH, tTHL		5	—	300	825			
			10	—	165	450			
			5	—	1000	2775			
			10	—	475	1275			
			5	—	400	1200	ns	13	
Minimum Clock Pulse Width	tWL, tWH		10	—	125	375			
Clock Rise and Fall Time	t <sub>r</sub> CL, t <sub>f</sub> CL		5	—	—	15	μs	13	
			10	—	—	15			
Set Up Time:	tSLH, tSHL		5	—	20	40	ns	14	
			10	—	10	20			
			5	—	1675	4590	ns	14	
			10	—	485	1320			
Data Hold Time	t <sub>Dh</sub>		5	—	20	40	ns	15	
Maximum Clock Frequency:	f <sub>CL</sub>		10	—	10	20			
Count Mode			5	0.13	0.36	—	MHz	11	
Shift Mode	f <sub>CL</sub>		10	0.46	1.35	—			
			5	0.33	0.90	—			
			10	1.4	3.8	—			
Input Capacitance	C <sub>I</sub>	ANY INPUT	—	5	—	pF			

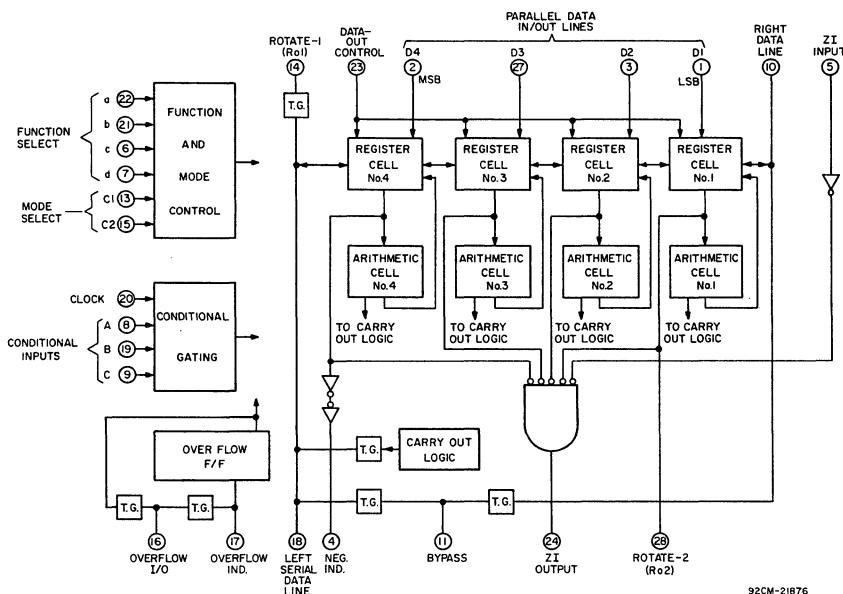


Fig. 3 - Simplified logic diagram.

## LOGIC DESCRIPTION

### OPERATIONAL MODES

The CD4057A arithmetic logic unit operates in one of four possible modes. These modes control the transfer of information, either serial data or arithmetic operation carries, to and from the serial-data lines. Fig. 5 shows the manner in which the four modes control the data on the serial-data lines.

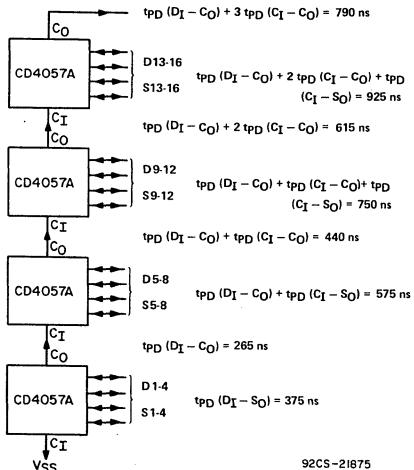
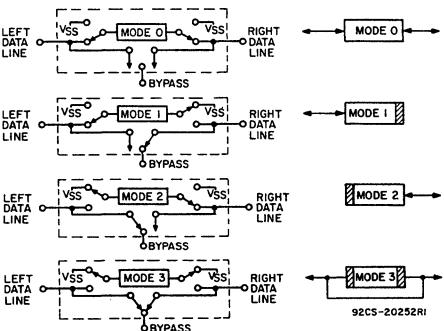
Fig. 4 - Typical speed characteristics of a 16-bit ALU at  $V_{DD} = 10 \text{ V}$ .

Fig. 5 - Schematic of "Mode" concept.

In MODE 0, data can enter or leave from either the left or the right serial-data line.

In MODE 1, data can enter or leave only on the left serial-data line;

In MODE 2, data can enter or leave only on the right serial-data line.

In MODE 3, serial data can neither enter nor leave the register, regardless of the nature of the operation. Furthermore, the register is by-passed electrically, i.e., there is an electrical bidirectional path between the right and left serial data terminals.

The two input lines labeled C1 and C2 in the terminal assignment diagram define one of four possible modes shown in Table I.

Through the use of mode control, individual arithmetic arrays can be cascaded to form one large processor or many processors of various lengths.

TABLE I – MODE DEFINITION

C2	C1	MODE
0	0	0
0	1	1
1	0	2
1	1	3

Examples of how one "hard-wired" combination of three ALU's can form (a) a 12-bit parallel processor, (b) one 8-bit and one 4-bit parallel processor, or (c) three 4-bit parallel processors, merely by changes in the modes of each ALU are shown in Fig. 6.

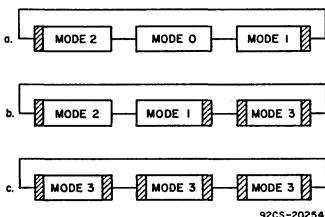


Fig. 6 – "Mode" connections for parallel processor:  
 (a) 12-bit unit,  
 (b) one 8-bit and one 4-bit unit  
 (c) three 4-bit units.

Data-flow interruptions are shown by shaded areas. With these three ALU's and the four available modes, 61 more system combinations can be formed. If 4 ALU's are used,  $4^4$  combinations (256) are possible. Fig. 7 shows a diagram of 4 CD4057A's interconnected to form a 16-bit parallel processor.

NOTE: The BYPASS terminal of the "most significant" CD4057A is connected to the bypass terminal of the "least significant" CD4057A. The bypass terminals on all other CD4057A's are left floating. This interconnection is performed whenever more than one CD4057A are used to form a processor.

## INSTRUCTION REPERTOIRE

Four encoded lines are used to represent 16 instructions. Encoded instructions are as follows:

a b c d

0 0 0 0	NO-OP (Operational Inhibit)
0 0 0 1	AND
0 0 1 0	Count down
0 0 1 1	Count up
0 1 0 0	Subtract Stored number from zero (SMZ)
0 1 0 1	Subtract from parallel data lines (SM) (stored number from parallel data lines)
0 1 1 0	Add (AD)
0 1 1 1	Subtract (SUB) (Parallel data lines from stored number)
1 0 0 0	Set to all ones (SET)
1 0 0 1	Clear to all zeroes (CLEAR)
1 0 1 0	Exclusive-OR
1 0 1 1	OR
1 1 0 0	Input Data (From parallel data lines)
1 1 0 1	Left shift
1 1 1 0	Right shift
1 1 1 1	Rotate (cycle) right

All instructions are executed on the positive edge of the clock.

## PARALLEL COMMANDS

- a. CLEAR — sets register to zero.
- b. SET — sets register to all ones.
- c. OR — processes contents of register with value on parallel-data lines in a logical OR function.
- d. AND — processes contents of register with value on parallel-data lines in a logical AND function.
- e. Exclusive-OR — processes contents of register with data on parallel-data lines in a logical Exclusive-OR function.
- f. IN — loads data on parallel-data lines into register.
- g. DATA OUT CONTROL — unloads contents of register and overflow flip-flop onto parallel data lines and overflow I/O independent of all other controls.
- h. SUB:

In Mode 0, adds to the contents of the register the one's complement of the data on the parallel-data lines. Carries can enter on the right serial data line and can leave on the left serial data line. The overflow indicator does not change state.

In Mode 1, adds to the contents of the register the two's complement of the data on the parallel-data lines. Generated carries can leave on the left serial line. The CARRY IN is set to zero. The overflow indicator does not change state.

In Mode 2, same as Mode 0, except carries cannot leave on the right serial-data line. The absence or presence of an overflow is registered.

In Mode 3, same as Mode 1, except carries cannot leave on the left serial-data line. The absence or presence of an overflow is registered.

#### i. COUNT UP:

In Mode 0, adds to the contents of the register the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters the parallel-data lines.

In Mode 1, internally adds a one to the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.

In Mode 2, adds to the contents of the register the data on the right serial-data line. No data enters or leaves the left serial-data line.

In Mode 3, internally adds a one to the contents of the register. No data enters or leaves the register on any serial-data or parallel-data line.

In all modes, with the DATA OUT control "high" the count is presented on the parallel data lines (D1-D4).

#### j. COUNT DOWN:

In Mode 0, subtracts a one (2's complement form) from the contents of the register and adds to this result the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters on the parallel-data lines.

In Mode 1, internally subtracts a one from the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.

In Mode 2, subtracts a one from the contents of the register and adds to this result the data on the right serial-data line. No data enters or leaves on the left serial-data line.

In Mode 3, internally subtracts a one from the contents of the register. No data enters or leaves on the serial-data lines.

In all modes, with the DATA OUT control "high" the count is presented on the parallel data lines (D1-D4).

#### k. ADD (AD):

In Mode 0, adds the contents of the register to the data on the parallel-data lines and the right serial-data line. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, adds the contents of the register to the data on the parallel-data lines and allows any resulting carry to leave on the left serial-data line. The right serial-data line is open-circuited. The overflow indicator does not change state. The CARRY-IN is set to zero.

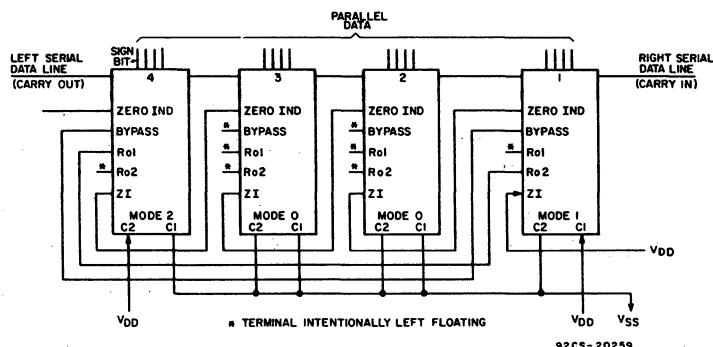


Fig.7 — Connection for 16-bit Arithmetic Logic Unit.

In Mode 2, adds the contents of the register to the data on the parallel data lines and the right serial data line. Any overflow sets the overflow indicator. The left serial data line is open-circuited. The absence or presence of an overflow is registered.

In Mode 3, adds contents of the register to the data on the parallel-data lines. Any resulting carry sets the overflow indicator. The two serial-data lines are open circuited. The absence or presence of an overflow is registered. The CARRY-IN is set to zero.

- I. SM— same operation as AD except the contents of the register are two's complemented during addition in Mode 1 and Mode 3. In Mode 0 or Mode 2, the contents of the register are one's complemented and added to the data on the right serial-data line and the parallel-data lines. Overflows occurring in Mode 1 or Mode 0 do not alter the overflow indicator. The presence or absence of overflows is registered on the overflow indicator in Mode 2 or Mode 3.

#### m. SMZ:

In Mode 0, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, two's complements the contents of the register and permits any carry to leave on the left serial-data line. No data can enter the right serial-data line. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Carries cannot leave the left serial data line. The absence or presence of an overflow alters the overflow indicator.

In Mode 3, two's complements the contents of the register. Serial data can neither enter the right serial-data line nor leave the left serial-data line. The overflow indicator is at zero. The CARRY-IN is set to zero.

- n. NO-OP — no operation takes place. The clock input is inhibited and the state of all registers and indicators remains unchanged.

### SERIAL-SHIFT OPERATIONS

- a. ROTATE (cycle) RIGHT — This operation is internal. The contents of the register shift to the right, cyclic fashion with the leftmost stage accepting data from the rightmost stage regardless of the mode. Data can leave the register serially on the right data line only while the

register is in Mode 2 or Mode 0. Data can enter the left data line serially while the register is in Mode 1 or Mode 0. The Ro1 terminal of the "Most Significant" CD4057A must be connected to the Ro2 terminal of the "Least Significant" CD4057A. All other Ro1 and Ro2 terminals must be left floating. When only one CD4057A is used, Ro1 must be connected to Ro2.

- b. RIGHT SHIFT - The contents of the register shift to the right and serial operations are as follows:

In Mode 0, data can enter serially on the left data line, shift through the register, and leave on the right data line.

In Mode 1, data can enter serially on the left data line. The right data line effectively is open-circuited.

In Mode 2, data can leave serially on the right data line. The left data line effectively is open-circuited. Vacant spaces are filled with zeros.

In Mode 3, serial data can neither enter nor leave the register; however, the contents shift to the right and vacated places are filled with zeros.

In all modes, with the DATA OUT control "high" the data is presented on the parallel data lines (D1-D4).

- c. LEFT SHIFT — The contents of the register shift to the left and serial operations are as follows:

In Mode 0, data can enter the right data line, shift through the register, and leave on the left data line.

In Mode 1, data can leave serially on the left data line. The right data line effectively is open-circuited. All vacant positions are filled with zeros.

In Mode 2, data can enter serially on the right data line. The left data line effectively is open-circuited.

In Mode 3, data can neither enter nor leave the register; however, the contents shift to the left, and vacated places are filled with zeros.

In all modes, with the DATA OUT control "high" the data is presented on the parallel data lines (D1-D4).

Because the "DATA OUT" control instruction is independent of the other 16 instructions, care must be taken not to activate this control when data are to be loaded into the processor. This instruction should only be activated when the processor is executing a NO-OP, any SHIFT, SMZ, COUNT UP or DOWN, CLEAR, or SET.

If a data line, serial or parallel, is used as an input and the logic state of that line is not defined (i.e., the line is an open circuit), then the result of any operation using that line is undefined.

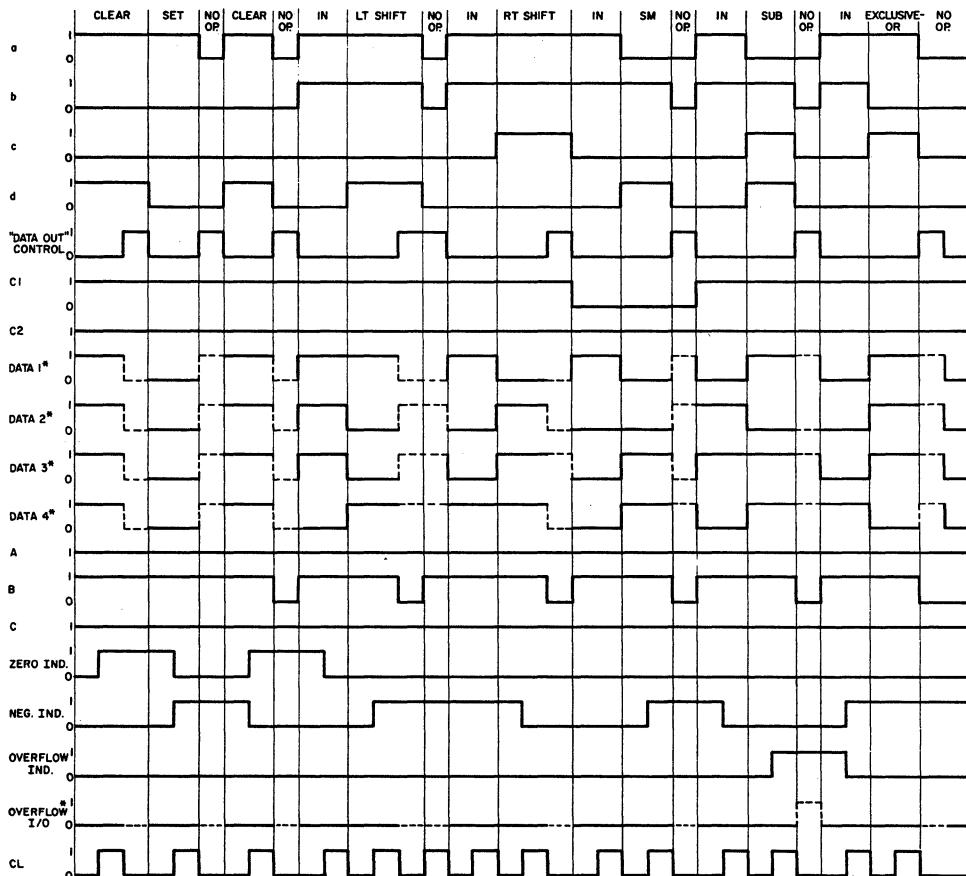
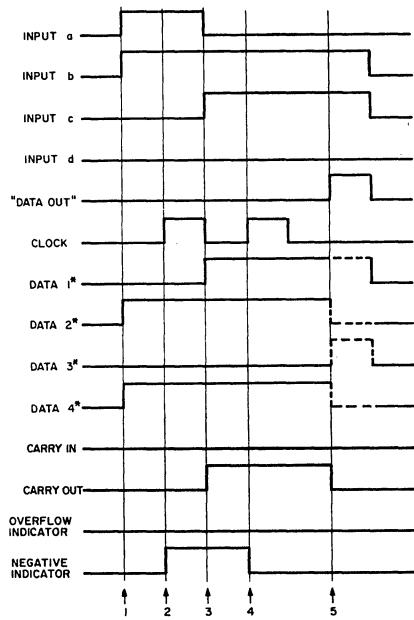


Fig. 8 – Timing Diagram.

## OPERATIONAL SEQUENCE FOR ARITHMETIC ADD CYCLE

1. Apply IN Instruction and Word A on Parallel Data Lines (D1-D4).
2. Apply CLOCK to load Word A into the register.
3. Apply OP CODE Instruction and Word B on Data Lines.
4. Apply CLOCK to load resulting function of A and B into the register.
5. Apply "DATA OUT" control to present result to Parallel Data Lines.

**NOTE:** Transitions of Step 2 and Step 3 may occur almost simultaneously; i.e. separated by only one data-hold time.



\* SOLID LINE REPRESENTS INPUT FROM EXTERIOR SOURCE WHEN "DATA OUT" IS LOW. DASHED LINES REPRESENT OUTPUT WHEN "DATA OUT" IS HIGH

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Fig. 9 – Add cycle waveforms.

## ZERO DETECTION

The condition of "all zeros" is indicated by a "1" on the Zero Indicator terminal of the "Most Significant" CD4057A. As shown in Fig. 7, terminal Z1 of the CD4057A containing the least significant set of bits is connected to  $V_{DD}$ . Zero indication is independent of modes.

## NEGATIVE-NUMBER DETECTION

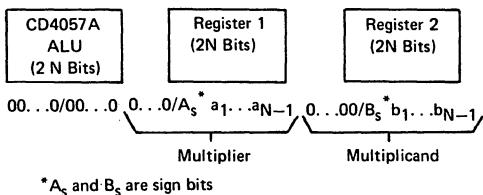
The NEG IND terminal of the CD4057A is connected to the output of the flip-flop that is in the most significant bit position. A "1" on the NEG IND terminal indicates a negative number is in the register. This detection is also independent of modes.

## COMPLEMENTING NUMBERS

1. One's complement of number in ALU register.
  - a) ALU must be in MODE 0 or MODE 2.
  - b) Zero on Rt. Data Line.
  - c) Execute an SMZ instruction.
2. One's complement of number to be loaded into ALU register.
  - a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
  - b) ALU must be in MODE 0 or MODE 2.
  - c) Execute an SUB instruction.
3. Two's complement of number in ALU register.
  - a) ALU must be in MODE 1 or MODE 3.
  - b) Execute an SMZ instruction.
4. Two's complement of number to be loaded into ALU register.
  - a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
  - b) ALU must be in MODE 1 or MODE 3.
  - c) Execute an SUB instruction.

The following algorithms are given as a general guideline to demonstrate some of the capabilities of the CD4057A.

## MULTIPLICATON OF TWO N-BIT NUMBERS



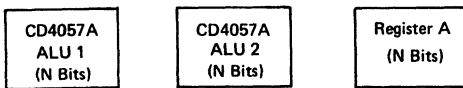
\*  $A_s$  and  $B_s$  are sign bits

### Multiplication Algorithm

1. Clear ALU to Zero
2. Store  $A_s \oplus B_s$  in External Flip-Flop.
3. If  $A_s = 1$ , Complement Register 1.
4. If  $B_s = 1$ , Complement Register 2.
5. Load Register 2 into ALU.
6. Do Shift Left on ALU N Times  
( $N = \text{number of bits}$ ).
7. Do N Times:  
(1)
  - a) If MSB of ALU = 1  
(Negative Indicator = High),  
Then shift ALU left 1 bit;  
add Register 1 to ALU.

- b) If MSB of ALU = 0  
 (Negative Indicator = Low),  
 Then shift ALU left 1 bit.
  - 8. If  $A_s \oplus B_s = 1$ , then Complement ALU.
  - 9. Answer in ALU.

## Division Algorithm



$$\frac{A_s a_1 \dots a_{N-1}}{\text{Dividend}} \quad \frac{a_N \dots a_{2N-1}}{\text{Divisor}} \quad \frac{B_s b_1 \dots b_{N-1}}{\text{Divisor}}$$

1. Store  $A_s \oplus B_s$  in External Flip-Flop.
  2. If  $A_s = 1$ , complement ALU 1 and ALU 2.
  3. If  $B_s = 1$ , complement Register A.
  4. Check for Divisor = 0
    - a) If Divisor = 0; stop, indicates division by 0.
    - b) If Divisor  $\neq 0$ ; continue.
  5. Apply SUB instruction to ALU 1 and Register A to ALU 1 data lines.
    - a) If  $C_0 = 0$  (Dividend < Divisor), Stop, indicates overflow.
    - b) If  $C_0 = 1$  (Dividend  $\geq$  Divisor), Continue.
  6. Put a zero on RT. data line of ALU 2 and shift ALU 1 & ALU 2 left 1 bit.
  7. Do "N" times.
 

Apply SUB instruction to ALU 1 and Register A to ALU 1 data lines.

    - a) If  $C_0 = 1$ , then clock ALU 1, and put a 1 on right data line of ALU 2.
    - b) If  $C_0 = 0$ , then no clock, and put a 0 on right data line of ALU 2.
  8. If sign Flip Flop = 1, complement ALU 2.
  9. Answer in ALU 2.

**TABLE II – CONDITIONAL-INPUTS TRUTH TABLE**

A	B	C	OPERATION PERMITTED
0	X	X	Yes
1	0	0	Yes
1	0	1	No
1	1	0	No
1	1	1	Yes

X = don't care

Two examples of how the conditional operation can be used are as follows:

- ### 1) For the Multiplication Algorithm

$A = 1$ , for step 7 (1)

**A = 0, for step 7 (2)**

B =

**C = negative Indicator**

- ## 2) For the Division Algorithm

$A = 1$ , for step 7 (1)

$A = 0$ , for step 7 (2)

B =

$C = C_0$  (left data line)

#### **OVERFLOW DETECTION**

The CD4057A is capable of detecting and indicating the presence or absence of an arithmetic two's-complement overflow. A two's-complement overflow is defined as having occurred if the signs of the two initial words are the same and the sign of the result is different while performing a carry-generating instruction.

For example: (+) 0.110

Overflows can be detected and indicated only during operation in Mode 2 or Mode 3 and can occur for only four instructions (AD, SMZ, SM, and SUB). If an overflow is detected and stored in the overflow flip-flop, any one of the five instructions AD, SMZ, SM, SUB, or IN can change the overflow indicator.

When any of the three subtraction instructions is used, the sign bit of the data being subtracted is complemented and this value is used as one of the two initial signs to detect overflows. If an overflow has occurred, the final sign of the sum or difference is one's complemented and stored in the most-significant-bit position of the register.

The overflow flip-flop is updated at the same time the new result is stored in the CD4057A. Whenever data on the parallel-data lines are loaded into the CD4057A, whatever is on the Overflow I/O line is loaded into the overflow flip-flop. Also, whenever data are dumped on the parallel data lines from the CD4057A, the contents of the overflow flip-flop are dumped on the Overflow I/O line. Thus overflows may be stored elsewhere and then fed into the CD4057A at another time.

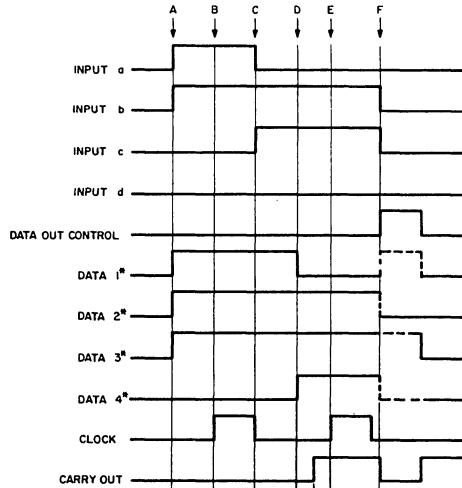
## CONDITIONAL OPERATION

Inhibition of the clock pulse can be accomplished with a programmed NO-OP instruction or through conditional inputs terminals A, B, and C. In a system of many CD4057A's, each CD4057A can be made to automatically control its own operation or the operation of any other CD4057A in the system in conjunction with the Overflow, Zero, or Negative (Number) indicators. Table II, the conditional-inputs truth table, defines the interactions among A, B, and C.

## OPERATIONAL SEQUENCE AND WAVEFORMS FOR PROPAGATION-DELAY MEASUREMENTS

### 1. DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT

- Apply Word A and IN instruction
- Apply Clock to load word A into register
- Apply AD instruction
- Apply Word B (data in)
- Apply Clock to load result (sum out)
- Apply DATA OUT CONTROL to look at result



- ① DATA IN
- ② CARRY OUT
- ③ SUM OUT
- ④ → ② DATA IN TO CARRY OUT
- ④ → ③ DATA IN TO SUM OUT

\* SOLID LINE REPRESENTS INPUT FROM EXTERIOR SOURCE WHEN "DATA OUT" IS LOW. DASHED LINES REPRESENT OUTPUT WHEN "DATA OUT" IS HIGH

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Fig. 10(a) – DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT.

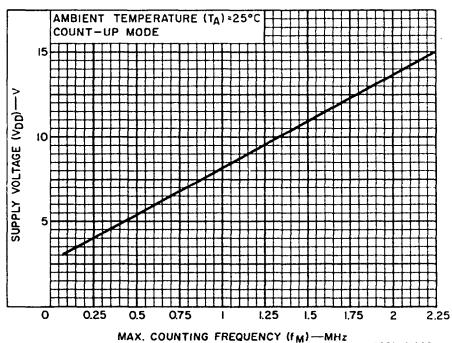
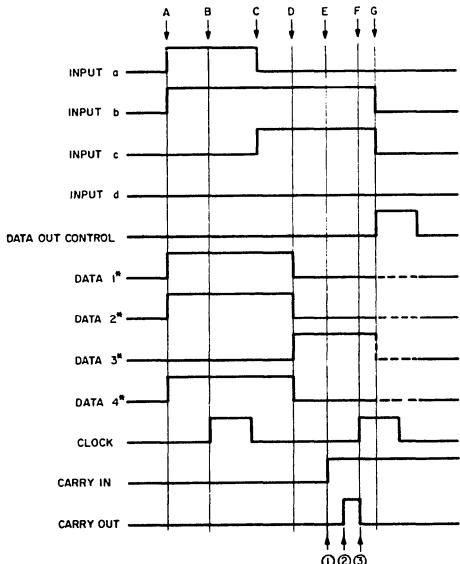


Fig. 11 – Max. counting frequency vs. supply voltage for a typical CD4057A.

### 2. CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT

- Apply Word A and IN instruction
- Apply Clock to load word A into register
- Apply AD instruction
- Apply Word B
- Apply CARRY IN (carry in)
- Apply Clock to load result (sum out)
- Apply DATA OUT CONTROL to look at result



- ① CARRY IN
- ② CARRY OUT
- ③ SUM OUT
- ④ → ② CARRY IN TO CARRY OUT
- ④ → ③ CARRY IN TO SUM OUT

\* SOLID LINE REPRESENTS INPUT FROM EXTERIOR SOURCE WHEN "DATA OUT" IS LOW. DASHED LINES REPRESENT OUTPUT WHEN "DATA OUT" IS HIGH

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Fig. 10(b) – CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT.

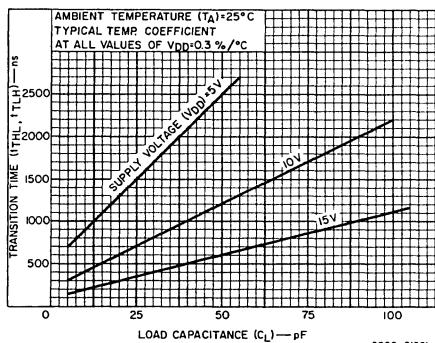


Fig. 12 – Transition time vs. load capacitance for Data Outputs (D1-D4).

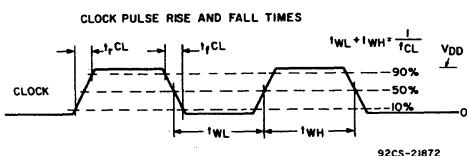


Fig. 13 – Clock Pulse Rise and Fall Times.

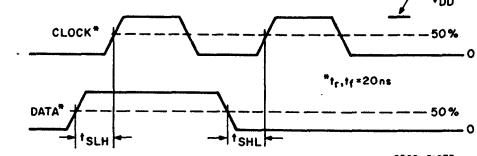


Fig. 14 – Data setup time.

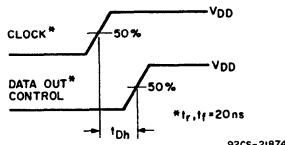


Fig. 15 – Data hold time.

## TEST CIRCUITS

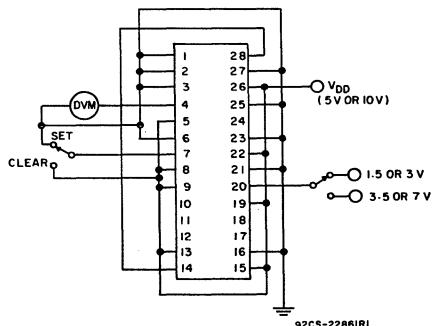


Fig. 16 – Noise immunity for "SET" instruction (see Timing Diagram)

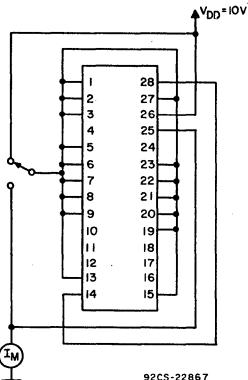


Fig. 17 – Quiescent device current.

## TYPICAL APPLICATION

The CD4057A has been designed for use as a parallel processor in flexible, programmable, easily expandable, special or general purpose computers, where minimization of external connections and data busing are primary design goals.

The block diagram of Fig. 18 is an example of a computer that processes 8 bits in parallel.

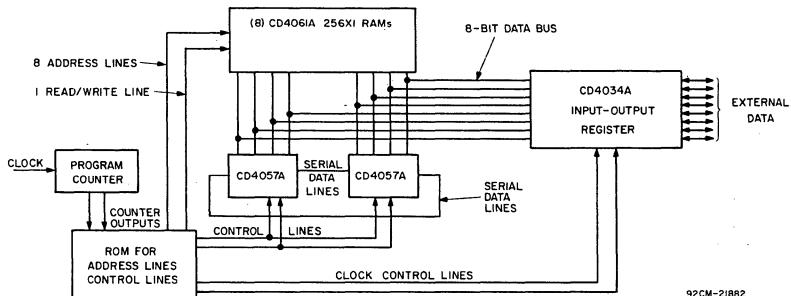
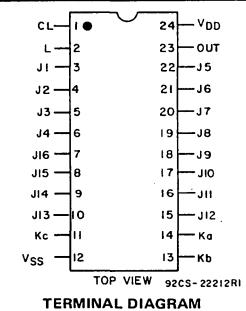


Fig. 18 – Example of Computer Organization Using CD4057A.

**Preliminary Data**



RCA Preliminary CD4059AD<sup>®</sup> is a divide-by-N down counter that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one-clock-pulse wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down counter is preset by means of 16 jam inputs.

## COS/MOS Programmable Divide-by-"N" Counter

### Features:

- Synchronous programmable  $\div N$  counter:  
 $N = 3$  to  $9999$  or  $15,999$
- 4 BCD decades of counting on one chip
- Low power consumption:  $30 \mu\text{W}$  (typ.) at  $V_{DD} = 10 \text{ V}$
- Presettable down counters
- Fully static operation
- Mode select control of initial decade counting function ( $\div 10, 8, 5, 4, 2$ )
- $T^2L$  drive capability
- Master preset initialization
- Latchable  $\div N$  output

### Applications:

- Communication set frequency synthesizers  
VHF, UHF, FM, AM, etc.
- Fixed or programmable frequency division
- "Time out" timer for consumer application industrial controls

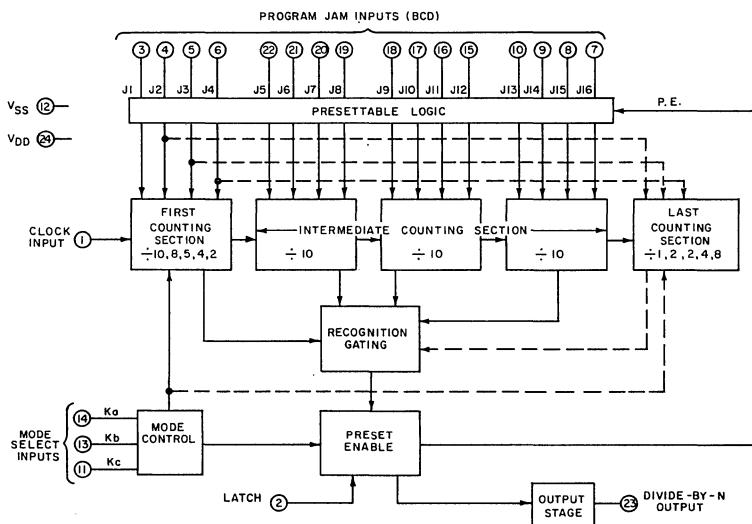


Fig. 1—Functional block diagram.

92CM-22213

The three mode select inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the  $\div 2$  mode only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If  $\div 10$  is desired for the first section, set Ka = 1, Kb = 1, and Kc = 0; jam inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade ( $\div 10$ ) counters presettable by means of jam inputs J5 through J16.

The mode select inputs permit frequency synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. In addition, these inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, 100, multiplied by the number of the  $\div N$  mode. For example, in the  $\div 8$  mode, the number from which counting down begins can be preset to:

$$\begin{array}{rl} \text{3rd decade:} & 1500 \\ \text{2nd decade:} & 150 \\ \text{1st decade:} & 15 \\ \text{Last counting section} & \underline{1000} \\ & 2665 \times 8 = 21,320 \end{array}$$

plus the first counting section can be preset to 7

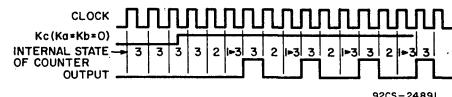
Therefore 21,327 is the

maximum possible count in the  $\div 8$  mode.

The highest count of the various modes is shown in the column entitled: "extended" counter range, max., of Table I.

Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected. Whenever the master preset mode is used, control signals Kb = 0 and Kc = 0 must be applied for at least 3 full clock pulses. A "1" on the latch input will cause the counter output to remain "high" until the latch input returns to "0". If the latch input is "0" the output pulse will remain high for only 1 cycle of the clock-input signal.

After the master preset mode inputs have been changed to one of the  $\div$  modes, the next positive-going clock transition changes an internal flip-flop so that the countdown begins at the second positive-going clock transition. Thus, after an MP mode, there is always one extra count before the output goes high. See illustration below for total count of 3. ( $\div 8$  mode)



As illustrated in the sample applications, this device is particularly advantageous in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.) where programmable divide-by-"N" counters are an integral part of the synthesizer phase-locked-loop subsystem. Note that the Preliminary CD4059A can also be used to perform the synthesizer "Fixed Divide by P" counting function. For additional information, see RCA-ICAN-6716 "Low Power Digital Frequency Synthesizers Utilizing COS/MOS IC's." The Preliminary CD4059A can also be used in general-purpose counters for instrumentation functions such as totalizers, production counters, and "time out" timers.

The Preliminary CD4059A is available in 24-lead ceramic dual-in-line packages.

TABLE I

MODE	MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			DESIGN COUNTER RANGE		EXTENDED COUNTER RANGE	
	Ka	Kb	Kc	Divides by:	Can be preset to a maximum of:	Jam inputs used:	Divides by:	Can be preset to a maximum of:	Jam inputs used:	Min.	Max.	Max.	
First counting section divides by:													
2	1	1	1	2	1	J1	8	7	J2,J3,J4	3	15,999	17,331	
4	0	1	1	4	3	J1,J2	4	3	J3,J4	3	15,999	18,663	
5	1	0	1	5	4	J1,J2,J3	2	1	J4	3	9,999	13,329	
8	0	0	1	8	7	J1,J2,J3	2	1	J4	3	15,999	21,327	
10	1	1	0	10	9	J1,J2,J3,J4	1	0	—	3	9,999	16,659	
Master Preset (MP)	X	0	0	MP			MP			—	—	—	

X = Don't Care

**MAXIMUM RATINGS, Absolute-Maximum Values:**

Storage Temperature Range . . . . .	-65 to +150 °C		
Operating Temperature Range . . . . .	-55 to +125 °C		
DC Supply Voltage Range (V <sub>DD</sub> - V <sub>SS</sub> ) . . . . .	15 V		
Device Dissipation (Per Pkg.) . . . . .	200	mW	
All Inputs . . . . .	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>		
Recommended DC Supply Voltage (V <sub>DD</sub> - V <sub>SS</sub> ) . . . . .	3 to 15	V	
Lead Temperature (During soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . .	265	°C	

**STATIC ELECTRICAL CHARACTERISTICS AT T<sub>A</sub> = 25°C**Typical Temperature Coefficient at all values of V<sub>DD</sub> = -0.3%/°C

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		TYPICAL VALUES			UNITS
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	Min.	Typ.	Max.	
		5	—	—	1	—	
Quiescent Device Current	I <sub>L</sub>	10	—	—	3	—	μA
		5	—	—	5	—	
Quiescent Device Dissipation/Package	P <sub>D</sub>	10	—	—	30	—	μW
		0.4	4.5	1.3	2.6	—	
Output Drive Current: n-Channel (Sink)	I <sub>DN</sub>	0.5	10	—	12	—	mA
		4.1	4.5	—	-0.4	—	
p-Channel (Source)	I <sub>DP</sub>	9.5	10	—	-1.5	—	mA

**DYNAMIC ELECTRICAL CHARACTERISTICS AT T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF**Typical Temperature Coefficient for all values of V<sub>DD</sub> = 0.3%/°C

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
		V <sub>DD</sub> Volts	Min.	Typ.	Max.	—	
Propagation Delay Time	t <sub>PHL</sub> , t <sub>PLH</sub>	5	—	280	—	—	ns
		10	—	140	—	—	
Transition Time	t <sub>THL</sub>	5	—	35	—	—	ns
		10	—	25	—	—	
t <sub>T LH</sub>		5	—	90	—	—	ns
		10	—	50	—	—	
Clock Rise or Fall Time	t <sub>C L</sub> , t <sub>f CL</sub>	5	—	—	15	—	μs
		10	—	—	5	—	
Maximum Clock Frequency: All ÷ Modes	f <sub>C L</sub>	5	—	2.5	—	—	MHz
		10	—	5	—	—	
Input Capacitance	C <sub>I</sub>	Any input	—	5	—	—	pF

**"HOW TO PRESET PRELIMINARY CD4059AD TO DESIRED N"**

The value N is determined as follows:

$$N = [\text{MODE}^*] [1000 \times \text{Decade 5 Preset} + 100X \text{Decade 4 Preset} + 10X \text{Decade 3 Preset} + 1X \text{Decade 2 Preset}] + \text{Decade 1}$$
 (1)

Preset

\* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}}$$
 (2)

Examples:

A) N = 8479, Mode = 5

$$\begin{array}{r} 1695 + 4 \\ \hline 5 \quad | \quad 8479 \\ \text{Mode} \qquad \qquad \qquad N \end{array}$$

Preset Values

MODE SELECT = 5

PROGRAM JAM INPUTS (BCD)

			4				1				5				9				6			
Ka	Kb	Kc	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16				
1	0	1	0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0				

To verify the results use equation 1 :

$$N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4$$

$$N = 8479$$

B) N = 12382, Mode = 8

$$\begin{array}{r} 1547 + 6 \\ \hline 8 \quad | \quad 12382 \end{array}$$

MODE SELECT = 8

PROGRAM JAM INPUTS

			6				1				7				4				5			
Ka	Kb	Kc	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16				
0	0	1	0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0				

To verify:

$$N = 8 (1000 X 1 + 100 X 5 + 10 X 4 + 1 X 7) + 6$$

$$N = 12382$$

C) N = 8479, Mode = 10

$$\begin{array}{r} 0847 + 9 \\ \hline 10 \quad | \quad 8479 \end{array}$$

MODE SELECT = 10

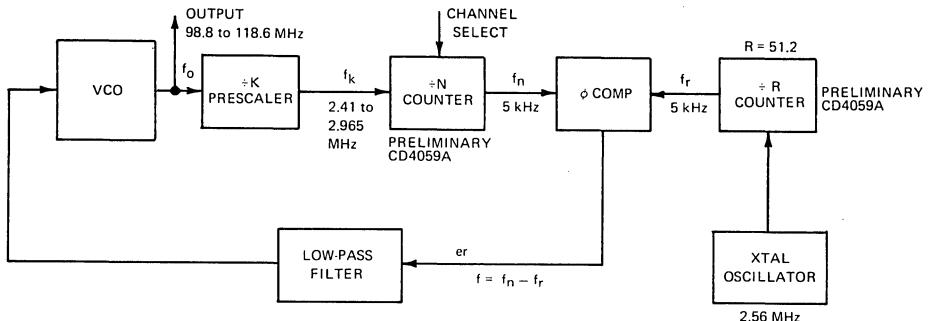
PROGRAM JAM INPUTS

			9				7				4				8			
Ka	Kb	Kc	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	1	0	1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

$$N = 10 (1000 X 0 + 100 X 8 + 10 X 4 + 1 X 7) + 9$$

$$N = 8479$$

**APPLICATIONS****1) DIGITAL PLL FOR FM BAND SYNTHESIZER****Calculating Min & Max "N" Values:**Output Freq. Range ( $f_O$ ) = 98.8 to 118.6 MHzChannel Spacing Freq. ( $f_c$ ) = 200 kHzDivision Factor ( $k$ ) = 40

$$\text{Reference Freq. } (f_r) = \frac{f_c}{k} = \frac{200}{40} \text{ kHz} = 5 \text{ kHz}$$

$$f_k = \frac{f_o}{40} : f_{k\text{Max.}} = \frac{118.6 \text{ MHz}}{40} = 2.965 \text{ MHz}; f_{k\text{Min.}} = \frac{98.8 \text{ MHz}}{40} = 2.47 \text{ MHz}$$

$$\therefore N = \frac{f_o}{f_c}$$

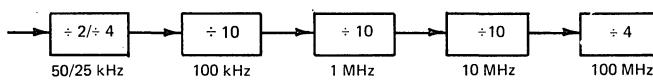
$$N_{\text{Max.}} = \frac{118.6 \text{ MHz}}{200 \text{ kHz}} = 593$$

$$N_{\text{Min.}} = \frac{98.8 \text{ MHz}}{200 \text{ kHz}} = 494$$

$$R = \frac{2.56 \text{ MHz}}{5 \text{ kHz}} = 512$$

**2)  $\div N$  Counter Configuration for UHF – 220 to 400 MHz**

Channel Spacing: 50 kHz or 25 kHz

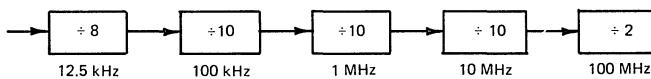


$$N_{\text{Max.}} = \frac{400 \text{ MHz}}{25 \text{ kHz}} = 16,000 \quad N_{\text{Max.}} = \frac{400 \text{ MHz}}{50 \text{ kHz}} = 8,000$$

$$N_{\text{Min.}} = \frac{220 \text{ MHz}}{25 \text{ kHz}} = 8,800 \quad N_{\text{Min.}} = \frac{220 \text{ MHz}}{50 \text{ kHz}} = 4,400$$

**3)  $\div N$  Counter Configuration for VHF – 116 to 160 MHz**

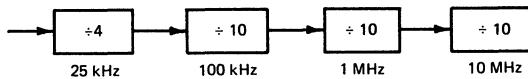
Channel Spacing = 12.5 kHz



$$N_{\text{Max.}} = \frac{160 \text{ MHz}}{12.5 \text{ kHz}} = 12,800 \quad N_{\text{Min.}} = \frac{116 \text{ MHz}}{12.5 \text{ kHz}} = 9,300$$

## 4)÷N Counter Configuration for VHF – 30 to 80 MHz

Channel Spacing: 25 kHz

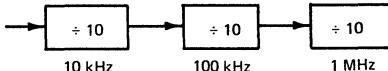


$$N_{\text{Max}} = \frac{80 \text{ MHz}}{25 \text{ kHz}} = 3,200$$

$$N_{\text{Min}} = \frac{30 \text{ MHz}}{25 \text{ kHz}} = 1200$$

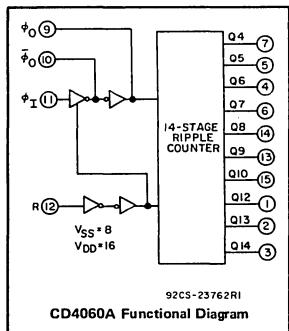
## 5)÷N Counter Configuration for AM – 995 to 2055 kHz

Channel Spacing = 10 kHz



$$N_{\text{Max}} = \frac{2055 \text{ kHz}}{10 \text{ kHz}} = 205$$

$$N_{\text{Min}} = \frac{995 \text{ kHz}}{10 \text{ kHz}} = 99$$



# **COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator**

#### **Features:**

- 4-MHz operating frequency (typ.) at  $V_{DD} - V_{SS} = 10\text{ V}$
  - Common reset
  - Fully static operation
  - 10 buffered outputs available

The RCA-CD4060A consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of  $\phi_1(\phi_0)$ . All inputs and outputs are fully buffered.

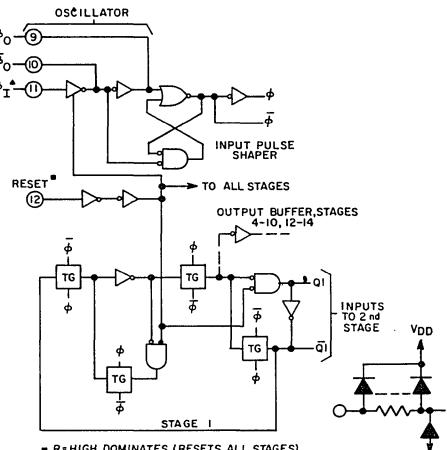
The CD4060A is supplied in 16-lead dual-in-line welded-seal ceramic packages (D), plastic packages (E), ceramic packages (F), flat packs (K), and in chip form (H).

### *Oscillator Features:*

- All active components on chip
  - RC or crystal oscillator configuration

### *Applications:*

- Timers
  - Frequency dividers



**Fig. 1—Logic diagram of CD4060A oscillator, pulse shaper, and 1 of 14 counter stages.**

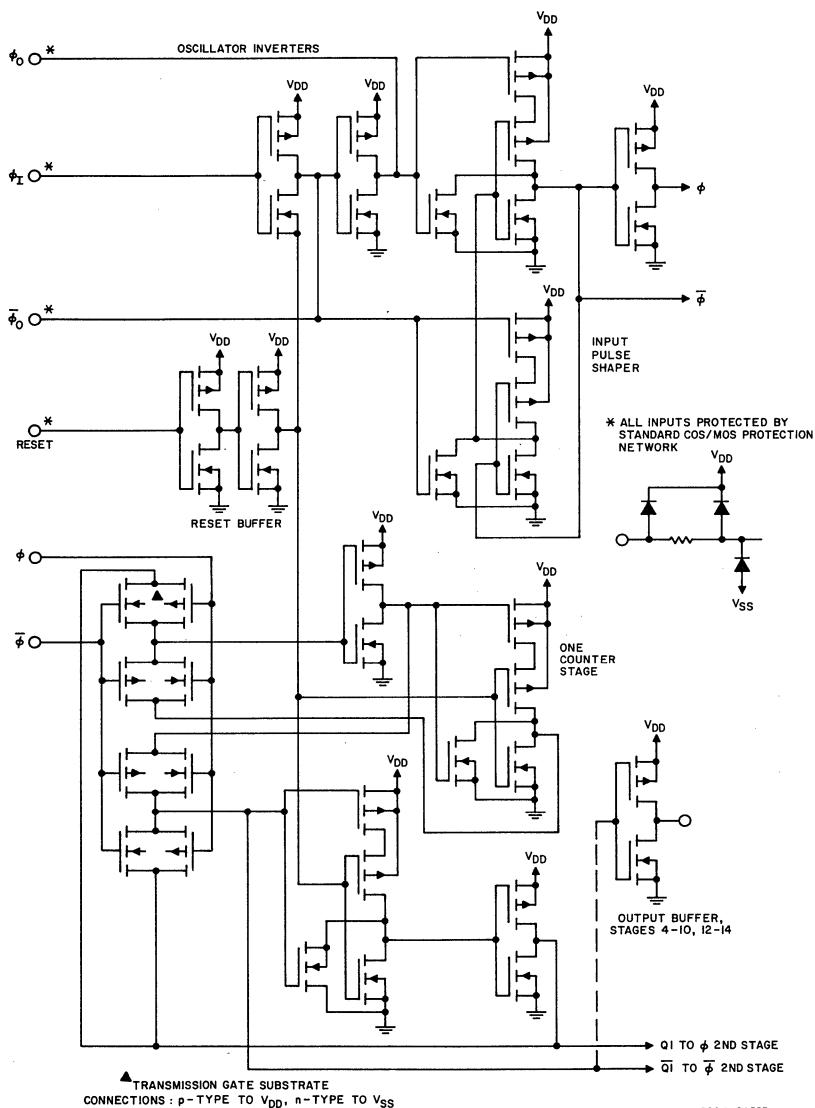


Fig. 2—Schematic diagram of input pulse shapers, reset buffers, and 1 of 14 binary counter stages of the CD4060A.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs .....  $V_{SS} \leq V_i \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4060AD CD4060AF CD4060AK CD4060AH CERAMIC PACKAGE LIMITS										UNITS	FIG. NO.	
				-55°C			25°C			125°C						
		$V_O$ V	$V_{DD}$ V	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	$I_L$		5	—	—	15	—	0.5	15	—	—	900	$\mu A$	16		
			10	—	—	25	—	1	25	—	—	1500				
Quiescent Device Dissipation/Package	$P_D$		5	—	—	75	—	2.5	75	—	—	4500	$\mu W$	—		
			10	—	—	250	—	10	250	—	—	15000				
Output Voltage: Low-Level	$V_{OL}$	Fan Out = 50	5	—	—	0.01	—	0	0.01	—	—	0.05	V	—		
			10	—	—	0.01	—	0	0.01	—	—	0.05				
High-Level	$V_{OH}$	Fan Out = 50	5	4.99	—	—	4.99	5	—	4.95	—	—	V	—		
			10	9.99	—	—	9.99	10	—	9.95	—	—				
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	17,18	
			1	10	3	—	—	3	4.5	—	2.9	—	—			
	$V_{NH}$		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—			
			9	10	2.9	—	—	3	4.5	—	3	—	—			
Output Drive Current: N-Channel (Sink)	$I_{DN}$		0.5	5	0.22	—	—	0.18	0.36	—	0.125	—	—	$mA$	3,4	
			0.5	10	0.44	—	—	0.36	0.75	—	0.25	—	—			
P-Channel (Source)	$I_{DP}$		4.5	5	-0.15	—	—	-0.125	-0.25	—	-0.085	—	—	$mA$	5,6	
			9.5	10	-0.3	—	—	-0.25	-0.5	—	-0.175	—	—			
Input Current	$I_I$	Any Input	—	—	—	—	—	$\pm 10^{-5}$	$\pm 1$	—	—	—	$\mu A$	—		

▲ Data does not apply to terminals 9 or 10.

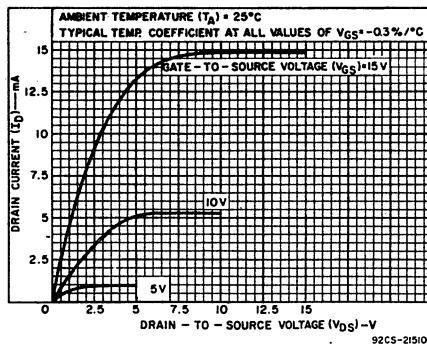


Fig. 3—Typical n-channel drain characteristics.

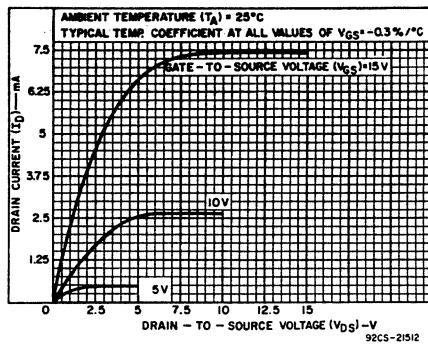


Fig. 4—Minimum n-channel drain characteristics.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs.....  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ )) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4060AE PLASTIC PACKAGE LIMITS									UNITS	FIG. NO.		
		$V_O$ V	$V_{DD}$ V	-40°C			25°C			85°C						
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	$I_L$			5	—	—	50	—	1	50	—	—	700	$\mu A$	16	
				10	—	—	100	—	2	100	—	—	1400			
Quiescent Device Dissipation/Package	$P_D$			5	—	—	250	—	5	250	—	—	3500	$\mu W$	—	
				10	—	—	1000	—	20	1000	—	—	14000			
Output Voltage: Low-Level	$V_{OL}$	Fan Out = 50		5	—	—	0.01	—	0	0.01	—	—	0.05	V	—	
				10	—	—	0.01	—	0	0.01	—	—	0.05			
High-Level	$V_{OH}$	Fan Out = 50		5	4.99	—	—	4.99	5	—	4.95	—	—	V	—	
				10	9.99	—	—	9.99	10	—	9.95	—	—			
Noise Immunity (Any Input)	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	V	17,18	
				1	10	3	—	—	3	4.5	—	2.9	—			
	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—			
				9	10	2.9	—	—	3	4.5	—	3	—			
Output Drive Current: N-Channel (Sink)	$I_{DN}$			0.5	5	0.21	—	—	0.18	0.36	—	0.15	—	$mA$	3,4	
				0.5	10	0.42	—	—	0.36	0.75	—	0.3	—			
P-Channel (Source)	$I_{DP}$			4.5	5	-0.145	—	—	-0.125	-0.25	—	-0.1	—	$mA$	5,6	
				9.5	10	-0.29	—	—	-0.25	-0.5	—	-0.2	—			
Input Current	$I_I$	Any Input		—	—	—	—	—	$\pm 10^{-5}$	$\pm 1$	—	—	—	$\mu A$	—	

▲ Data does not apply to terminals 9 or 10.

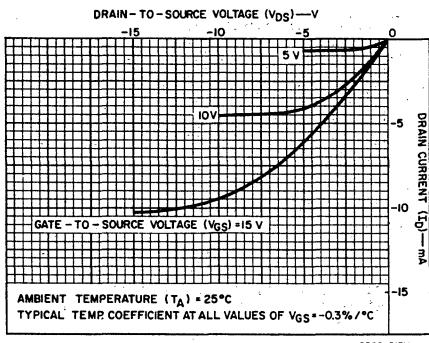


Fig. 5—Typical p-channel drain characteristics.

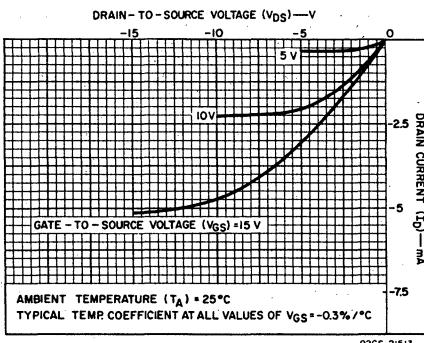


Fig. 6—Minimum p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$  (unless otherwise specified), Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	CERAMIC TYPES			PLASTIC TYPES			UNITS	FIG. NO.	
			V <sub>DD</sub>	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
<b>Input-Pulse Operation</b>											
Propagation Delay Time $\phi_1$ to Q4 Out	t <sub>PHL</sub> , t <sub>PLH</sub>		5	—	900	1800	—	900	1900	ns	7
			10	—	450	900	—	450	950		
Propagation Delay Time, $Q_n$ to $Q_{n+1}$	t <sub>PHL</sub> , t <sub>PLH</sub>		5	—	450	900	—	450	950	ns	8
			10	—	225	450	—	225	475		
Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>		5	—	150	300	—	150	350	ns	9
			10	—	75	150	—	75	175		
Min. Input-Pulse Width	t <sub>WL</sub> , t <sub>WH</sub>	f = 100 kHz	5	—	200	400	—	200	500	ns	—
			10	—	75	110	—	75	125		
Input-Pulse Rise & Fall Time	t <sub>rφ</sub> , t <sub>fφ</sub>		5	—	—	15	—	—	15	μs	—
			10	—	—	7.5	—	—	7.5		
Max. Input-Pulse Frequency	f <sub>φ</sub>		5	1	1.75	—	0.9	1.75	—	MHz	10
			10	3	4	—	2.75	4	—		
Input Capacitance	I <sub>I</sub>		—	5	—	—	5	—	—	pF	—
<b>Reset Operation</b>											
Propagation Delay Time	t <sub>PHL</sub>		5	—	500	1000	—	500	1250	ns	—
			10	—	250	500	—	250	600		
Minimum Reset Pulse Width	t <sub>WH</sub>		5	—	500	1000	—	500	1250	ns	—
			10	—	250	500	—	250	600		

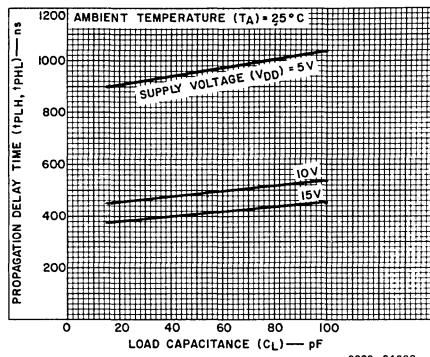


Fig. 7—Typical propagation delay time vs. load capacitance ( $\phi_1$  to Q4 output).

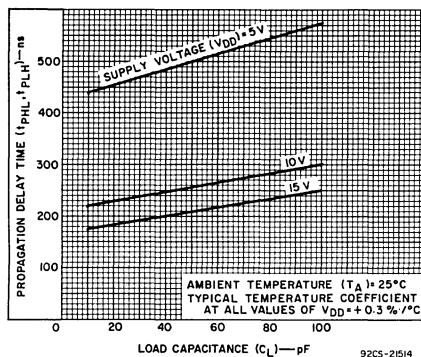


Fig. 8—Typical propagation delay time vs. load capacitance ( $Q_n$  to  $Q_{n+1}$ ).

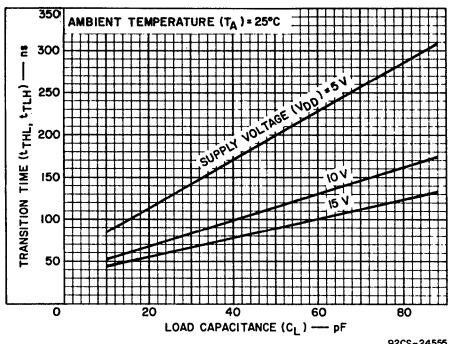


Fig. 9—Typical output transition time vs. load capacitance.

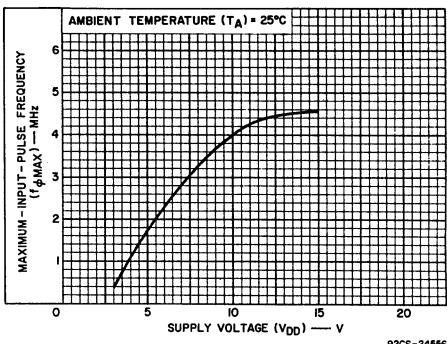


Fig. 10—Typical maximum-input-pulse frequency vs. supply voltage.

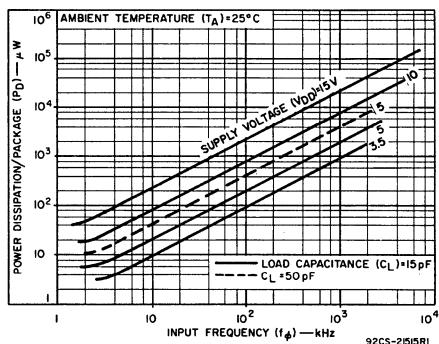


Fig. 11—Typical dynamic power dissipation characteristics.

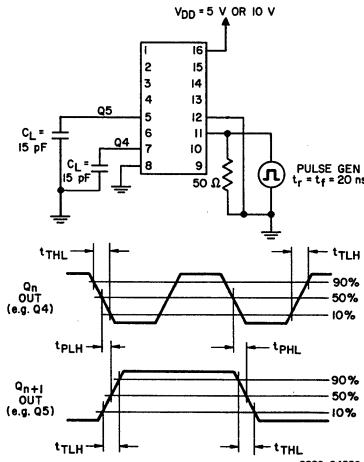


Fig. 13—Propagation delay and transition time test circuit—input-pulse operation.

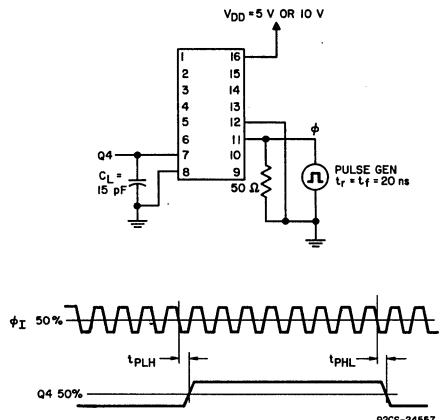


Fig. 12—Propagation delay time test circuit—input-pulse operation.

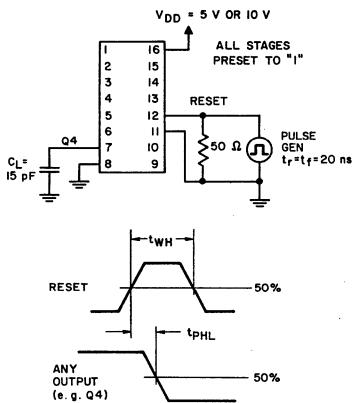


Fig. 14—Test circuit for propagation delay time between reset pulse and any output.

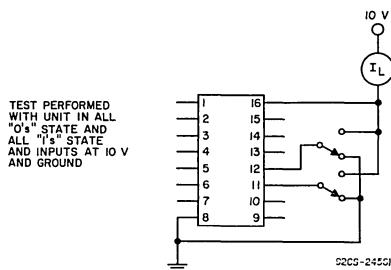


Fig. 16—Quiescent device current test circuit.

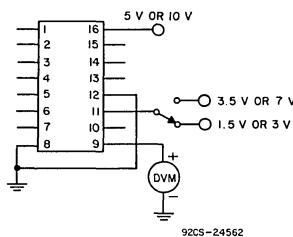


Fig. 17—Input-pulse noise immunity test circuit.

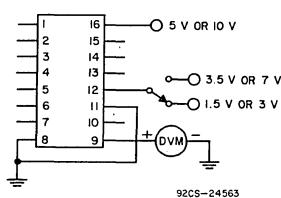


Fig. 18—Reset-pulse noise immunity test circuit.

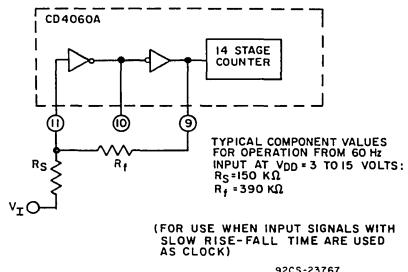


Fig. 20—Input pulse-shaping circuit (Schmitt-Trigger) for CD4060A.

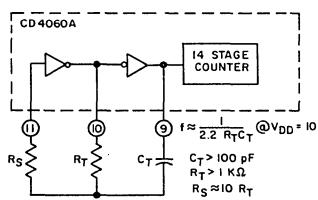


Fig. 19—Typical RC oscillator circuit.

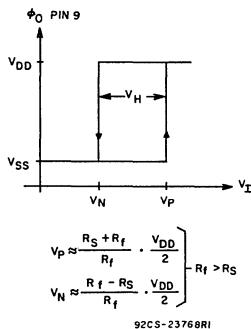


Fig. 21—Input circuit characteristics for circuit in Fig. 20.

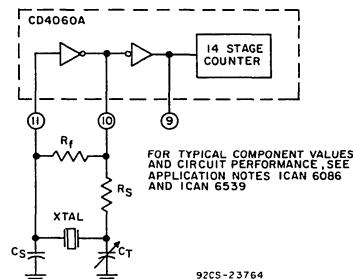
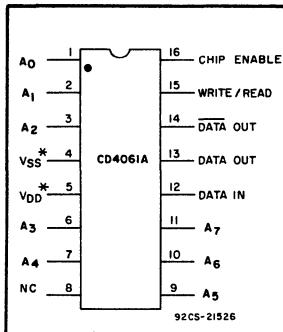


Fig. 22—Typical crystal oscillator circuit.



# Digital Integrated Circuits

Monolithic Silicon  
**CD4061AD**  
**CD4061AH**



## COS/MOS 256-Word by 1-Bit Static Random-Access Memory

### Features:

- Low standby power: 10 Nanowatts/bit (typ.) @  $V_{DD} = 10$  V
- Access time: 380 ns (max.) @  $V_{DD} = 10$  V
- Single 3-to-15 V power supply
- COS/MOS input/output logic compatibility
- TTL output drive capability
- Three-state data outputs for bus-oriented systems
- 1101-type pin designations\*
- Separate data output and data input lines
- Noise immunity: 45% of  $V_{DD}$  (typ.)
- Fully decoded addressing
- Single write/read control line

RCA-CD4061A is a single monolithic integrated circuit containing a 256-word by 1-bit fully static, random-access, NDRO memory. The memory is fully decoded and requires 8 address input lines ( $A_0 - A_7$ ) to select one of 256 storage locations. Additional connections are provided for a WRITE/READ command CHIP ENABLE, DATA IN, and DATA OUT and DATA OUT lines.

To perform READ and WRITE operations the CHIP-ENABLE signal must be low. When the CHIP-ENABLE signal is high, read and write operations are inhibited and the output is a high impedance. To change addresses, the CHIP-ENABLE signal must be returned to a high level, regardless of the logic level of the WRITE/READ input. In a multiple package application, the CHIP-ENABLE signal may be used to permit the selection of individual packages.

Output-voltage levels appear on the outputs only when the CHIP-ENABLE and WRITE/READ signals are both low. Separate data inputs and outputs are provided; they may be tied together, or, to eliminate interaction between READ and WRITE functions, may be used separately. The circuit arrangement permits the outputs from many arrays to be tied to a common bus.

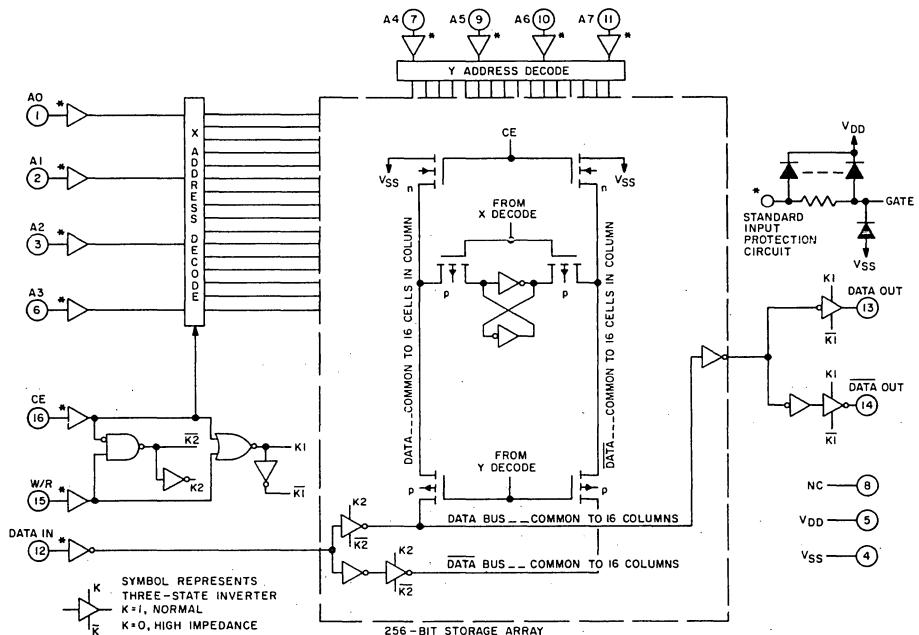
All input and output lines are buffered. The CD4061A output buffers are capable of direct interfacing with TTL devices.

The CD4061A is available in a hermetically sealed 16-lead dual-in-line ceramic package (CD4061AD) or in chip form (CD4061AH).

### MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE .....	-65 to +150 °C
OPERATING-TEMPERATURE RANGE .....	-55 to +125 °C
DC SUPPLY-VOLTAGE RANGE	
( $V_{DD} - V_{SS}$ ) .....	-0.5 to +15 V
DEVICE DISSIPATION (PER PKG.) .....	200 mW
ALL INPUTS .....	$V_{SS} \leq V_i \leq V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE	
( $V_{DD} - V_{SS}$ ) .....	3 to 15 V
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max. ....	265 °C

\* The pin designations are compatible with other static 256-Bit memories and are, therefore, not compatible with standard COS/MOS CD4000A-series devices; i.e.  $V_{DD}$  is pin 5 and  $V_{SS}$  is pin 4.



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Fig. 1 - CD4061A logic diagram.

## CD4061A OPERATIONAL MODES

OPERATION	ADDRESS LINES	CHIP-ENABLE	WRITE/READ	DATA IN	DATA OUTPUTS
Write "0"	Stable	0	1	0	High-Impedance
Write "1"	Stable	0	1	1	High-Impedance
Read	Stable	0	0	X	Valid 1 or 0
*Read/Write	Stable	0	0/1	X	Valid 1 or 0/High-Impedance
Address Change	Changing	1	X	X	High-Impedance

X = Don't Care

\* For a READ/WRITE operation on the same address, chip-enable may be held to a logic 0 for both successive operations.

**STATIC ELECTRICAL CHARACTERISTICS** (All inputs .....  $V_{SS} \leq V_I \leq V_{DD}$ )  
 (Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) ..... 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS								UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.		
				-55°C			25°C			125°C					
		$V_O$ Volts	$V_{DD}$ Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	$I_L$			5	—	—	5	—	0.12	5	—	—	150	$\mu A$	14
				10	—	—	10	—	0.25	10	—	—	300		
Quiescent Device Dissipation/Package	$P_D$			5	—	—	—	—	0.6	25	—	—	750	$\mu W$	—
				10	—	—	—	—	2.5	100	—	—	3000		
Output Voltage Low-Level	$V_{OL}$			5	—	—	0.01	—	0	0.01	—	—	0.05	$V$	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
High-Level	$V_{OH}$			5	4.99	—	—	4.99	5	—	4.95	—	—	$V$	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
Noise Immunity (All Inputs)	$V_{NL}$			0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	$V$	17
				1	10	3	—	—	3	4.5	—	2.9	—		
Noise Immunity (All Inputs)	$V_{NH}$			4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	$V$	17
				9	10	2.9	—	—	3	4.5	—	3	—		
Output Drive Current: (Data Out, Data Out) N-Channel (Sink)	$I_{DN}$			0.4	4.5	2	—	—	1.6	2.5	—	1.1	—	$mA$	3, 4, 12
				0.5	10	4.3	—	—	3.5	5	—	2.4	—		
P-Channel (Source)	$I_{DP}$			2.5	5	-1.1	—	—	-0.9	-1.8	—	-0.65	—	$mA$	5, 6, 13
				4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—		
Output Off Resistance (High-Impedance State)	$R_o(Off)$			9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—	$M\Omega$	—
				5	10	—	—	10	—	—	10	—	—		
				10	10	—	—	10	—	—	10	—	—		

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$ ,  $C_L = 50 \text{ pF}$ , and  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS	CHARAC- TERISTIC CURVES & TEST CIRCUITS Fig. No.	
			$V_{DD}$ (Volts)	Min.*	Typ.			
READ CYCLE	Read Cycle Time	$t_{RC}$	5	1200	1000	—	ns	2
			10	550	450	—		
	Chip-Enable Hold Time	$t_{CEH}$	5	40	0	—	ns	2
			10	0	—	—		
	Chip-Enable Pulse Width	$t_{CE}$	5	700	500	—	ns	2
			10	350	250	—		
	Chip-Enable Setup Time	$t_{CES}$	5	460	—	—	ns	2
			10	200	—	—		
	Read Access Time	$t_{RA}$	5	—	450	750	ns	2, 9, 10
			10	—	250	380		
WRITE CYCLE	Write Cycle Time	$t_{WC}$	5	1200	1000	—	ns	2
			10	550	450	—		
	Chip-Enable Hold Time	$t_{CEH}$	5	40	0	—		
			10	0	—	—		
	Chip-Enable Pulse Width	$t_{CE}$	5	700	500	—		
			10	350	250	—		
	Chip-Enable Setup Time	$t_{CES}$	5	460	—	—		
			10	200	—	—		
	Write Hold Time	$t_{WH}$	5	150	100	—		
			10	100	70	—		
	Write Pulse Width	$t_W$	5	150	100	—	ns	2
			10	100	70	—		
	Data Setup Time	$t_{DS}$	5	140	80	—		
			10*	80	35	—		
	Data Hold Time	$t_{DH}$	5	25	10	—		
			10	20	10	—		
	Output Transition Time	$t_{TLH}$	5	—	60	100	ns	7
			10	—	50	75		
	Output Transition Time	$t_{THL}$	5	—	35	60	ns	8
			10	—	25	40		
CHIP-ENABLE	Input Rise and Fall Time	$t_{CE}$	5	—	—	15	$\mu\text{s}$	
			10	—	—	5		
			15	—	—	1		

\* See "Symbol Definitions"

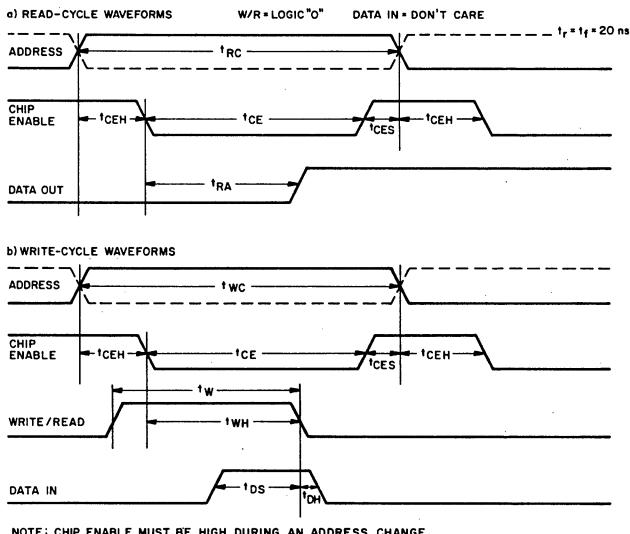


Fig. 2 — Typical write-read waveforms.

92CM-23853

**SYMBOL DEFINITIONS****READ CYCLE**

**t<sub>RC</sub> — READ CYCLE TIME** — Time required between address changes during a read cycle. Minimum read cycle time is equal to t<sub>CEH</sub> (min.) + t<sub>CE</sub> (min.) + t<sub>CES</sub> (min.). (See Definitions below).

**t<sub>CEH</sub> — CHIP-ENABLE HOLD TIME** — Time required before chip-enable level can be lowered after an address transition.

**t<sub>CE</sub> — CHIP-ENABLE PULSE WIDTH** — Time required for the chip to be active for valid reading of output data.

**t<sub>CES</sub> — CHIP-ENABLE SETUP TIME** — Time required before an address transition can take place after chip-enable level has been increased. t<sub>CES</sub>(min.) + t<sub>CEH</sub>(min.) is the minimum time required to discharge internal nodes and allow settling of address decoders during an address transition. Chip-enable level must be raised during each address change, even if read cycles only or write cycles only are successively performed. However, if address is not changed, chip enable may remain in its active (low) state during successive read and write cycles.

**t<sub>RA</sub> — READ ACCESS TIME** — Measured from chip-enable transition; time before output data is valid.

**WRITE CYCLE**

**t<sub>WC</sub> — WRITE CYCLE TIME** — Time required between address changes during a write cycle. This time sets the maximum

operating frequency for the memory, with minimum write cycle time equal to t<sub>CEH</sub> (min.) + t<sub>CE</sub> (min.) + t<sub>CES</sub> (min.).

**t<sub>CEH</sub> — CHIP-ENABLE HOLD TIME** — See Definition under read cycle.

**t<sub>CE</sub> — CHIP-ENABLE PULSE WIDTH** — See Definition under read cycle.

**t<sub>CES</sub> — CHIP-ENABLE SETUP TIME** — See Definition under read read cycle.

**t<sub>WH</sub> — WRITE HOLD TIME** — Measured from chip-enable transition; time required before negative transition of write pulse can occur for successful write operation.

**t<sub>W</sub> — WRITE PULSE WIDTH** — Time required for W/R pulse to be high. Note that no specification for positive transition of this pulse is made — it may occur before or after the chip-enable transition. In many applications, the W/R control is normally low and is strobed high during a write cycle.

**t<sub>DS</sub> — DATA SETUP TIME** — Measured from write-pulse negative transition; time required for data input to be valid.

**t<sub>DH</sub> — DATA HOLD TIME** — Measured from write-pulse negative transition; time required for data input to be valid after W/R is returned to a low level. The minimum data pulse width is equal to t<sub>DS</sub> (min.) + t<sub>DH</sub> (min.).

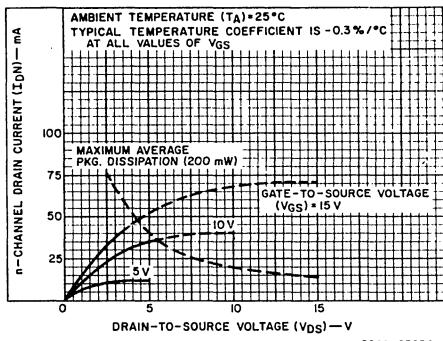


Fig. 3 – Typical n-channel drain characteristics.

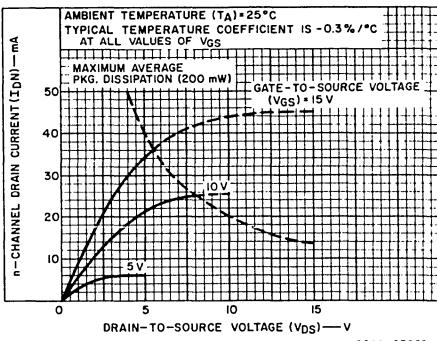


Fig. 4 – Minimum n-channel drain characteristics.

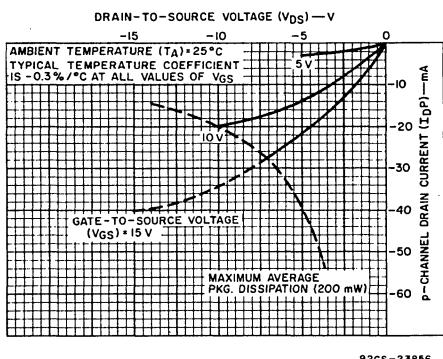


Fig. 5 – Typical p-channel drain characteristics.

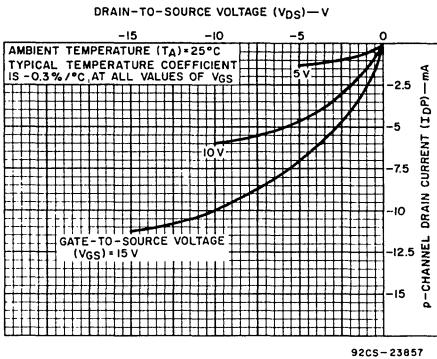
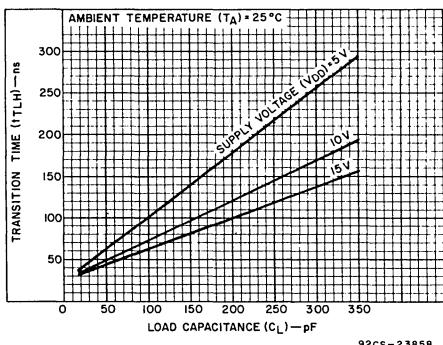
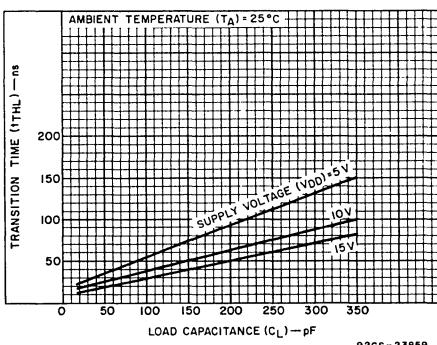


Fig. 6 – Minimum p-channel drain characteristics.

Fig. 7 – Typical low-to-high transition time ( $t_{TLH}$ ) vs  $C_L$ .Fig. 8 – Typical high-to-low transition time ( $t_{THL}$ ) vs  $C_L$ .

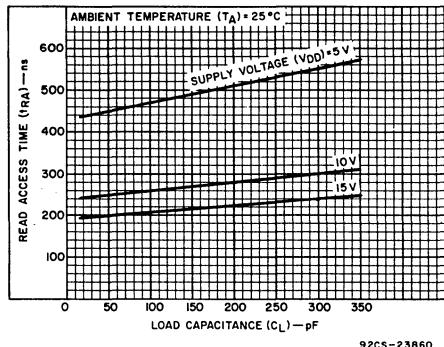
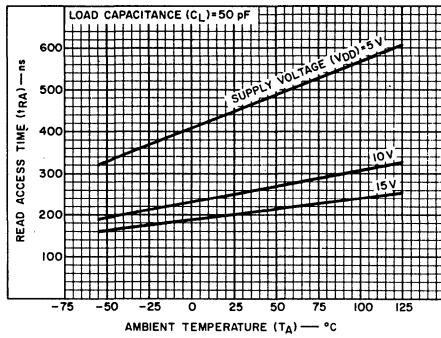
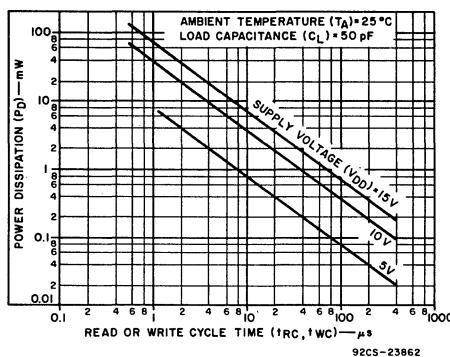
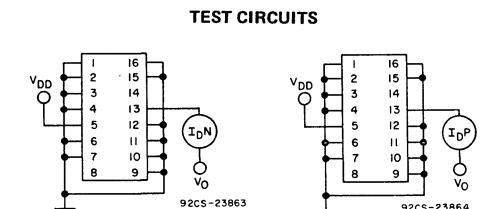
Fig. 9 – Typical read access time ( $t_{RA}$ ) vs  $C_L$ .Fig. 10 – Typical read access time ( $t_{RA}$ ) vs temperature.

Fig. 11 – Typical power dissipation vs cycle time.



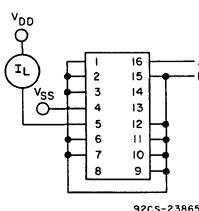
Note: At address 0, "0" stored in memory.

Note: At address 0, "1" stored in memory.

Fig. 12 – n-channel drive current. Fig. 13 – p-channel drive current.

#### Note:

Power dissipation measured using random data pattern. Input pulse delays and widths set to minimum values specified on data sheet with the exception of cycle time, 15 V setups identical to 10 V data sheet values, with the exception of  $t_{CE} = 400$  ns.



Test	A	B	Memory Cells
1	0	0	All 0
2	1	1	All 0
3	0	1	All 0
4	0	0	All 1
5	1	1	All 1
6	0	1	All 1

Fig. 14 – Quiescent device current.

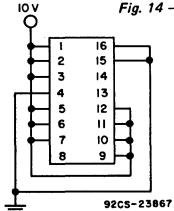


Fig. 16 – Bias life.

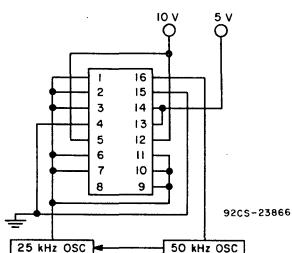


Fig. 15 – Operating life.

AO	1	16	CE
A1	2	15	W/R
A2	3	14	D <sub>O</sub>
A3	4	13	DO
V <sub>DD</sub>	5	12	DI
V <sub>SS</sub>	6	11	AT
A4	7	10	A6
	8	9	A5

92CS-23868

#### Description of Test:

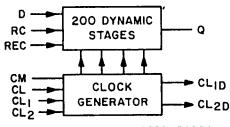
Functional test run with random data input. All inputs toggle between 30% and 70% of  $V_{DD}$ .

Fig. 17 – Noise immunity.

Note: Connection to all terminals in Figs. 15 & 16 (except 4 and 5) are made through 47 kΩ resistors.



## COS/MOS 200-Stage Dynamic Shift Register



CD4062A Functional Diagram

The RCA-CD4062A is a 200-stage dynamic shift register with provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended for low-power, low clock-line capacitance requirements. Single-phase clocking is specified for medium-speed operation (< 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (< 5 pF), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise and fall time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 pF/phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL<sub>1</sub> for two-phase operation.

The CD4062A is supplied in a 16-lead flat pack (K), a 12-lead TO-5 style package (T), and in chip form (H).

### Special Features:

- Operation from a single 3-V to 15-V positive or negative power supply
- Minimum shift rates over full temperature range –  
Single phase clock:  $3 \text{ V} \leq V_{DD} \leq 10 \text{ V}$ ;  $f_{min} = 10 \text{ kHz}$ ;  
 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  ( $f_{min} = 1 \text{ kHz}$  up to  $T_A \leq 75^\circ\text{C}$ )

Two-phase clock:  $3 \text{ V} \leq V_{DD} \leq 15 \text{ V}$ ;  $f_{min} = 10 \text{ kHz}$ ;  
 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  ( $f_{min} = 1 \text{ kHz}$  up to  $T_A \leq 75^\circ\text{C}$ )

- Low power dissipation  
0.3 mW/bit at 1 MHz and 10 V  
0.04 mW/bit at 0.5 MHz and 5 V  
(alternating 1-0 data pattern)
- Data output TTL-DTL compatible
- Recirculating capability
- Delayed two-phase clock outputs available for cascading registers
- Asynchronous ripple-type presettable to all 1's or 0's
- Ultra-low-power-dissipation standby operation

### Applications:

- Serial shift registers
- Time-delay circuits
- CRT refresh memory
- Long serial memory

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE.....	-55 to +125°C
DC SUPPLY-VOLTAGE RANGE ( $V_{DD}-V_{SS}$ ).....	-0.5 to +15 V
DEVICE DISSIPATION (PER PACKAGE) .....	200 mW
ALL INPUTS .....	$V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):

AT DISTANCE  $1/16 \pm 1/32$  IN. (1.59  $\pm$  0.79 MM) ..... 265°C

FROM CASE FOR 10 S MAX. .... 265°C

### RECOMMENDED OPERATING CONDITIONS

DC SUPPLY VOLTAGE ( $V_{DD}-V_{SS}$ ): SINGLE-PHASE CLOCK	3 to 10 V
TWO-PHASE CLOCK	3 to 15 V
INPUT VOLTAGE SWING .....	$V_{DD}$ to $V_{SS}$

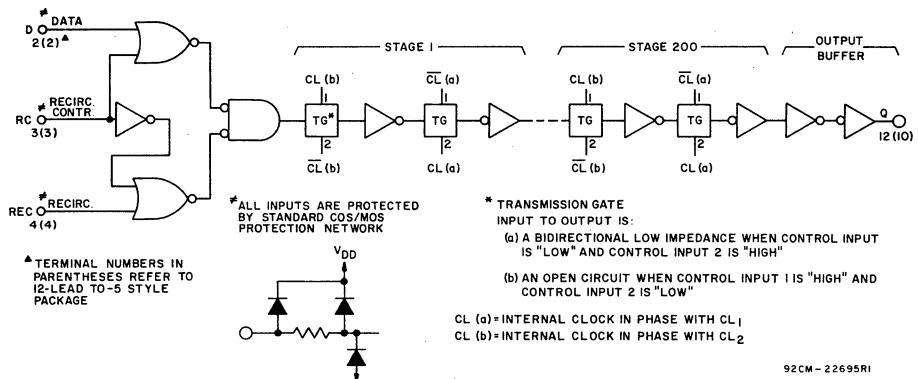


Fig. 1—CD4062A logic block diagram.

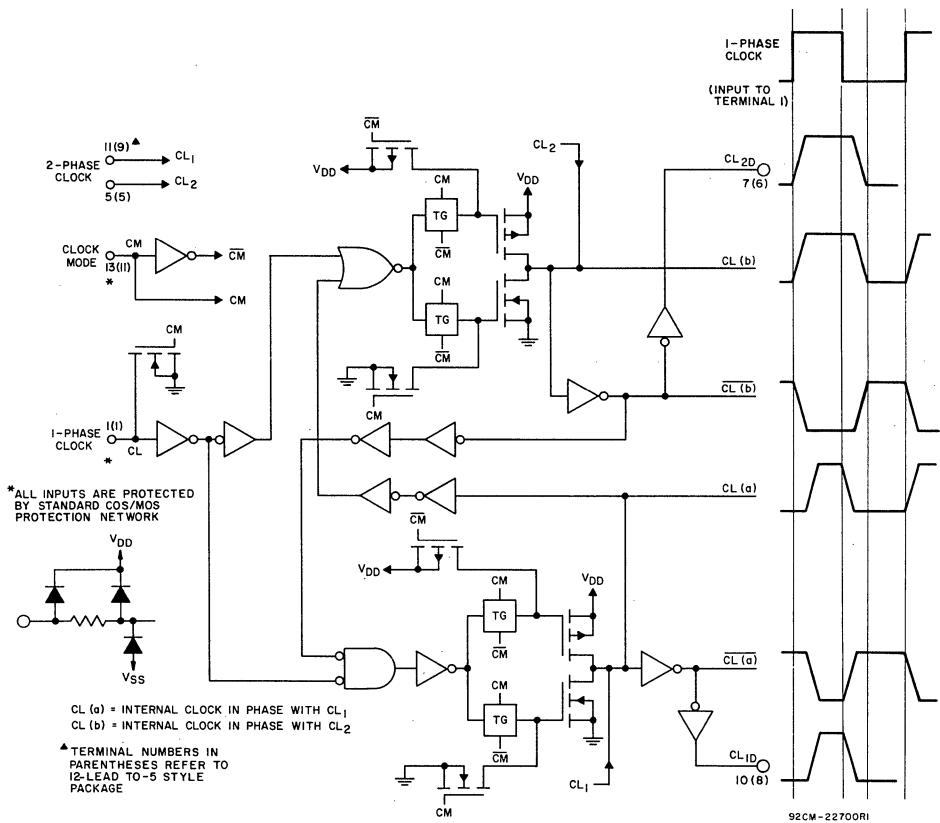
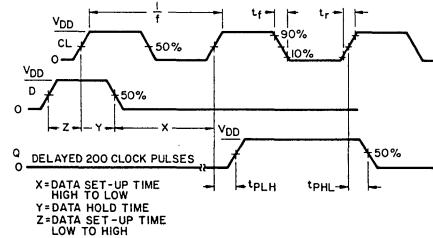


Fig. 2—Clock circuit logic diagram.

**STATIC ELECTRICAL CHARACTERISTICS, All Inputs .....  $V_{SS} \leq V_I \leq V_{DD}$**   
**Recommended DC Supply Voltage ( $V_{DD}-V_{SS}$ ) ..... 3 to 15 V**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS						UNITS	FIG. NO.		
		$V_O$ V	$V_{DD}$ V	-55°C		25°C		125°C						
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.				
Quiescent Device Current	$I_L$	CM=High $CL_1$ =High $CL_2$ =Low	5	—	12	—	0.5	12	—	720	$\mu A$	19		
			10	—	25	—	1	25	—	1500				
Quiescent Device Dissipation/Package	$P_D$	CM=High $CL_1$ =High $CL_2$ =Low	5	—	60	—	2.5	60	—	3600	$\mu W$	—		
			10	—	250	—	10	250	—	15000				
Output Voltage: Low-Level	$V_{OL}$		5	—	0.01	—	0	0.01	—	0.05	$V$	—		
			10	—	0.01	—	0	0.01	—	0.05				
High-Level	$V_{OH}$		5	4.99	—	4.99	5	—	4.95	—	$V$	—		
			10	9.99	—	9.99	10	—	9.95	—				
Noise Immunity (Any Input)	$V_{NL}$		0.8	5	1.5	—	1.5	2.25	—	1.4	$V$	20		
			1.0	10	3	—	3	4.5	—	2.9				
	$V_{NH}$		4.2	5	1.4	—	1.5	2.25	—	1.5				
			9.0	10	2.9	—	3	4.5	—	3				
Output Drive Current: N-Channel (Sink)	$I_{DN}$	Q Output	0.4	4.5	1.6	—	1.3	2.6	—	0.91	$mA$	13,21		
			0.5	10	5	—	4	8*	—	3.2				
		CL <sub>1D</sub> , CL <sub>2D</sub>	0.5	5	0.87	—	0.7	1.4	—	0.49				
			0.5	10	2.2	—	1.8	3.6	—	1.26				
P-Channel (Source)	$I_{DP}$	Q Output	4.5	5	-0.31	—	-0.25	-0.5	—	-0.17	$mA$	14,22		
			2.5	5	-0.93	—	-0.75	-1.5	—	-0.52				
		CL <sub>1D</sub> , CL <sub>2D</sub>	4.5	10	-0.87	—	-0.7	-1.4	—	-0.49				
			9.5	10	-1.1	—	-0.9	-1.8	—	-0.63				
Input Current	$I_I$	Any Input	—	—	—	—	—	10	—	—	pA	—		

\* Maximum power dissipation rating  $\leq 200$  mW.



92CS-22702

Fig. 3-Timing diagram—single-phase clock.

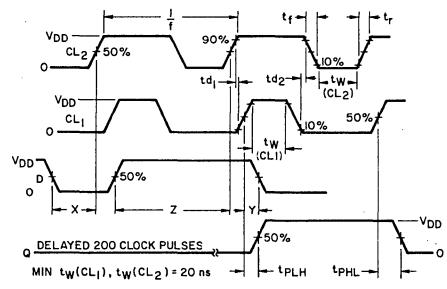
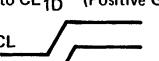
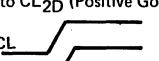
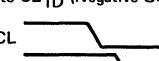
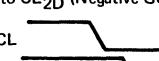
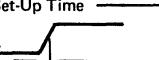
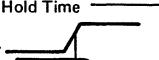


Fig. 4-Timing diagram—two-phase clock.

DYNAMIC CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ , except  $t_rCL$  and  $t_fCL$

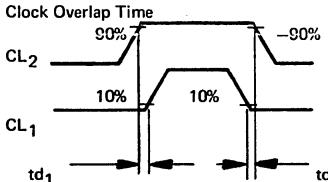
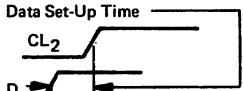
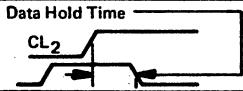
Single-Phase-Clock Operation; Clock Mode (CM) = Low;  $3 \text{ V} \leq V_{DD} \leq 10 \text{ V}$  (See Figure 3)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	FIG. NO.
			$V_{DD} \text{ V}$	MIN.	TYP.	MAX.		
Maximum Clock Frequency (50% Duty Cycle)	$f_{CL}$	$t_r, t_f = 20 \text{ ns}$	5	0.5	1	—	MHz	—
			10	1	2	—		
Minimum Clock Frequency (50% Duty Cycle)	$f_{CL}$		5	150	10	—	Hz	18
			10	150	10	—		
Clock Rise and Fall Times**	$t_rCL, t_fCL$		5	—	—	10	$\mu\text{s}$	—
			10	—	—	1		
Average Input Capacitance All Inputs Except $CL_1$ and $CL_2$	$C_I$			—	5	—	pF	—
Propagation Delays:	$t_{PLH}, t_{PHL}$		5	—	1000	2000	ns	—
CL to Q	$t_{PLH}$		10	—	400	800		
CL to $CL_{1D}$ (Positive Going)	$t_{PLH}$	(50% Points)	5	—	750	1500		
	$t_{PLH}$		10	—	300	600		
CL to $CL_{2D}$ (Positive Going)	$t_{PLH}$	(50% Points)	5	—	500	1000		
	$t_{PLH}$		10	—	200	400		
CL to $CL_{1D}$ (Negative Going)	$t_{PHL}$	(50% Points)	5	—	450	900		
	$t_{PHL}$		10	—	175	350		
CL to $CL_{2D}$ (Negative Going)	$t_{PHL}$	(50% Points)	5	—	750	1500		
	$t_{PHL}$		10	—	300	600		
Transition Time:	$t_{TLH}, t_{THL}$		5	—	100	200	ns	—
Q Output	$t_{TLH}, t_{THL}$		10	—	50	100		
$CL_{1D}, CL_{2D}$	$t_{TLH}, t_{THL}$		5	—	200	400		
	$t_{TLH}, t_{THL}$		10	—	100	200		
Data Set-Up Time	$t_{SU}$		5	0	—	—		
	$t_{SU}$		10	0	—	—		
	$t_{SU}$		5	150	—	—		
▲ Data Hold Time	$t_{HOLD}$		10	50	—	—	ns	—
	$t_{HOLD}$		5	150	—	—		

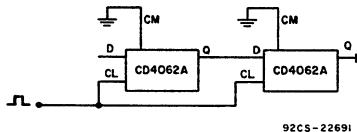
\*\* If more than one unit is cascaded in single-phase parallel clocked application,  $t_rCL$  should be made less than or equal to the sum of the propagation delay at 15 pF, and the transition time of the output driving stage. (See Figs. 5 and 7 for cascading options.)

▲ Use of delayed clock permits high-speed logic to precede CD4062A register (see cascade register operation).

Two-Phase Clock Operation ( $CL_1$ ,  $CL_2$ ); Clock Mode (CM) = High;  $3 V \leq V_{DD} \leq 15 V$ . See Figure 4.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	FIG. NO.
			V <sub>DD</sub> V	MIN.	TYP.	MAX.	
Maximum Clock Frequency	$f_{CL}$		5	1.25	2.5	—	MHz
			10	2.5	5	—	
Minimum Clock Frequency	$f_{CL}$		5	150	10	—	Hz
			10	150	10	—	
Clock Overlap Time 				40	—	—	ns
Average Input Capacitance $CL_1$ , $CL_2$	$C_I$			—	50	—	pF
Propagation Delays $CL_1$ to Q $CL_1$ to $CL_{1D}$ $CL_2$ to $CL_{2D}$	$t_{PHL}$ , $t_{PLH}$		5	—	250	500	ns
			10	—	100	200	
			5	—	250	500	
			10	—	100	200	
Data Set-Up Time 	$t_{SU}$		5	300	150	—	ns
			10	100	50	—	
Data Hold Time 	$t_{HOLD}$		5	0	—	—	ns
			10	0	—	—	
Clock Rise and Fall Times	$t_{r,CL_1, CL_2}$ $t_{f,CL_1, CL_2}$			No Restrictions If Clock Overlap Require- ment Is Met			

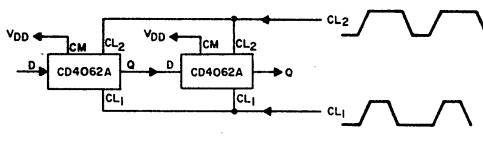
### CASCADED REGISTER OPERATION



#### FEATURES:

- Low clock capacitance  $\sim 5$  pF/package
- Medium-speed operation  $\sim 1$  MHz @ 10 V
- Stringent clock rise and fall times required

Fig. 5—Single-phase clocking (CM = GND).



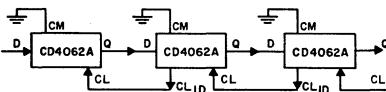
#### FEATURES:

- High-speed operation  $\sim 5$  MHz @  $V_{DD} = 10$  V
- No clock rise and fall time requirements if clock overlap specification is met
- Clock input capacitance only 50 pF/phase/package

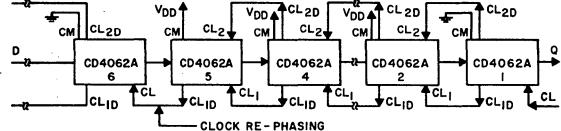
Fig. 6—Two-phase clocking.

## CASCADED REGISTER OPERATION (CONT'D)

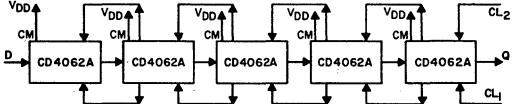
## a) SINGLE PHASE CLOCK INPUT (LOW SPEED)



## b) SINGLE-PHASE - CLOCK INPUT (MEDIUM SPEED)

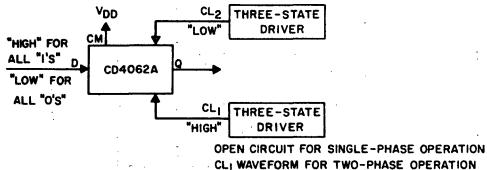


## c) TWO - PHASE - CLOCK INPUT (HIGHER SPEED)



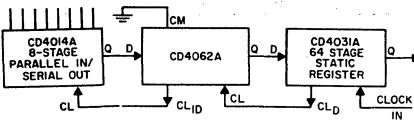
92CS-22699

Fig. 7—Use of delayed-clock outputs.

OPEN CIRCUIT FOR SINGLE-PHASE OPERATION  
CL<sub>2</sub> WAVEFORM FOR TWO-PHASE OPERATIONOPEN CIRCUIT FOR SINGLE-PHASE OPERATION  
CL<sub>1</sub> WAVEFORM FOR TWO-PHASE OPERATION

92CS-22692RI

Fig. 8—Asynchronous set/reset and standby.



92CS-22690

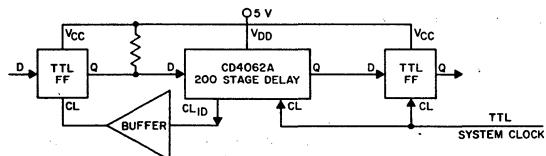
## FEATURES:

- Ripple-type set/reset to all 1's/0's
- Ultra-low standby power dissipation

## FEATURES:

- 64 stage static register delayed clock compatible with single-phase clock input on CD4062A
- CL<sub>1D</sub> delayed clock output on CD4062A compatible with other COS/MOS registers

Fig. 9—Compatibility with other COS/MOS registers/ logic.



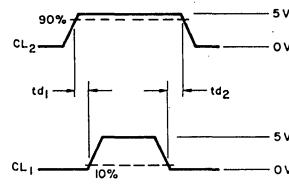
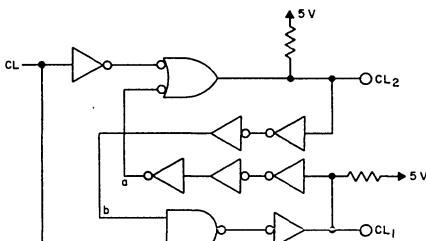
92CS-22698

Fig. 10—Compatibility with TTL/DTL systems.

## FEATURES:

- Single TTL supply level
- "Race"-Free: High speed TTL driving medium speed COS/MOS

## SIMPLE TWO-PHASE CLOCK GENERATOR CIRCUITS FOR DRIVING CD4062A



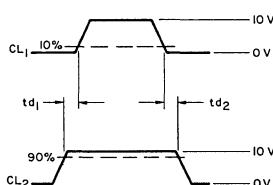
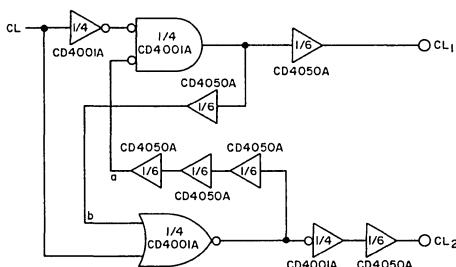
92CM-22697

## REQUIRED:

- 1 QUAD 2 NAND OR TRIPLE 3 NAND  
(SN5400/7400 OR (SN5410/7410)
- 1 HEX INVERTER (SN5404/7404)

t<sub>d1</sub> AND t<sub>d2</sub> ≈ 40 ns WITH THIS CIRCUITt<sub>d1</sub> AND t<sub>d2</sub> MAY BE ADJUSTED BY  
ADDING MORE INVERTER DELAYS OR  
CAPACITIVELY LOADING POINTS a AND b.

Fig. 11-TTL-5-volt levels (only 2-gate packages required).



92CM-22701

## REQUIRED:

- 1 CD4001A-QUAD 2 INPUT NOR GATE
- 1 CD4050A-HEX BUFFER (NON-INVERTING)

t<sub>d1</sub> AND t<sub>d2</sub> ≈ 100 ns WITH THIS CIRCUIT @ 10 Vt<sub>d1</sub> AND t<sub>d2</sub> MAY BE ADJUSTED BY ADDING  
MORE INVERTER DELAYS OR CAPACITIVELY  
LOADING a AND b.

Fig. 12-CMOS-3-15 volt levels (only 2-gate packages required).

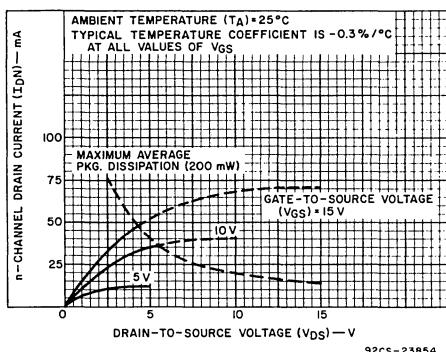


Fig. 13—Typical n-channel drain characteristics for Q output.

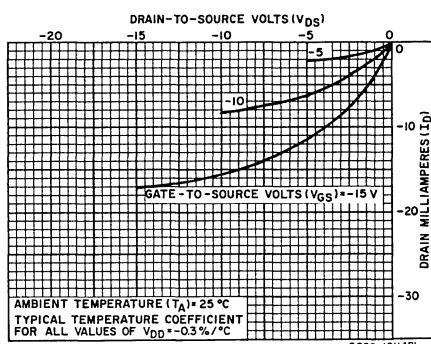
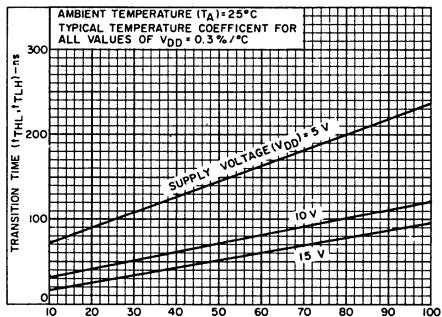


Fig. 14—Typical p-channel drain characteristics for Q output.



NOTE:  $t_{THL}$  FOR Q OUTPUT IS SIGNIFICANTLY LESS THAN  $t_{TLH}$

Fig. 15—Typical transition time vs.  $C_L$  for data outputs.

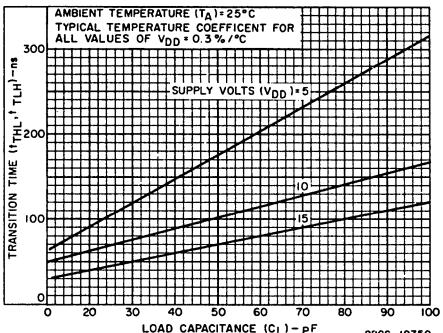


Fig. 16—Typical transition time vs.  $C_L$  for delayed clock output.

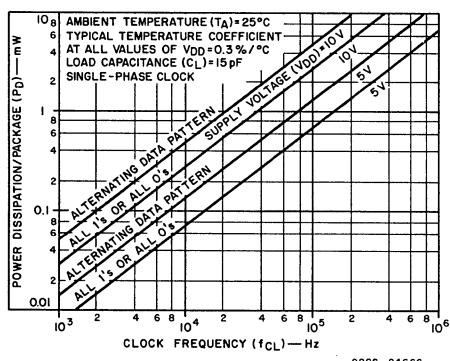


Fig. 17—Typical power dissipation vs. frequency.

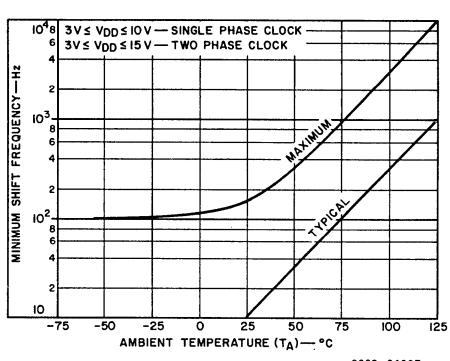


Fig. 18—Minimum shift frequency vs. ambient temperature.

## TEST CIRCUITS

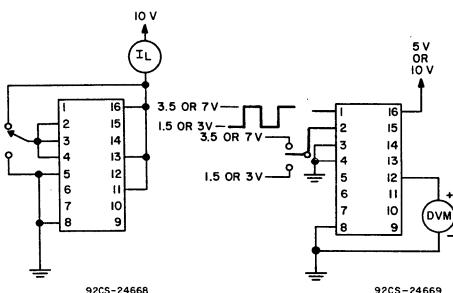


Fig. 19—Quiescent device current.

Fig. 20—Noise immunity.

In single-phase clock mode inputs  $CL_1$  and  $CL_2$  should be left unconnected.

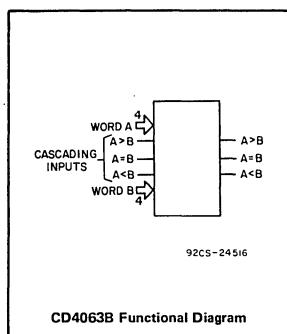
In two-phase clock mode 1-phase clock input may be left unconnected because an internal pulldown device is provided.



## Digital Integrated Circuits

Monolithic Silicon

## CD4063B Types



## COS/MOS 4-Bit Magnitude Comparator

*Features:*

- Standard B-series output drive
- Expansion to 8, 16 . . . 4N bits by cascading units
- Medium-speed operation: compares two 4-bit words in 250 ns (typ.) at 10 V

*Applications:*

- Servo motor controls
- Process controllers

The RCA-CD4063B is a low-power 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs ( $A_3, B_3$ , through  $A_0, B_0$ ), three outputs ( $A < B$ ,  $A = B$ ,  $A > B$ ) and three cascading inputs ( $A < B$ ,  $A = B$ ,  $A > B$ ) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: ( $A < B$ ) = low, ( $A = B$ ) = high, ( $A > B$ ) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs ( $A < B$ ,  $A = B$ , and  $A > B$ ) on the least significant comparator are connected to a low, a high, and a low level, respectively.

All outputs have equal source- and sink-current capabilities and conform to standard B-series output drive (see Static Electrical Characteristics).

The CD4063B is supplied in 16-lead dual-in-line welded-seal ceramic packages (D), plastic packages (E), ceramic packages (F), flat packs (K), and in chip form (H).

TRUTH TABLE

INPUTS								OUTPUTS		
COMPARING				CASCADING				$A < B$	$A = B$	$A > B$
$A_3, B_3$	$A_2, B_2$	$A_1, B_1$	$A_0, B_0$	$A < B$	$A = B$	$A > B$				
$A_3 > B_3$	X	X	X	X	X	X	0	0	1	
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	0	0	1	
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	0	0	1	
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	0	0	1	
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	0	1	0	0	1	
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	1	0	0	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	1	0	0	1	0	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	1	0	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	1	0	0	0
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	1	0	0	0
$A_3 < B_3$	X	X	X	X	X	X	1	0	0	0

X = Don't Care

1 ≡ High State

0 ≡ Low State

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4063BD, BK, BF, BH CERAMIC PACKAGE LIMITS									UNITS	FIG. NO.		
		VO Volts	VDD Volts	-55°C			25°C			125°C						
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	IL			5	—	—	5	—	0.02	5	—	—	300	μA	12	
				10	—	—	10	—	0.02	10	—	—	600			
				15	—	—	—	—	0.02	—	—	—	—			
Output Voltage Low-Level	VOL			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—	
				10	—	—	0.01	—	0	0.01	—	—	0.05			
				15	—	—	—	—	0	—	—	—	—			
High-Level	VOH			5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	
				10	9.99	—	—	9.99	10	—	9.95	—	—			
				15	—	—	—	—	15	—	—	—	—			
Noise Immunity	VNL	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	13		
		1	10	3	—	—	3	4.5	—	2.9	—	—				
		1.5	15	—	—	—	—	6.75	—	—	—	—				
	VNH	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—				
		9	10	2.9	—	—	3	4.5	—	3	—	—				
		13.5	15	—	—	—	—	6.75	—	—	—	—				
Output Drive Current: N-Channel (Sink)	IDN			0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	mA	3,4	
				0.5	10	1.1	—	—	0.9	1.8	—	0.65	—			
				1.5	15	—	—	—	3	6	—	—	—			
P-Channel (Source)	IDP			2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	mA	5,6	
				4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—			
				9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—			
				13.5	15	—	—	—	-3	-6	—	—	—			
Input Current	I <sub>I</sub>			15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE:

CERAMIC-PACKAGE TYPES ..... -55 to +125°C

PLASTIC-PACKAGE TYPES ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE

V<sub>DD</sub>\* ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)

from case for 10 seconds max. ..... 265°C

\* All voltage values are referenced to V<sub>SS</sub> terminal.OPERATING CONDITIONS AT T<sub>A</sub> = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	—	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	-0.5 V to V <sub>DD</sub> + 0.5 V	V	—

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4063BE PLASTIC PACKAGE LIMITS								UNITS	FIG. NO.	
		VO Volts	VDD Volts	-40°C			25°C			85°C				
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	IL	5 10 15	— — —	—	—	50	—	0.02	50	—	—	700	μA	12
				—	—	100	—	0.02	100	—	—	1400		
				—	—	—	—	0.02	—	—	—	—		
Output Voltage: Low-Level	VOL	5 10 15	— — —	—	0.01	—	0	0.01	—	—	—	0.05	V	—
				—	—	0.01	—	0	0.01	—	—	0.05		
				—	—	—	—	0	—	—	—	—		
High-Level	VOH	5 10 15	4.99 9.99 —	—	—	4.99	5	—	4.95	—	—	—	—	—
				—	—	9.99	10	—	9.95	—	—	—		
				—	—	—	—	15	—	—	—	—		
Noise Immunity	VNL	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	13
		1	10	3	—	—	3	4.5	—	2.9	—	—		
		1.5	15	—	—	—	6.75	—	—	—	—	—		
	VNH	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—		
		9	10	2.9	—	—	3	4.5	—	3	—	—		
		13.5	15	—	—	—	6.75	—	—	—	—	—		
Output Drive Current:	IDN	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	3,4
N-Channel (Sink)		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—		
		1.5	15	—	—	—	3	6	—	—	—	—		
P-Channel (Source)	IDP	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	5,6
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—		
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—		
		13.5	15	—	—	—	-3	-6	—	—	—	—		
Input Current	II	—	15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—

DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, and C<sub>L</sub> = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
				VDD Volts	Typ.	Max.		
Propagation Delay Time: Comparing Inputs to Outputs	t <sub>PHL</sub> , t <sub>PLH</sub>	—	—	5	625	1250	ns	7,8
				10	250	500		
Cascading Inputs to Outputs	t <sub>PHL</sub> , t <sub>PLH</sub>	—	—	5	500	1000	ns	9
				10	200	400		
Transition Time	t <sub>THL</sub> t <sub>TLH</sub>	—	—	5	100	200	ns	9
				10	50	100		
Average Input Capacitance	C <sub>I</sub>	Any Input		5	—	pF	—	—

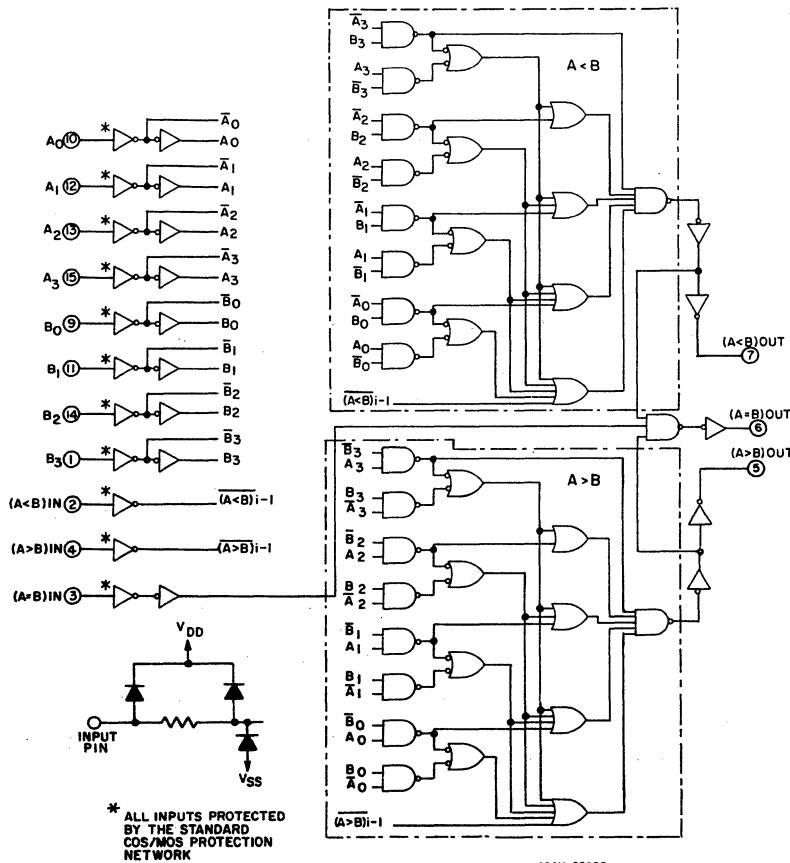
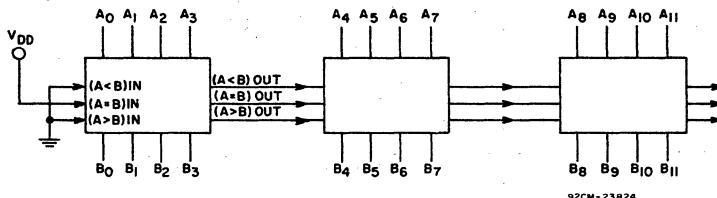


Fig. 1—Logic diagram CD4063B.



$t_p \text{ TOTAL} = t_p \text{ (COMPARE)} + 2 \times t_p \text{ (CASCADE)} . \text{AT } C_L = 15 \text{ pF (each output), } V_{DD} = 10V$   
(3 STAGES)

$$= 250 + 2 \times (200) = 650 \text{ ns (TYP.)}$$

Fig. 2—Typical speed characteristics of a 12-bit comparator.

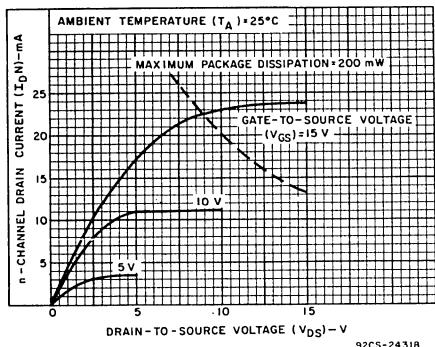


Fig. 3—Typical output-N-channel drain characteristics.

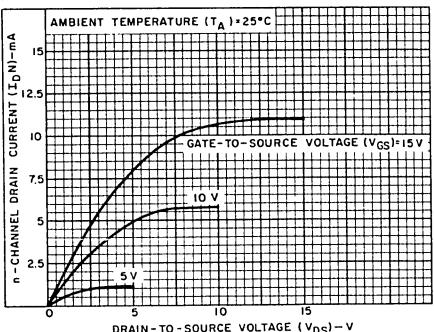


Fig. 4—Minimum output-N-channel drain characteristics.

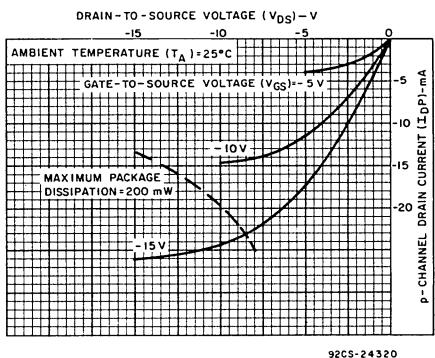


Fig. 5—Typical output-P-channel drain characteristics.

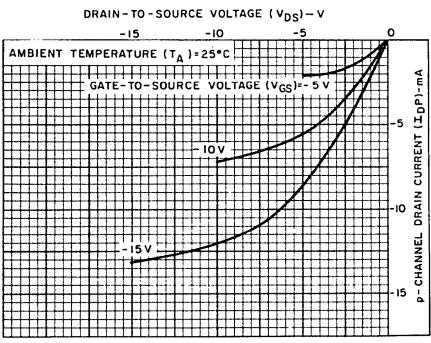


Fig. 6—Minimum output-P-channel drain characteristics.

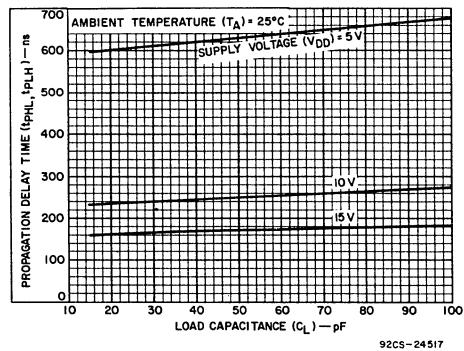


Fig. 7—Typical propagation delay time vs. load capacitance.

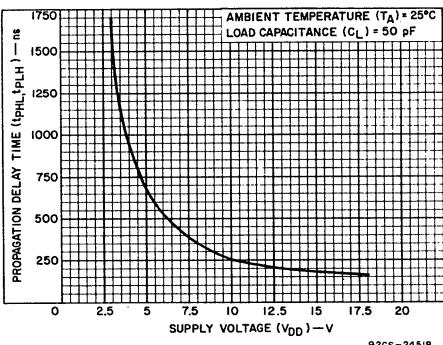


Fig. 8—Typical propagation delay time vs. supply voltage (“comparing inputs” to outputs).

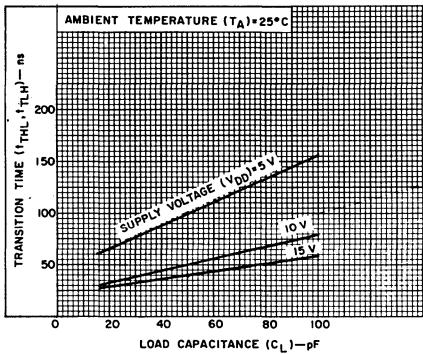


Fig. 9—Typical transition time vs. load capacitance.

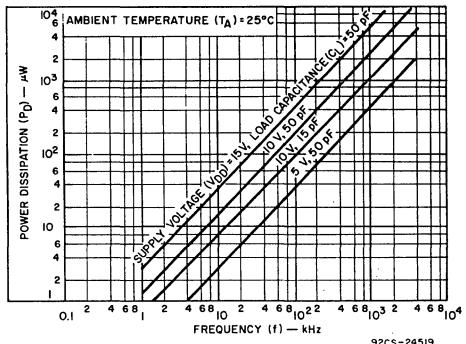


Fig. 10—Typical dynamic power dissipation characteristics.

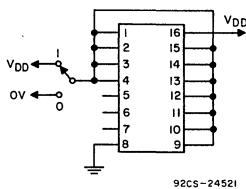


Fig. 11—Quiescent device current test circuit.

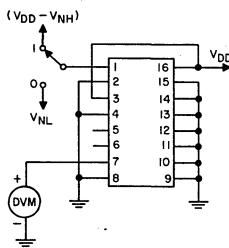


Fig. 12—Noise immunity test circuit.

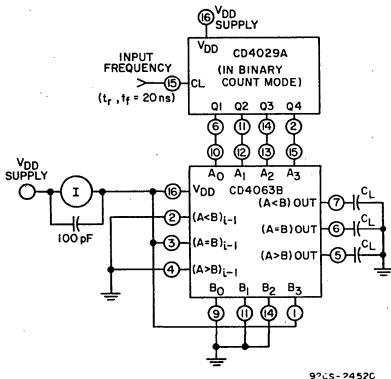
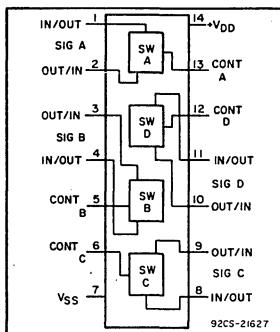


Fig. 13—Dynamic power dissipation test circuit.



# Digital Integrated Circuits

Monolithic Silicon

**CD4066AD CD4066AE  
CD4066AK CD4066AH**


## COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

### Applications:

- Analog signal switching/multiplexing
  - Signal gating Modulator
  - Squelch control Demodulator
  - Chopper Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

RCA-CD4066A is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016A, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V<sub>SS</sub> when the switch is OFF. This configuration minimizes the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016A is recommended.

The CD4066A is supplied in a 14-lead dual-in-line ceramic package (CD4066AD), in a 14-lead dual-in-line plastic package (CD4066AE), or in a 14-lead ceramic flat pack (CD4066AK). It is also available in chip form (CD4066AH).

### Special Features:

- 15-V digital or  $\pm 7.5$ -V peak-to-peak switching
- 80- $\Omega$  typical ON resistance for 15-V operation
- Switch ON resistance matched to within 5  $\Omega$  over 15-V signal-input range
- ON resistance flat over full peak-to-peak signal range
- High ON/OFF output-voltage ratio: 65 dB typ.  
@ f<sub>IS</sub> = 10 kHz, R<sub>L</sub> = 10 k $\Omega$
- High degree of linearity: < 0.5% distortion typ. @ f<sub>IS</sub> = 1 kHz,  
V<sub>IS</sub> = 5 V<sub>p-p</sub>, V<sub>DD</sub> - V<sub>SS</sub> ≥ 10 V, R<sub>L</sub> = 10 k $\Omega$
- Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance:  
10 pA typ. @ V<sub>DD</sub> - V<sub>SS</sub> = 10 V, T<sub>A</sub> = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10<sup>12</sup>  $\Omega$  typ.
- Low crosstalk between switches:  
-50 dB typ. @ f<sub>IS</sub> = 0.9 MHz, R<sub>L</sub> = 1 k $\Omega$
- Matched control-input to signal-output capacitance:  
Reduces output signal transients
- Frequency response, switch ON = 40 MHz (typ.)

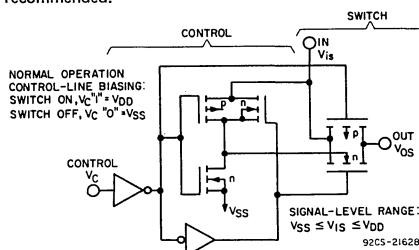


Fig. 1 — Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

**ELECTRICAL CHARACTERISTICS (All inputs . . . . .  $V_{SS} \leq V_I \leq V_{DD}$ )**  
**(Recommended DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . . 3 to 15 V)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS																		
			CD4066AD, CD4066AK																								
			-55°C		25°C		125°C																				
			Typ.	Max.	Typ.	Max.	Typ.	Max.																			
Quiescent Dissipation per Package All Switches OFF	$P_T$	<table border="1"> <thead> <tr> <th colspan="2">TERMINALS</th> <th>VOLTS APPLIED</th> </tr> </thead> <tbody> <tr> <td><math>V_{DD}</math></td> <td>14</td> <td>+ 10</td> </tr> <tr> <td><math>V_{SS}</math></td> <td>7</td> <td>GND</td> </tr> <tr> <td><math>V_C</math></td> <td>5,6,12,13</td> <td>GND</td> </tr> <tr> <td><math>V_{is}</math></td> <td>1,4,8,11</td> <td><math>\leq + 10</math></td> </tr> <tr> <td><math>V_{os}</math></td> <td>2,3,9,10</td> <td><math>\leq + 10</math></td> </tr> </tbody> </table>	TERMINALS		VOLTS APPLIED	$V_{DD}$	14	+ 10	$V_{SS}$	7	GND	$V_C$	5,6,12,13	GND	$V_{is}$	1,4,8,11	$\leq + 10$	$V_{os}$	2,3,9,10	$\leq + 10$	—	5	0.1	5	—	300	$\mu\text{W}$
TERMINALS		VOLTS APPLIED																									
$V_{DD}$	14	+ 10																									
$V_{SS}$	7	GND																									
$V_C$	5,6,12,13	GND																									
$V_{is}$	1,4,8,11	$\leq + 10$																									
$V_{os}$	2,3,9,10	$\leq + 10$																									
—	5	0.1	5	—	300	$\mu\text{W}$																					
All Switches ON		<table border="1"> <thead> <tr> <th colspan="2">TERMINALS</th> <th>VOLTS APPLIED</th> </tr> </thead> <tbody> <tr> <td><math>V_{DD}</math></td> <td>14</td> <td>+ 10</td> </tr> <tr> <td><math>V_{SS}</math></td> <td>7</td> <td>GND</td> </tr> <tr> <td><math>V_C</math></td> <td>5,6,12,13</td> <td>+ 10</td> </tr> <tr> <td><math>V_{is} = V_{os}</math></td> <td>1,4,8,11</td> <td><math>\leq + 10</math> (T<sub>TR,ru</sub> 100 <math>\Omega</math>)</td> </tr> </tbody> </table>	TERMINALS		VOLTS APPLIED	$V_{DD}$	14	+ 10	$V_{SS}$	7	GND	$V_C$	5,6,12,13	+ 10	$V_{is} = V_{os}$	1,4,8,11	$\leq + 10$ (T <sub>TR,ru</sub> 100 $\Omega$ )	—	5	0.1	5	—	300	$\mu\text{W}$			
TERMINALS		VOLTS APPLIED																									
$V_{DD}$	14	+ 10																									
$V_{SS}$	7	GND																									
$V_C$	5,6,12,13	+ 10																									
$V_{is} = V_{os}$	1,4,8,11	$\leq + 10$ (T <sub>TR,ru</sub> 100 $\Omega$ )																									

SIGNAL INPUTS ( $V_{is}$ ) AND OUTPUTS ( $V_{os}$ )

ON Resistance	$R_{ON}$	$R_L = 10 \text{ k}\Omega$	$V_C = V_{DD}$	$V_{SS}$	$V_{is}$						
			+7.5 V	-7.5 V	-7.5 V to +7.5 V	60	220	80	280	145	
			+15 V	0 V	0 to +15 V	85	400	120	500	190	
			+5 V	-5 V	-5 V to +5 V	160	3000	270	5000	360	
			+10 V	0 V	0 to +10 V					550	
			+2.5 V	-2.5 V	-2.5 V to +2.5 V					5500	
			+5 V	0 V	0 to +5 V						
			+7.5 V or +15 V	-7.5 V or 0 V	+7.5 to -7.5 V or +15 to 0 V	—	—	5	—	—	
$\Delta$ ON Resistance Between Any 2 of 4 Switches	$\Delta R_{ON}$	$R_L = 10 \text{ k}\Omega$	+5 V or +10 V	-5 V or 0 V	+5V to -5V or +10V to 0V	—	—	10	—	—	
			+5 V or +10 V	-5 V or 0 V	+5V to -5V or +10V to 0V	—	—	—	—	—	
			$R_L = 10 \text{ k}\Omega$ $f_{is} = 1 \text{ kHz}$	+5 V	-5 V	5 V (p-p)▲	—	—	0.4	—	—
			$V_{DD}$ +7.5 V	$V_C = V_{SS}$ -7.5 V	$V_{is}$ ±7.5 V	—	* ±100	±0.1	* ±100	—	* ±200
Input or Output Leakage—Switch OFF (Effective OFF Resistance)			+5 V	-5 V	±5 V	—	±100*	±0.01	±100*	—	±200*
			$V_C = V_{DD} = +5\text{V}$	$V_{SS} = -5\text{V}$	$V_{os}$ $20 \log_{10} \frac{V_{os}}{V_{is}} = -3 \text{ dB}$	—	—	40	—	—	MHz
Frequency Response—Switch ON (Sine Wave Input)		$R_L = 1 \text{ k}\Omega$	$V_{DD} = +5\text{V}$	$V_C = V_{SS} = -5\text{V}$	$V_{os}$ $20 \log_{10} \frac{V_{os}}{V_{is}} = -50 \text{ dB}$	—	—	1.25	—	—	MHz
Feedthrough Switch OFF		$V_{is} = 5 \text{ V (p-p)}$	$V_C(A) = V_{DD} = +5\text{V}$	$V_C(B) = V_{SS} = -5\text{V}$	$V_{os}(B)$ $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50 \text{ dB}$	—	—	0.9	—	—	MHz
Crosstalk Between any 2 of the 4 switches (Frequency at -50 dB)		$R_L = 1 \text{ k}\Omega$ $V_{is}(A) = 5 \text{ V (p-p)}$	$V_{DD} = +5 \text{ V}$ , $V_C = V_{SS} = -5 \text{ V}$			—	—	—	—	—	MHz
Capacitance Input	$C_{IS}$					—	—	8	—	—	pF
Output	$C_{OS}$					—	—	8	—	—	
Feedthrough	$C_{IOS}$					—	—	0.5	—	—	
Propagation Delay Signal Input to Signal Output	$t_{pd}$		$V_C = V_{DD} = +10 \text{ V}$ , $V_{SS} = \text{GND}$ , $C_L = 15 \text{ pF}$	$V_{is} = 10 \text{ V}$ (square wave)	$t_f = t_i = 20 \text{ ns}$ (input signal)	—	—	10	—	—	ns

**ELECTRICAL CHARACTERISTICS (All inputs . . . . . V<sub>SS</sub> ≤ V<sub>I</sub> ≤ V<sub>DD</sub>)**  
 (Recommended DC Supply Voltage (V<sub>DD</sub>-V<sub>SS</sub>). . . . . 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	
			CD4066AD, CD4066AK							
			-55°C	25°C	125°C	Typ.	Max.	Typ.		
			Typ.	Max.	Typ.	Max.	Typ.	Max.		
Control (V <sub>C</sub> )										
Noise Immunity ■	V <sub>NL</sub>	V <sub>IS</sub> ≤ V <sub>DD</sub>	V <sub>DD</sub> -V <sub>SS</sub> = 10 V I <sub>IS</sub> = 10 μA	-	-	4.5	-	-	V	
Input Current	I <sub>C</sub>		V <sub>DD</sub> -V <sub>SS</sub> = 10 V V <sub>C</sub> ≤ V <sub>DD</sub> -V <sub>SS</sub>	-	-	±10	-	-	pA	
Average Input Capacitance	C <sub>C</sub>			-	-	5	-	-	pF	
Crosstalk Control Input to Signal Output		V <sub>DD</sub> -V <sub>SS</sub> =10V V <sub>C</sub> = 10 V (square wave)	R <sub>L</sub> = 10 kΩ	-	-	50	-	-	mV	
Propagation Delays	t <sub>PD</sub> C	t <sub>RC</sub> = t <sub>TC</sub> = 20 ns	R <sub>L</sub> = 300Ω V <sub>IS</sub> ≤ 10V, C <sub>L</sub> = 15 pF	-	-	35	-	-	ns	
Maximum Allowable Control Input Repetition Rate		V <sub>DD</sub> = 10 V, V <sub>SS</sub> = GND, R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 15 pF V <sub>C</sub> = 10 V (square wave) t <sub>r</sub> = t <sub>f</sub> = 20 ns		-	-	10	-	-	MHz	

\* Limit determined by minimum feasible leakage measurement for automatic testing.

■ Minimum value for all temperatures shown is 2 V.

△ Symmetrical about 0 volts.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	
			CD4066AE							
			-40°C	25°C	85°C	Typ.	Max.	Typ.		
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.		
Quiescent Dissipation per Package All Switches OFF		V <sub>DD</sub> 14 + 10 V <sub>SS</sub> 7 GND V <sub>C</sub> 5.6, 12, 13 GND V <sub>IS</sub> 1.4, 8, 11 ≤ +10 V <sub>OS</sub> 2, 3, 9, 10 ≤ +10	-	50	0.1	50	-	300	μW	
All Switches ON	P <sub>T</sub>	V <sub>DD</sub> 14 + 10 V <sub>SS</sub> 7 GND V <sub>C</sub> 5.6, 12, 13 + 10 V <sub>IS</sub> = V <sub>OS</sub> 1.4, 8, 11 ≤ +10 (T <sub>kr</sub> = 100 Ω)	-	50	0.1	50	-	300	μW	

**SIGNAL INPUTS (V<sub>IS</sub>) AND OUTPUTS (V<sub>OS</sub>)**

ON Resistance	R <sub>ON</sub>	R <sub>L</sub> = 10 kΩ	V <sub>C</sub> =V <sub>DD</sub>	V <sub>SS</sub>	V <sub>IS</sub>	80 250 80 280 130 300 100 450 120 500 170 520 190 3500 270 5000 330 5200	Ω		
			+7.5 V	-7.5 V	-7.5 V to +7.5 V				
			+15 V	0 V	0 to +15 V				
			+5 V	-5 V	-5 V to +5 V				
			+10 V	-0 V	0 to +10 V				
			+2.5 V	-2.5 V	-2.5 V to +2.5 V				
			+5 V	0 V	0 to +5 V				
			+7.5 V or +15 V	-7.5 V or 0 V	+7.5 to -7.5 V to 0 V				
ΔON Resistance Between Any 2 of 4 Switches	ΔR <sub>ON</sub>	R <sub>L</sub> = 10 kΩ	+5 V or +10 V	-5 V or 0 V	+5V to -5V to 0V				
			+5 V	-5 V	+10V to 0V				
Sine Wave Response (Distortion)		R <sub>L</sub> = 10 kΩ f <sub>IS</sub> = 1 kHz	+5 V	-5 V	5 V (p-p) ▲	-	0.4	-	%

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS						UNITS	
			CD4066AE							
			-40°C		25°C		85°C			
			Typ.	Max.	Typ.	Max.	Typ.	Max.		
Input or Output Leakage—Switch OFF (Effective OFF Resistance)		$V_{DD} = +5 \text{ V}$ $V_C = V_{SS} = -5 \text{ V}$ $V_{IS} = 5 \text{ V} (\text{p-p})$	—	$\pm 100^*$	$\pm 0.1$	$\pm 100^*$	—	$\pm 200$	nA	
Frequency Response— Switch ON (Sine Wave Input)		$R_L = 1 \text{ k}\Omega$ $V_{IS} = 5 \text{ V} (\text{p-p})$	$V_C = V_{DD} = +5 \text{ V}$ $V_{OS} = -5 \text{ V}$ $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -3 \text{ dB}$	—	40	—	—	—	MHz	
Feedthrough Switch OFF			$V_{DD} = +5 \text{ V}$ , $V_C = V_{SS} = -5 \text{ V}$ $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -50 \text{ dB}$	—	—	1.25	—	—	MHz	
Crosstalk Between any 2 of the 4 switches (Frequency at -50 dB)		$R_L = 1 \text{ k}\Omega$ $V_{IS} (\text{A}) = 5 \text{ V} (\text{p-p})$	$V_C(\text{A}) = V_{DD} = +5 \text{ V}$ $V_C(\text{B}) = V_{SS} = -5 \text{ V}$ $20 \log_{10} \frac{V_{OS}(\text{B})}{V_{IS}(\text{A})} = -50 \text{ dB}$	—	—	0.9	—	—	MHz	
Capacitance	Input	$C_{IS}$	$V_{DD} = +5 \text{ V}$ , $V_C = V_{SS} = -5 \text{ V}$	—	—	8	—	—	pF	
	Output	$C_{OS}$		—	—	8	—	—		
	Feedthrough	$C_{IOS}$		—	—	0.5	—	—		
Propagation Delay Signal Input to Signal Output	$t_{pd}$		$V_C = V_{DD} = +10 \text{ V}$ , $V_{SS} = \text{GND}$ , $C_L = 15 \text{ pF}$ $V_{IS} = 10 \text{ V}$ (square wave) $t_r = t_f = 20 \text{ ns}$ (input signal)	—	—	10	—	—	ns	
Control ( $V_C$ )										
Noise Immunity	$V_{NL}$		$V_{DD} - V_{SS} = 10 \text{ V}$ $I_{IS} = 10 \mu\text{A}$	—	—	4.5	—	—	V	
Input Current	$I_C$	$V_{IS} \leq V_{DD}$	$V_{DD} - V_{SS} = 10 \text{ V}$ $V_C \leq V_{DD} - V_{SS}$	—	—	$\pm 10$	—	—	pA	
Average Input Capacitance	$C_C$			—	—	5	—	—	pF	
Crosstalk Control Input to Signal Output			$V_{DD} - V_{SS} = 10 \text{ V}$ $V_C = 10 \text{ V}$ (square wave) $t_{RC} = t_{FC} = 20 \text{ ns}$	$R_L = 10 \text{ k}\Omega$	—	—	50	—	mV	
Propagation Delays	$t_{pdC}$			$R_L = 300 \Omega$ $V_{IS} \leq 10 \text{ V}$ , $C_L = 15 \text{ pF}$	—	—	35	—	ns	
Maximum Allowable Control Input Repetition Rate			$V_{DD} = 10 \text{ V}$ , $V_{SS} = \text{GND}$ , $R_L = 1 \text{ k}\Omega$ $C_L = 15 \text{ pF}$ $V_C = 10 \text{ V}$ (square wave) $t_r = t_f = 20 \text{ ns}$		—	—	10	—	MHz	

\* Limit determined by minimum feasible leakage measurement for automatic testing.

▲ Symmetrical about 0 volts.

■ Minimum value for all temperatures shown is 2 V.

**MAXIMUM RATINGS, Absolute-Maximum Values:**STORAGE TEMPERATURE RANGE . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$ 

OPERATING TEMPERATURE RANGE:

Ceramic Packages . . . . .  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ Plastic Packages . . . . .  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ 

DISSIPATION PER PACKAGE . . . . . 200 mW

DC SUPPLY VOLTAGES:

 $V_{DD} - V_{SS}$ ;  $V_{DD} - V_{EE}$  . . . . . -0.5 to +15 VALL SIGNAL AND DIGITAL CONTROL INPUTS .  $V_{SS} \leq V_I \leq V_{DD}$ **MINIMUM RECOMMENDED POWER SUPPLY VOLTAGES** $V_{DD} - V_{SS}$ ;  $V_{DD} - V_{EE}$  . . . . . 3 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$  mm)  
from case for 10 seconds max.. . . . .  $265^\circ\text{C}$ **SPECIAL CONSIDERATIONS — CD4066A**

1. In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from CD4066A.

2. In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from  $R_{ON}$  values shown).

No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the signal.

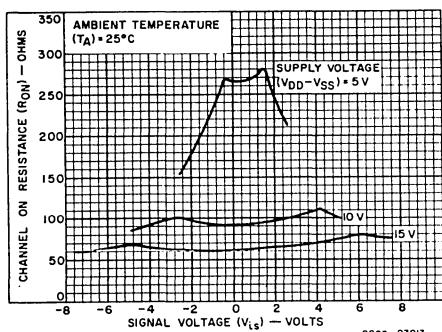


Fig.2 (a) — Typical channel ON resistance vs. signal voltage for three values of supply voltage ( $V_{DD} - V_{SS}$ ).

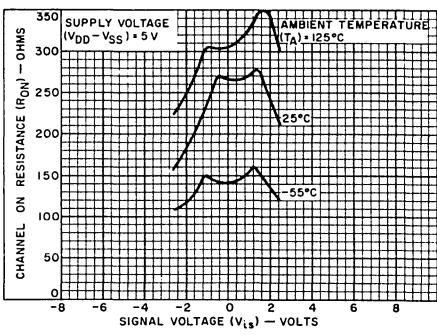


Fig.2 (b) — Typical channel ON resistance vs. signal voltage with supply voltage ( $V_{DD} - V_{SS}$ ) = 5 V.

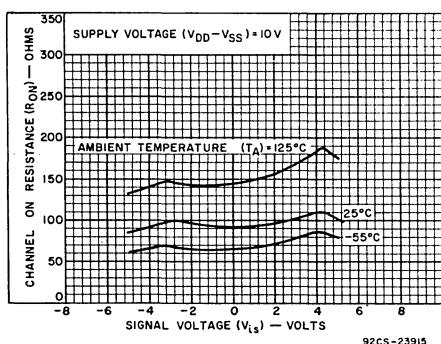


Fig.2 (c) — Typical channel ON resistance vs. signal voltage with supply voltage ( $V_{DD} - V_{SS}$ ) = 10 V.

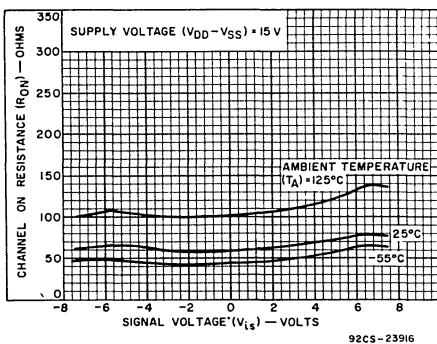


Fig.2 (d) — Typical channel ON resistance vs. signal voltage with supply voltage ( $V_{DD} - V_{SS}$ ) = 15 V.

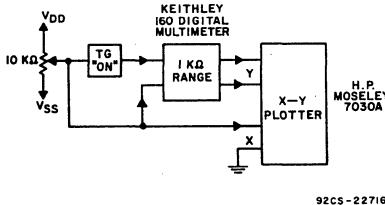


Fig.3 — Channel ON resistance measurement circuit.

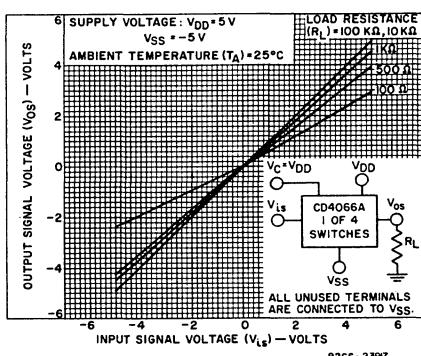
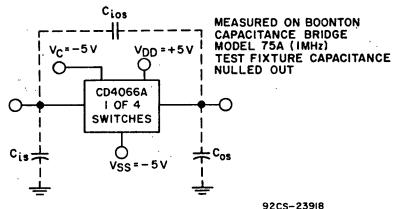
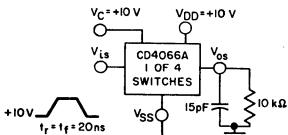


Fig.4 — Typical ON characteristics for 1 of 4 channels.

## TEST CIRCUITS



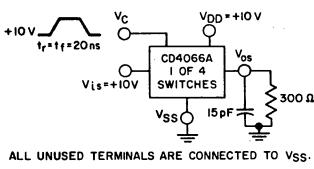
*Fig.5 – Capacitance.*



ALL UNUSED INPUTS ARE CONNECTED TO V<sub>SS</sub>.

**92CS-23920**

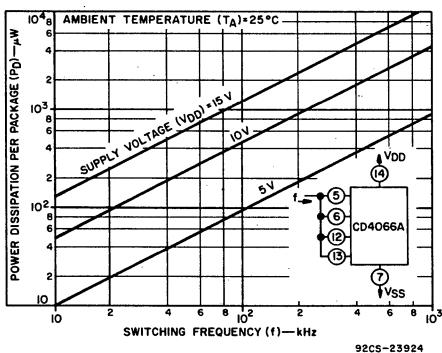
*Fig.7 – Propagation delay time signal input ( $V_{IS}$ ) to signal output ( $V_{OS}$ ).*



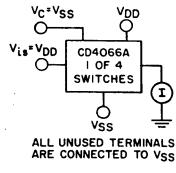
ALL UNUSED TERMINALS ARE CONNECTED TO VSS.

92CS-23922

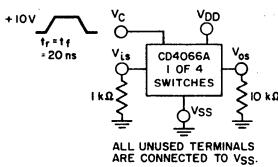
*Fig.9 – Propagation delay  $t_{PI}$ ,  $t_{PHI}$ , control-signal output.*



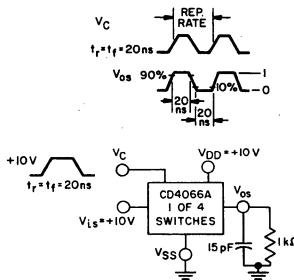
**Fig.11 – Power dissipation per package vs switching frequency.**



*Fig.6 – OFF switch input or output leakage*



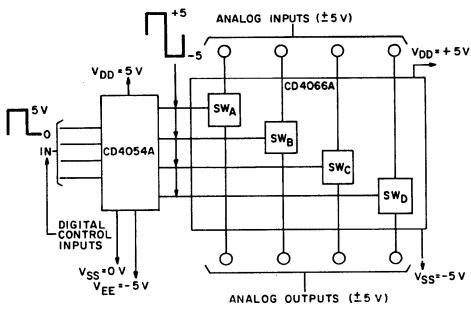
*Fig.8 – Crosstalk-control input to signal output*



ALL UNUSED INPUTS ARE CONNECTED TO V<sub>SS</sub>.

**92CS-23923**

*Fig.10 – Maximum allowable control input repetition rate.*



*Fig.12 – Bidirectional signal transmission via digital control logic.*

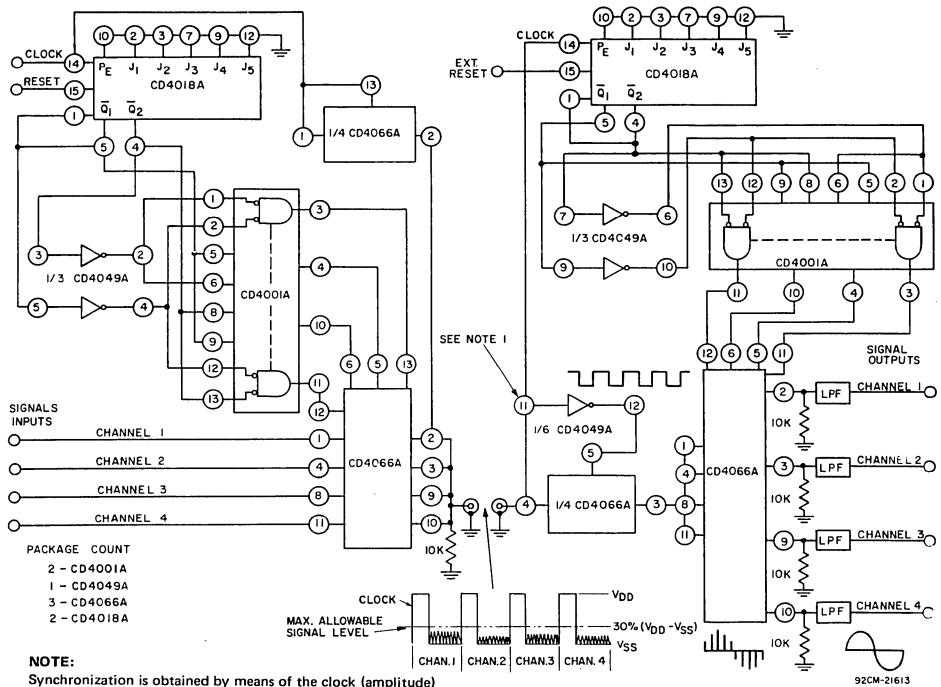
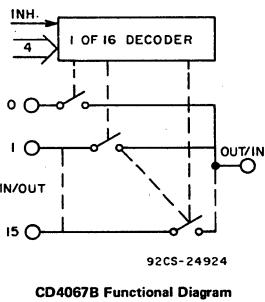


Fig. 13 — 4-channel PAM multiplex system diagram.

**Preliminary CD4067BD**  
**Preliminary CD4097BD**

**Preliminary Data**



## COS/MOS Analog Multiplexers/Demultiplexers

CD4067B—Single 16-Channel Multiplexer/Demultiplexer

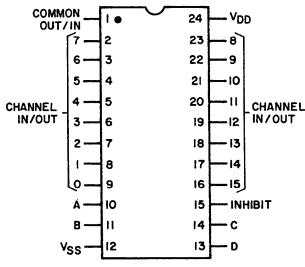
CD4097B—Differential 8-Channel Multiplexer/Demultiplexer

The RCA-CD4067B and -CD4097B COS/MOS analog multiplexers/demultiplexers\* are digitally controlled analog switches having low "on" impedance, low "off" leakage current, and internal address decoding. In addition, the "on" resistance is relatively constant over the full input-signal range. The CD4067B is a 16-channel multiplexer with four binary control inputs, A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch. A logic "1" present at the inhibit input turns all channels off.

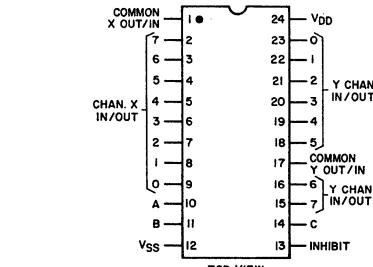
The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

The CD4067B, CD4097B are supplied in a 24-lead dual-in-line welded-seal ceramic package. (CD4067BD, CD4097BD).

\*When the devices are used as demultiplexers, the in/out terminals are the outputs and the common out/in terminal(s) is/are the input(s).



TERMINAL ASSIGNMENTS



ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			TYPICAL VALUES	UNITS			
			$V_{DD}(\text{V})$	$V_{SS}(\text{V})$					
Quiescent Device Current  SIGNAL INPUTS ( $V_{IS}$ ) AND OUTPUTS ( $V_{OS}$ )	$I_L$		5	0	0.1	$\mu\text{A}$			
			10	0	0.2				
			15	0	0.5				
"ON" Resistance (Peak for $V_{SS} \leq V_{IS} \leq V_{DD}$ )									
$\Delta$ "ON" Resistance Between Any 2 Channels	$\Delta R_{ON}$	(Any Channel Selected)	$R_L = 10 \text{ k}\Omega$	+7.5	-7.5	$\Omega$			
				+15	0				
				+5	-5				
				+10	0				
				+2.5	-2.5				
				+5	0				
				+7.5	-7.5				
Sine Wave Distortion		$R_L = 10 \text{ k}\Omega$ $f_{IS} = 1 \text{ kHz}$ $5 \text{ V (p-p)}^{\Delta}$		+15	0	$\%$			
"OFF" Any Channel OFF				+5	-5				
Channel Leakage Current				+2.5	-2.5				
All Channels	CD4067B	Inhibit = +5 V		+5	-5	$\text{nA}$			
OFF (Output)	CD4097B			+5	-5				
+5	-5			+5	-5				
Frequency Response— Channel "ON" (Sine Wave Input)		$R_L = 1 \text{ k}\Omega$ $V_{IS} = 5 \text{ V (p-p)}$ $C_L = 10 \text{ pF}$		$V_C = V_{DD} = +5 \text{ V}$ , $V_{SS} = -5 \text{ V}$ , $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -3 \text{ dB}$	40	$\text{MHz}$			
Feedthrough Channel "OFF"				$V_{DD} = +5 \text{ V}$ , $V_C = V_{SS} = -5 \text{ V}$ , $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -40 \text{ dB}$	1				
Crosstalk Between Any 2 of the 16 Switches (Frequency at -40 dB)		$R_L = 1 \text{ k}\Omega$ $V_{IS} (\text{A}) = 5 \text{ V (p-p)}$ $C_L = 10 \text{ pF}$		$V_C (\text{A}) = V_{DD} = +5 \text{ V}$ , $V_C (\text{B}) = V_{SS} = -5 \text{ V}$ , $20 \log_{10} \frac{V_{OS} (\text{B})}{V_{IS} (\text{A})} = -40 \text{ dB}$	1	$\text{MHz}$			
Capacitance	Input	$C_{IS}$		+5	-5	5	$\text{pF}$		
	Output (Common OUT/IN)	$C_{OS}$		CD4067B		60			
	Feedthrough	$C_{IOS}$		CD4097B		30			
Propagation Delay: Signal Input to Signal Output		$t_{PLH}, t_{PHL}$		0.2					
				30		ns			

▲ Symmetrical about 0 volts.

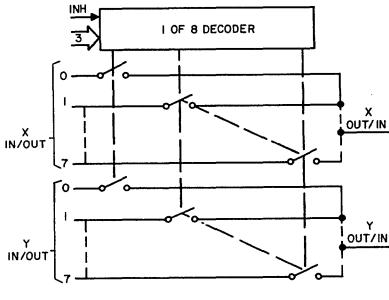
## ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
			V <sub>DD</sub> -V <sub>SS</sub> (V)		
<b>CONTROL (V<sub>C</sub>) INPUTS A, B, C, D AND Inhibit</b>					
Noise Immunity	V <sub>NL</sub> , V <sub>NH</sub>	I <sub>is</sub> = 10 $\mu$ A R <sub>L</sub> = 1 k $\Omega$ V <sub>is</sub> = V <sub>DD</sub> through 1 k $\Omega$	15	6.75	V
			10	4.5	
			5	2.25	
Average Input Capacitance	C <sub>C</sub>		10	5	pF
Turn-On Propagation Delay: Control Input to Signal Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 10 k $\Omega$ V <sub>C</sub> = V <sub>DD</sub> (square) V <sub>is</sub> $\leq$ V <sub>DD</sub> t <sub>r</sub> , t <sub>f</sub> = 20 ns	15	140	ns
			10	200	
			5	400	
			15	140	
			10	200	
			5	400	
			10	200	
			5	400	
Inhibit Recovery Time *			10	200	ns

\* Time after Inhibit is removed during which channel information is valid.

CD4067B TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15



CD4097B Functional Diagram

## SPECIAL CONSIDERATIONS

1. In applications where separate power sources are used to drive V<sub>DD</sub> and the signal inputs, the V<sub>DD</sub> current capability should exceed V<sub>DD</sub>/R<sub>L</sub> (R<sub>L</sub> = effective external load). This provision avoids any permanent current flow or clamp action on the V<sub>DD</sub> supply when power is applied or removed from the CD4067B, CD4097B.
2. In certain applications, the external load-resistor current may include both V<sub>DD</sub> and signal-line components. To avoid drawing V<sub>DD</sub> current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R<sub>ON</sub> values shown).

No V<sub>DD</sub> current will flow through R<sub>L</sub> if the switch current flows into terminal 1 on the CD4067B; terminals 1 and 17 on the CD4097B.

CD4097B TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

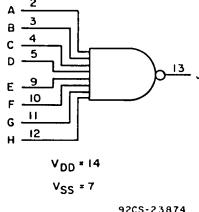


## Digital Integrated Circuits

Monolithic Silicon

## CD4068B Types

## COS/MOS 8-Input NAND Gate



CD4068B Functional Diagram

The RCA-CD4068B NAND gate provides the system designer with direct implementation of the positive-logic 8-input NAND function and supplements the existing family of COS/MOS gates.

This device has equal source- and sink-current capabilities and

## Features:

- Medium-Speed Operation —  $t_{PHL} = 130$  ns,  $t_{PLH} = 100$  ns (typ.) at 10 V
- Standard B-Series Output Drive

conforms to standard B-series output drive (see Static Electrical Characteristics).

The CD4068B is supplied in a 14-lead dual-in-line welded-seal ceramic package (D), plastic package (E), ceramic package (F), flat package (K), and in chip form (H).

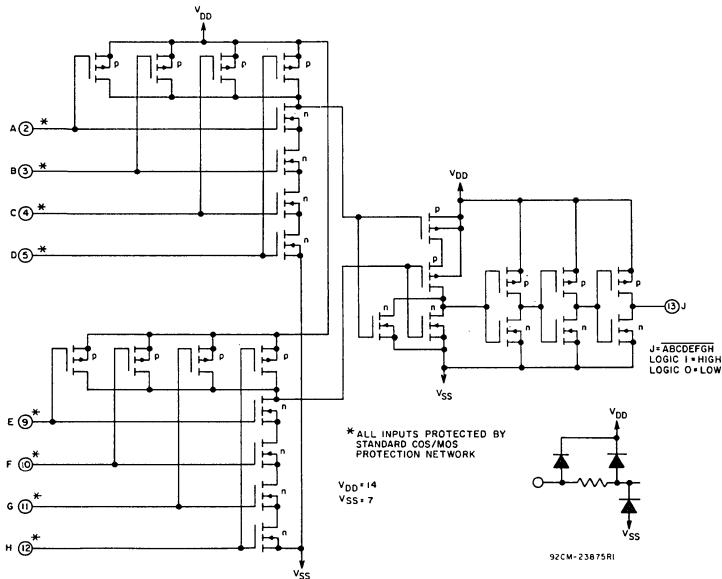


Fig. 1—CD4068B schematic diagram.

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4068BD CD4068BK CD4068BH CERAMIC PACKAGE LIMITS									UNITS	FIG. NO.		
		VO Volts	VDD Volts	-55°C			25°C			125°C						
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	IL	5	—	—	0.5	—	0.01	0.5	—	—	30	—	μA	13		
			10	—	—	1	—	0.01	1	—	—	60				
			15	—	—	—	—	0.01	—	—	—	—				
Output Voltage Low-Level	VOL	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—		
			10	—	—	0.01	—	0	0.01	—	—	0.05				
			15	—	—	—	—	0	—	—	—	—				
High-Level	VOH	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—		
			10	9.99	—	—	9.99	10	—	9.95	—	—				
			15	—	—	—	—	15	—	—	—	—				
Noise Immunity	VNL	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	14		
		9	10	3	—	—	3	4.5	—	2.9	—	—				
		13.5	15	—	—	—	—	6.75	—	—	—	—				
	VNH	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—				
		1	10	2.9	—	—	3	4.5	—	3	—	—				
		1.5	15	—	—	—	—	6.75	—	—	—	—				
Output Drive Current: N-Channel (Sink)	IDN	0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	—	mA	4, 5		
			0.5	10	1.1	—	—	0.9	1.8	—	0.65	—	—			
			1.5	15	—	—	—	3	6	—	—	—				
P-Channel (Source)	IDP	2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—	—	mA	6, 7		
		4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—	—				
		9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—	—				
		13.5	15	—	—	—	-3	-6	—	—	—	—				
Input Current	II	15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	—	μA	—		

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE:

CERAMIC-PACKAGE TYPES ..... -55 to +125°C

PLASTIC-PACKAGE TYPES ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE

V<sub>DD</sub>\* ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)

from case for 10 seconds max. ..... 265°C

\* All voltage values are referenced to V<sub>SS</sub> terminal.OPERATING CONDITIONS AT T<sub>A</sub> = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	—	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	-0.5 V to V <sub>DD</sub> + 0.5 V	V	—

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4068BE PLASTIC PACKAGE LIMITS								UNITS	FIG. NO.	
		VO Volts	V <sub>DD</sub> Volts	-40°C			25°C			85°C				
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	I <sub>L</sub>	5 10 15	— — —	—	—	5	—	0.01	5	—	—	70	μA	13
				—	—	10	—	0.01	10	—	—	140		
				—	—	—	—	0.01	—	—	—	—		
Output Voltage: Low-Level	V <sub>OL</sub>	5 10 15	— — —	—	0.01	—	0	0.01	—	—	—	0.05	V	—
				—	0.01	—	0	0.01	—	—	—	0.05		
				—	—	—	0	—	—	—	—	—		
High-Level	V <sub>OH</sub>	5 10 15	4.99 9.99 —	—	—	4.99	5	—	4.95	—	—	—	—	—
				—	—	9.99	10	—	9.95	—	—	—		
				—	—	—	15	—	—	—	—	—		
Noise Immunity	V <sub>NL</sub>	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	14
		9	10	3	—	—	3	4.5	—	2.9	—	—		
		13.5	15	—	—	—	6.75	—	—	—	—	—		
	V <sub>NH</sub>	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—		
		1	10	2.9	—	—	3	4.5	—	3	—	—		
		1.5	15	—	—	—	6.75	—	—	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4 0.5 1.5	5 10 15	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	4, 5
				1	—	—	0.9	1.8	—	0.75	—	—		
				—	—	3	6	—	—	—	—	—		
P-Channel (Source)	I <sub>DP</sub>	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	6, 7
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—		
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—		
		13.5	15	—	—	—	-3	-6	—	—	—	—		
Input Current	I <sub>I</sub>	15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, and C<sub>L</sub> = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
		V <sub>DD</sub> Volts	Typ.	Max.				
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>			5 10 15	325 130 100	650 260 —	ns	8, 10
Low-to-High Level	t <sub>PLH</sub>			5 10 15	250 100 75	500 200 —	ns	9, 10
Transition Time	t <sub>THL</sub> t <sub>TLH</sub>			5 10 15	100 50 40	200 100 80	ns	11
Average Input Capacitance	C <sub>I</sub>	Any Input		5	—	pF	—	

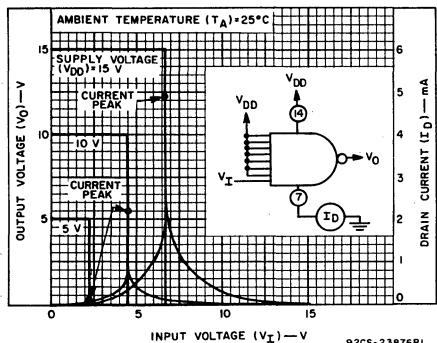


Fig. 2—Typical voltage and current transfer characteristics.

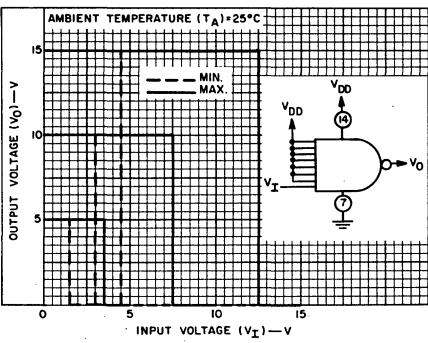


Fig. 3—Min. and max. voltage transfer characteristics.

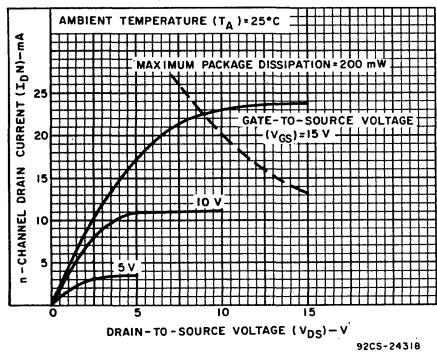


Fig. 4—Typical output-N-channel drain characteristics.

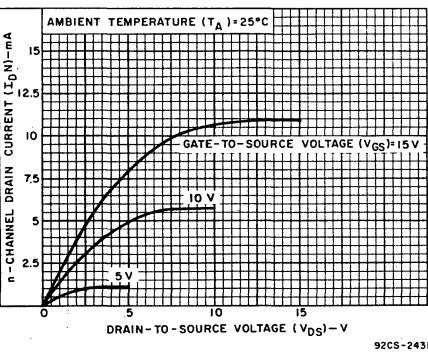


Fig. 5—Minimum output-N-channel drain characteristics.

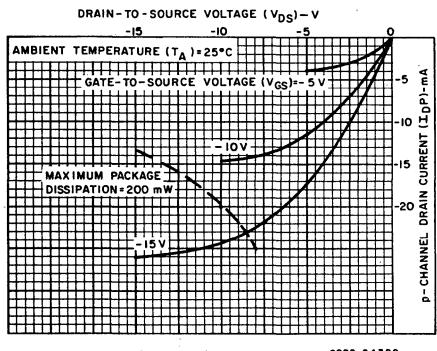


Fig. 6—Typical output-P-channel drain characteristics.

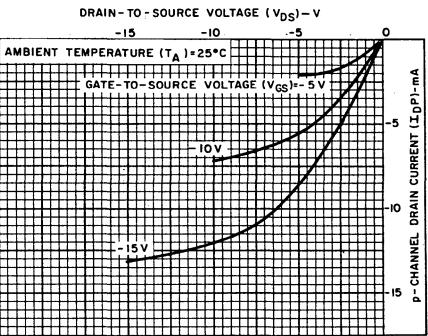


Fig. 7—Minimum output-P-channel drain characteristics.

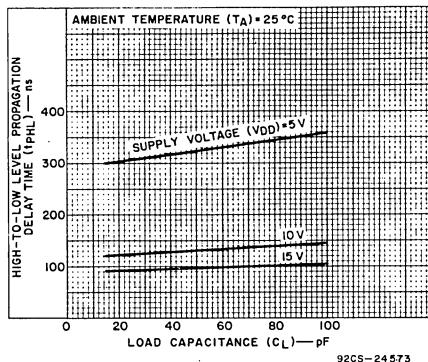


Fig. 8—Typical high-to-low level propagation delay time vs. load capacitance.

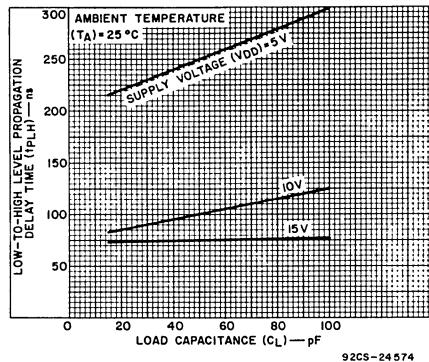


Fig. 9—Typical low-to-high level propagation delay time vs. load capacitance.

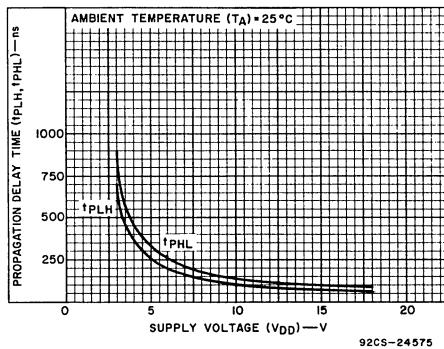


Fig. 10—Typical propagation delay time vs. supply voltage.

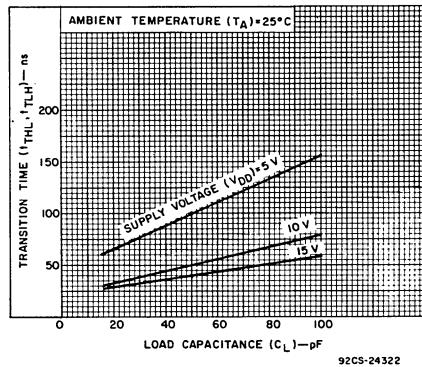


Fig. 11—Typical transition time vs. load capacitance.

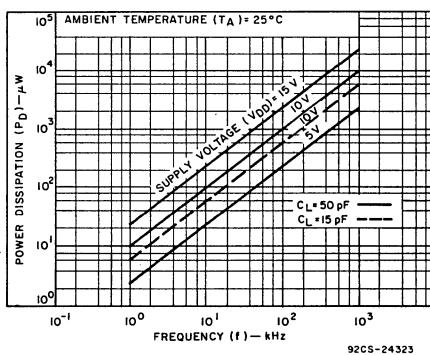


Fig. 12—Typical power dissipation vs. frequency.

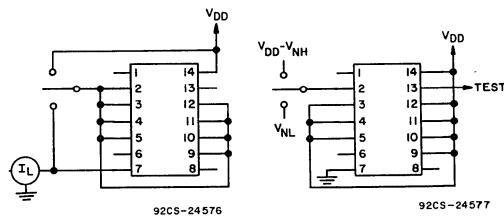


Fig. 13—Quiescent device current test circuit.

Fig. 14—Noise immunity test circuit.



## STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	SYMBOL	TEST CONDI-TIONS		CD4069BD, BF, BK, BH CERAMIC PACKAGE LIMITS								UNITS	FIG. NO.	
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-55°C			25°C			125°C				
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	I <sub>L</sub>	5	—	—	0.5	—	0.01	0.5	—	—	30	—	μA	17
		10	—	—	1	—	0.01	1	—	—	60	—		
		15	—	—	—	—	0.01	—	—	—	—	—		
Output Voltage: Low-Level	V <sub>OL</sub>	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—
		10	—	—	0.01	—	0	0.01	—	—	0.05	—		
		15	—	—	—	—	0	—	—	—	—	—		
High-Level	V <sub>OH</sub>	5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	—
		10	9.99	—	—	9.99	10	—	9.95	—	—	—		
		15	—	—	—	—	15	—	—	—	—	—		
Noise Immunity	V <sub>NL</sub>	3.6	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	18
		7.2	10	3	—	—	3	4.5	—	2.9	—	—		
		10.8	15	—	—	—	—	6.75	—	—	—	—		
	V <sub>NH</sub>	1.4	5	1.4	—	—	1.5	2.25	—	1.5	—	—		
		2.8	10	2.9	—	—	3	4.5	—	3	—	—		
		4.2	15	—	—	—	—	6.75	—	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	—	mA	5, 6
		0.5	10	1.1	—	—	0.9	1.8	—	0.65	—	—		
		1.5	15	—	—	—	3	6	—	—	—	—		
P-Channel (Source)	I <sub>DP</sub>	2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—	—	mA	7, 8
		4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—	—		
		9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—	—		
		13.5	15	—	—	—	-3	-6	—	—	—	—		
Input Current	I <sub>I</sub>	15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, and C<sub>L</sub> = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS		UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
		V <sub>DD</sub> Volts		Typ.	Max.		
Propagation Delay Time:	t <sub>PHL</sub> , t <sub>PLH</sub>	5	65	125	—	ns	9, 10
		10	40	80	—		
		15	30	—	—		
Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	5	100	200	—	ns	11
		10	50	100	80		
		15	40	—	—		
Average Input Capacitance	C <sub>I</sub>	Any Input	5	—	pF	—	—

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS	CD4069BE PLASTIC PACKAGE LIMITS										UNITS	FIG. NO.	
			-40°C			25°C			85°C						
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>		5	—	—	5	—	0.01	5	—	—	70	μA	17	
			10	—	—	10	—	0.01	10	—	—	140			
			15	—	—	—	—	0.01	—	—	—	—			
Output Voltage: Low-Level	V <sub>OL</sub>		5	—	—	0.01	—	0	0.01	—	—	0.05	V	—	
			10	—	—	0.01	—	0	0.01	—	—	0.05			
			15	—	—	—	—	0	—	—	—	—			
High-Level	V <sub>OH</sub>		5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	
			10	9.99	—	—	9.99	10	—	9.95	—	—			
			15	—	—	—	—	15	—	—	—	—			
Noise Immunity	V <sub>NL</sub>	3.6	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	18	
		7.2	10	3	—	—	3	4.5	—	2.9	—	—			
		10.8	15	—	—	—	—	6.75	—	—	—	—			
	V <sub>NH</sub>	1.4	5	1.4	—	—	1.5	2.25	—	1.5	—	—			
		2.8	10	2.9	—	—	3	4.5	—	3	—	—			
		4.2	15	—	—	—	—	6.75	—	—	—	—			
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	5, 6	
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—			
		1.5	15	—	—	—	3	6	—	—	—	—			
P-Channel (Source)	I <sub>DP</sub>	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	7, 8	
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—			
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—			
		13.5	15	—	—	—	-3	-6	—	—	—	—			
Input Current	I <sub>I</sub>		15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—	

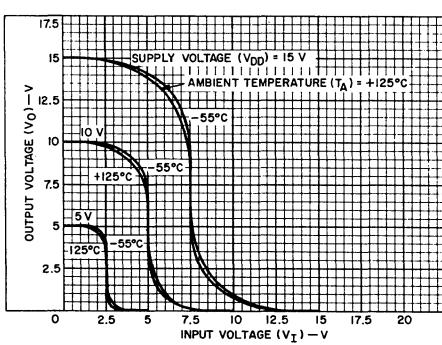
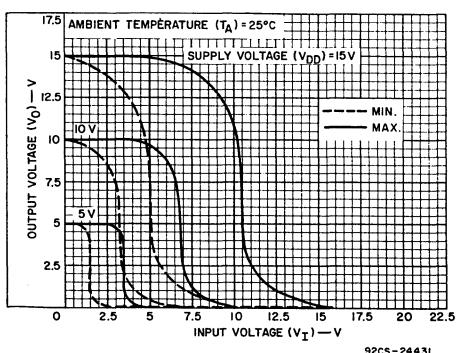


Fig. 2—Min. and max. voltage transfer characteristics.

Fig. 2—Min. and max. voltage transfer characteristics.

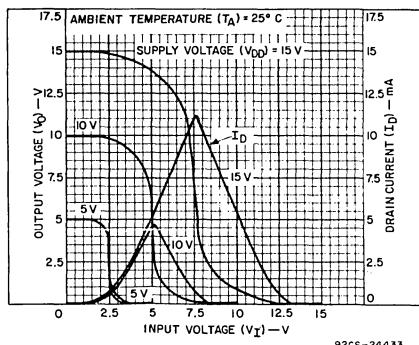


Fig. 4—Typical current and voltage transfer characteristics.

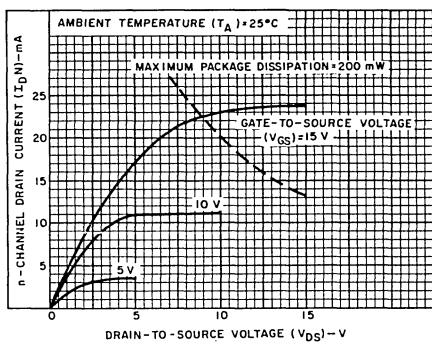


Fig. 5—Typical output-N-channel drain characteristics.

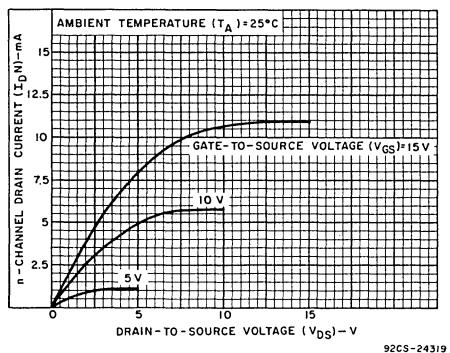


Fig. 6—Minimum output-N-channel drain characteristics.

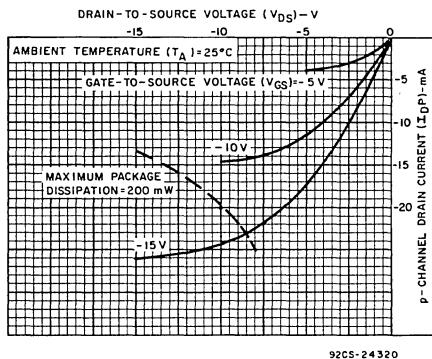


Fig. 7—Typical output-P-channel drain characteristics.

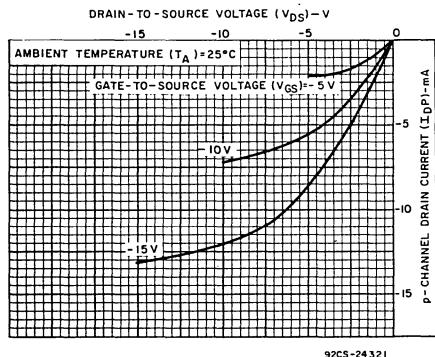


Fig. 8—Minimum output-P-channel drain characteristics.

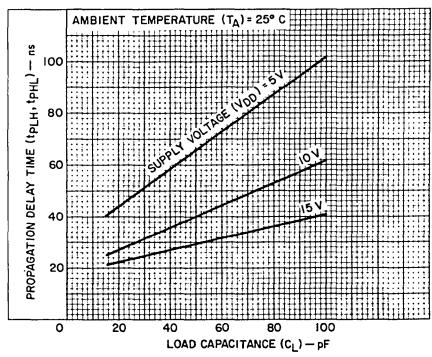


Fig. 9—Typical propagation delay time vs. load capacitance.

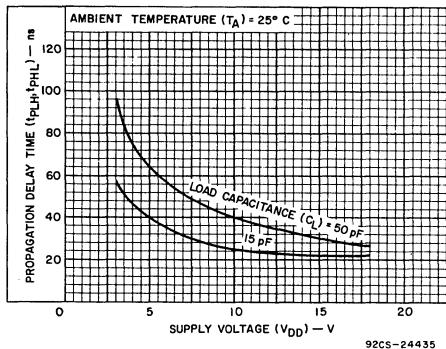


Fig. 10—Typical propagation delay time vs. supply voltage.

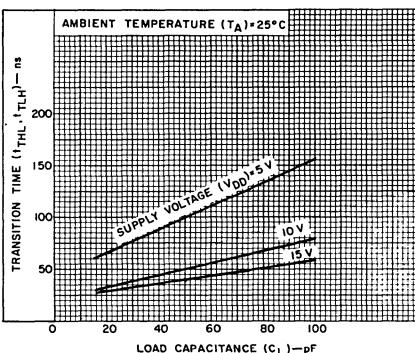


Fig. 11—Typical transition time vs. load capacitance.

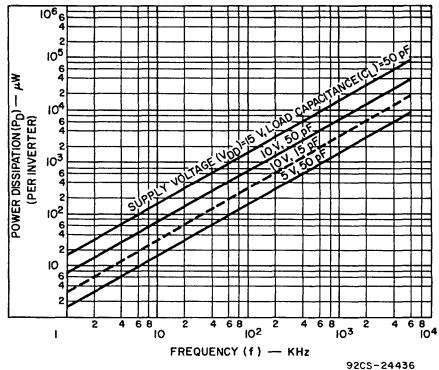


Fig. 12—Typical dynamic power dissipation.

## APPLICATIONS

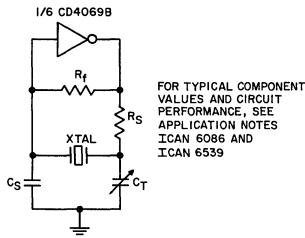


Fig. 13—Typical crystal oscillator circuit.

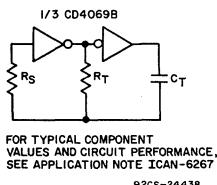


Fig. 14—Typical RC oscillator circuit.

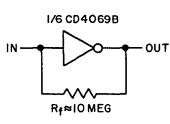


Fig. 15—High-input impedance amplifier.

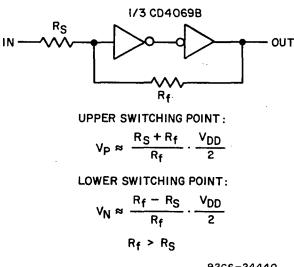


Fig. 16—Input pulse shaping circuit (Schmitt trigger).

## TEST CIRCUITS

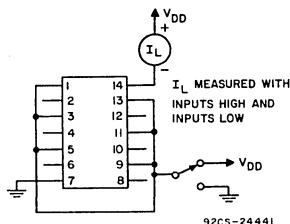


Fig. 17—Quiescent device current.

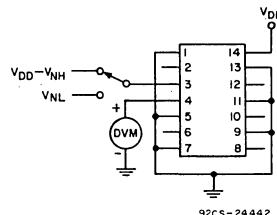


Fig. 18—Noise immunity.

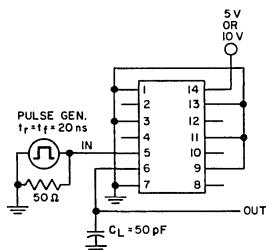
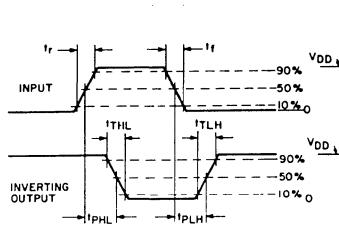
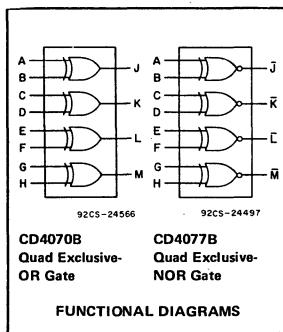


Fig. 19—Dynamic electrical characteristics test circuit and waveforms.

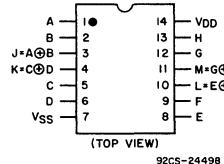


## Preliminary CD4070BE, CD4077BE

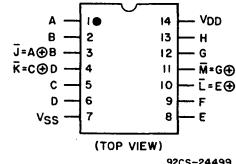


### COS/MOS

**Quad Exclusive-OR Gate—CD4070B**  
**Quad Exclusive-NOR Gate—CD4077B**



TERMINAL ASSIGNMENT  
CD4070B



TERMINAL ASSIGNMENT  
CD4077B

The RCA-CD4070B contains four independent exclusive-OR gates. RCA-CD4077B contains four independent exclusive-NOR gates.

Type CD4070B is pin-for-pin compatible with RCA-CD4030A and in addition has greater current-sourcing capability and a higher input impedance.

The CD4070B and CD4077B are supplied in 14-lead dual-in-line plastic packages.

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE:

(V<sub>DD</sub>\*). ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

ALL INPUTS ..... V<sub>SS</sub> ≤ V<sub>I</sub> ≤ V<sub>DD</sub>

LEAD TEMPERATURE (DURING SOLDERING)

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)  
from case for 10 s max. ..... +265°C

\* All voltage values are referenced to V<sub>SS</sub> terminal.

### OPERATING CONDITIONS AT T<sub>A</sub> = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	-	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	-0.5 V to V <sub>DD</sub> + 0.5 V	V	-

### TRUTH TABLE CD4070B

1 of 4 Gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High Level

" 0 = Low Level

$$J = A \oplus B$$

### TRUTH TABLE CD4077B

1 of 4 Gates

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High Level

" 0 = Low Level

$$\bar{J} = A \oplus B$$

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES CD4070B CD4077B	UNITS
		$V_O$ Volts	$V_{DD}$ Volts		
Quiescent Device Current	$I_L$		5	0.01	$\mu\text{A}$
			10	0.01	
Output Drive Current:  N-Channel (Sink)	$I_{DN}$	$V_I = V_{SS}$	0.4	5	$\text{mA}$
			0.5	10	
			4.6	5	
	$I_{DP}$	$V_I = V_{DD}$	2.5	5	
			9.5	10	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES CD4070B CD4077B	UNITS
		$V_{DD}$ Volts			
Propagation Delay:  High-to-Low	$t_{PHL}$		5	175	$\text{ns}$
			10	70	
Low-to-High	$t_{PLH}$		5	175	$\text{ns}$
			10	70	
Transition Time:  High-to-Low	$t_{THL}$		5	100	$\text{ns}$
			10	50	
Low-to-High	$t_{TLH}$		5	100	$\text{ns}$
			10	50	
Average Input Capacitance	$C_I$	Any Input		5	$\text{pF}$



## STATIC ELECTRICAL CHARACTERISTICS

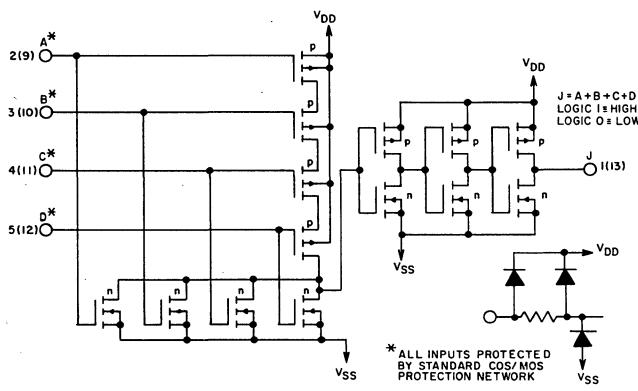
CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4071BD, BF, BK, BH CD4075BD, BF, BK, BH CERAMIC PACKAGE LIMITS								UNITS	FIG. NO.		
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-55°C			25°C			125°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>			5	—	—	5	—	0.01	0.5	—	—	30	μA	15
				10	—	—	10	—	0.01	1	—	—	60		
				15	—	—	—	—	0.01	—	—	—	—		
Output Voltage Low-Level	V <sub>OL</sub>			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
				15	—	—	—	—	0	—	—	—	—		
High-Level	V <sub>OH</sub>			5	4.99	—	—	4.99	5	—	4.95	—	—	V	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
				15	—	—	—	—	15	—	—	—	—		
Noise Immunity	V <sub>NL</sub>		0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	4, 5, 16
			1	10	3	—	—	3	4.5	—	2.9	—	—		
			1.5	15	—	—	—	—	6.75	—	—	—	—		
	V <sub>NH</sub>		4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—		
			9	10	2.9	—	—	3	4.5	—	3	—	—		
			13.5	15	—	—	—	—	6.75	—	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>			0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	mA	6, 7
				0.5	10	1.1	—	—	0.9	1.8	—	0.65	—		
				1.5	15	—	—	—	3	6	—	—	—		
P-Channel (Source)	I <sub>DP</sub>			2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—	mA	8, 9
				4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—		
				9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—		
				13.5	15	—	—	—	-3	-6	—	—	—		
Input Current	I <sub>I</sub>			15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, and C<sub>L</sub> = 50 pF

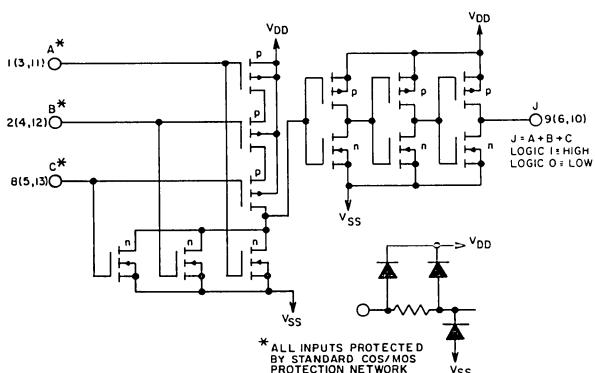
CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS		UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
		V <sub>DD</sub> Volts	Typ.	Max.			
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>		5 10 15	250 100 75	500 200 —	ns	10, 12
Low-to-High Level	t <sub>TPLH</sub>		5 10 15	175 70 55	350 140 —	ns	11, 12
Transition Time	t <sub>TTHL</sub> t <sub>TLH</sub>		5 10 15	100 50 40	200 100 80	ns	13
Average Input Capacitance	C <sub>I</sub>	Any Input	5	—	pF	—	—

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	SYMBOL	TEST CONDI-TIONS		CD4071BE, CD4072BE, CD4075BE PLASTIC PACKAGE LIMITS								UNITS	FIG. NO.		
		VO Volts	VDD Volts	-40°C			25°C			85°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>	5	—	—	5	—	0.01	0.5	—	—	70	—	µA	15	
		10	—	—	10	—	0.01	10	—	—	140	—			
		15	—	—	—	—	0.01	—	—	—	—	—			
Output Voltage: Low-Level	V <sub>OL</sub>	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—	
		10	—	—	0.01	—	0	0.01	—	—	0.05	—			
		15	—	—	—	—	0	—	—	—	—	—			
High-Level	V <sub>OH</sub>	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—	
		10	9.99	—	—	9.99	10	—	9.95	—	—	—			
		15	—	—	—	—	15	—	—	—	—	—			
Noise Immunity	V <sub>NL</sub>	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	4, 5, 16	
		1	10	3	—	—	3	4.5	—	2.9	—	—			
		1.5	15	—	—	—	—	6.75	—	—	—	—			
	V <sub>NH</sub>	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—			
		9	10	2.9	—	—	3	4.5	—	3	—	—			
		13.5	15	—	—	—	—	6.75	—	—	—	—			
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	—	—	—	—	—	—	—	—	—	—	—	mA	6, 7	
		0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—			
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—			
P-Channel (Source)	I <sub>DP</sub>	1.5	15	—	—	—	3	6	—	—	—	—	mA	8, 9	
		2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—			
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—			
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—			
Input Current		13.5	15	—	—	—	-3	-6	—	—	—	—	µA	—	
		15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	µA	—	

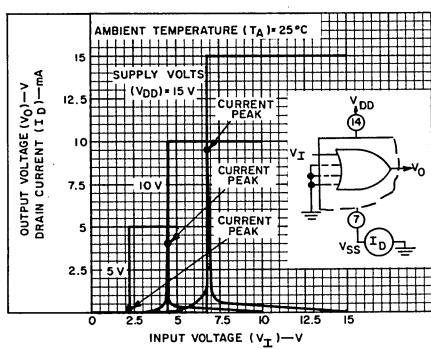


*Fig. 2—CD4072B schematic diagram (1 of 2 identical OR gates)*



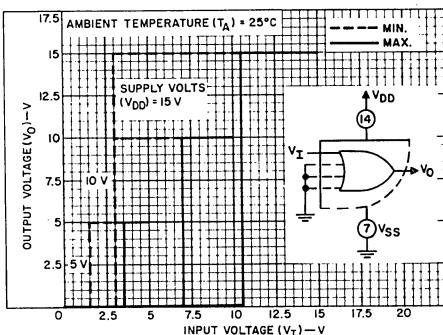
92CS-23814RI

Fig. 3—CD4075B schematic diagram (1 of 3 identical OR gates).



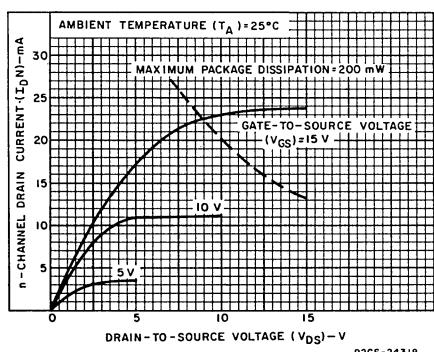
92CS-23815RI

Fig. 4—Typical voltage and current transfer characteristics.



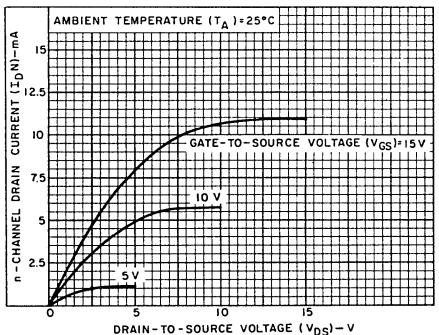
92CS-24488

Fig. 5—Min. and max. voltage transfer characteristics.



92CS-24318

Fig. 6—Typical output N-channel drain characteristics.



92CS-24319

Fig. 7—Minimum output N-channel drain characteristics.

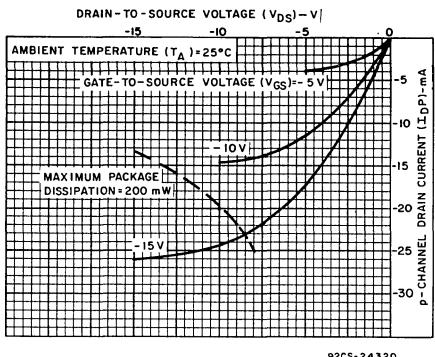


Fig. 8—Typical output-P-channel drain characteristics.

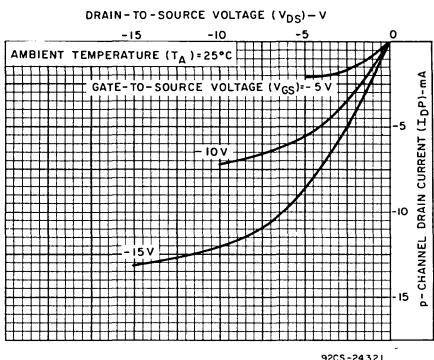


Fig. 9—Minimum output-P-channel drain characteristics.

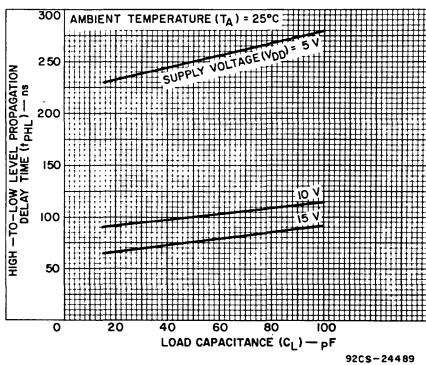


Fig. 10—Typical high-to-low level propagation delay time vs. load capacitance.

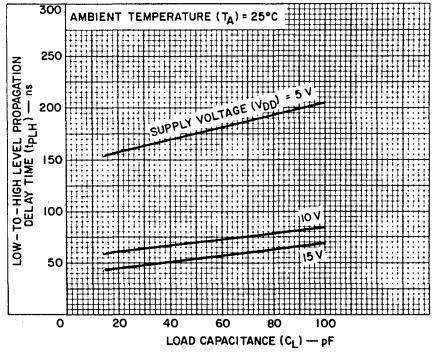


Fig. 11—Typical low-to-high level propagation delay time vs. load capacitance.

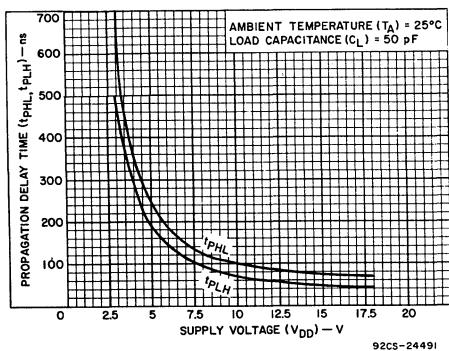


Fig. 12—Typical propagation delays vs. supply voltage.

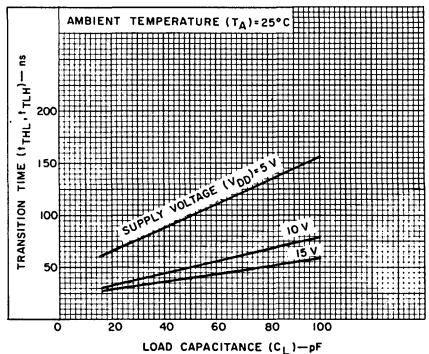


Fig. 13—Typical transition time vs. load capacitance.

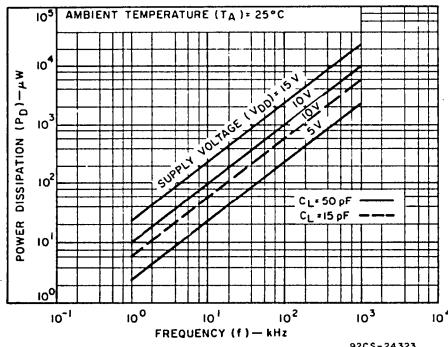
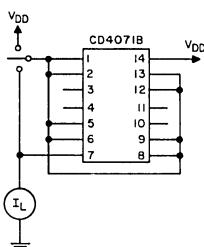


Fig. 14—Typical dynamic power dissipation vs. frequency.



CD4075B — PUT METER IN SAME  
PLACE AS CD4071B  
TIE PINS 1, 2, 3, 4, 5, 9, 10, 11, 13  
TO SWITCH.

CD4072B — PUT METER IN SAME  
PLACE AS CD4071B  
TIE PINS 2, 3, 4, 5, 9, 10, 11, 12  
TO SWITCH.

92CS-24492

Fig. 15—Quiescent current test circuits.

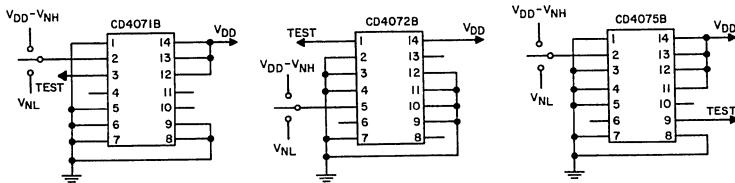


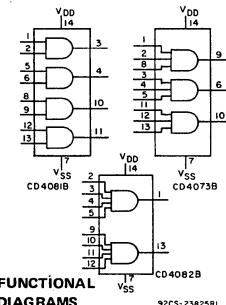
Fig. 16—Noise immunity test circuits.

92CM-24493RI



# Digital Integrated Circuits

Monolithic Silicon

**CD4081B Types  
CD4082B Types  
CD4073B Types**


## COS/MOS AND Gates

CD4081B Quad 2-Input AND Gate

CD4082B Dual 4-Input AND Gate

CD4073B Triple 3-Input AND Gate

### Features:

- Medium-Speed Operation –  $t_{PLH} = 85$  ns (typ.);  $t_{PHL} = 65$  ns (typ.) at 10 V
- Standard B-Series Output Drive

The RCA-CD4081B, -CD4082B, and -CD4073B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates. These devices have equal source- and sink-current capabilities and conform to standard B-series output drive (see

### Static Electrical Characteristics).

The CD4081B, CD4082B, and CD4073B are supplied in 14-lead dual-in-line plastic packages (E), welded-seal ceramic package (D), ceramic packages (F), ceramic flat packs (K), and chip form (H).

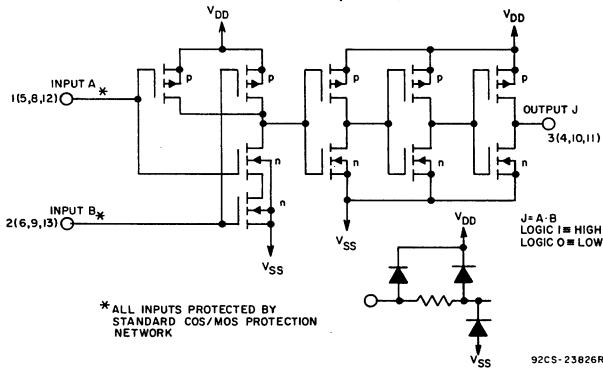


Fig. 1—CD4081B schematic diagram (1 of 4 identical AND gates).

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE:	
CERAMIC-PACKAGE TYPES .....	-55 to +125°C
PLASTIC-PACKAGE TYPES .....	-40 to +85 °C
DC SUPPLY-VOLTAGE RANGE	
$V_{DD}$ *	-0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .....	200 mW
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ....	265°C

\* All voltage values are referenced to  $V_{SS}$  terminal.

### OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	-	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD} +$ 0.5 V	V	-

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4081BD, BK, BF, BH CD4073BD, BK, BF, BH CERAMIC PACKAGE LIMITS								UNITS	FIG. NO.		
		VO Volts	VDD Volts	-55°C			25°C			125°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	IL	5	—	—	0.5	—	0.01	0.5	—	—	30	—	μA	15	
		10	—	—	1	—	0.01	1	—	—	60	—			
		15	—	—	—	—	0.01	—	—	—	—	—			
Output Voltage: Low-Level	VOL	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—	
		10	—	—	0.01	—	0	0.01	—	—	0.05	—			
		15	—	—	—	—	0	—	—	—	—	—			
High-Level	VOH	5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	—	
		10	9.99	—	—	9.99	10	—	9.95	—	—	—			
		15	—	—	—	—	15	—	—	—	—	—			
Noise Immunity	VNL	0.8	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	4, 5, 16	
		1	10	3	—	—	3	4.5	—	2.9	—	—			
		1.5	15	—	—	—	6.75	—	—	—	—	—			
	VNH	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—			
		9	10	2.9	—	—	3	4.5	—	3	—	—			
		13.5	15	—	—	—	6.75	—	—	—	—	—			
Output Drive Current: N-Channel (Sink)	IDN	0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	—	mA	6, 7	
		0.5	10	1.1	—	—	0.9	1.8	—	0.65	—	—			
		1.5	15	—	—	—	3	6	—	—	—	—			
P-Channel (Source)	IDP	2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—	—	mA	8, 9	
		4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—	—			
		9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—	—			
		13.5	15	—	—	—	-3	-6	—	—	—	—			
Input Current	II	15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	—	μA	—	

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20 \text{ ns}$ , and  $C_L = 50 \text{ pF}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
				V <sub>DD</sub> Volts	Typ.	Max.		
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>			5	160	320	ns	10, 12
				10	65	130		
Low-to-High Level	t <sub>PLH</sub>			5	210	420	ns	11, 12
				10	85	170		
Transition Time	t <sub>THL</sub>			5	100	200	ns	13
				10	50	100		
Average Input Capacitance	C <sub>I</sub>	Any Input		5	—	pF	—	

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4081BE, CD4082BE, CD4073BE PLASTIC PACKAGE LIMITS								UNITS	FIG. NO.		
		VO Volts	VDD Volts	-40°C			25°C			85°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>	5	—	—	5	—	0.01	5	—	—	70	—	μA	15	
		10	—	—	10	—	0.01	10	—	—	140	—			
		15	—	—	—	—	0.01	—	—	—	—	—			
Output Voltage: Low-Level	V <sub>OL</sub>	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—	
		10	—	—	0.01	—	0	0.01	—	—	0.05	—			
		15	—	—	—	—	0	—	—	—	—	—			
High-Level	V <sub>OH</sub>	5	4.99	—	—	4.99	5	—	4.95	—	—	—	—	—	
		10	9.99	—	—	9.99	10	—	9.95	—	—	—			
		15	—	—	—	—	15	—	—	—	—	—			
Noise Immunity	V <sub>NL</sub>	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—	V	4, 5, 16	
		10	3	—	—	3	4.5	—	2.9	—	—	—			
		15	—	—	—	—	6.75	—	—	—	—	—			
	V <sub>NH</sub>	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—			
		10	2.9	—	—	3	4.5	—	3	—	—	—			
		15	—	—	—	—	6.75	—	—	—	—	—			
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	6, 7	
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—			
		1.5	15	—	—	—	3	6	—	—	—	—			
P-Channel (Source)	I <sub>DP</sub>	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	8, 9	
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—			
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—			
		13.5	15	—	—	—	-3	-6	—	—	—	—			
Input Current	I <sub>I</sub>	15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—	

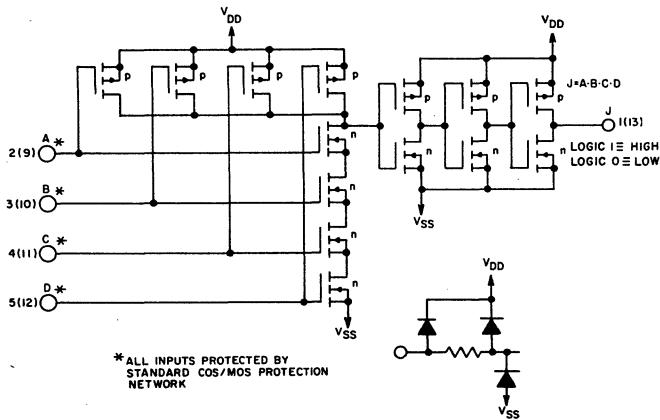


Fig. 2—CD4082B schematic diagram (1 of 2 identical AND gates).

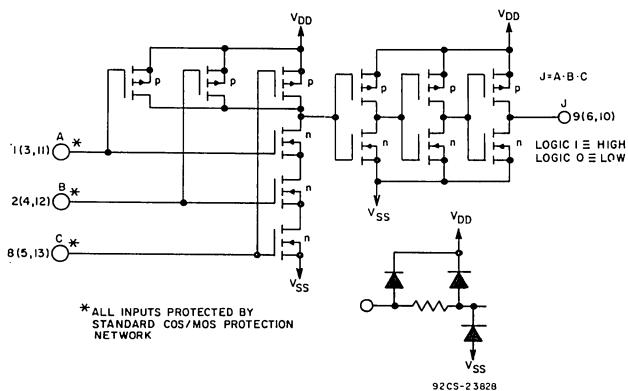


Fig. 3—CD4073B schematic diagram (1 of 3 identical AND gates).

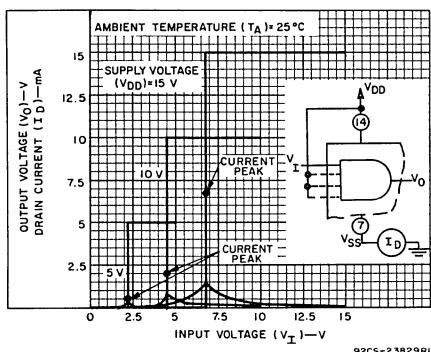


Fig. 4—Typical voltage and current transfer characteristics.

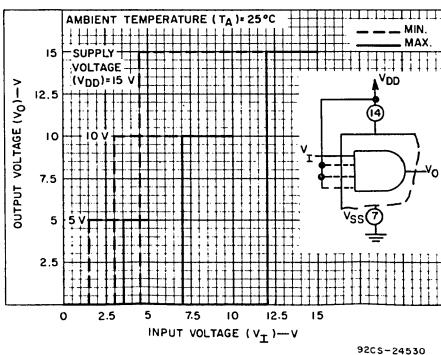


Fig. 5—Min. and max. voltage transfer characteristics.

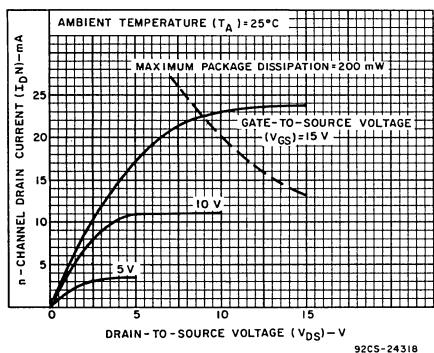


Fig. 6—Typical output-N-channel drain characteristics.

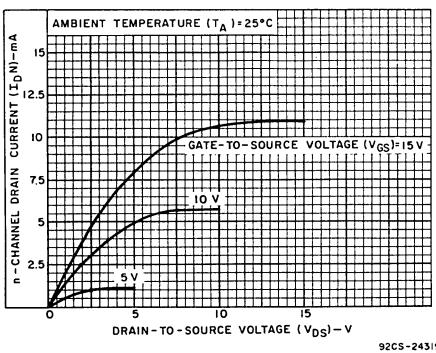


Fig. 7—Minimum output-N-channel drain characteristics.

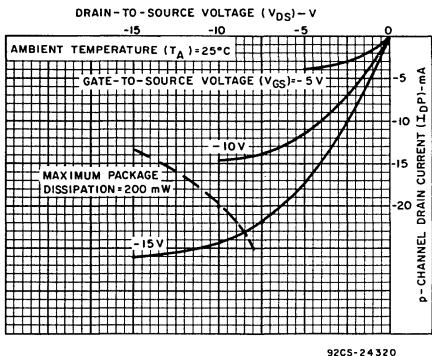


Fig. 8—Typical output-P-channel drain characteristics.

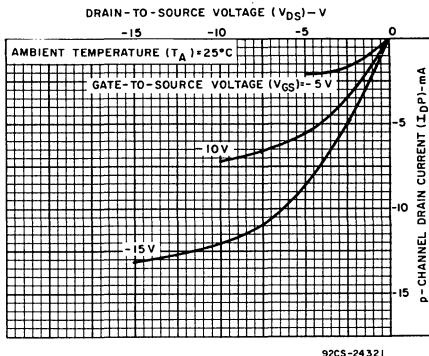


Fig. 9—Minimum output-P-channel drain characteristics.

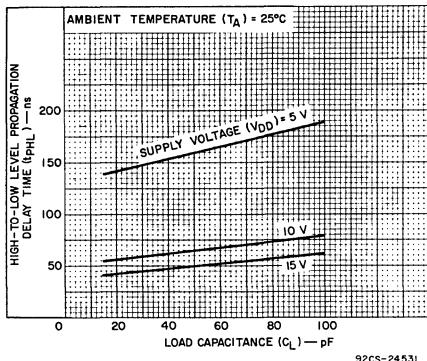


Fig. 10—Typical high-to-low level propagation delay vs. load capacitance.

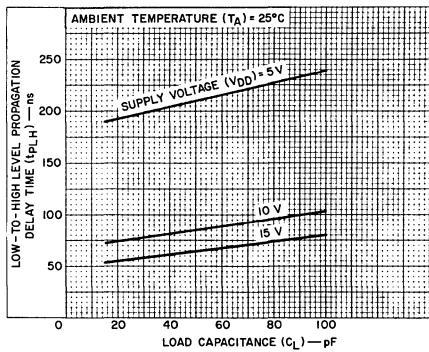


Fig. 11—Typical low-to-high level propagation delay vs. load capacitance.

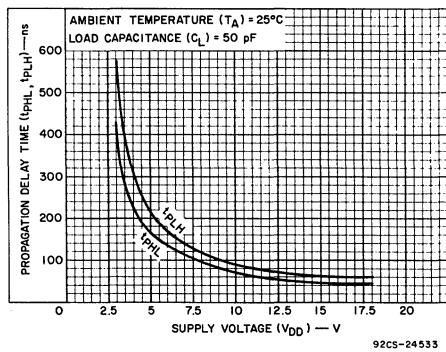


Fig. 12—Typical propagation delays vs. supply voltage.

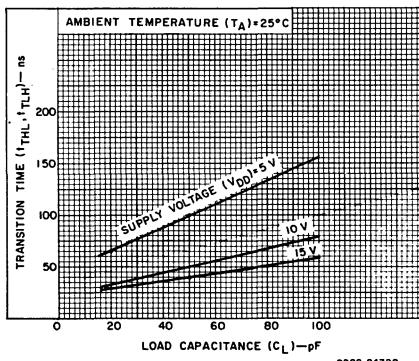


Fig. 13—Typical transition time vs. load capacitance.

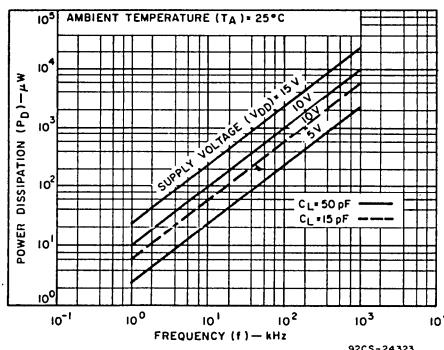
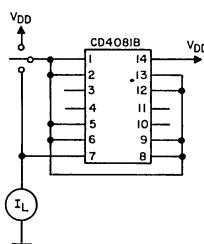


Fig. 14—Typical dynamic power dissipation vs. frequency.

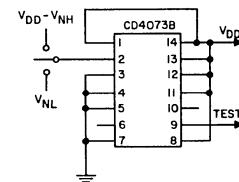


CD4073B – PUT METER IN SAME  
PLACE AS CD4081  
TIE PINS 1, 2, 3, 4, 5, 10, 11, 12, 13  
TO SWITCH.

CD4082B – PUT METER IN SAME  
PLACE AS CD4081  
TIE PINS 2, 3, 4, 5, 9, 10, 11, 12  
TO SWITCH.

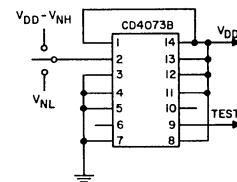
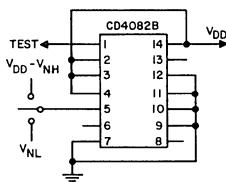
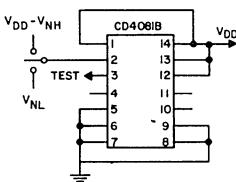
92CS-24534

Fig. 15—Quiescent current test circuits.



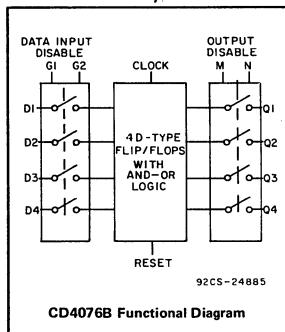
92CM-24535

Fig. 16—Noise immunity test circuits.



**Preliminary CD4076BE**

Preliminary Data▲



CD4076B Functional Diagram

The RCA-CD4076BE four-bit register includes D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled (present a high impedance) independently of the clock by a high logic level at either Output Disable input.

**CD4076BE**  
Truth Table

Reset	Clock	Data Input Disable G1	G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	—	1	X	X	Q	NC
0	—	X	1	X	Q	NC
0	—	0	0	1	1	
0	—	0	0	0	0	
0	1	X	X	X	Q	NC
0	—	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 ≡ High Level

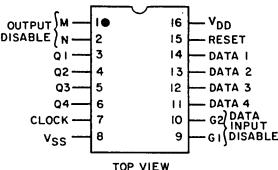
0 ≡ Low Level

X = Don't Care

NC = No Change

## COS/MOS 4-Bit D-Type Register

With 3-State Outputs



92CS-24887  
**CD4076B**  
TERMINAL ASSIGNMENT

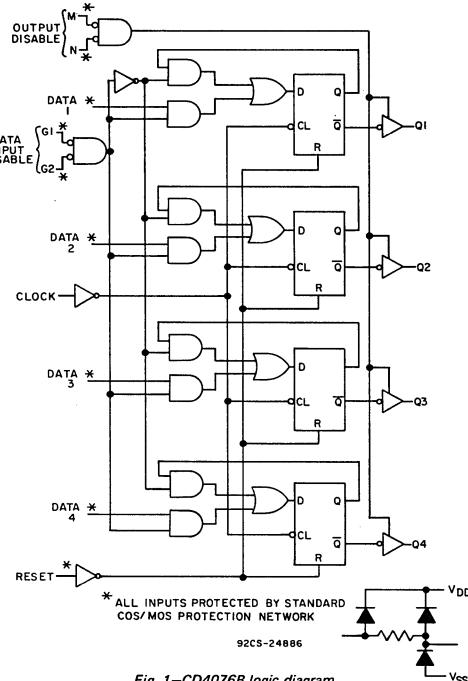


Fig. 1—CD4076B logic diagram.

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4076B TYPICAL VALUES	UNITS
		$V_O$ (V)	$V_{DD}$ (V)		
Quiescent Device Current	$I_L$		5	0.02	$\mu\text{A}$
			10	0.02	
Output Device Current: N-Channel (Sink)	$I_{DN}$	0.4	5	0.8	$\text{mA}$
		0.5	10	1.8	
	$I_{DP}$	4.6	5	-0.8	
		2.5	5	-3.2	
		9.5	10	-1.8	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	$V_{DD}$ (V)	TYPICAL VALUES	UNITS
Propagation Delay	$t_{PHL}, t_{PLH}$	5	260	$\text{ns}$
		10	120	
Transition Time	$t_{THL}, t_{PLH}$	5	100	$\text{ns}$
		10	50	
Data Setup Time	$t_{SUHL}, t_{SULH}$	5	100	$\text{ns}$
		10	60	
Minimum Clock Pulse Width	$t_{WL}, t_{WH}$	5	125	$\text{ns}$
		10	50	
Minimum Reset Pulse Width	$t_{WH(R)}$	5	75	$\text{ns}$
		10	40	
Reset Propagation Delay	$t_{PHL(R)}$	5	230	$\text{ns}$
		10	120	
Data Input Disable Setup Time	$t_{SU(DIS)}$	5	100	$\text{ns}$
		10	60	
Clock Rise and Fall Time	$t_{rCL}, t_{fCL}$	5	15	$\mu\text{s}$
		10	15	
Clock Frequency	$f_{CL}$	5	4	$\text{MHz}$
		10	10	
3-State Propagation Delay Output 1 or 0 to High Impedance	$t_p(I-H), t_p(O-H)$	5	110	$\text{ns}$
		10	65	
3-State Propagation Delay, High Impedance to 1 or 0	$t_p(H-I), t_p(H-O)$	5	80	$\text{ns}$
		10	45	

**MAXIMUM RATINGS, Absolute-Maximum Values:**

STORAGE-TEMPERATURE RANGE..... -65 to +150°C  
 OPERATING-TEMPERATURE RANGE..... -40 to +85 °C

**DC SUPPLY-VOLTAGE RANGE**

$V_{DD}$  \* ..... -0.5 to +18 V  
 DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

ALL INPUTS .....  $V_{SS} \leq V_I \leq V_{DD}$

**LEAD TEMPERATURE (DURING SOLDERING):**

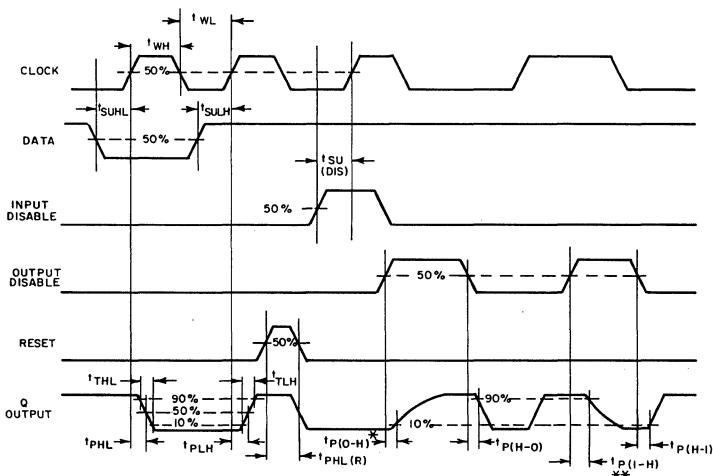
At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$  mm)  
 from case for 10 seconds max. ..... 265°C

\* All voltage values are referenced to  $V_{SS}$  terminal.

**OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$** 

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	-	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD} +$ 0.5 V	V	-



\* OUTPUT TIED TO  $V_{DD}$  THROUGH  $1\text{k}\Omega$   
 \*\* OUTPUT TIED TO  $V_{SS}$  THROUGH  $1\text{k}\Omega$

92CM-24888

Fig. 2—Timing diagram.

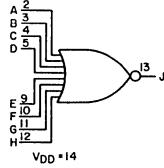


## Digital Integrated Circuits

Monolithic Silicon

## CD4078B Type

## COS/MOS 8-Input NOR Gate



CD4078B Functional Diagram

## Features:

- Medium-speed operation — t<sub>PHL</sub> = 80 ns, t<sub>PLH</sub> = 170 ns (typ.) at 10 V
- Standard B-series output drive

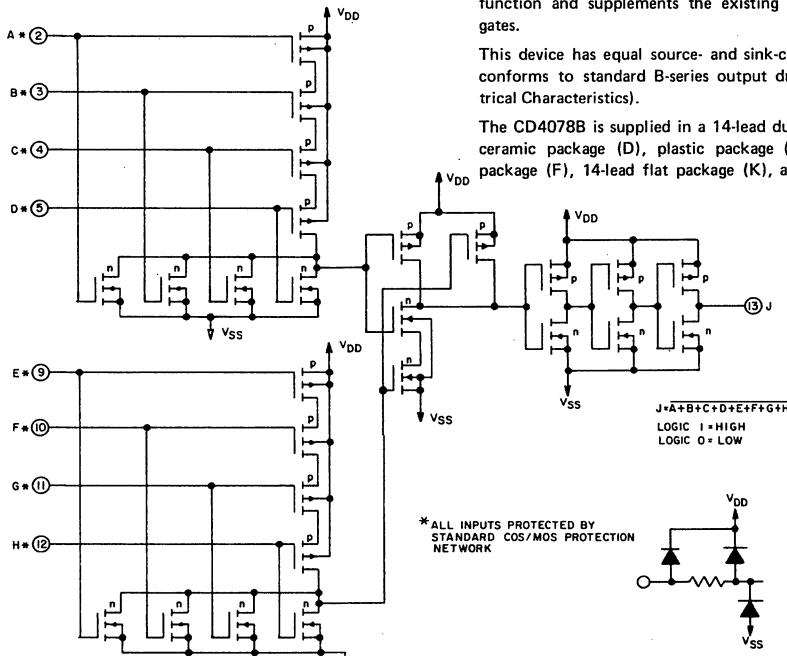
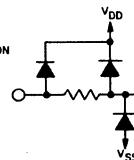


Fig. 1—CD4078B schematic diagram.



92CM-23678RI

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4078BD CD4078BK CD4078BH CERAMIC PACKAGE LIMITS						UNITS	FIG. NO.		
		VO Volts	VDD Volts	-55°C			25°C			UNITS	FIG. NO.		
				Min.	Typ.	Max.	Min.	Typ.	Max.				
Quiescent Device Current	IL	5	—	—	0.5	—	0.01	0.5	—	—	30	μA	13
		10	—	—	1	—	0.01	1	—	—	60		
		15	—	—	—	—	0.01	—	—	—	—		
Output Voltage Low-Level	VOL	5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
		10	—	—	0.01	—	0	0.01	—	—	0.05		
		15	—	—	—	—	0	—	—	—	—		
High-Level	VOH	5	4.99	—	—	4.99	5	—	4.95	—	—	V	—
		10	9.99	—	—	9.99	10	—	9.95	—	—		
		15	—	—	—	—	15	—	—	—	—		
Noise Immunity	VNL	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	V	14
		9	10	3	—	—	3	4.5	—	2.9	—		
		13.5	15	—	—	—	6.75	—	—	—	—		
	VNH	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—		
		1	10	2.9	—	—	3	4.5	—	3	—		
		1.5	15	—	—	—	6.75	—	—	—	—		
Output Drive Current: N-Channel (Sink)	IDN	0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	mA	4,5
		0.5	10	1.1	—	—	0.9	1.8	—	0.65	—		
		1.5	15	—	—	—	3	6	—	—	—		
P-Channel (Source)	IDP	2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—	mA	6,7
		4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—		
		9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—		
		13.5	15	—	—	—	-3	-6	—	—	—		
Input Current	I <sub>I</sub>		15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	μA	—

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE:

CERAMIC-PACKAGE TYPES ..... -55 to +125°C

PLASTIC-PACKAGE TYPES ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE

V<sub>DD</sub> \* ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)  
from case for 10 seconds max. ..... 265°C\* All voltage values are referenced to V<sub>SS</sub> terminal.OPERATING CONDITIONS AT T<sub>A</sub> = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	—	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	-0.5 V to V <sub>DD</sub> + 0.5 V	V	—

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4078BE								UNITS	FIG. NO.	
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	-40°C			25°C			85°C				
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	I <sub>L</sub>		5	—	—	5	—	0.01	5	—	—	70	μA	13
			10	—	—	10	—	0.01	10	—	—	140		
			15	—	—	—	—	0.01	—	—	—	—		
Output Voltage: Low-Level	V <sub>OL</sub>		5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
			10	—	—	0.01	—	0	0.01	—	—	0.05		
			15	—	—	—	—	0	—	—	—	—		
High-Level	V <sub>OH</sub>		5	4.99	—	—	4.99	5	—	4.95	—	—	—	—
			10	9.99	—	—	9.99	10	—	9.95	—	—		
			15	—	—	—	—	15	—	—	—	—		
Noise Immunity	V <sub>NL</sub>	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	14
		9	10	3	—	—	3	4.5	—	2.9	—	—		
		13.5	15	—	—	—	—	6.75	—	—	—	—		
	V <sub>NH</sub>	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—		
		1	10	2.9	—	—	3	4.5	—	3	—	—		
		1.5	15	—	—	—	—	6.75	—	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	4,5
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—		
		1.5	15	—	—	—	3	6	—	—	—	—		
P-Channel (Source)	I <sub>DP</sub>	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	6,7
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—		
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—		
		13.5	15	—	—	—	-3	-6	—	—	—	—		
Input Current	I <sub>I</sub>		15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, and C<sub>L</sub> = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS			UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
		V <sub>DD</sub> Volts		Typ.	Max.			
Propagation Delay Time: High-to-Low Level	t <sub>PHL</sub>			5	200	400	ns	8,10
				10	80	160		
Low-to-High Level	t <sub>PLH</sub>			5	425	850	ns	9,10
				10	170	340		
Transition Time	t <sub>THL</sub>			5	100	200	ns	11
				10	50	100		
Average Input Capacitance	C <sub>I</sub>	Any Input		5	—	pF	—	

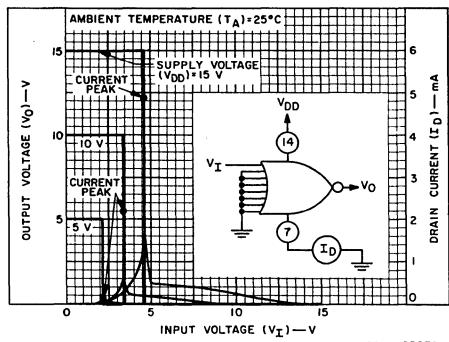


Fig. 2—Typical voltage and current transfer characteristics.

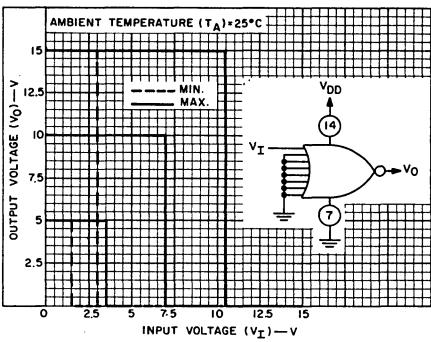


Fig. 3—Min. and max. voltage transfer characteristics.

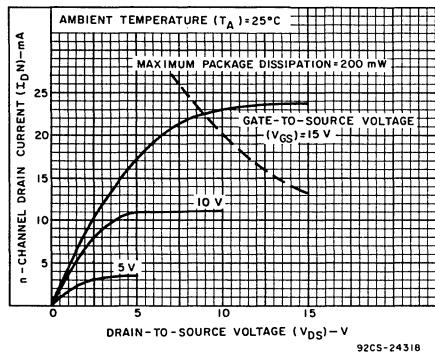


Fig. 4—Typical output n-channel drain characteristics.

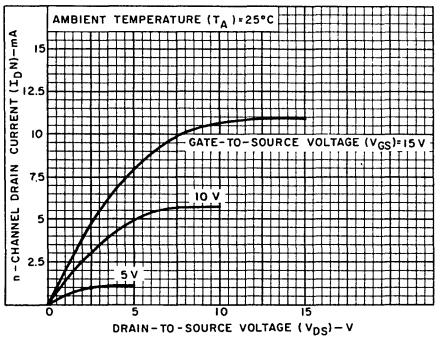


Fig. 5—Minimum output n-channel drain characteristics.

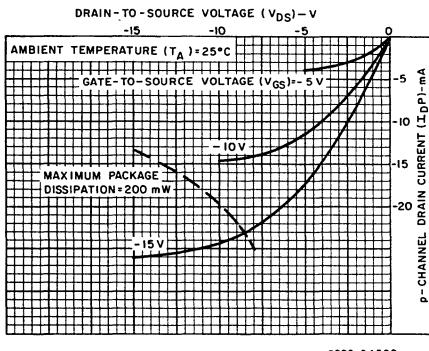


Fig. 6—Typical output p-channel drain characteristics.

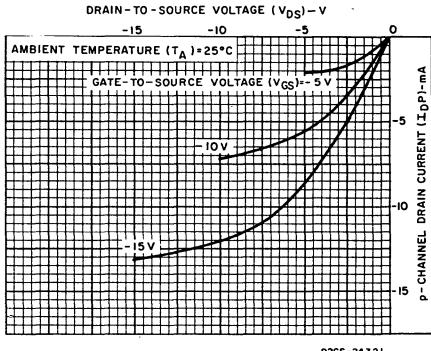


Fig. 7—Minimum output p-channel drain characteristics.

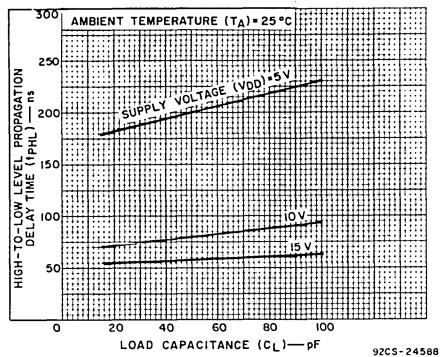


Fig. 8—Typical high-to-low level propagation delay time vs. load capacitance.

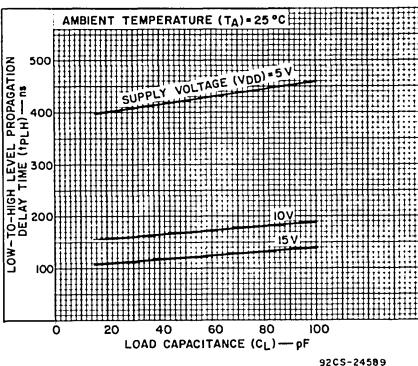


Fig. 9—Typical low-to-high level propagation delay time vs. load capacitance.

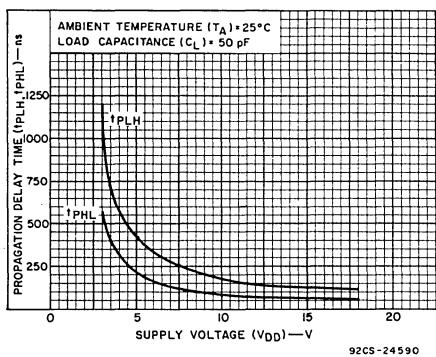


Fig. 10—Typical propagation delay time vs. supply voltage.

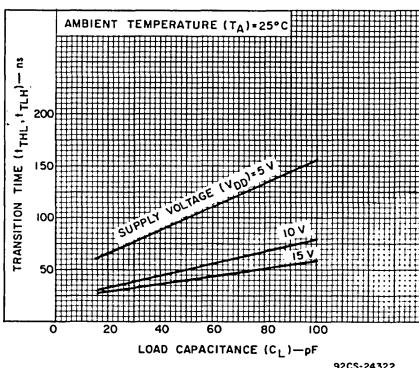


Fig. 11—Typical transition time vs. load capacitance.

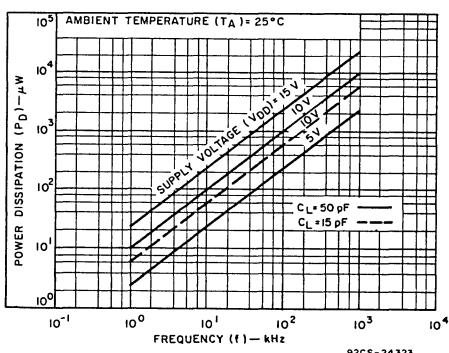


Fig. 12—Typical power dissipation vs. frequency.

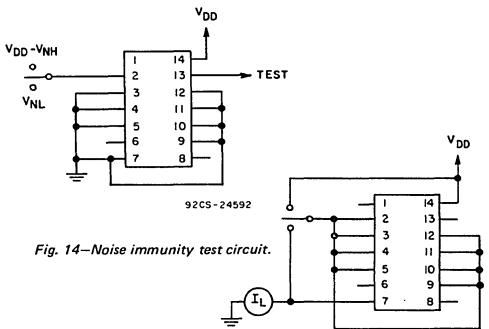


Fig. 14—Noise immunity test circuit.

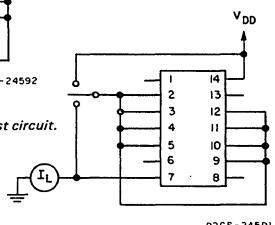


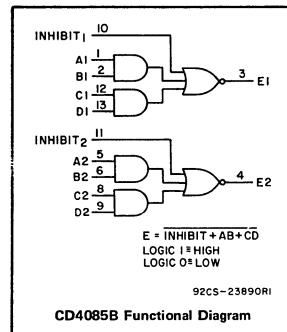
Fig. 13—Quiescent device current test circuit.



# Digital Integrated Circuits

Monolithic Silicon

## CD4085B Type



### COS/MOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

#### Features:

- Medium-speed operation –  $t_{PHL} = 90$  ns;  $t_{PLH} = 125$  ns (typ.) at 10 V
- Individual inhibit controls
- Standard B-series output drive

The RCA-CD4085B contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input OR gate followed by an inverter. Individual inhibit controls are provided for both A-O-I gates. This device has equal source- and sink-current capabilities and conforms to standard B-series

output drive (see Static Electrical Characteristics).

The CD4085B is supplied in a 14-lead dual-in-line welded-seal ceramic package (D), plastic package (E), ceramic package (F), ceramic flat pack (K), and chip form (H).

#### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE:	
CERAMIC-PACKAGE TYPES .....	-55 to +125°C
PLASTIC-PACKAGE TYPES .....	-40 to +85 °C

DC SUPPLY-VOLTAGE RANGE	
$V_{DD}$ .....	-0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) .....	200 mW
--	--------

ALL INPUTS .....	$V_{SS} \leq V_I \leq V_{DD}$
------------------	-------------------------------

LEAD TEMPERATURE (DURING SOLDERING):	
--------------------------------------	--

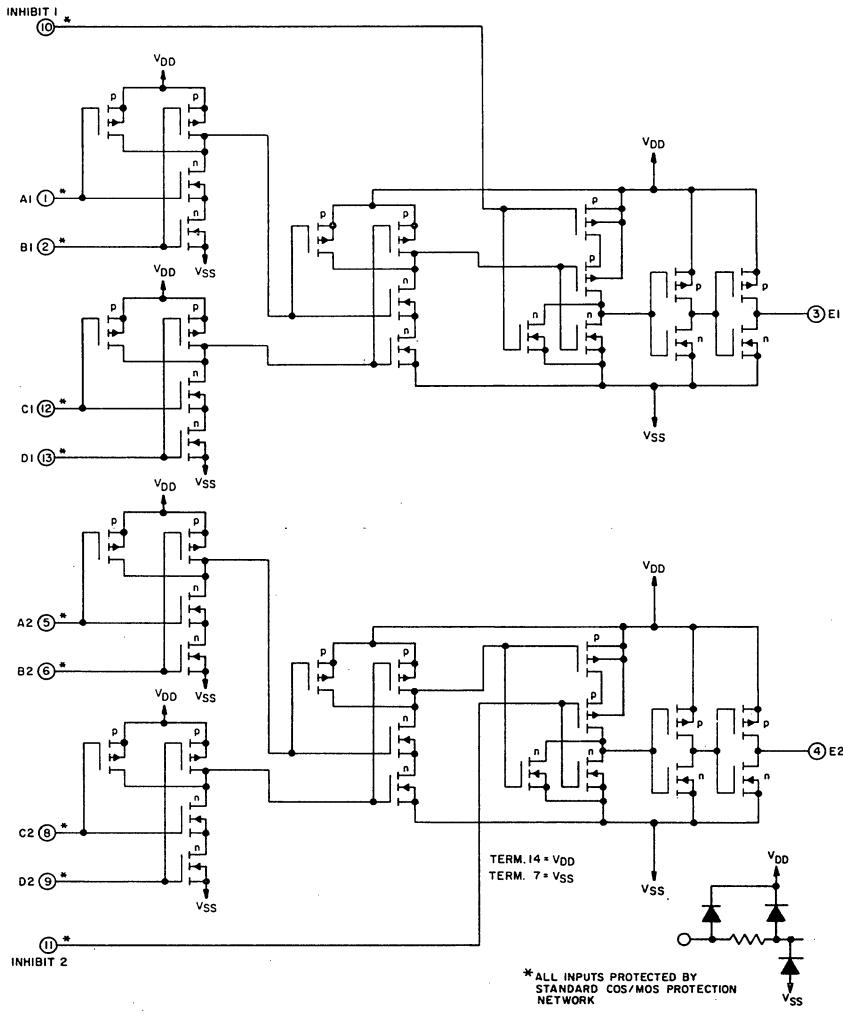
At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$  mm)  
from case for 10 seconds max. ....  $265^\circ\text{C}$

\* All voltage values are referenced to  $V_{SS}$  terminal.

#### OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	— 0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	— — — —	— — — —	V	—



\* ALL INPUTS PROTECTED BY  
STANDARD CMOS PROTECTION  
NETWORK

92CL-2389IRI

Fig. 1—CD4085B schematic diagram.

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4085BD CD4085BF CD4085BH CERAMIC PACKAGE LIMITS						UNITS	FIG. NO.	
		VO Volts	VDD Volts	-55°C			25°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
Quiescent Device Current	IL			5	—	—	5	—	0.02	5	—	30
				10	—	—	10	—	0.02	10	—	60
				15	—	—	—	—	0.02	—	—	—
Output Voltage Low-Level	VOL			5	—	—	0.01	—	0	0.01	—	0.05
				10	—	—	0.01	—	0	0.01	—	0.05
				15	—	—	—	—	0	—	—	—
High-Level	VOH			5	4.99	—	—	4.99	5	—	4.95	—
				10	9.99	—	—	9.99	10	—	9.95	—
				15	—	—	—	—	15	—	—	—
Noise Immunity	VNL		4.2	5	1.5	—	—	1.5	2.25	—	1.4	—
			9	10	3	—	—	3	4.5	—	2.9	—
			13.5	15	—	—	—	—	6.75	—	—	—
	VNH		0.8	5	1.4	—	—	1.5	2.25	—	1.5	—
			1	10	2.9	—	—	3	4.5	—	3	—
			1.5	15	—	—	—	—	6.75	—	—	—
Output Drive Current: N-Channel (Sink)	IDN		0.4	5	0.5	—	—	0.4	0.8	—	0.3	—
			0.5	10	1.1	—	—	0.9	1.8	—	0.65	—
			1.5	15	—	—	—	3	6	—	—	—
P-Channel (Source)	IDP		2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—
			4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—
			9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—
			13.5	15	—	—	—	-3	-6	—	—	—
Input Current	II		15	—	—	—	—	—	$\pm 10^{-5}$	$\pm 1$	—	—

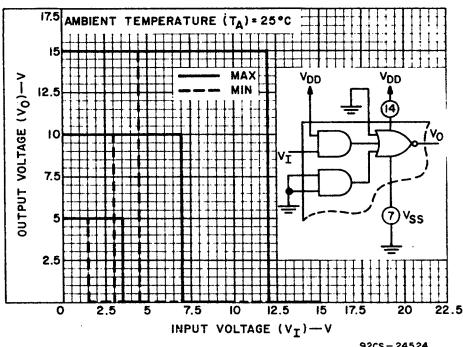
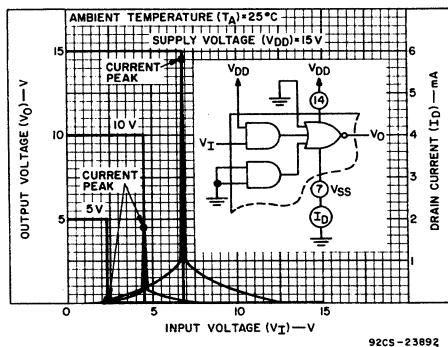


Fig. 2—Typical voltage and current transfer characteristics.

Fig. 3—Min. and max. voltage transfer characteristics.

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4085BE PLASTIC PACKAGE LIMITS								UNITS	FIG. NO.	
		$V_O$ Volts	$V_{DD}$ Volts	-40°C			25°C			85°C				
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	IL	5 10 15	— — —	5 10 —	— — —	— — —	0.01 0.01 0.01	5 10 —	— — —	— — —	— — —	70 140 —	$\mu A$	13
				5 10 15	— — —	0.01 0.01 —	0 0 —	0.01 0.01 —	— — —	— — —	— — —	0.05 0.05 —		
				5 10 15	4.99 9.99 —	— — —	4.99 9.99 —	5 10 —	— — —	4.95 9.95 —	— — —	— — —		
Output Voltage: Low-Level	VOL	5 10 15	— — —	5 10 —	— — —	— — —	0 0 —	0 0.01 —	— — —	— — —	— — —	— — —	V	—
				5 10 15	9.99 — —	— — —	9.99 — —	10 — —	— — —	9.95 — —	— — —	— — —	— — —	
				5 10 15	— — —	— — —	— — —	15 — —	— — —	— — —	— — —	— — —	— — —	
Noise Immunity	VNL	4.2 9 13.5	5 10 15	1.5 3 —	— — —	— — —	1.5 3 —	2.25 4.5 6.75	— — —	1.4 2.9 —	— — —	— — —	V	14
		0.8 1 1.5	5 10 15	1.4 2.9 —	— — —	— — —	1.5 3 —	2.25 4.5 6.75	— — —	1.5 3 —	— — —	— — —		
		— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —		
	VNH	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —		
		— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —		
		— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —	— — —		
Output Drive Current: N-Channel (Sink)	IDN	0.4 0.5 1.5	5 10 15	0.45 1 —	— — —	— — —	0.4 0.9 3	0.8 1.8 6	— — —	0.36 0.75 —	— — —	— — —	mA	4, 5
P-Channel (Source)	IDP	2.5 4.6 9.5 13.5	5 5 10 15	-1.8 -0.45 -1 —	— — — —	— — — —	-1.6 -0.4 -0.9 -3	-3.2 -0.8 -1.8 -6	— — — —	-1.3 -0.36 -0.75 —	— — — —	mA	6, 7	
Input Current	II	—	15	—	—	—	—	$\pm 10^{-5}$	$\pm 1$	—	—	—	$\mu A$	—

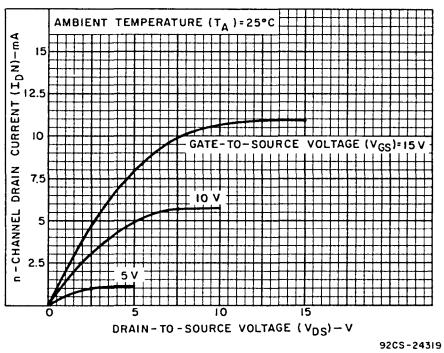
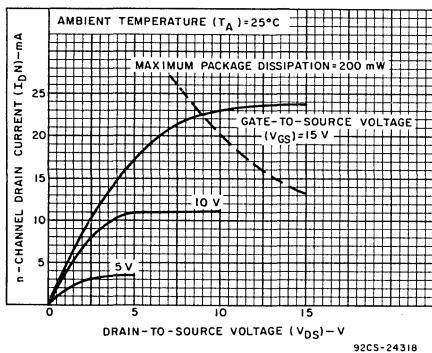
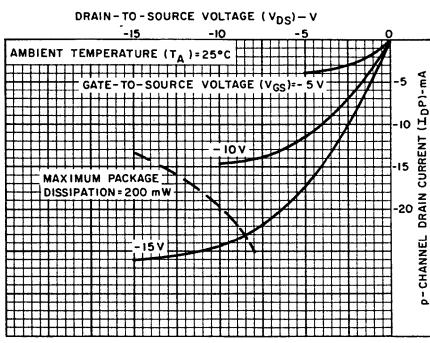


Fig. 4—Typical output n-channel drain characteristics.

Fig. 5—Minimum output n-channel drain characteristics.

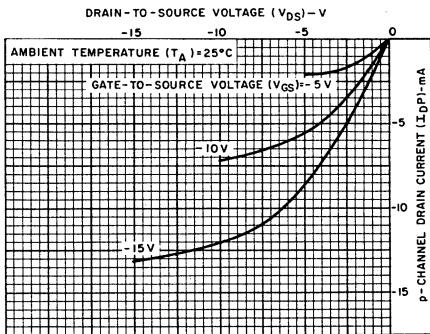
DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS		UNITS	FIG. NO.	
		$V_{DD}$	V	Typ.	Max.			
Propagation Delay Time (Data): High-to-Low Level	$t_{PHL}$			5	225	450	ns	8, 10
				10	90	180		
				15	65	—		
Low-to-High Level	$t_{PLH}$			5	310	620	ns	9, 10
				10	125	250		
				15	90	—		
Propagation Delay Time (Inhibit): High-to-Low Level	$t_{PHL}(\text{INH})$			5	150	300	ns	—
				10	60	120		
				15	40	—		
Low-to-High Level	$t_{PLH}(\text{INH})$			5	250	500	ns	—
				10	100	200		
				15	70	—		
Transition Time	$t_{THL}, t_{TLH}$			5	100	200	ns	11
				10	50	100		
				15	40	80		
Average Input Capacitance	$C_I$	Any Input		5	—	pF	—	—



92CS-24320

Fig. 6—Typical output p-channel drain characteristics.



92CS-24321

Fig. 7—Minimum output p-channel drain characteristics.

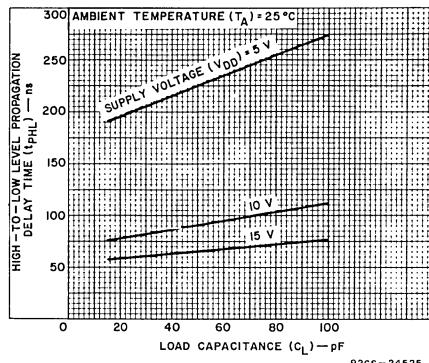


Fig. 8—Typical data high-to-low level propagation delay time vs. load capacitance.

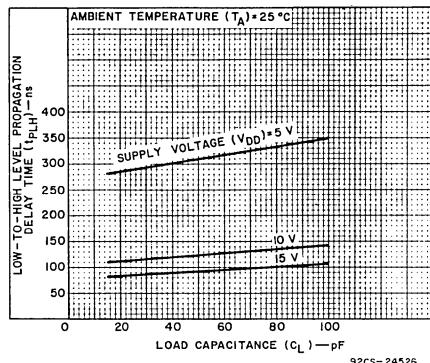


Fig. 9—Typical data low-to-high level propagation delay time vs. load capacitance.

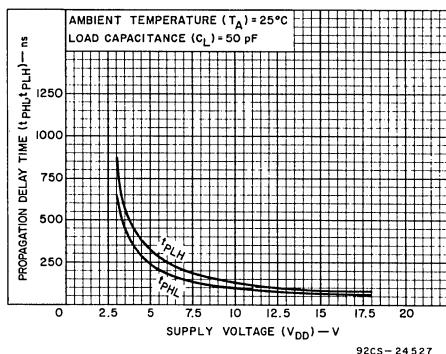


Fig. 10—Typical data propagation delay time vs. supply voltage.

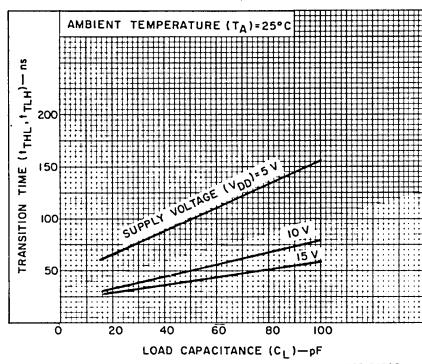


Fig. 11—Typical transition time vs. load capacitance.

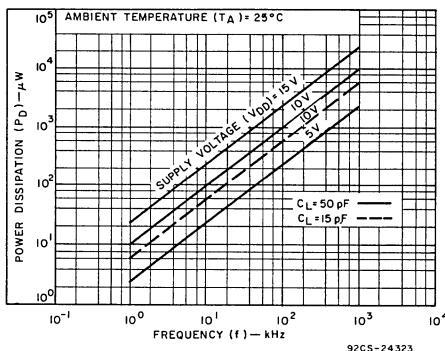


Fig. 12—Typical power dissipation vs. frequency.

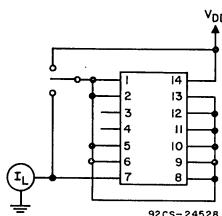


Fig. 13—Quiescent device current test circuit.

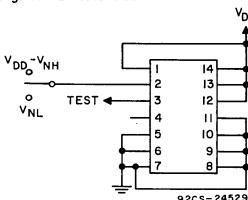


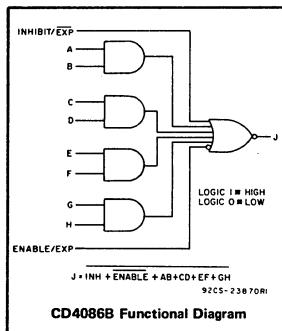
Fig. 14—Noise immunity test circuit.



# Digital Integrated Circuits

Monolithic Silicon

## CD4086B Type



### COS/MOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

#### Features:

- Medium-speed operation —  $t_{PHL} = 90 \text{ ns}$ ;  $t_{PLH} = 140 \text{ ns}$  (typ.) at 10 V
- INHIBIT and ENABLE inputs
- Standard B-series output drive

The RCA-CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/EXP input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/EXP is tied to  $V_{SS}$  and ENABLE/EXP to  $V_{DD}$ . See Fig. 2 and its associated explanation for applications where a capability greater than 4-wide is required. This device has equal source- and

sink-current capabilities and conforms to standard B-series output drive (see Static Electrical Characteristics).

The CD4086B is supplied in the 14-lead dual-in-line welded-seal ceramic package (D), ceramic package (F), plastic package (E), ceramic flat pack (K), and in chip form (H).

#### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE:

CERAMIC-PACKAGE TYPES ..... -55 to +125°C

PLASTIC-PACKAGE TYPES ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE

$V_{DD}$  \* ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)  
from case for 10 seconds max. ..... 265°C

\* All voltage values are referenced to  $V_{SS}$  terminal.

#### OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	-	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD}$ + 0.5 V	V	-

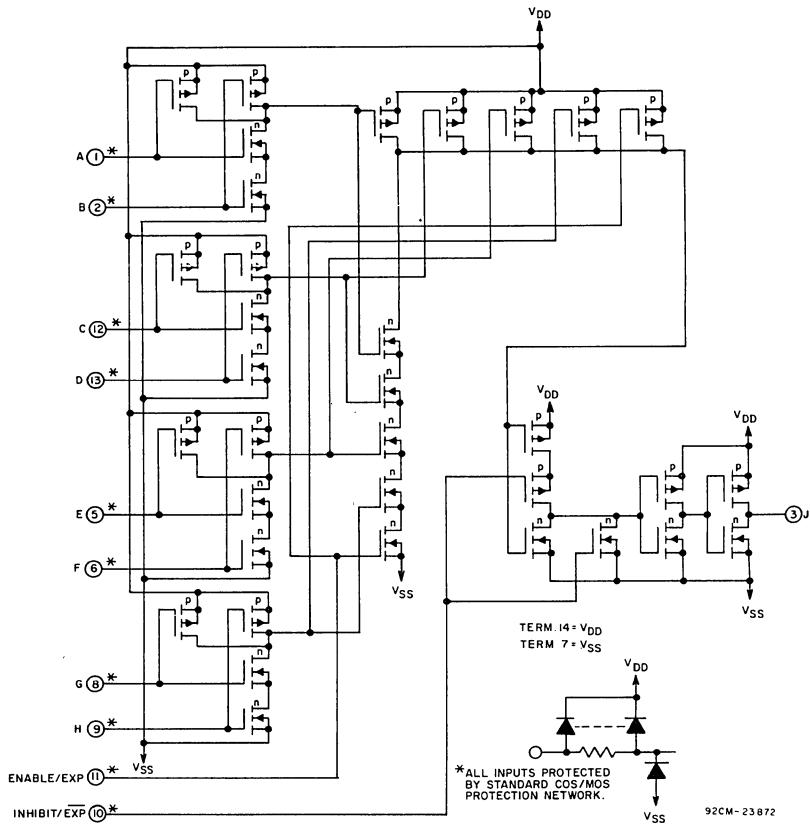


Fig. 1—CD4086B schematic diagram.

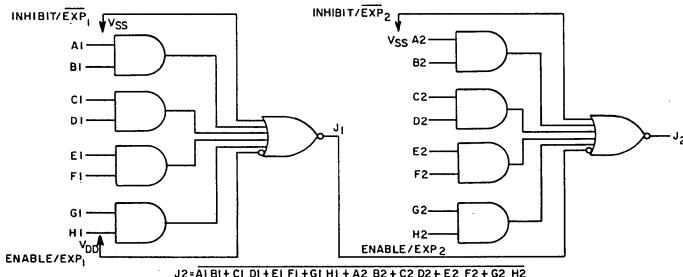


Fig. 2—Two CD4086B's connected as an 8-wide 2-input A-O-I gate.

Fig. 2 above shows two CD4086B's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086B is fed directly to the ENABLE/EXP2 line of the second CD4086B. In a similar fashion, any NAND gate

output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/EXP input with the same result.

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4086BD CD4086BF CD4086BK CD4086BH CERAMIC PACKAGE LIMITS						UNITS	FIG. NO.	
		VO Volts	VDD Volts	-55°C			25°C			125°C		
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
Quiescent Device Current	IL			5	—	0.5	—	0.01	0.5	—	—	30
				10	—	1	—	0.01	1	—	—	60
				15	—	—	—	0.01	—	—	—	—
Output Voltage Low-Level	VOL			5	—	0.01	—	0	0.01	—	—	0.05
				10	—	0.01	—	0	0.01	—	—	0.05
				15	—	—	—	0	—	—	—	—
High-Level	VOH			5	4.99	—	—	4.99	5	—	4.95	—
				10	9.99	—	—	9.99	10	—	9.95	—
				15	—	—	—	—	15	—	—	—
Noise Immunity	VNL		4.2	5	1.5	—	—	1.5	2.25	—	1.4	—
			9	10	3	—	—	3	4.5	—	2.9	—
			13.5	15	—	—	—	—	6.75	—	—	—
	VNH		0.8	5	1.4	—	—	1.5	2.25	—	1.5	—
			1	10	2.9	—	—	3	4.5	—	3	—
			1.5	15	—	—	—	—	6.75	—	—	—
Output Drive Current: N-Channel (Sink)	IDN		0.4	5	0.5	—	—	0.4	0.8	—	0.3	—
			0.5	10	1.1	—	—	0.9	1.8	—	0.65	—
			1.5	15	—	—	—	3	6	—	—	—
P-Channel (Source)	IDP		2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—
			4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—
			9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—
			13.5	15	—	—	—	-3	-6	—	—	—
Input Current	II		15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—

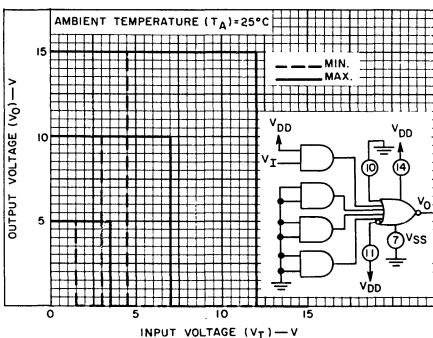
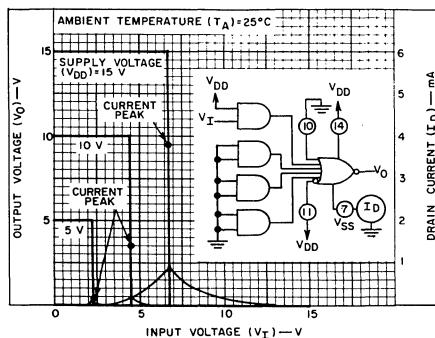


Fig. 3—Typical voltage and current transfer characteristics.

Fig. 4—Min. and max. voltage transfer characteristics.

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4086BE PLASTIC PACKAGE LIMITS								UNITS	FIG. NO.		
		VO Volts	VDD Volts	-40°C			25°C			85°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	IL			5	—	—	5	—	0.01	5	—	—	70	μA	14
				10	—	—	10	—	0.01	10	—	—	140		
				15	—	—	—	—	0.01	—	—	—	—		
Output Voltage: Low-Level	VOL			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
				15	—	—	—	—	0	—	—	—	—		
High-Level	VOH			5	4.99	—	—	4.99	5	—	4.95	—	—	—	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
				15	—	—	—	—	15	—	—	—	—		
Noise Immunity	VNL	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	—	V	15
		9	10	3	—	—	3	4.5	—	2.9	—	—	—		
		13.5	15	—	—	—	—	6.75	—	—	—	—	—		
	VNH	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—	—		
		1	10	2.9	—	—	3	4.5	—	3	—	—	—		
		1.5	15	—	—	—	—	6.75	—	—	—	—	—		
Output Drive Current: N-Channel (Sink)	IDN	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	—	mA	5, 6
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—	—		
		1.5	15	—	—	—	3	6	—	—	—	—	—		
P-Channel (Source)	IDP	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	—	mA	7, 8
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—	—		
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—	—		
		13.5	15	—	—	—	-3	-6	—	—	—	—	—		
Input Current	II		15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	—	μA	—

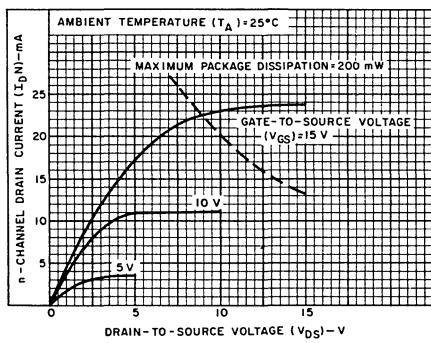


Fig. 5—Typical output n-channel drain characteristics.

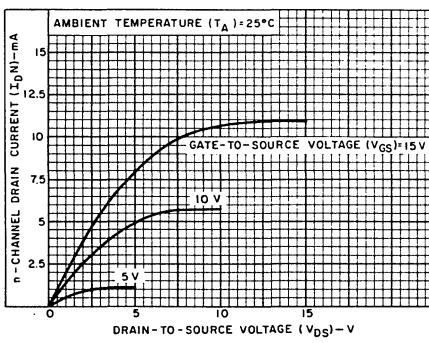


Fig. 6—Minimum output n-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS	Fig. No.	
			VDD Volts	TYP. MAX.			
Propagation Delay Time (Data): High-to-Low Level	$t_{PHL}$		5	225	450	ns	9, 11
			10	90	180		
			15	60	—		
Low-to-High Level	$t_{PLH}$		5	350	700	ns	10, 11
			10	140	280		
			15	100	—		
Propagation Delay Time (Inhibit): High-to-Low Level	$t_{PHL}(\text{INH})$		5	150	300	ns	—
			10	60	120		
			15	40	—		
Low-to-High Level	$t_{PLH}(\text{INH})$		5	250	500	ns	—
			10	100	200		
			15	70	—		
Transition Time	$t_{THL}$ , $t_{TLH}$		5	100	200	ns	12
			10	50	100		
			15	40	80		
Average Input Capacitance	$C_I$	Any Input	5	—	pF	—	—

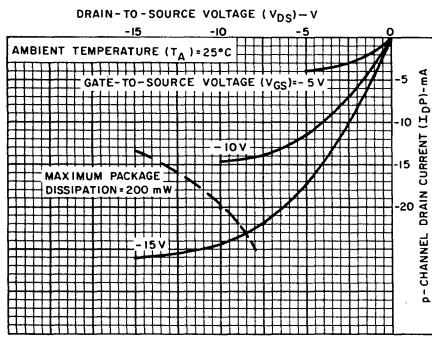


Fig. 7—Typical output p-channel drain characteristics.

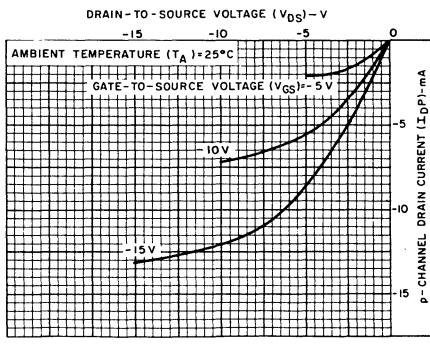


Fig. 8—Minimum output p-channel drain characteristics.

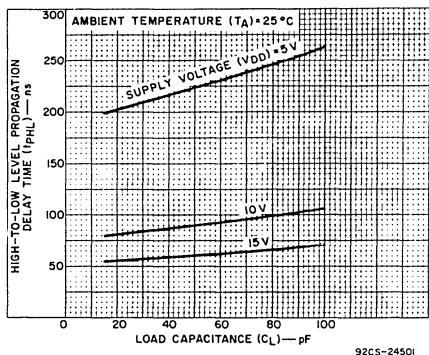


Fig. 9—Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

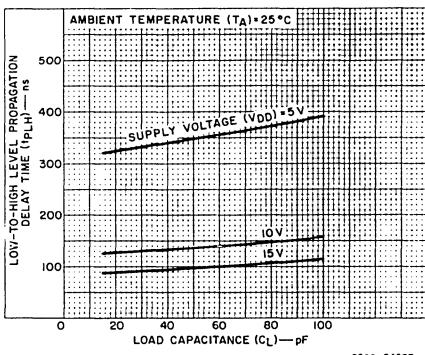


Fig. 10—Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

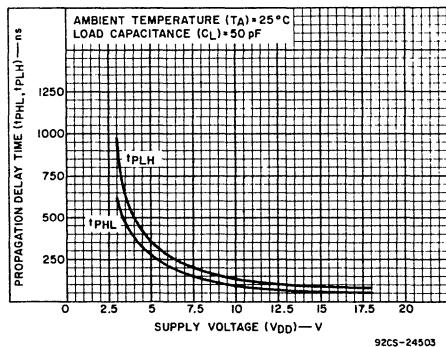


Fig. 11—Typical DATA or ENABLE propagation delay time vs. supply voltage.

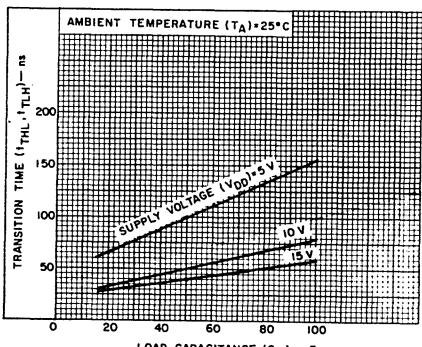


Fig. 12—Typical transition time vs. load capacitance.

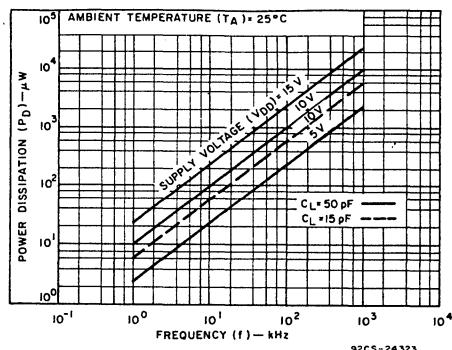


Fig. 13—Typical power dissipation vs. frequency.

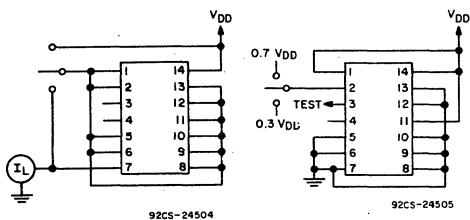
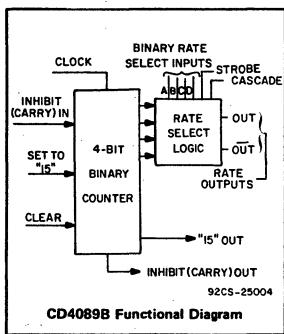


Fig. 14—Quiescent device current test circuit.

Fig. 15—Noise immunity test circuit.

**Preliminary CD4089BE**



The RCA-CD4089B is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural and trigonometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits CD4089B devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figs. 3 and 4). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

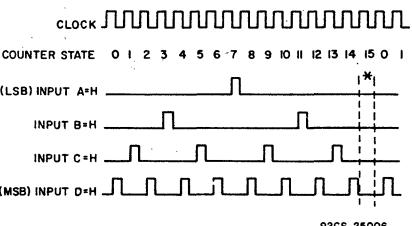
$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16} \times \frac{13}{16} = \frac{143}{256}$$

The CD4089B has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Fig. 1.

If more than one binary input bit is high, the resulting pulse train is a combination of the above separate pulse trains.



\*An output bit may be filled in in this counter state by a less significant CD4089B cascaded in the Add mode.

Fig. 1—Timing diagram.

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			TYPICAL VALUES	UNITS
			$V_O$ V	$V_{DD}$ V		
Quiescent Device Current	$I_L$			5	0.02	$\mu\text{A}$
				10	0.02	
Output Drive Current: All Outputs N-Channel (Sink)	$I_{DN}$		0.4	5	0.8	$\text{mA}$
				0.5	1.8	
				4.6	-0.8	
	$I_{DP}$		5	2.5	-3.2	
				9.5	-1.8	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		$V_{DD}$ V	TYPICAL VALUES	UNITS
Propagation Delay	$t_{PHL}, t_{PLH}$	Clock to "Out"	5	180		$\text{ns}$
			10	90		
	$t_{PLH}, t_{PHL}$	Clock to "Inhibit Out"	5	260		
			10	130		
Transition Time	$t_{TLH}, t_{THL}$		5	100		$\text{ns}$
			10	50		
Maximum Clock Frequency	$f_{CL}(\text{Max.})$		5	2		$\text{MHz}$
			10	4.5		
Maximum Clock Rise and Fall Time	$t_r, t_f(\text{Max.})$		5	15		$\mu\text{s}$
			10			

## MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE .....  $-65 \text{ to } +150^\circ\text{C}$ OPERATING-TEMPERATURE RANGE .....  $-40 \text{ to } +85^\circ\text{C}$ 

## DC SUPPLY-VOLTAGE RANGE

 $V_{DD}$ \* .....  $-0.5 \text{ to } +18 \text{ V}$ DEVICE DISSIPATION (PER PACKAGE) .....  $200 \text{ mW}$ ALL INPUTS .....  $V_{SS} \leq V_I \leq V_{DD}$ 

LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79 \text{ mm}$ )from case for 10 seconds max. .....  $265^\circ\text{C}$ \* All voltage values are referenced to  $V_{SS}$  terminal.OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$ 

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	—	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	—0.5 V to $V_{DD} +$ 0.5 V	V	—

TRUTH TABLE

Inputs										Number of Pulses or Output Logic Level (H or L)			
D	C	B	A	No. of Clock Pulses	InhIN	Strobe	Cascade	Clear	Set	Pin 6 OUT	Pin 5 OUT	Pin 7 InhOUT	Pin 1 "15"
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

\* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

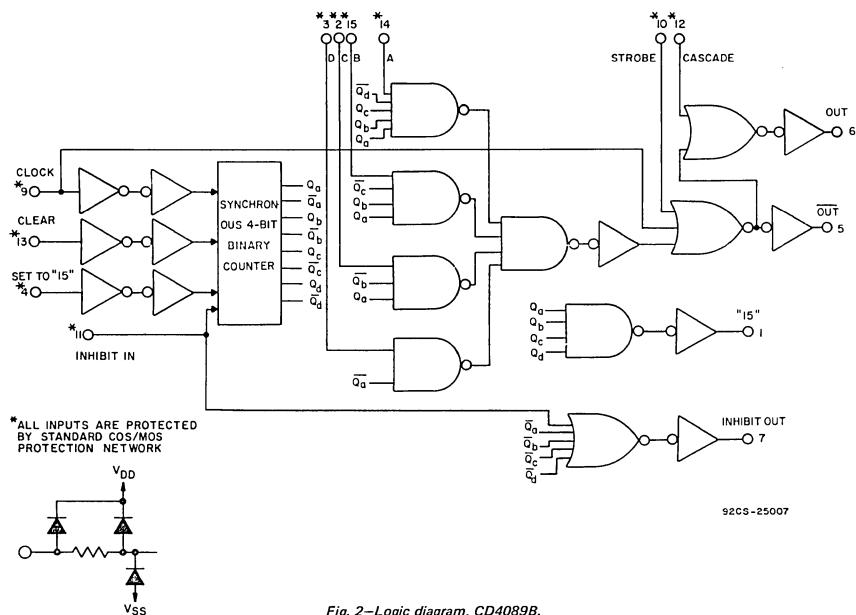


Fig. 2—Logic diagram, CD4089B.

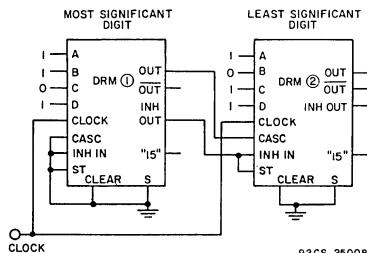


Fig. 3—Two CD4089B's cascaded in the "Add" mode with a preset number of 189.

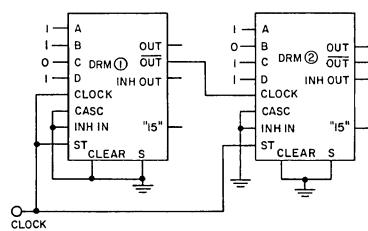


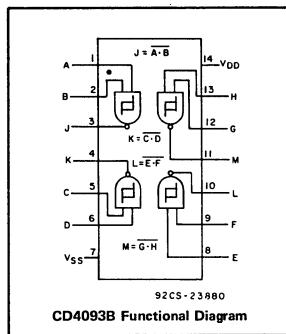
Fig. 4—Two CD4089B's cascaded in the "Multiply" mode with a preset number of 143.



# Digital Integrated Circuits

Monolithic Silicon

## CD4093B Type



### COS/MOS Quad 2-Input NAND Schmitt Triggers

#### Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.6 V at  $V_{DD} = 5$  V and 2 V at  $V_{DD} = 10$  V
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall times
- Standard B-series output drive

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage ( $V_P$ ) and the negative voltage ( $V_N$ ) is defined as hysteresis voltage ( $V_H$ ) (see Fig. 2).

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

The CD4093B is supplied in 14-lead dual-in-line plastic packages (E), welded-seal ceramic packages (D), ceramic packages (F), ceramic flat packs (K), and in chip form (H).

#### Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

#### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE .....  $-65$  to  $+150^\circ\text{C}$

OPERATING-TEMPERATURE RANGE:

CERAMIC-PACKAGE TYPES .....  $-55$  to  $+125^\circ\text{C}$

PLASTIC-PACKAGE TYPES .....  $-40$  to  $+85^\circ\text{C}$

DC SUPPLY-VOLTAGE RANGE

$V_{DD}$  \* .....  $-0.5$  to  $+18$  V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

ALL INPUTS .....  $V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$  mm)  
from case for 10 seconds max. .....  $265^\circ\text{C}$

\* All voltage values are referenced to  $V_{SS}$  terminal.

#### OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	—	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	—0.5 V to $V_{DD} + 0.5$ V	V	—

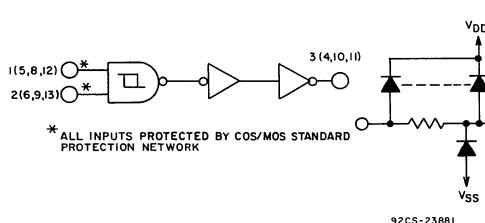


Fig. 1—Functional diagram—1 of 4 Schmitt triggers.

## STATIC ELECTRICAL CHARACTERISTICS

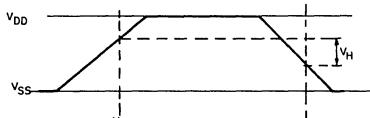
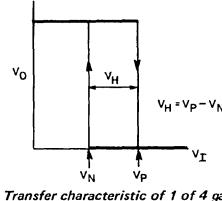
CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4093BD, BF, BK, BH CERAMIC PACKAGE LIMITS								UNITS	FIG. NO.		
		$V_O$	$V_{DD}$	-55°C			25°C			125°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	$I_L$	5	—	—	—	0.5	—	0.01	0.5	—	—	30	$\mu A$	20	
				10	—	—	1	—	0.01	1	—	—	60		
				15	—	—	—	—	0.01	—	—	—	—		
Output Voltage: Low-Level	$V_{OL}$	5	—	—	0.01	—	0	0.01	—	—	—	0.05	V	—	
				10	—	—	0.01	—	0	0.01	—	—	0.05		
				15	—	—	—	—	0	—	—	—	—		
High-Level	$V_{OH}$	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—	
				10	9.99	—	—	9.99	10	—	9.95	—	—		
				15	—	—	—	—	15	—	—	—	—		
Positive Trigger Threshold Voltage	$V_P$	5	—	3	—	2.3	2.9	3.5	—	2.9	—	—	V	2, 4	
				10	—	5.9	—	4.5	5.9	7	—	5.9	—		
				15	—	—	—	—	8.9	—	—	—	—		
Negative Trigger Threshold Voltage	$V_N$	5	—	2.6	—	1.5	2.3	2.7	—	2.1	—	—	V	2, 4	
				10	—	4	—	3	3.9	5.5	—	3.8	—		
				15	—	—	—	—	5.4	—	—	—	—		
Hysteresis Voltage	$V_H$	5	—	0.4	—	0.4	0.6	—	—	0.8	—	—	V	2, 4	
				10	—	1.9	—	1	2	—	—	2.1	—		
				15	—	—	—	—	3.5	—	—	—	—		
Noise Immunity	$V_{NL}$	0	5	—	3	—	2.3	2.9	3.5	—	2.9	—	V	3, 21	
		0	10	—	5.9	—	4.5	5.9	7	—	5.9	—			
		0	15	—	—	—	—	8.9	—	—	—	—			
	$V_{NH}$	5	5	—	2.2	—	2.3	2.7	3.5	—	2.9	—			
		10	10	—	6	—	4.5	6.1	7	—	6.2	—			
		15	15	—	—	—	—	9.6	—	—	—	—			
Output Drive Current: N-Channel (Sink)	$I_{DN}$	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	6, 7	
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—			
		1.5	15	—	—	—	3	6	—	—	—	—			
P-Channel (Source)	$I_{DP}$	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	8, 9	
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—			
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—			
		13.5	15	—	—	—	-3	-6	—	—	—	—			
Input Current	$I_I$		15	—	—	—	—	$\pm 10^{-5}$	$\pm 1$	—	—	—	$\mu A$	—	

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4093BE PLASTIC PACKAGE LIMITS								UNITS	FIG. NO.	
		V <sub>O</sub> V	V <sub>DD</sub> V	-40°C			25°C			85°C				
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current	I <sub>L</sub>	5	—	—	5	—	0.01	5	—	—	70	—	μA	20
		10	—	—	10	—	0.01	10	—	—	140	—		
		15	—	—	—	—	0.01	—	—	—	—	—		
Output Voltage: Low-Level	V <sub>OL</sub>	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—
		10	—	—	0.01	—	0	0.01	—	—	0.05	—		
		15	—	—	—	—	0	—	—	—	—	—		
High-Level	V <sub>OH</sub>	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—
		10	9.99	—	—	9.99	10	—	9.95	—	—	—		
		15	—	—	—	—	15	—	—	—	—	—		
Positive Trigger Threshold Voltage	V <sub>P</sub>	5	—	3	—	2.3	2.9	3.5	—	2.9	—	—	V	2, 4
		10	—	5.9	—	4.5	5.9	7	—	5.9	—	—		
		15	—	—	—	—	8.9	—	—	—	—	—		
Negative Trigger Threshold Voltage	V <sub>N</sub>	5	—	2.6	—	1.5	2.3	2.7	—	2.1	—	—	V	2, 4
		10	—	4	—	3	3.9	5.5	—	3.8	—	—		
		15	—	—	—	—	5.4	—	—	—	—	—		
Hysteresis Voltage	V <sub>H</sub>	5	—	0.4	—	0.4	0.6	—	—	0.8	—	—	V	2, 4
		10	—	1.9	—	1	2	—	—	2.1	—	—		
		15	—	—	—	—	3.5	—	—	—	—	—		
Noise Immunity	V <sub>NL</sub>	0	5	—	3	—	2.3	2.9	3.5	—	2.9	—	V	3, 21
		0	10	—	5.9	—	4.5	5.9	7	—	5.9	—		
		0	15	—	—	—	—	8.9	—	—	—	—		
	V <sub>NH</sub>	5	5	—	2.2	—	2.3	2.7	3.5	—	2.9	—		
		10	10	—	6	—	4.5	6.1	7	—	6.2	—		
		15	15	—	—	—	—	9.6	—	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	6, 7
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—		
		1.5	15	—	—	—	3	6	—	—	—	—		
P-Channel (Source)	I <sub>DP</sub>	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	8, 9
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—		
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—		
Input Current	I <sub>I</sub>	13.5	15	—	—	—	-3	-6	—	—	—	—	μA	—
		15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—		

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20 \text{ ns}$ , and  $C_L = 50 \text{ pF}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	ALL TYPES LIMITS		UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.	
			V <sub>DD</sub> Volts	Typ.	Max.		
Propagation Delay Time	$t_{\text{PHL}}, t_{\text{PLH}}$		5 10 15	300 150 120	600 300 240	ns	10, 12
Transition Time	$t_{\text{THL}}$ $t_{\text{TLH}}$		5 10 15	100 50 40	200 100 80	ns	11
Average Input Capacitance	$C_I$	Any Input	5	—	pF	—	—

a) Definition of  $V_p$ ,  $V_N$ , and  $V_H$ 

b) Transfer characteristic of 1 of 4 gates

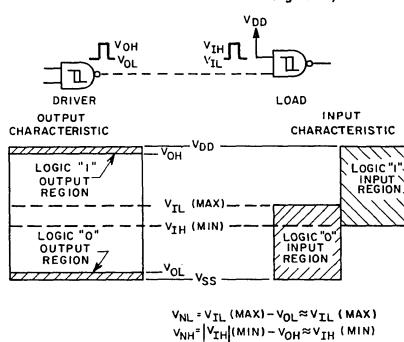
c) Test setup  
92CM-23682

Fig. 3—Input and output characteristics.

92CS-23883RI

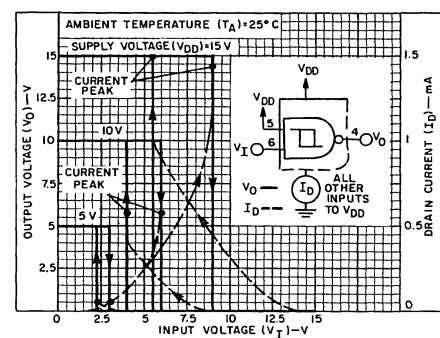


Fig. 4—Typical current and voltage transfer characteristics.

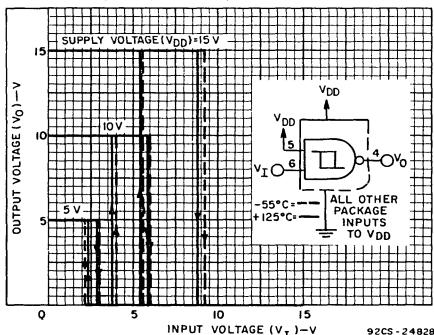


Fig. 5—Typical voltage transfer characteristics as a function of temperature.

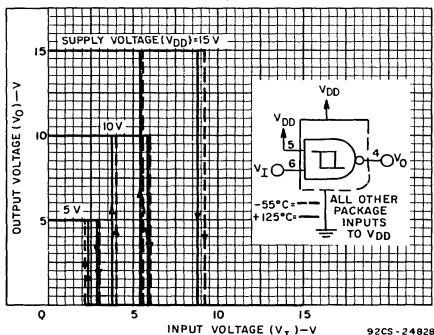


Fig. 6—Typical output-N-channel drain characteristics.

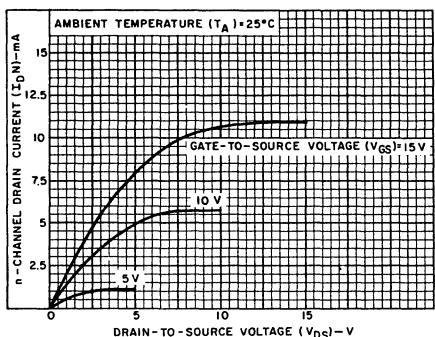


Fig. 7—Minimum output-N-channel drain characteristics.

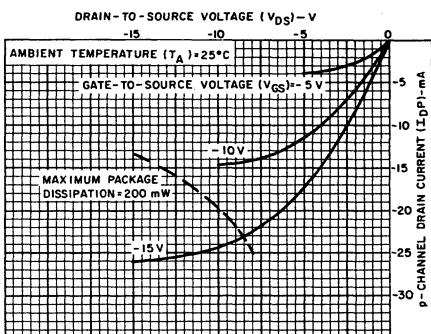


Fig. 8—Typical output-P-channel drain characteristics.

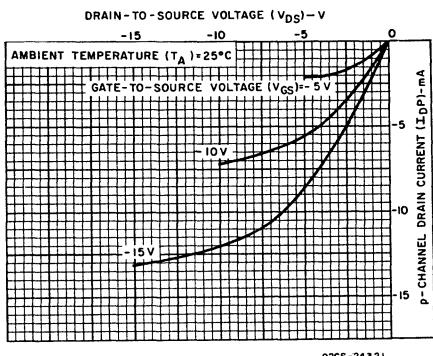


Fig. 9—Minimum output-P-channel drain characteristics.

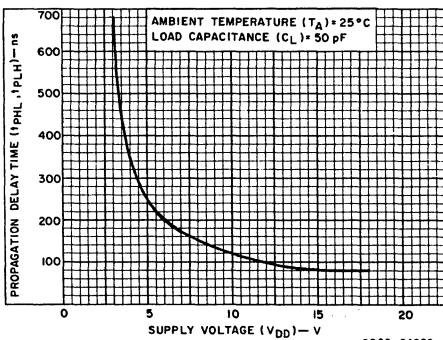


Fig. 10—Typical propagation delay time vs. supply voltage.

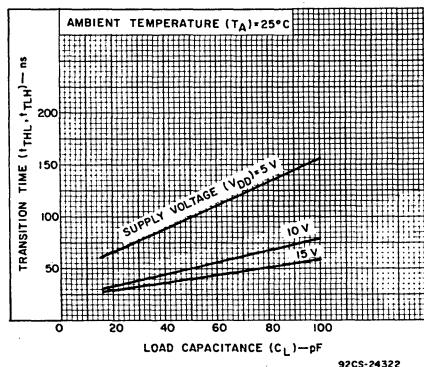


Fig. 11—Typical transition time vs. load capacitance.

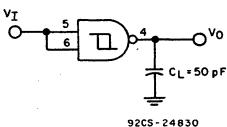


Fig. 12—Propagation delay and transition time test circuit.

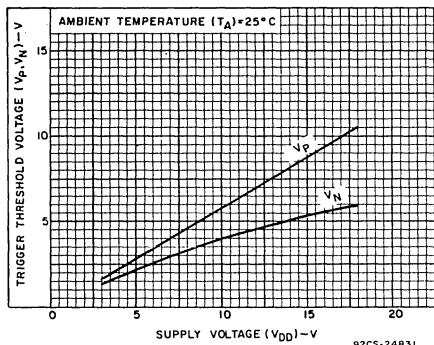
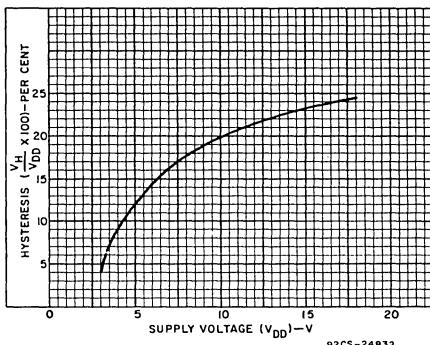
Fig. 13—Typical trigger threshold voltage vs.  $V_{DD}$ .

Fig. 14—Typical per cent hysteresis vs. supply voltage.

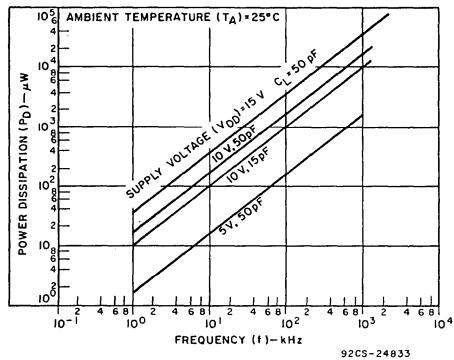


Fig. 15—Typical dissipation characteristics.

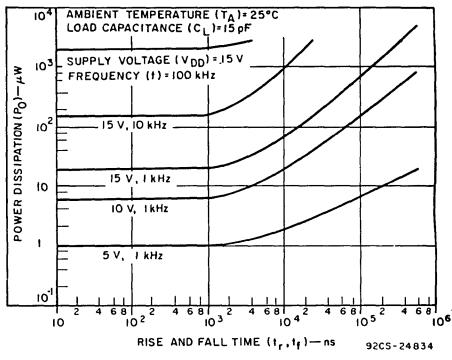


Fig. 16—Power dissipation vs. rise and fall times.

## APPLICATIONS

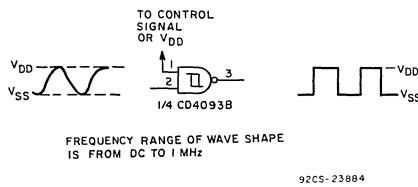


Fig. 17—Wave shaper.

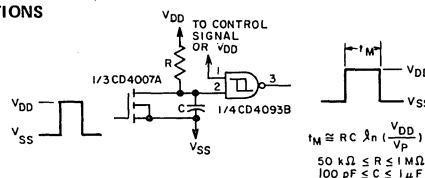
FOR THE RANGE OF  $R$  AND  $C$  GIVEN  $2 \mu\text{s} < I_M < 0.5\text{s}$ 

Fig. 18—Monostable multivibrator. 92CS-23886

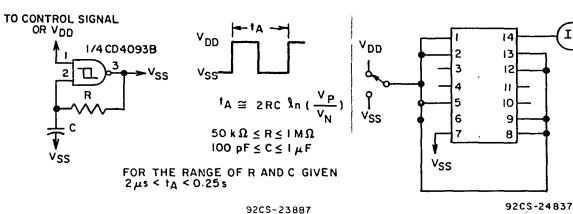


Fig. 19—Astable multivibrator.

Fig. 20—Quiescent device current test circuit.

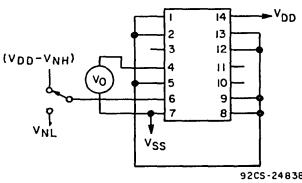
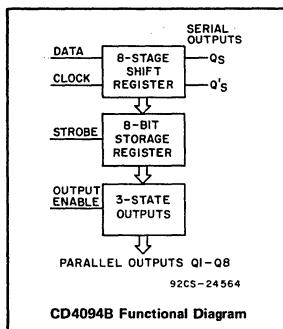


Fig. 21—Noise immunity test circuit.



The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the strobe input is high. Data in the storage register appears at the outputs whenever the output-enable signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q'S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B is supplied in a 16-lead dual-in-line plastic package.

**MAXIMUM RATINGS** *Absolute-Maximum Values:*

MAXIMUM RATINGS, Absolute Maximum Values	
STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE.....	-40 to +85 °C
DC SUPPLY-VOLTAGE RANGE:	
( $V_{DD}^*$ ) .....	-0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .....	200 mW
ALL INPUTS .....	$V_{SS} \leq V_I \leq V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)	
from case for 10 s max.....	+265°C

\* All voltage values are referenced to  $V_{SS}$  terminal.

## TRUTH TABLE

CL <sup>A</sup>	Output Enable	Strobe	Data	Q <sub>I</sub> Out	Q <sub>N</sub> Out	Q <sub>S</sub> Serial Output	Q' <sub>S</sub> Serial Output
	0	X	X	OC	OC	Q7	NC
	0	X	X	OC	OC	NC	Q7
	1	0	X	NC	NC	Q7	NC
	1	1	0	0	Q <sub>N-1</sub>	Q7	NC
	1	1	1	1	Q <sub>N-1</sub>	Q7	NC
	1	1	1	NC	NC	NC	Q7

▲ [Final Chapter](#)

• = Level Change  
× = Don't Care

X = Don't Care  
NC = No Change

NC = No Change

OC = Open Circuit

Logic 1 ≡ High

Logic 1 ≡ High  
Logic 0 ≡ Low

CREATIVE LEADERSHIP

**OPERATING CONDITIONS AT TA = 25°C**  
*For maximum reliability, nominal operating conditions should be*

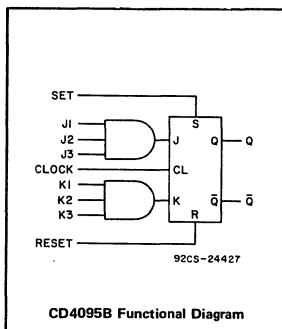
Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	—	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	-0.5 V to V <sub>DD</sub> + 0.5 V	V	—

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		$V_O$ Volts	$V_{DD}$ Volts		
Quiescent Device Current	$I_L$		5	0.5	$\mu\text{A}$
			10	1	
Output Drive Current:  N-Channel (Sink)	$I_{DN}$	$V_I = V_{SS}$	0.4	5	$\text{mA}$
			0.5	10	
			4.6	5	
	$I_{DP}$	$V_I = V_{DD}$	2.5	5	
			9.5	10	
			-	-1.8	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$  (except  $t_{rCL}$  and  $t_{fCL}$ )

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		$V_{DD}$ Volts			
Propagation Delay Time:					
Clock to Serial Out $Q_S$	$t_{PHL}, t_{PLH}$	$t_{PHL}$	5	300	$\text{ns}$
			10	120	
Clock to Serial Out $Q'_S$			5	215	
			10	90	
Clock to Parallel Out			5	375	
		$t_{PLH}$	10	150	
Strobe to Parallel Out			5	300	
			10	120	
Output Enable to Output			5	175	
			10	70	
Transition Time	$t_{THL}, t_{TLH}$	5	100	$\text{ns}$	$\text{ns}$
		10	50		
Minimum Strobe Pulse Width	$t_{WL}, t_{WH}$	5	75	$\text{ns}$	$\text{ns}$
		10	40		
Clock Rise and Fall Time	$t_{rCL}, t_{fCL}$	5	>15	$\mu\text{s}$	$\mu\text{s}$
		10	>15		
Setup Time	$t_{SU}$	5	45	$\text{ns}$	$\text{ns}$
		10	30		
Maximum Clock Frequency	$f_{CL}$ (50% Duty Cycle)	5	2	$\text{MHz}$	$\text{MHz}$
		10	4		
Average Input Capacitance	$C_I$	Any Input		5	$\text{pF}$



## COS/MOS Gated J-K Master-Slave Flip-Flops

With Set-Reset Capability

CD4095B Non-Inverting J and K Inputs

CD4096B Inverting and Non-Inverting J and K Inputs

The RCA-CD4095B and -CD4096B are JK Master/Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated JK inputs control transfer of information into the master section during clocked operation. Information on the JK inputs is transferred to the Q and  $\bar{Q}$  outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095B and CD4096B are supplied in 14-lead dual-in-line plastic packages (CD4095BE, CD4096BE).

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE.....	-40 to +85 °C
DC SUPPLY-VOLTAGE RANGE:	
( $V_{DD}^*$ ) .....	-0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .....	200 mW
ALL INPUTS.....	$V_{SS} \leq V_I \leq V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ....	+265°C

\* All voltage values are referenced to  $V_{SS}$  terminal.

### SYNCHRONOUS OPERATION ( $S=0, R=0$ )

Inputs Before Positive Clock Transition		Inputs After Positive Clock Transition	
J*	K*	Q	$\bar{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Toggles	

\*For CD4095B  
 $J = J_1 \cdot J_2 \cdot J_3$   
 $K = K_1 \cdot K_2 \cdot K_3$   
For CD4096B  
 $J = J_1 \cdot J_2 \cdot \bar{J}_3$   
 $K = K_1 \cdot K_2 \cdot \bar{K}_3$

### ASYNCHRONOUS OPERATION (J and K = DON'T CARE)

S	R	Q	$\bar{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	1	1

$$0 = V_{SS}, 1 = V_{DD}$$

### OPERATING CONDITIONS AT $T_A = 25^\circ C$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

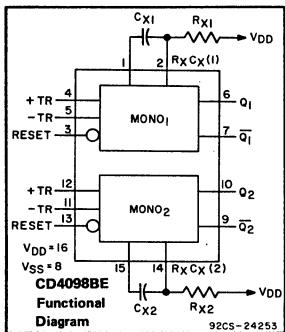
Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	-	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD} + 0.5$ V	V	-

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4095B, CD4096B TYPICAL VALUES	UNITS
		$V_O$	$V_{DD}-V_{SS}$		
Quiescent Device Current	$I_L$		5	0.01	$\mu\text{A}$
			10	0.02	
Output Device Current: N-Channel (Sink)	$I_{DN}$	0.4	5	0.8	$\text{mA}$
		0.5	10	1.8	
	$I_{DP}$	4.6	5	-0.8	
		2.5	5	-1.8	
		9.5	10	-1.8	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		CD4095B, CD4096B TYPICAL VALUES	UNITS
		$V_O$	$V_{DD}-V_{SS}$		
<b>Clocked Operation (Synchronous)</b>					
Propagation Delay Time	$t_{PHL}, t_{PLH}$		5	200	$\text{ns}$
			10	100	
Transition Time	$t_{THL}, t_{TLH}$		5	100	$\text{ns}$
			10	50	
Minimum Clock Pulse Width	$t_{WL}, t_{WH}$		5	75	$\text{ns}$
			10	30	
Maximum Clock Rise and Fall Time	$t_{rCL}, t_{fCL}$		5	15	$\mu\text{s}$
			10	5	
Setup Time	$t_{SUHL}, t_{SULH}$		5	150	$\text{ns}$
			10	75	
Maximum Clock Frequency (Toggle Mode)	$f_{CL}$		5	6	$\text{MHz}$
			10	16	
<b>Set and Reset Operation (Asynchronous)</b>					
Propagation Delay Time	$t_{PHL(R)}, t_{PLH(S)}$		5	175	$\text{ns}$
			10	85	
Minimum Pulse Width	$t_{WH(S)}, t_{WH(R)}$		5	100	$\text{ns}$
			10	50	
Average Input Capacitance	$C_I$	Any Input		5	$\text{pF}$



## COS/MOS Dual Monostable Multivibrator

Retriggerable/Resettable

### Features:

- Trigger propagation delays independent of  $R_X$ ,  $C_X$
- Triggering from leading or trailing edge
- Q and  $\bar{Q}$  buffered outputs available
- Separate resets
- Wide range of output-pulse widths
- Equal source and sink currents

### Applications:

- Pulse delay and timing
- Pulse shaping
- Astable Multivibrator

The RCA CD4098BE dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor ( $R_X$ ) and an external capacitor ( $C_X$ ) control the timing for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. The time delay from trigger input to output transition (trigger propagation delay) is independent of  $R_X$  and  $C_X$ .

Leading-edge-triggering ( $+T_R$ ) and trailing-edge-triggering ( $-T_R$ ) inputs are provided for triggering from either edge of an input pulse. An unused  $+T_R$  input should be tied to  $V_{SS}$ . An unused  $-T_R$  input should be tied to  $V_{DD}$ . A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to  $V_{DD}$ . However, if an entire

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE	.....	-65 to +150	°C
OPERATING-TEMPERATURE RANGE	.....	-40 to +85	°C
DC SUPPLY-VOLTAGE RANGE	.....		
$V_{DD}$	.....	-0.5 to +18	V
DEVICE DISSIPATION (PER PKG.)	.....	200	mW
ALL INPUTS	.....	$V_{SS} \leq V_I \leq V_{DD}$	

### OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	-	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD} +$ 0.5 V	V	-

\* All voltage values are referenced to  $V_{SS}$  terminal.

section of the CD4098BE is not used, its RESET should be tied to  $V_{SS}$ . See Table I.

In normal operation, the circuit retriggers on the application of each new pulse. To prevent retriggering when leading-edge triggering is used,  $\bar{Q}$  must be connected to  $-T_R$ . To prevent retriggering when trailing-edge triggering is used, Q must be connected to  $+T_R$ .

The time period (T) for this multivibrator can be approximated by:  $T_X = R_X C_X$ . Time periods as a function of  $R_X$  for values of  $C_X$  and  $V_{DD}$  are given in Fig. 1.

All outputs are independently buffered to provide equal source- and sink-current capabilities. The CD4098BE is available in a 16-lead dual-in-line plastic package (CD4098BE). This device is similar to type MC14528.

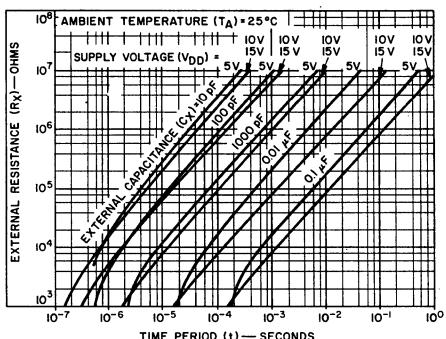


Fig. 1 —  $R_X$  vs. time period for various values of  $V_{DD}$  and  $C_X$ .

**TABLE I**  
**CD4098BE FUNCTIONAL TERMINAL CONNECTIONS**

FUNCTION	TO V <sub>DD</sub>		TO V <sub>SS</sub>		INPUT PULSE TO		OTHER CONNECTIONS	
	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>
LEADING-EDGE TRIGGER/ RETRIGGERABLE	3, 5	11, 13			4	12		
LEADING-EDGE TRIGGER/ NON-RETRIGGERABLE	3	13			4	12	5-7	11-9
TRAILING-EDGE TRIGGER/ RETRIGGERABLE	3	13	4	12	5	11		
TRAILING-EDGE TRIGGER/ NON-RETRIGGERABLE	3	13			5	11	4-6	12-10
UNUSED SECTION	5	11	3, 4	12, 13				

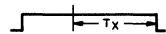
## NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD  $T_X$  REFERENCED FROM THE APPLICATION OF THE LAST INPUT PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD  $T_X$  REFERENCED FROM THE APPLICATION OF THE FIRST INPUT PULSE.

## INPUT PULSE TRAIN



## RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)



## NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

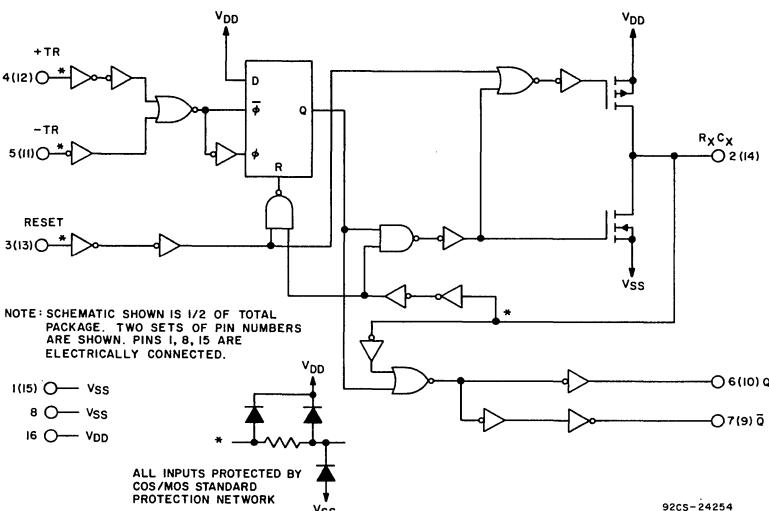
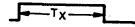


Fig. 2 — CD4098BE dual monostable multivibrator logic diagram.

STATIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		$V_O$ VOLTS	$V_{DD}$ VOLTS		
Quiescent Device Current	$I_L$		5	0.01	$\mu\text{A}$
			10	0.02	
Quiescent Device Dissipation/ Package	$P_D$		5	0.05	$\mu\text{W}$
			10	0.2	
Noise Immunity (Any Input)	$V_{NL}$	0.8	5	2.25	$\text{V}$
		1	10	4.5	
	$V_{NH}$	4.2	5	2.25	
		9	10	4.5	
Output Drive Current: N-Channel (Sink)	$I_{DN}$	0.4	5	0.8	$\text{mA}$
		0.5	10	1.8	
P-Channel (Source)	$I_{DP}$	4.6	5	-0.8	$\text{mA}$
		9.5	10	-1.8	
		2.5	5	-1.8	

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		$V_{DD}$ V	TYPICAL VALUES	UNITS
		$R_X$ ( $\text{k}\Omega$ )	$C_X$ ( $\text{pF}$ )			
Trigger Propagation Delay Time $+TR, -TR$ to $Q, \bar{Q}$	$t_{PLH}, t_{PHL}$	5	15	5 10	350 125	ns
		10	1000	5 10	350 125	
Minimum Trigger Pulse Width	$t_{WL}, t_{WH}$	5	15	5 10	75 30	ns
		10	1000	5 10	75 30	
Transition Time	$t_{THL}, t_{TLH}$	5	15	5 10	100 50	ns
		10	1000	5 10	125 75	
Reset Propagation Delay Time	$t_{PLH}, t_{PHL}$	5	15	5 10	400 150	ns
		10	1000	5 10	1100 700	
Minimum Reset Pulse Width	$t_{WL}$	5	15	5 10	50 25	ns
		10	1000	5 10	750 500	
Average Input Capacitance	$C_I$	Any Input			5	pF

## APPLICATIONS

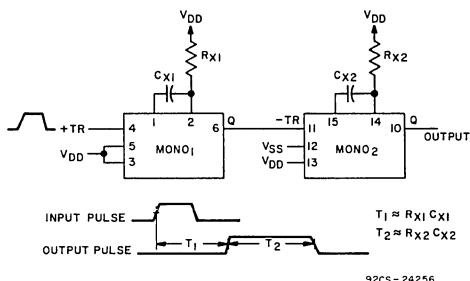


Fig. 3 – Pulse delay.

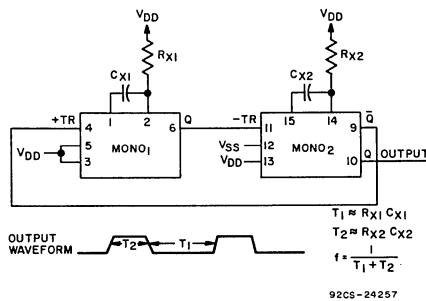


Fig. 4 – Astable multivibrator.



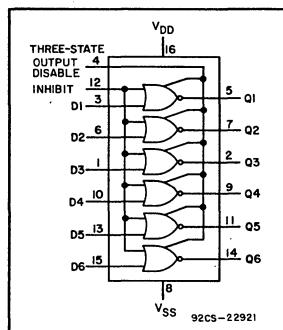
STATIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL		TEST CONDITIONS		TYPICAL VALUES	UNITS
			$V_O$ Volts	$V_{DD}$ Volts		
Quiescent Device Current	$I_L$			5	0.01	$\mu\text{A}$
				10	0.02	
Output Drive Current: N-Channel (Sink)	$I_{DN}$	$V_I = V_{DD}$	0.4	5	0.8	$\text{mA}$
			0.5	10	1.8	
	$I_{DP}$	$V_I = V_{SS}$	4.6	5	-0.8	
			2.5	5	-3.2	
			9.5	10	-1.8	

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL		TEST CONDITIONS		TYPICAL VALUES	UNITS	
			*	$V_{DD}$ Volts			
Propagation Delay: Data to Output	$t_{PLH},$ $t_{PHL}$	A0, A1, A2 Stable Write Disable, Reset = "0"	(1)	5	200	ns	
				10	85		
Write Disable to Output	$t_{PLH},$ $t_{PHL}$	A0, A1, A2 Stable Reset = "0"	(2)	5	225	ns	
				10	100		
Reset to Output	$t_{PHL}$		(3)	5	190	ns	
				10	85		
Minimum Pulse Width: Data	$t_{WL},$ $t_{WH}$		(4)	5	15	ns	
				10	5		
Address	$t_{WL},$ $t_{WH}$			5	0	ns	
				10	0		
Reset	$t_{WH}$		(5)	5	120	ns	
				10	60		
Setup Time: Data to Write Disable	$t_{SU}$	A0, A1, A2 Stable Reset = "0"	(6)	5	235	ns	
				10	105		
Write Disable to Address		Reset = "0"	(7)	5	80		
				10	35		
Hold Time: Address to Write Disable	$t_{HOLD}$	Reset = "0"	(8)	5	200	ns	
				10	100		
Data to Write Disable	$t_{HOLD}$	A0, A1, A2 Stable Reset = "0"	(9)	5	45	ns	
				10	15		

\* Circled numbers refer to times indicated on master timing diagram.



RCA-CD4502B contains six inverter/buffers with 3-state outputs. When the disable control input is at a logical 1, all six outputs become high impedance ( $> 10 \text{ M}\Omega$ ). This feature simplifies design by allowing common bussing of the outputs.

The CD4502B is also provided with an inhibit control which, when at logical 1, switches all six outputs to logical 0.

The CD4502B is supplied in a 16-lead dual-in-line plastic package (CD4502BE).

This device is similar to type MC14502.

#### OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	—	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	-0.5 V to V <sub>DD</sub> + 0.5 V	V	—

DISABLE	INHIBIT	Dn	On
0	0	0	1
0	1	X	0
1	X	X	HIGH IMPEDANCE

X = DON'T CARE

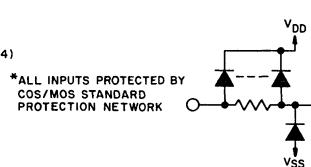
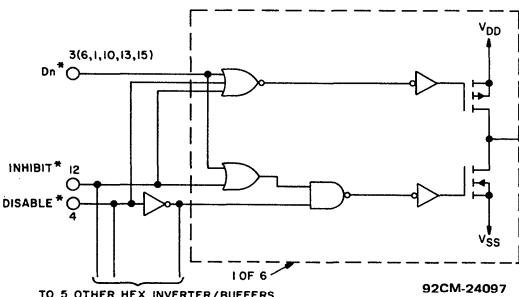
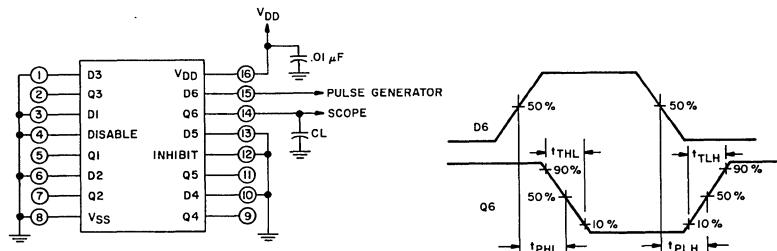


Fig.1 – Schematic Diagram – Input circuit and 1 of 6 identical inverter/buffers.

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS	CHARACTERISTIC CURVES AND TEST CIRCUITS Fig. No.	
		$V_o$	$V_{DD}$				
Quiescent Device Current	$I_L$			5 10	0.002 0.004	$\mu\text{A}$	—
Quiescent Device Dissipation/Package	$P_D$			5 10	0.01 0.04	$\mu\text{W}$	—
Output Voltage:							
Low Level	$V_{OL}$	$V_I = V_{DD}$ $I_O = 0$		5 10	0 0	V	—
High Level	$V_{OH}$	$V_I = V_{SS}$ $I_O = 0$		5 10	5 10	V	—
Noise Immunity	$V_{NL}$	$I_O = 0$	4.2 9	5 10	2.25 3.5	V	—
	$V_{NH}$		0.8 1	5 10	2.25 6.5	V	—
Output Drive Current :							
n-Channel (Sink)	$I_{DN}$	$V_I = V_{DD}$	0.4 0.5	5 10	5.7 12.5	mA	4
p-Channel (Source)	$I_{DP}$	$V_I = V_{SS}$	4.6 2.5 9.5	5 5 10	-0.8 -3.2 -1.8	mA	5

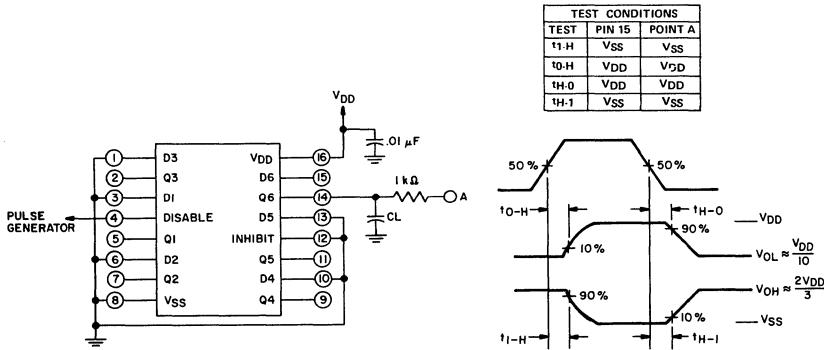


92CM-24098

Fig.2 — Data transition times &amp; delay times test circuit &amp; waveforms.

DYNAMIC CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$  AND  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS	CHARACTERISTIC CURVES AND TEST CIRCUITS Fig. No.
			V <sub>DD</sub> V			
Data or Inhibit Delay Times: High to Low	$t_{pH_L}$		5	135	ns	2
Low to High	$t_{pLH}$		10	55		
Disable Delay Times: Output 1 to High Impedance	$t_{1-H}$	See Fig.3	5	65	ns	3
High Impedance to Output 1	$t_{H-1}$		10	30		
Output 0 to High Impedance	$t_{0-H}$		5	260		
High Impedance to Output 0	$t_{H-0}$		10	105		
Transition Times:						
Low to High	$t_{TLH}$		5	100	ns	2
High to Low	$t_{THL}$		10	50		
Average Input Capacitance	$C_I$			5	pF	



92CM-24099.

Fig.3 – Disable delay times test circuit and waveforms.

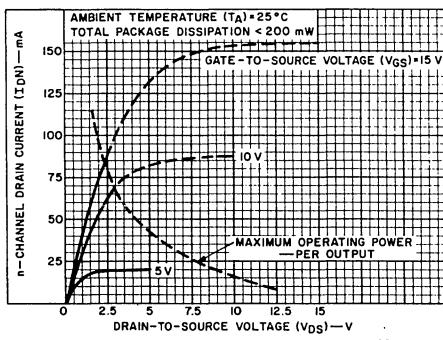


Fig. 4 – Typical n-channel drain characteristics.

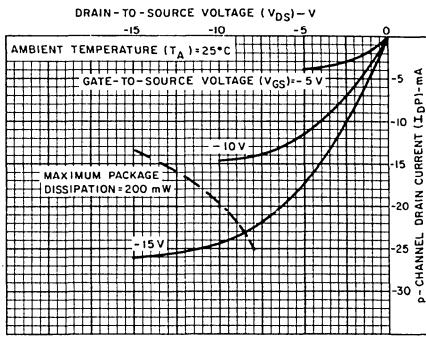
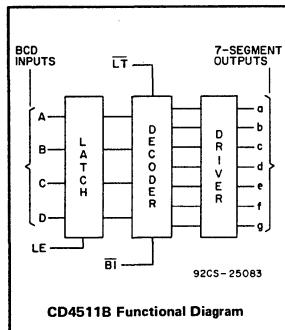
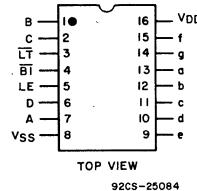
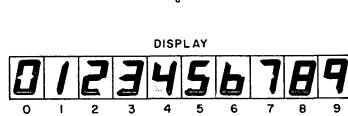


Fig. 8—Typical output-P-channel drain characteristics.

**Preliminary CD4511BE**



## COS/MOS BCD-to-Seven-Segment Latch Decoder Driver



**CD4511B**  
**TERMINAL ASSIGNMENT**

The RCA-CD4511B is a BCD-to-Seven-Segment Latch Decoder Driver constructed with COS/MOS logic and n-p-n bipolar transistor output drivers on a single monolithic structure. This device combines the low quiescent power dissipation and high noise immunity features of RCA COS/MOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B to drive LED's and other displays directly.

Lamp Test ( $\bar{LT}$ ) Blanking ( $\bar{BI}$ ) and Latch Enable (LE) inputs are provided to test the display, shut off or intensity modulate it, and store a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

The CD4511B is supplied in a 16-lead dual-in-line plastic package (CD4511BE).

This device is similar to type MC14511.

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE.....	-40 to +85 °C
DC SUPPLY-VOLTAGE RANGE	
V <sub>DD</sub> .....	-0.5 to +18 V
MAXIMUM CONTINUOUS OUTPUT	
DRIVE CURRENT/OUTPUT .....	25 mA
MAXIMUM CONTINUOUS OUTPUT	
POWER/OUTPUT .....	50 mW
ALL INPUTS .....	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ....	265°C

\* All voltage values are referenced to V<sub>SS</sub> terminal.

### OPERATING CONDITIONS AT T<sub>A</sub> = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	-	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	-0.5 V to V <sub>DD</sub> + 0.5 V	V	-

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			TYPICAL VALUES	UNITS
		$I_{OH}$ mA	$V_{OL}$ V	$V_{DD}$ V		
Quiescent Device Current	$I_L$			5	5	mA
				10	10	
Output Drive Voltage  High-Level (Source)	$V_{OH}$	0		5	4.5	V
		10		5	4.1	
		25		5	3.5	
		0		10	9.5	
		10		10	9.1	
		25		10	8.7	
Output Drive Current (Sink)	$I_{OL}$		0.4	5	0.8	mA
			0.5	10	2	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 15 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
			$V_{DD}$ V		
Propagation Delay:  High-to-Low	$t_{PHL}$		5	720	ns
			10	290	
		$t_{PLH}$	5	640	
			10	250	
Transition Time:  High-to-Low	$t_{THL}$		5	30	ns
			10	17	
		$t_{TLH}$	5	1000	
			10	1000	
Setup Time	$t_{SU}$		5	90	ns
			10	38	
Hold Time	$t_{HOLD}$		5	-90	ns
			10	-38	
Minimum Latch Enable Pulse Width	$t_W(\text{LE})$		5	260	ns
			10	110	
Average Input Capacitance	$C_I$	Any Input		5	pF

TRUTH TABLE

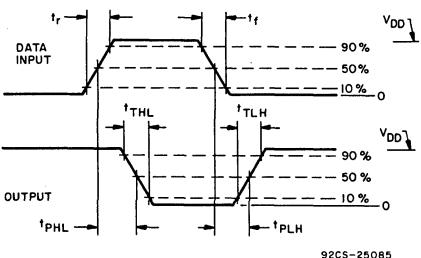
LE	$\bar{B}_1$	$\bar{L}_T$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	0	0	1	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	0	0	1	1	0	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	0	0	1	1	1	1	1	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	0	0	1	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*	*	*	*	*	*	*	

 $X \equiv$  Don't Care

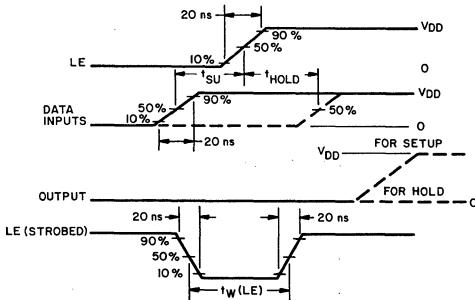
\*Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD &gt; 1001).

DYNAMIC WAVEFORMS



92CS-25085



92CS-25086

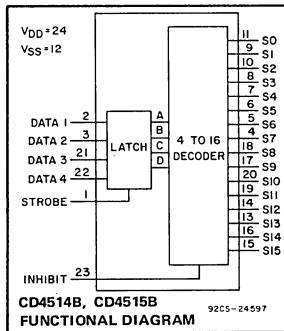


# Digital Integrated Circuits

Monolithic Silicon

## CD4514B Types

## CD4515B Types



The RCA-CD4514B<sup>▲</sup> and -CD4515B<sup>▲</sup> are monolithic integrated circuits consisting of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0 (CD4514B) or 1 (CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are supplied in 24-lead ceramic packages. They are also available in chip form. These devices are similar to the types MC14514 and MC14515.

<sup>▲</sup> Formerly CD4064A and CD4065A, respectively.

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE.....	-55 to +125°C
DC SUPPLY-VOLTAGE RANGE	
V <sub>DD</sub> *	-0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .....	200 mW
ALL INPUTS .....	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)	
from case for 10 seconds max. ....	265°C

\* All voltage values are referenced to V<sub>SS</sub> terminal.

## COS/MOS 4-Bit Latch/4-to-16 Line Decoder

CD4514B Output "High" on Select  
CD4515B Output "Low" on Select

### Features:

- Strobed input latch
- Inhibit control

### Applications:

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding
- Program-counter decoding
- Control decoder

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS				SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	0	1	0	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care

**OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$** 

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	—	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD} + 0.5$ V	V	—
Setup Time	5 10	250 100	None	ns	A
Strobe Pulse Width	5 10	350 100	None	ns	A

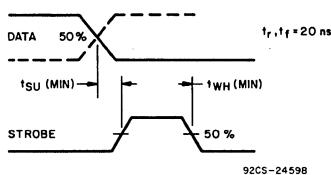


Fig. A—Waveforms for setup time and strobe pulse width.

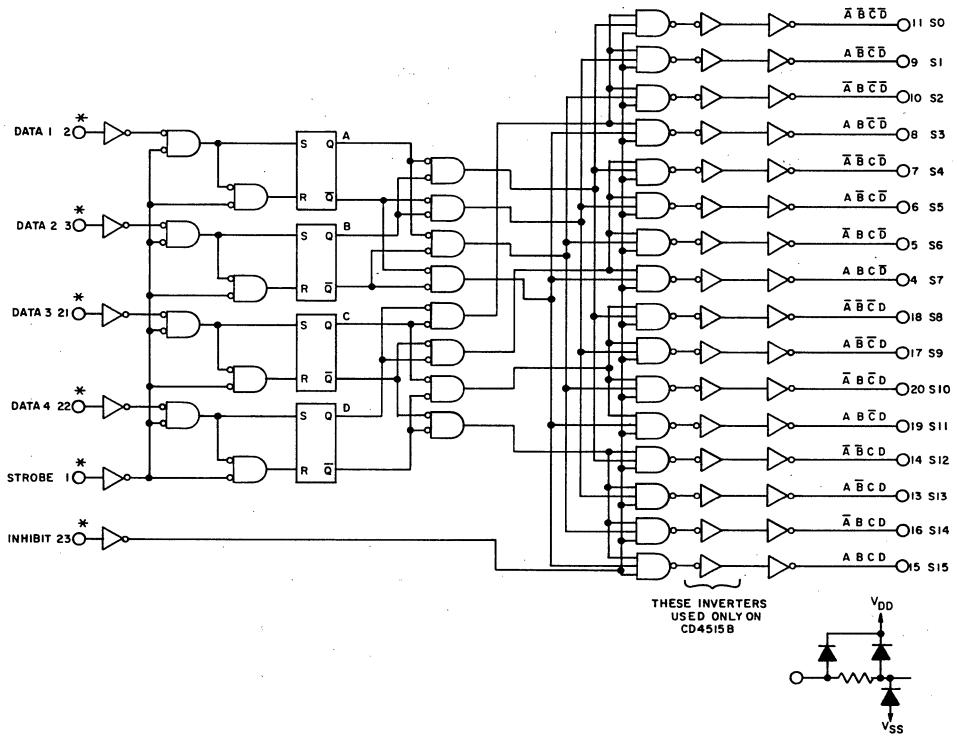


Fig. 1—Logic diagram for CD4514B and CD4515B.

\* ALL INPUTS PROTECTED BY STANDARD COS/MOS PROTECTION NETWORK

92CL-23770RI

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CERAMIC PACKAGE LIMITS								UNITS	FIG. NO.		
		V <sub>O</sub> (V)	V <sub>DD</sub>	-55°C			25°C			125°C					
				▲	●	V	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>			5	—	—	5	—	0.02	5	—	—	300	μA	3
				10	—	—	10	—	0.02	10	—	—	600		
				15	—	—	—	—	0.02	—	—	—	—		
Output Voltage Low-Level	V <sub>OL</sub>			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
				15	—	—	—	—	0	—	—	—	—		
High-Level	V <sub>OH</sub>			5	4.99	—	—	4.99	5	—	4.95	—	—	—	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
				15	—	—	—	—	15	—	—	—	—		
Noise Immunity Any Input	V <sub>NL</sub>	0.8	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	2
		1	9	10	3	—	—	3	4.5	—	2.9	—	—		
		1.5	13.5	15	—	—	—	—	6.75	—	—	—	—		
Noise Immunity Any Input	V <sub>NH</sub>	4.2	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—	V	2
		9	1	10	2.9	—	—	3	4.5	—	3	—	—		
		13.5	1.5	15	—	—	—	—	6.75	—	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>			0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	mA	4, 7, 8
				0.5	10	1.1	—	—	0.9	2	—	0.65	—		
				1.5	15	—	—	—	—	7.8	—	—	—		
P-Channel (Source)	I <sub>DP</sub>			4.6	5	-0.25	—	—	-0.2	-0.4	—	-0.15	—	mA	4, 9, 10
				2.5	5	-1	—	—	-0.8	-1.6	—	-0.60	—		
				9.5	10	-0.62	—	—	-0.5	-0.9	—	-0.35	—		
Input Current	I <sub>I</sub>	Any Input	15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—

▲ For CD4514B

● For CD4515B

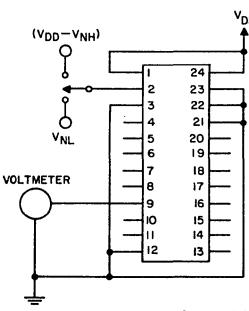


Fig. 2—Noise immunity test circuit.

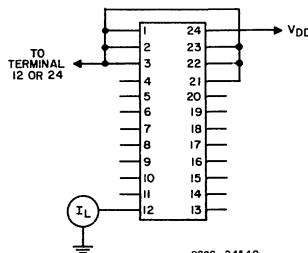
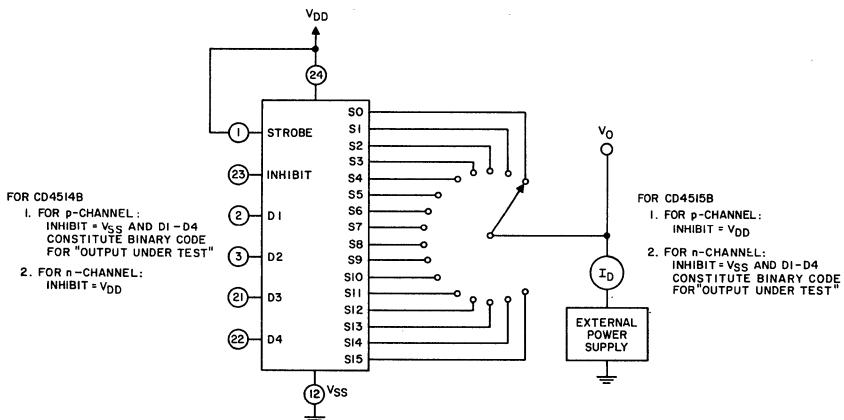


Fig. 3—Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS	CHARAC- TERISTIC CURVES & TEST CKTS. Fig. No.			
			$V_{DD}$ Volts	TYP.	MAX.				
Propagation Delay Time: Strobe or Data	$t_{PHL},$ $t_{PLH}$		5	550	1100	ns	6, 11, 15		
			10	225	450				
			15	150	—				
Inhibit			5	400	800	ns	6, 12		
			10	150	300				
			15	100	—				
Transition Time: High-to-Low	$t_{THL}$		5	100	200	ns	6, 14		
			10	50	100				
			15	40	80				
	$t_{TLH}$		5	200	400	ns	6, 13		
			10	100	200				
			15	80	160				
Average Input Capacitance	$C_I$	Any Input	5	—	pF	—	—		



92CS-24541

Fig. 4—Drain characteristics test circuit.

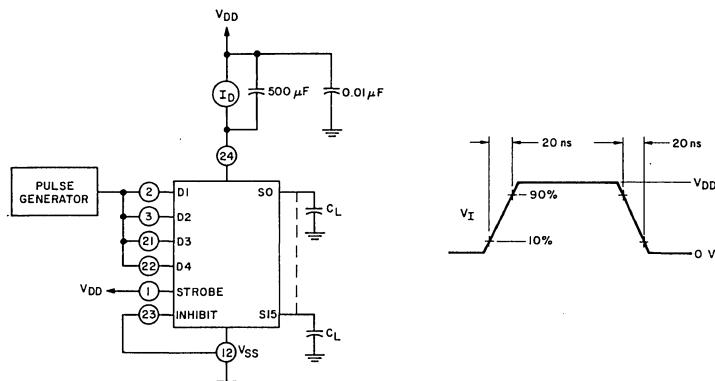


Fig. 5—Dynamic power dissipation test circuit and waveform.

92CS-24542

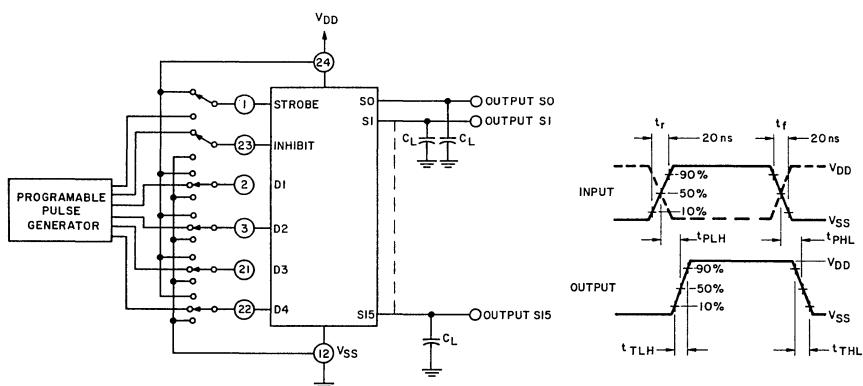
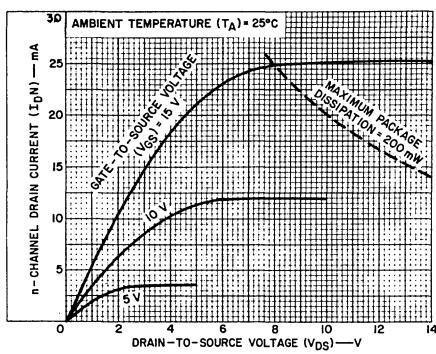


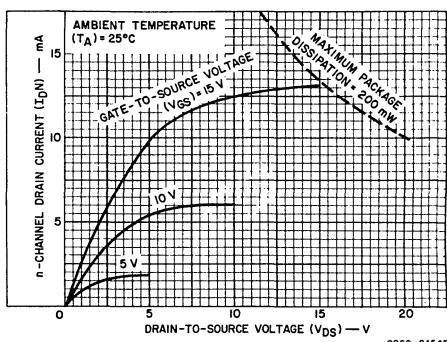
Fig. 6—Switching time test circuit and waveforms.

92CS-24543



92CS-24544

Fig. 7—Typical output-N-channel drain characteristics.



92CS-24545

Fig. 8—Minimum output-N-channel drain characteristics.

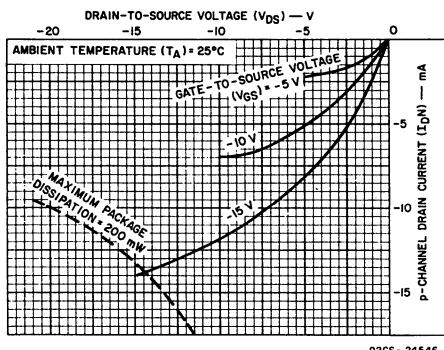


Fig. 9—Typical output-P-channel drain characteristics.

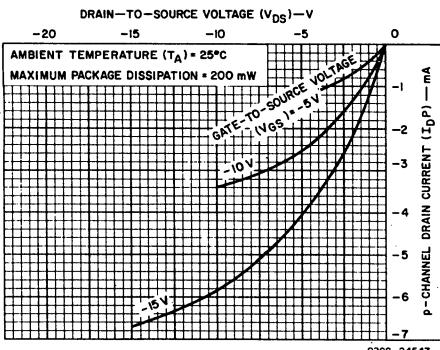


Fig. 10—Minimum output-P-channel drain characteristics.

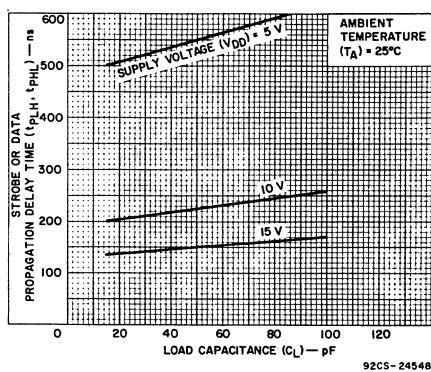


Fig. 11—Typical strobe or data propagation delay time vs. load capacitance.

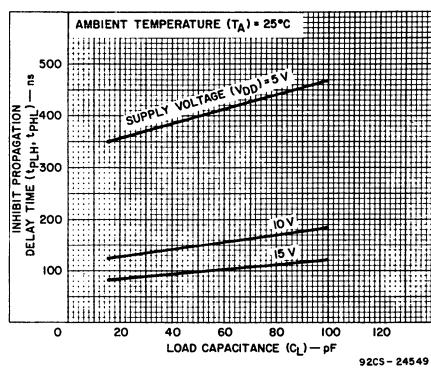


Fig. 12—Typical inhibit propagation delay time vs. load capacitance.

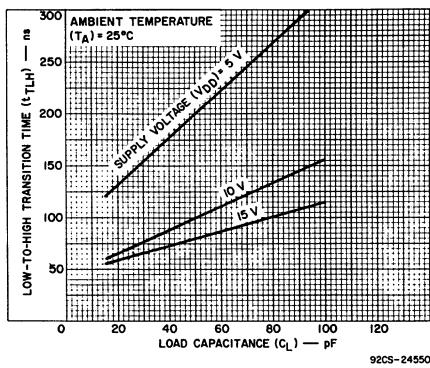


Fig. 13—Typical low-to-high transition time vs. load capacitance.

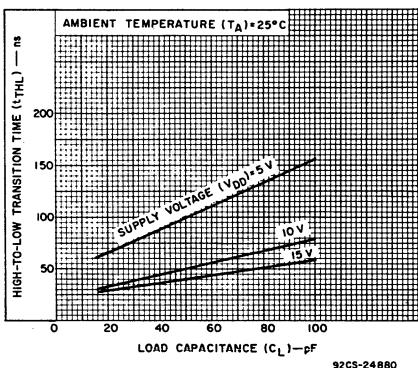


Fig. 14—Typical high-to-low transition time vs. load capacitance.

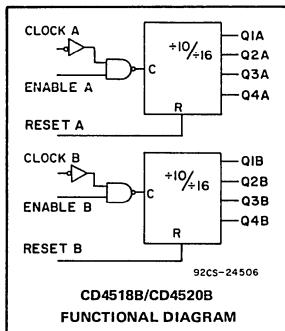


## Digital Integrated Circuits

Monolithic Silicon

CD4518B Types

CD4520B Types



The RCA-CD4518B\* Dual BCD Up Counter and CD4520B\* Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained "high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines.

The counter can be cascaded in the ripple mode by connecting Q4 of the enable input of the subsequent counter while the clock input of the latter is held low.

All outputs have equal source- and sink-current capabilities and conform to standard B-Series output drive (see Static Electrical Characteristics).

The CD4518B and CD4520B are available in 16-lead dual-in-line plastic packages (E), dual-in-line welded-seal ceramic packages (D), dual-in-line ceramic packages (F), ceramic flat packs (K), and in chip form (H).

These devices are similar to types MC14518 and MC14520.

\* Formerly CD4083A and CD4084A, respectively.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

STORAGE-TEMPERATURE RANGE..... -65 to +150°C

OPERATING-TEMPERATURE RANGE:

CERAMIC-PACKAGE TYPES ..... -55 to +125°C

PLASTIC-PACKAGE TYPES ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE

$V_{DD}$  ^ ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79 mm)

from case for 10 seconds max. ..... 265°C

<sup>▲</sup> All voltage values are referenced to  $V_{SS}$  terminal.

**COS/MOS Dual Up Counters**

CD4518B Dual BCD Up Counter

CD4520B Dual Binary Up Counter

**Features:**

- Medium-speed operation — 6-MHz typical clock frequency at 10 V
- Positive- or negative-edge triggering
- Standard B-series output drive
- Synchronous internal carry propagation

**Applications:**

- Multistage synchronous counting
- Multistage ripple counting
- Synchronous frequency dividers

**OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$** 

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	—	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD} +$ 0.5 V	V	—
Enable Pulse Width	5 10 15	440 200 140	None	ns	—
Clock Pulse Width	5 10 15	200 100 70	None	ns	—
Clock Input Frequency	5 10 15	DC	1.5 3 4	MHz	—
Clock or Enable Input Rise or Fall Time	4 - 15	None	15	$\mu\text{s}$	—
Reset Pulse Width	5 10 15	250 110 80	None	ns	—

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4518BD, BF, BK, BH CD4520BD, BF, BK, BH CERAMIC PACKAGE LIMITS								UNITS	FIG. NO.		
		VO Volts	VDD Volts	-55°C			25°C			125°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>			5	—	—	5	—	0.02	5	—	—	300	μA	16
				10	—	—	10	—	0.02	10	—	—	600		
				15	—	—	—	—	0.02	—	—	—	—		
Output Voltage Low-Level	V <sub>OL</sub>			5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
				10	—	—	0.01	—	0	0.01	—	—	0.05		
				15	—	—	—	—	0	—	—	—	—		
High-Level	V <sub>OH</sub>			5	4.99	—	—	4.99	5	—	4.95	—	—	—	—
				10	9.99	—	—	9.99	10	—	9.95	—	—		
				15	—	—	—	—	15	—	—	—	—		
Noise Immunity	V <sub>NL</sub>	0.8	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	15
		1	9	10	3	—	—	3	4.5	—	2.9	—	—		
		1.5	13.5	15	—	—	—	—	6.75	—	—	—	—		
	V <sub>NH</sub>	0.8	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—		
		1	9	10	2.9	—	—	3	4.5	—	3	—	—		
		1.5	13.5	15	—	—	—	—	6.75	—	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	—	mA	4, 5	
		0.5	10	1.1	—	—	0.9	1.8	—	0.65	—	—			
		1.5	15	—	—	—	3	6	—	—	—	—			
		2.5	5	-2	—	—	-1.6	-3.2	—	-1.2	—	—			
P-Channel (Source)	I <sub>DP</sub>	4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—	—	mA	6, 7	
		9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—	—			
		13.5	15	—	—	—	-3	-6	—	—	—	—			
		—	—	—	—	—	—	—	—	—	—	—			
Input Current	I <sub>I</sub>	15	—	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—	

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, and C<sub>L</sub> = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS		UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.
		V <sub>DD</sub> Volts	Typ.	Max.			
Propagation Delay Time: Clock or Enable to Output	t <sub>PHL</sub> , t <sub>PLH</sub>		5	280	560	ns	8
			10	115	230		
Reset to Output	t <sub>PLH</sub>		15	80	—		
			5	330	660	ns	8
Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>		10	130	260		
			15	90	—		
Average Input Capacitance	C <sub>I</sub>	Any Input	5	—	pF	—	—

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS												UNITS	FIG. NO.		
		VO Volts	VDD Volts	-40°C			25°C			85°C							
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.					
Quiescent Device Current	IL	5	—	—	50	—	0.02	50	—	—	700	—	μA	16			
		10	—	—	100	—	0.02	100	—	—	1400	—					
		15	—	—	—	—	0.02	—	—	—	—	—					
Output Voltage: Low-Level	VOL	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—			
		10	—	—	0.01	—	0	0.01	—	—	0.05	—					
		15	—	—	—	—	0	—	—	—	—	—					
High-Level	VOH	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	15			
		10	9.99	—	—	9.99	10	—	9.95	—	—	—					
		15	—	—	—	—	15	—	—	—	—	—					
Noise Immunity	VNL	0.8	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	15		
		1	9	10	3	—	—	3	4.5	—	2.9	—	—				
		1.5	13.5	15	—	—	—	6.75	—	—	—	—	—				
	VNH	0.8	4.2	5	1.4	—	—	1.5	2.25	—	1.5	—	—				
		1	9	10	2.9	—	—	3	4.5	—	3	—	—				
		1.5	13.5	15	—	—	—	6.75	—	—	—	—	—				
Output Drive Current: N-Channel (Sink)	IDN	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	—	mA	4, 5			
		0.5	10	1	—	—	0.9	1.8	—	0.75	—	—					
		1.5	15	—	—	—	3	6	—	—	—	—					
P-Channel (Source)	IDP	2.5	5	-1.8	—	—	-1.6	-3.2	—	-1.3	—	—	mA	6, 7			
		4.6	5	-0.45	—	—	-0.4	-0.8	—	-0.36	—	—					
		9.5	10	-1	—	—	-0.9	-1.8	—	-0.75	—	—					
		13.5	15	—	—	—	-3	-6	—	—	—	—					
Input Current	II	15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	—	μA	—			

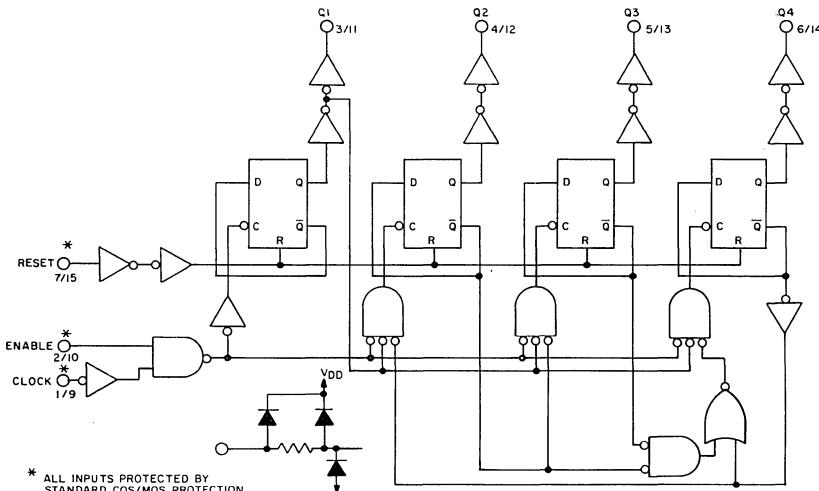


Fig. 1-Decade counter (CD4518B) logic diagram for one of two identical counters.

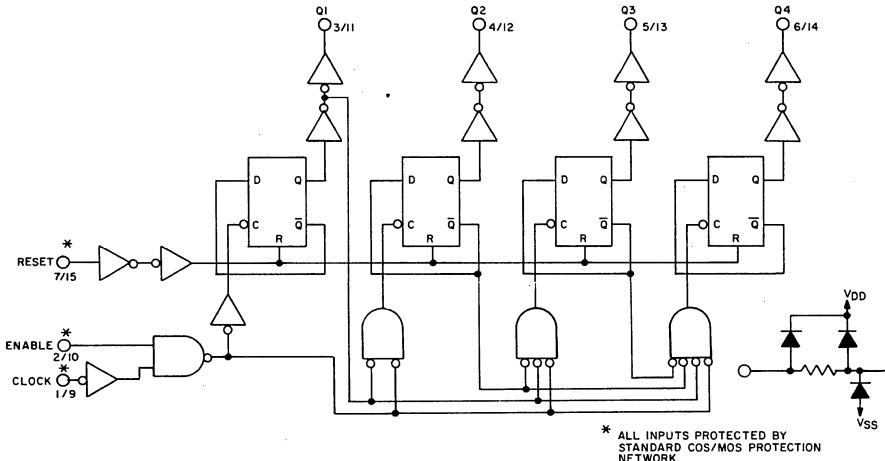
## TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

1 ≡ High State

0 ≡ Low State



92CM-23773RI

Fig. 2—Binary counter (CD4520B) logic diagram for one of two identical counters.

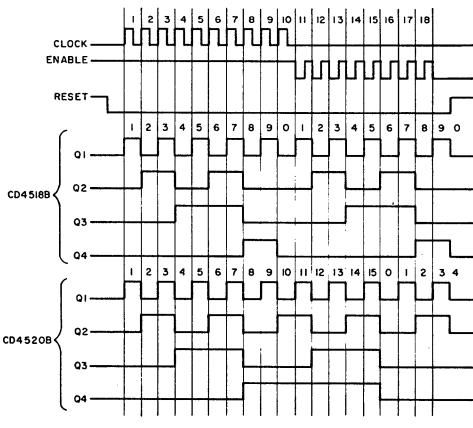


Fig. 3—Timing diagrams for CD4518B and CD4520B.

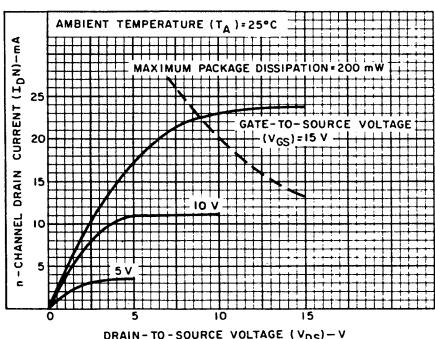


Fig. 4—Typical output-N-channel drain characteristics.

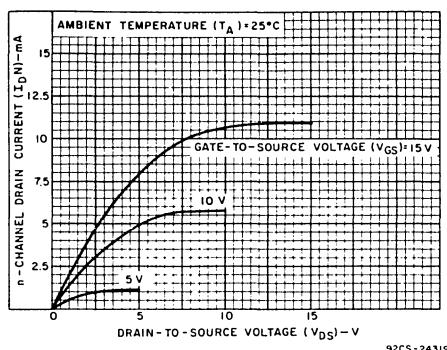


Fig. 5—Minimum output-N-channel drain characteristics.

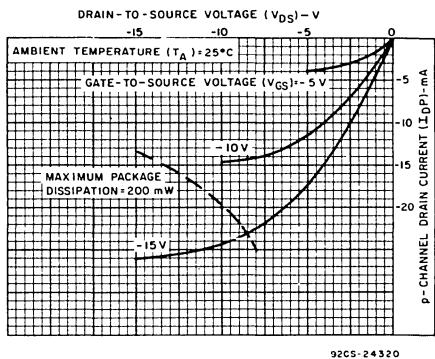


Fig. 6—Typical output-P-channel drain characteristics.

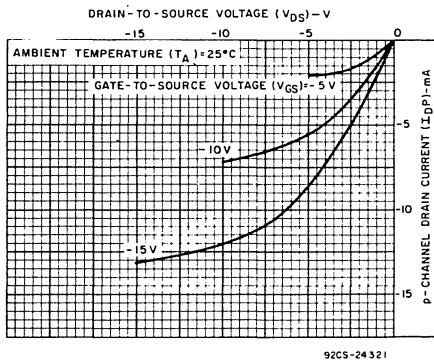


Fig. 7—Minimum output-P-channel drain characteristics.

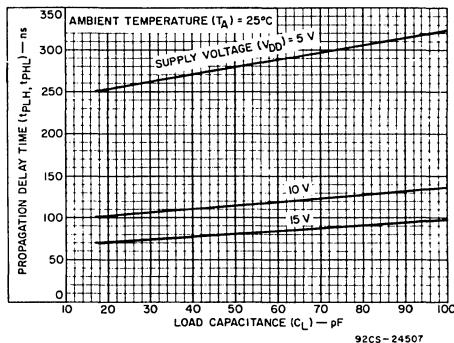


Fig. 8—Typical propagation delay vs. load capacitance (clock or enable to output).

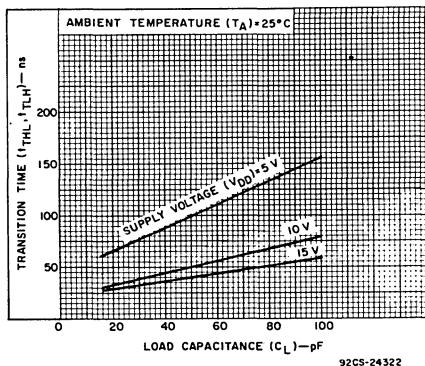


Fig. 9—Typical transition time vs. load capacitance.

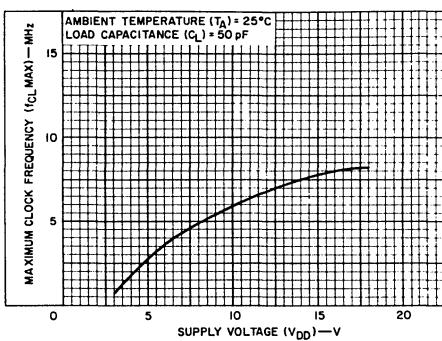
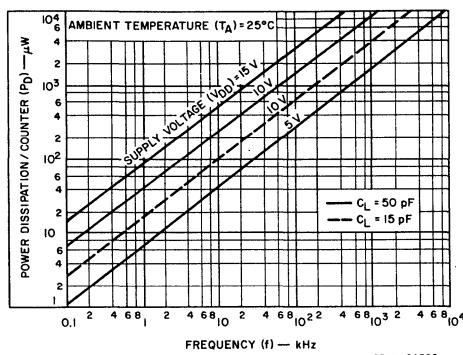
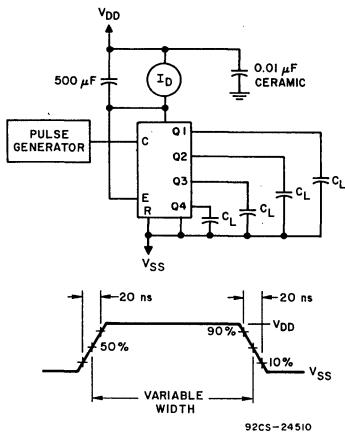


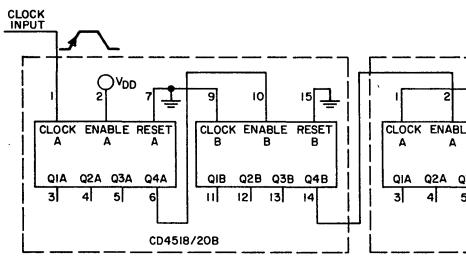
Fig. 10—Typical maximum-clock-frequency vs. supply voltage.



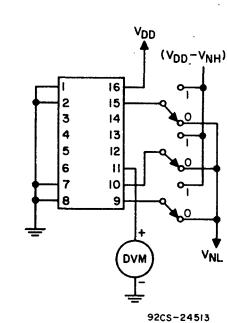
92CS-24509



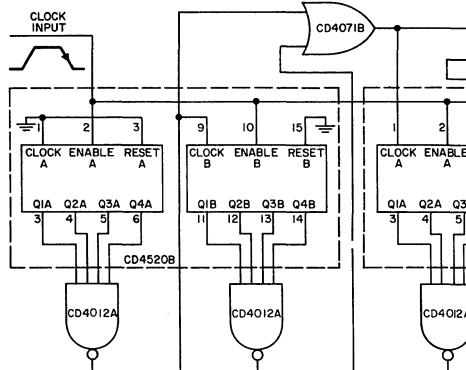
92CS-24510



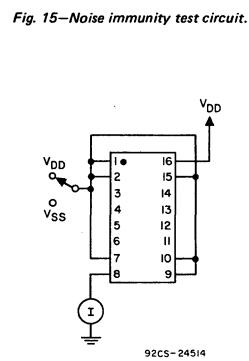
92CS-24011



92CS-24515

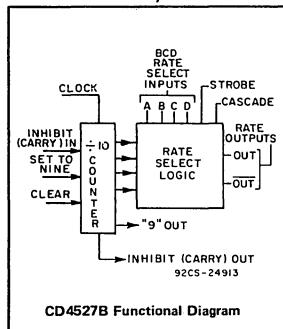


92CM-24512



92CS-24514

Preliminary Data<sup>▲</sup>



The RCA-CD4527B is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527B devices may be cascaded in two different modes: the Add mode and the Multiply mode. See Figs. 3 and 4. In the Add mode,

$$\text{Output Rate} = (\text{Clock Rate})$$

$$(0.1 \text{ BCD}_1 + 0.01 \text{ BCD}_2 + 0.001 \text{ BCD}_3 + \dots).$$

In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

$$\text{e.g. } \frac{9}{10} \times \frac{4}{10} = \frac{36}{100}, \text{ or } 36 \text{ output}$$

pulses for every 100 clock input pulses.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE

$V_{DD}$  \* ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

ALL INPUTS .....  $V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)

from case for 10 seconds max. ..... 265°C

\* All voltage values are referenced to  $V_{SS}$  terminal.

**OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	-	0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD} +$ 0.5 V	V	-

TRUTH TABLE

Inputs								Number of Pulses or Output Logic Level (H or L)					
D	C	B	A	No. of Clock Pulses	Inh <sub>IN</sub>	Strobe	Cascade	Clear	Set	Pin 6 OUT	Pin 5 OUT	Pin 7 Inh <sub>OUT</sub>	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

\* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			TYPICAL VALUES	UNITS
			$V_O$ V	$V_{DD}$ V		
Quiescent Device Current	$I_L$		5	0.02	0.02	$\mu\text{A}$
Output Drive Current: All Outputs N-Channel (Sink)	$I_{DN}$		0.4	5	0.8	$\text{mA}$
			0.5	10	1.8	
			4.6	5	-0.8	
	$I_{DP}$		2.5	5	-3.2	
			9.5	10	-1.8	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $C_L = 50 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		$V_{DD}$	V		
Propagation Delay	$t_{PHL}, t_{PLH}$	Clock to "Out"	5	180	ns
			10	90	
	$t_{PLH}$	Clock to "Inhibit Out"	5	260	
			10	130	
Transition Time	$t_{TLH}, t_{THL}$		5	100	ns
			10	50	
Maximum Clock Frequency	$f_{CL}(\text{Max.})$		5	2	MHz
			10	4.5	
Maximum Clock Rise and Fall Time	$t_r, t_f(\text{Max.})$		5	15	$\mu\text{s}$
			10		

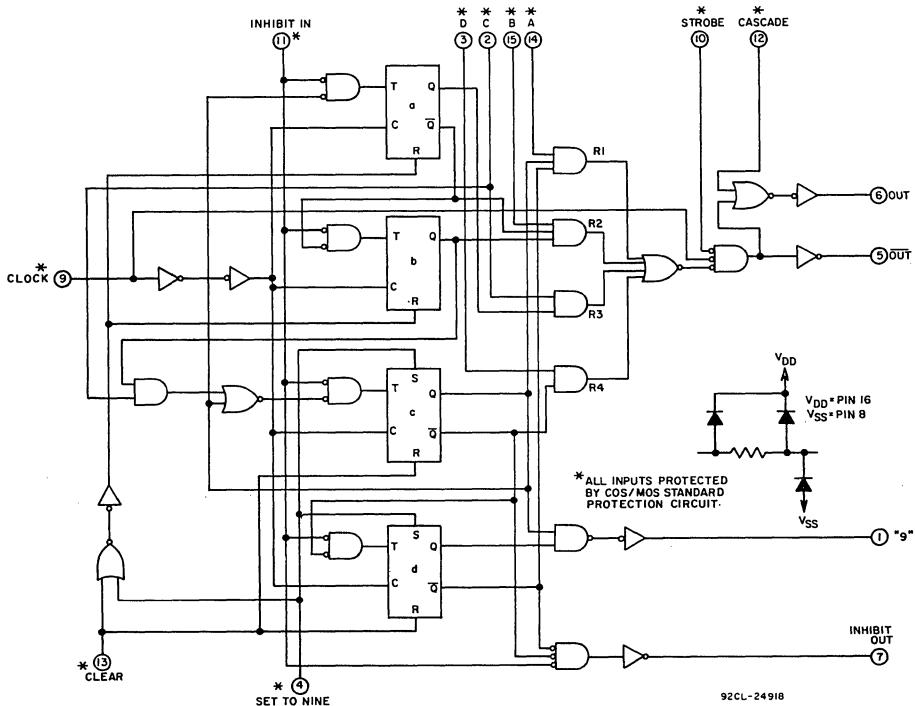


Fig. 1—Logic diagram.

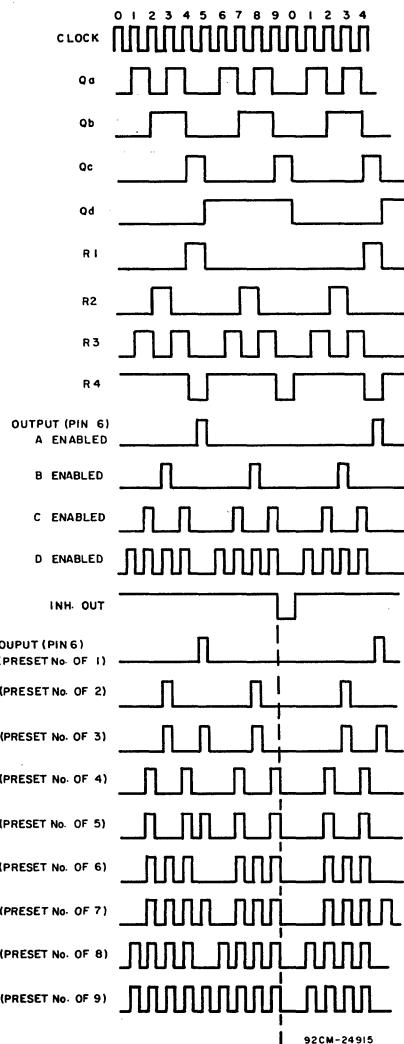


Fig. 2—Timing diagram.

92CM-24915

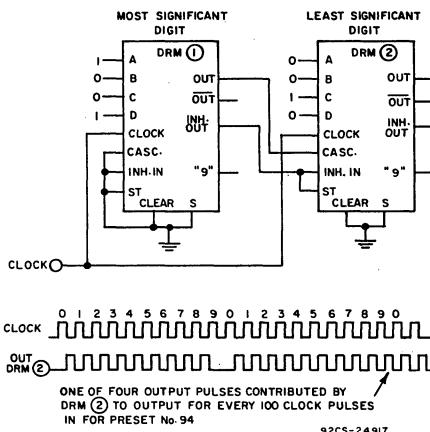


Fig. 3—Two CD4527B's cascaded in the "Add" mode with a preset number of 94.

92CS-24917

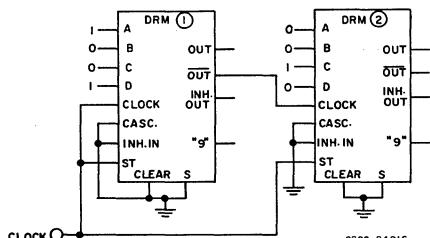
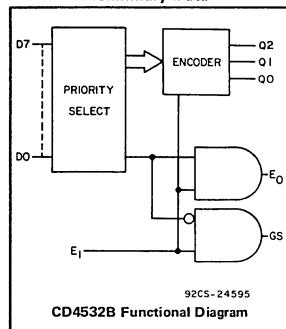


Fig. 4—Two CD4527B's cascaded in the "Multiply" mode with a preset number of 36.

92CS-24916

## Preliminary CD4532BE

### Preliminary Data



The RCA-CD4532B consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E<sub>I</sub> is low. When E<sub>I</sub> is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group

select line GS is high to indicate that priority inputs are present. The enable-out (E<sub>O</sub>) is high when no priority inputs are present.

The CD4532B is available in the 16-lead dual-in-line plastic package (CD4532BE).

This device is similar to type MC14532.

### OPERATING CONDITIONS AT T<sub>A</sub> = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V <sub>DD</sub>	Min.	Max.	Units	Fig.
Supply Voltage Range	—	3	18	V	—
Input Voltage Swing (Recommended V <sub>SS</sub> to V <sub>DD</sub> )	—	0.2 V <sub>DD</sub> to 0.8 V <sub>DD</sub> (Any one input)	—0.5 V to V <sub>DD</sub> + 0.5 V	V	—

### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE.....	-65 to +150°C
OPERATING-TEMPERATURE RANGE.....	-40 to +85 °C
DC SUPPLY-VOLTAGE RANGE:	
(V <sub>DD</sub> * ).....	-0.5 to +18 V
DEVICE DISSIPATION (PER PACKAGE) .....	200 mW
ALL INPUTS.....	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>DD</sub>
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ....	+265°C

\* All voltage values are referenced to V<sub>SS</sub> terminal.

TRUTH TABLE

Input									Output				
E <sub>I</sub>	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E <sub>O</sub>
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	0	X	X	X	1	0	1	1	0
1	0	0	0	0	0	0	1	X	1	0	1	0	0
1	0	0	0	0	0	0	0	1	1	0	0	1	0
1	0	0	0	0	0	0	0	0	1	0	0	0	0

X = Don't Care

Logic 1 ≡ High

Logic 0 ≡ Low

STATIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
		$V_O$ Volts	$V_{DD}$ Volts		
Quiescent Device Current	$I_L$		5	0.02	$\mu\text{A}$
			10	0.02	
Output Drive Current: N-Channel (Sink)	$I_{DN}$		0.4	5	$\text{mA}$
			0.5	10	
	$I_{DP}$		4.6	5	
			2.5	5	
			9.5	10	

DYNAMIC ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ;  $C_L = 15 \text{ pF}$ , Input  $t_r, t_f = 20 \text{ ns}$ 

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V_{DD}$ Volts	TYPICAL VALUES	UNITS
Propagation Delay Time: $E_I$ to $E_O$	$t_{PHL}, t_{PLH}$	5	150	$\text{ns}$
		10	80	
		5	120	
		10	60	
		5	225	
		10	110	
		5	250	
		10	120	
		5	225	
		10	100	
Transition Time	$t_{THL}, t_{TLH}$	5	60	$\text{ns}$
		10	30	

For Operating and Handling Considerations, see RCA Application Note ICAN-6000.

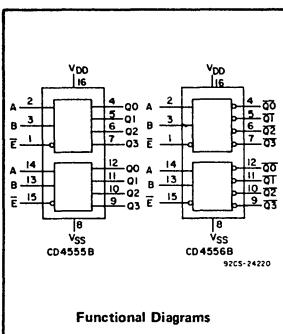


## Digital Integrated Circuits

Monolithic Silicon

CD4555B Types

CD4556B Types



## COS/MOS Dual Binary to 1 of 4 Decoder/Demultiplexers

CD4555B: Outputs High on Select

CD4556B: Outputs Low on Select

*Features:*

- Standard "B" series output drive
- Expandable with multiple packages

*Applications:*

- Decoding      ■ Code conversion      ■ Function selection
- Demultiplexing (using Enable input as a data input)
- Memory chip-enable selection

The RCA-CD4555B and CD4556B\* are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ( $\bar{E}$ ), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. All outputs have equal source- and sink-current capabilities and conform to standard "B" series output drive (see Static Electrical Characteristics). The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

These devices are supplied in 16-lead dual-in-line plastic packages (E), welded-seal ceramic packages (D), ceramic packages (F), ceramic flat packs (K), and in chip form (H).

\* Formerly CD4091A & CD4092A, respectively.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

STORAGE-TEMPERATURE RANGE ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE:

CERAMIC-PACKAGE TYPES ..... -55 to +125°C

PLASTIC-PACKAGE TYPES ..... -40 to +85 °C

DC SUPPLY-VOLTAGE RANGE

 $V_{DD}$  ..... -0.5 to +18 V

DEVICE DISSIPATION (PER PACKAGE) ..... 200 mW

ALL INPUTS .....  $V_{SS} \leq V_I \leq V_{DD}$ 

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)  
from case for 10 seconds max. ..... 265°C\* All voltage values are referenced to  $V_{SS}$  terminal.

TRUTH TABLE

INPUTS		OUTPUTS CD4555B				OUTPUTS CD4556B			
ENABLE	SELECT	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0 0	0	0	0	1	1	1	1	0
0	0 1	0	0	1	0	1	1	0	1
0	1 0	0	1	0	0	1	0	1	1
0	1 1	1	0	0	0	0	1	1	1
1	X X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH

LOGIC 0 ≡ LOW

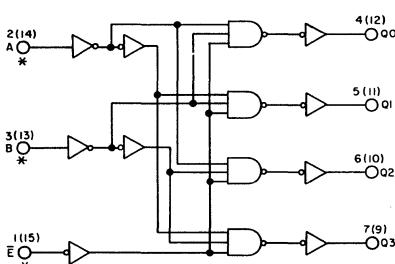
**OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$** 

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

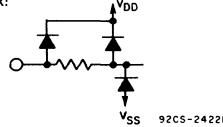
Characteristic	$V_{DD}$	Min.	Max.	Units	Fig.
Supply Voltage Range	-	3	18	V	-
Input Voltage Swing (Recommended $V_{SS}$ to $V_{DD}$ )	-0.2 $V_{DD}$ to 0.8 $V_{DD}$ (Any one input)	-0.5 V to $V_{DD}$ + 0.5 V		V	-

## STATIC ELECTRICAL CHARACTERISTICS

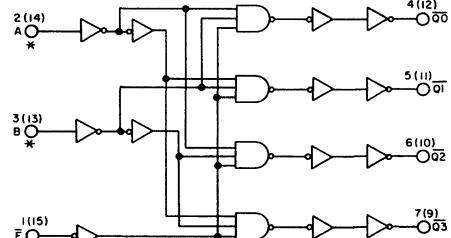
CHARAC- TERISTIC	SYMBOL	TEST CONDI- TIONS		CD4555BD, BF, BK, BH CD4556BD, BF, BK, BH CERAMIC PACKAGE LIMITS								UNITS	FIG. NO.		
		VO Volts	VDD Volts	-55°C			25°C			125°C					
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	IL	5	—	—	5	—	0.02	5	—	—	300	—	μA	15	
		10	—	—	10	—	0.02	10	—	—	600	—			
		15	—	—	—	—	0.02	—	—	—	—	—			
Output Voltage Low-Level	VOL	5	—	—	0.01	—	0	0.01	—	—	0.05	—	V	—	
		10	—	—	0.01	—	0	0.01	—	—	0.05	—			
		15	—	—	—	—	0	—	—	—	—	—			
High-Level	VOH	5	4.99	—	—	4.99	5	—	4.95	—	—	—	V	—	
		10	9.99	—	—	9.99	10	—	9.95	—	—	—			
		15	—	—	—	—	15	—	—	—	—	—			
Noise Immunity (Any Input)	VNL	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	—	V	16, 17	
		9	10	3	—	—	3	4.5	—	2.9	—	—			
		13.5	15	—	—	—	6.75	—	—	—	—	—			
	VNH	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—	—			
		1	10	2.9	—	—	3	4.5	—	3	—	—			
		1.5	15	—	—	—	6.75	—	—	—	—	—			
Output Drive Current: N-Channel (Sink)	IDN	0.4	5	0.5	—	—	0.4	0.8	—	0.3	—	—	mA	—	
		0.5	10	1.1	—	—	0.9	1.8	—	0.65	—	—			
		1.5	15	—	—	—	3	6	—	—	—	—			
P-Channel (Source)	IDP	2.5	5	-2	—	—	-1.6	-3.2	—	-1.15	—	—	mA	—	
		4.6	5	-0.5	—	—	-0.4	-0.8	—	-0.3	—	—			
		9.5	10	-1.1	—	—	-0.9	-1.8	—	-0.65	—	—			
		13.5	15	—	—	—	-3	-6	—	—	—	—			
Input Current	I <sub>I</sub>		15	—	—	—	—	±10 <sup>-5</sup>	±1	—	—	—	μA	—	



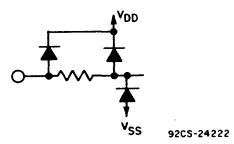
\* ALL INPUTS PROTECTED BY STANDARD COS/MOS PROTECTION NETWORK:



92CS-24221



\* ALL INPUTS PROTECTED BY STANDARD COS/MOS PROTECTION NETWORK:



92CS-24222

Fig. 1—CD4555B logic diagram (1 of 2 identical circuits).

Fig. 2—CD4556B logic diagram (1 of 2 identical circuits).

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	SYMBOL	CD4555BE, CD4556BE PLASTIC PACKAGE LIMITS										UNITS	FIG. NO.
		V <sub>O</sub> Volts	V <sub>DD</sub> Volts	−40°C			25°C			85°C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current	I <sub>L</sub>	5	—	—	50	—	0.02	50	—	—	700	μA	15
		10	—	—	100	—	0.02	100	—	—	1400		
		15	—	—	—	—	0.02	—	—	—	—		
Output Voltage: Low-Level	V <sub>OL</sub>	5	—	—	0.01	—	0	0.01	—	—	0.05	V	—
		10	—	—	0.01	—	0	0.01	—	—	0.05		
		15	—	—	—	—	0	—	—	—	—		
High-Level	V <sub>OH</sub>	5	4.99	—	—	4.99	5	—	4.95	—	—	—	—
		10	9.99	—	—	9.99	10	—	9.95	—	—		
		15	—	—	—	—	15	—	—	—	—		
Noise Immunity (Any Input)	V <sub>NL</sub>	4.2	5	1.5	—	—	1.5	2.25	—	1.4	—	V	16, 17
		9	10	3	—	—	3	4.5	—	2.9	—		
		13.5	15	—	—	—	—	6.75	—	—	—		
	V <sub>NH</sub>	0.8	5	1.4	—	—	1.5	2.25	—	1.5	—		
		1	10	2.9	—	—	3	4.5	—	3	—		
		1.5	15	—	—	—	—	6.75	—	—	—		
Output Drive Current: N-Channel (Sink)	I <sub>DN</sub>	0.4	5	0.45	—	—	0.4	0.8	—	0.36	—	mA	—
		0.5	10	1	—	—	0.9	1.8	—	0.75	—		
		1.5	15	—	—	—	3	6	—	—	—		
P-Channel (Source)	I <sub>DP</sub>	2.5	5	−1.8	—	—	−1.6	−3.2	—	−1.3	—	mA	—
		4.6	5	−0.45	—	—	−0.4	−0.8	—	−0.35	—		
		9.5	10	−1	—	—	−0.9	−1.8	—	−0.75	—		
		13.5	15	—	—	—	−3	−6	—	—	—		
Input Current	I <sub>I</sub>	15	—	—	—	—	—	±10 <sup>−5</sup>	±1	—	—	μA	—

DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, and C<sub>L</sub> = 50 pF

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS		UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS FIG. NO.	
				V <sub>DD</sub> Volts	Typ.			
Propagation Delay Time: A or B Input to Any Output	t <sub>PHL</sub> , t <sub>PLH</sub>			5	220	440	ns	7, 9, 19, 20
				10	95	190		
Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>			5	100	200	ns	10
				10	50	100		
Average Input Capacitance	C <sub>I</sub>	Any Input		5	—	pF	—	

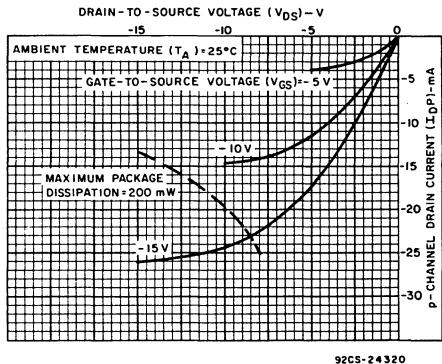


Fig. 3—Typical output-P-channel drain characteristics.

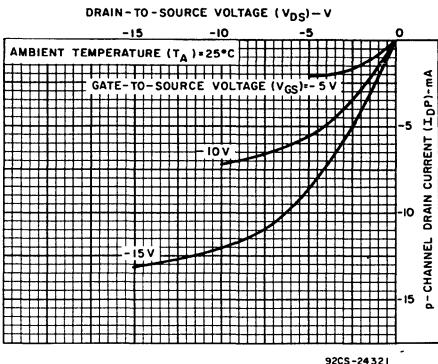


Fig. 4—Minimum output-P-channel drain characteristics.

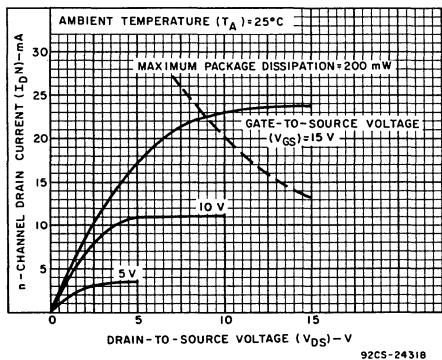


Fig. 5—Typical output-N-channel drain characteristics.

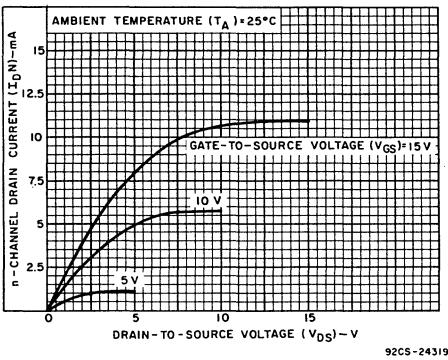


Fig. 6—Minimum output-N channel drain characteristics.

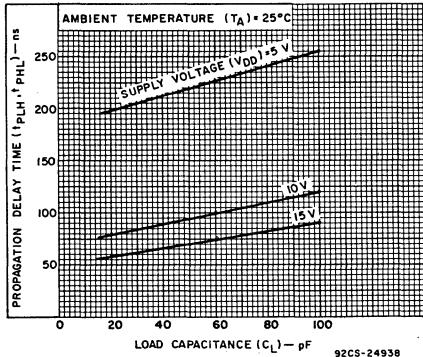


Fig. 7—Typical propagation delay time vs. load capacitance (A or B input to any output).

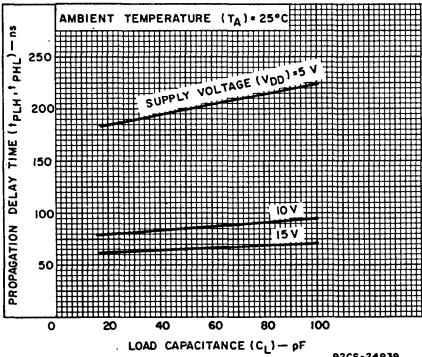


Fig. 8—Typical propagation delay time vs. load capacitance (E input to any output).

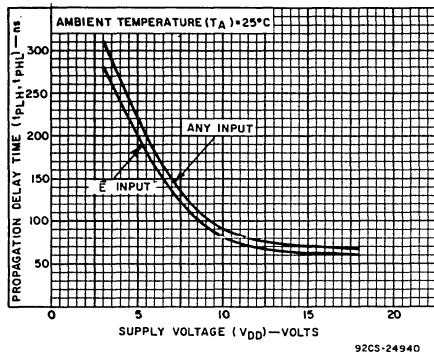


Fig. 9—Typical propagation delay time vs. supply voltage.

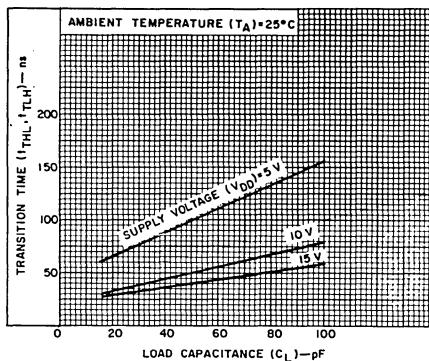


Fig. 10—Typical transition time vs. load capacitance.

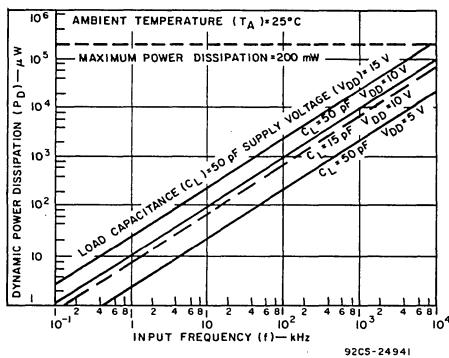
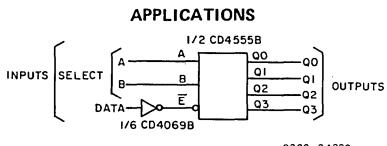
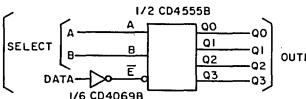


Fig. 11—Typical dynamic power dissipation vs. frequency.



## APPLICATIONS



SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

Fig. 12—1-of-4 line data demultiplexer using CD4555B.

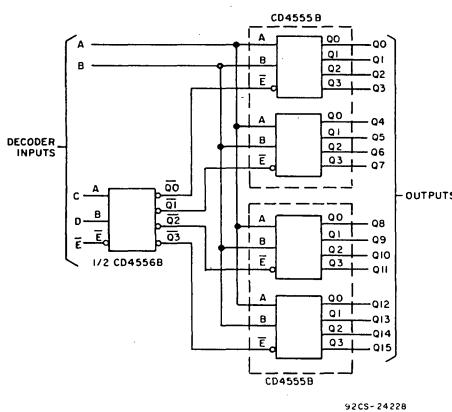


Fig. 13—1-of-16 decoder using CD4555B/CD4556B.

INPUTS		Q OUTPUTS																		
E	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

 $X = \text{don't care}$

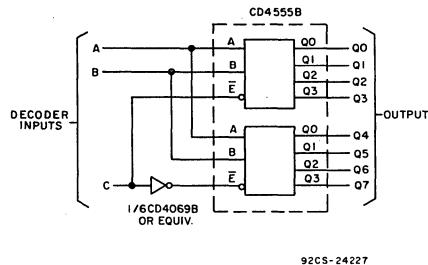


Fig. 14—1-of-8 decoder using CD4555B.

TRUTH TABLE										
INPUTS	Q OUTPUTS									
C	B	A	0	1	2	3	4	5	6	7
0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

I<sub>L</sub> MEASURED WITH INPUTS HIGH AND INPUTS LOW

92CS-24944

Fig. 15—Quiescent device current test circuit.

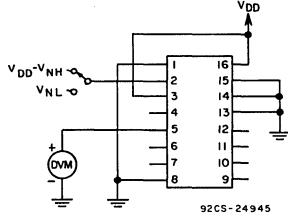


Fig. 16—CD4555B noise immunity test circuit. Fig. 17—CD4556B noise immunity test circuit. Fig. 18—Dynamic power dissipation test circuit.

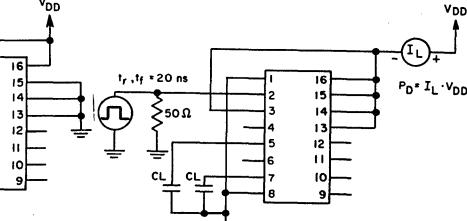
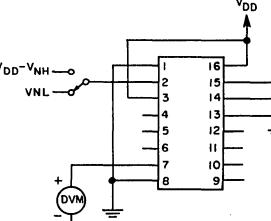
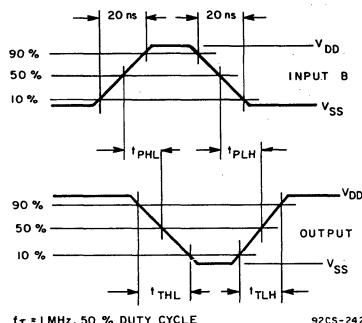
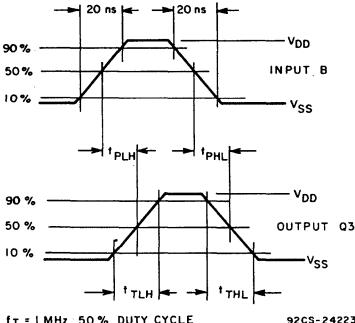
 $I_D = I_L \cdot V_{DD}$ 

Fig. 19—CD4555B B input to Q3 output dynamic signal waveforms.

Fig. 20—CD4556B B input to Q3 output dynamic signal waveforms.

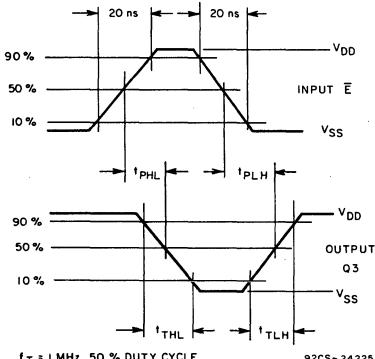


Fig. 21—CD4555B E-bar input to Q3 output dynamic signal waveforms.

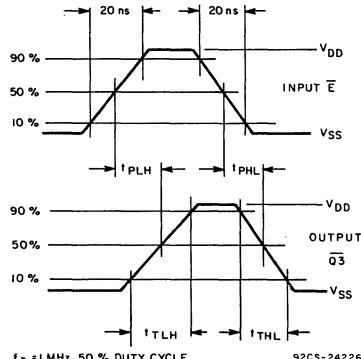


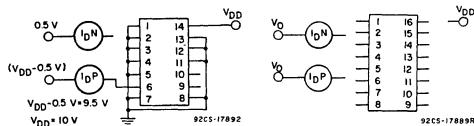
Fig. 22—CD4556B E-bar input to Q3 output dynamic signal waveforms.

# **Appendix**

## Appendix

### DRIVE CURRENT TEST CIRCUIT CONNECTIONS To be used as an example of test method.

Example:  
CD4000A IDP



Example:  
16-Lead Types

Type	MΦ	Ground	V <sub>DD</sub>	V <sub>O</sub>
CD4000A	IDN	1,4,7,8,11,13	5,14	6
	IDP	1,5,7,8,11-13	14	
CD4001A	IDN	2,5,9,12,13	1,14	3
	IDP	1,2,5-9,12,13	14	
CD4002A	IDN	3-5,7,9-12	2,14	1
	IDP	2,5-7,9-12	14	
CD4006A*	IDN	1,4-7	14	13
	IDP	4-7	1,14	
CD4007A	IDN	3,7,10	6,14	8
	IDP	3,6,7,10	14	13
CD4008A	IDN	1-9,15	16	14
	IDP	8	1-7,9,15,16	
CD4009A	IDN	5,7-9,11,14	1,3,16	2
	IDP	3,5-7,9-11,14	1,16	
CD4010A	IDN	3,5-7,9,11,14	1,16	2
	IDP	5,7-9,11,14	1,3,16	
CD4011A	IDN	5-9,12,13	1,2,14	3
	IDP	1,5-9,12,13	2,14	
CD4012A	IDN	7,9-12	2-5,14	1
	IDP	2,7-9-12	3-5,14	
CD4013A	IDN	3,5-11	4,14	1
	IDP	3-5,7-11	6,14	
CD4014A*	IDN	1,4-8,11,13-15	9,16	3
	IDP	4-8,11,13-15	1,9,16	
CD4015A*	IDN	1,6-8,14,15	16	5
	IDP	1,6,8,14,15	7,16	
CD4017A	IDN	8	13-16	3
	IDP	8	13-16	2
CD4018A	IDN	1-3,7-10,12	14-16	11
	IDP	1-3,7,8,10	9,12,14-16	
CD4019A	IDN	1-9	14-16	13
	IDP	1-8	9,14-16	
CD4020A*	IDN	8,11	16	9
	IDP	8,11	16	
CD4021A	IDN	1,4-8,10,11, 13-15	9,16	3
	IDP	4-8,10,11,13-15	1,9,16	
CD4022A*	IDN	8,13,15	16	2
	IDP	8,13,15	16	
CD4023A	IDN	1,2,7,8,11-13	3-5,14	6
	IDP	1-3,7,8,11-13	4,5,14	

Refer to applicable data sheet for V<sub>O</sub> values.

Voltage outputs shall be supplied by an external power supply.

Type	MΦ	Ground	V <sub>DD</sub>	V <sub>O</sub>
CD4024A* (K,D,E)	IDN	1,7	2,14	12
	IDP	2,7	14	
CD4024A* (T)	IDN	1,12	2,3	11
	IDP	3,12	2	
CD4025A	IDN	1-4,7,8,11-13	5,14	6
	IDP	1-5,7,8,11-13	14	
CD4026A	IDN	1-3,8,15	16	10
	IDP	1,2,8	3,15,16	
CD4027A	IDN	3,5-13	4,16	1
	IDP	3-6,8-13	7,16	
CD4028A	IDN	8,10-13	16	2
	IDP	8,10-13	16	3
CD4029A	IDN	3,4,8,10,12, 13,15	1,5,9,16	6
	IDP	5,8,15	1,3,4,9,10,12, 13,16	
CD4030A	IDN	1,2,5-9,12,13	14	3
	IDP	2,5-9,12,13	1,14	
CD4031A	IDN	1,2,8,10,15	7,16	6
	IDP	1,2,7,8,10,15	16	
CD4032A	IDN	2,3,5-8,10-15	16	9
	IDP	2,3,5,6,8,10-15	7,16	
CD4033A	IDN	1-3,8,14	15,16	10
	IDP	1-3,8,15	14,16	
CD4034A	IDN	1-8,10-12,15	9,13,14,24	16
	IDP	10-12,15	1-9,13,14,24	
CD4035A	IDN	2,4,6-12	2,5,16	1
	IDP	2,4,6-12	5,16	
CD4036A	IDN	3-12,21-23	1,2,24	13
	IDP	11,12,21-23	1-10,24	
CD4037A	IDN	7	1-5,14	10
	IDP	2-7	14	
CD4038A	IDN	2,3,5-8,10-15	10,11,16	9
	IDP	2,3,5,6,8,12-15	7,10,11,16	
CD4039A	IDN	3-12,21-23	1,2,24	13
	IDP	11,12,21-23	1-10,24	
CD4040A*	IDN	8,10	11,16	9
	IDN	8,11	16	
CD4041A (TRUE)	IDN	3,6,7,10,13	14	1
	IDP	6,7,10,13	3,14	
CD4041A (COMP)	IDN	6,7,10,13	3,14	2
	IDP	3,6,7,10,13	14	

◆ M = Measurement

\* These types must be clocked into the proper state.

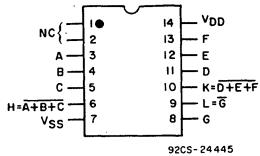
## DRIVE-CURRENT TEST-CIRCUIT CONNECTIONS (Cont'd)

Type	MΦ	Ground	V <sub>DD</sub>	V <sub>O</sub>	Type	MΦ	Ground	V <sub>DD</sub>	V <sub>O</sub>
CD4042A	I <sub>DN</sub>	4,7,8,13,14	5,6,16	2	CD4062AK*	I <sub>DN</sub>	2-5,8	11,13,16	7
	I <sub>DP</sub>	7,8,13,14	4-6,16			I <sub>DP</sub>	3-5,8	2,11,13,16	
CD4043A	I <sub>DN</sub>	4,6-8,11,12 14,15	3,5,16	2	CLD	I <sub>DN</sub>	2-5,8	11,13,16	12
	I <sub>DP</sub>	3,6-8,11,12 14,15	4,5,16			I <sub>DP</sub>	3-5,8	2,11,13,16	
CD4044A	I <sub>DN</sub>	4,8	3,5-7,11,12, 14-16	13	Q	I <sub>DN</sub>	2-5,7	9,11,12	6
	I <sub>DP</sub>	3,8	4-7,11,12, 14-16			I <sub>DP</sub>	3-5,7	2,9,11,12	
CD4045A (φ to 16)	I <sub>DN</sub>	2,14	1,3	8	CLD	I <sub>DN</sub>	2-5,7	9,11,12	10
	I <sub>DP</sub>	2,14	1,3			I <sub>DP</sub>	3-5,7	2,9,11,12	
CD4046A COMP 1	I <sub>DN</sub>	5,8,9	3,14,16	2	CD4063B	I <sub>DN</sub>	1,3,4,8-15	3,16	5
	I <sub>DP</sub>	5,8,9,14	3,16			I <sub>DP</sub>	1-3,8-15	4,16	
	I <sub>DN</sub>	5,8,9,14	3,16	13	CD4066A	I <sub>DN</sub>	NO I <sub>DN</sub> , I <sub>DP</sub>		
	I <sub>DP</sub>	5,8,9	3,14,16			I <sub>DP</sub>	7	2-5,9-12,14	13
CD4047A	I <sub>DN</sub>	5,7,12	4,6,8,9,14	10	CD4068B	I <sub>DP</sub>	2-5,7,9-12	14	
	I <sub>DP</sub>	7,9	3-6,8,12,14			I <sub>DN</sub>	7	1,3,5,9,11,13,14	2
CD4048A	I <sub>DN</sub>	3-14	2,15,16	1	CD4069B	I <sub>DP</sub>	1,3,5,7,9,11,13	14	10
	I <sub>DP</sub>	2-14	15,16			I <sub>DN</sub>	1,2,5,9,12,13	14	
CD4049A	I <sub>DN</sub>	5,7-9,11,14	1,3	2	CD4071B	I <sub>DP</sub>	7	1,2,5-9,12,13,14	1
	I <sub>DP</sub>	5,7-9,11,14	1			I <sub>DN</sub>	2-5,7,9-12	14	
CD4050A	I <sub>DN</sub>	3,5-7,9,11,14	1	2	CD4072B	I <sub>DP</sub>	7	2-5,9-12,14	6
	I <sub>DP</sub>	5,7-9,11,14	1,3			I <sub>DN</sub>	1-5,7,8,11-13	14	
CD4054A	I <sub>DN</sub>	2,7-15	1,16	3	CD4073B	I <sub>DP</sub>	7	1-5,8,11-14	6
	I <sub>DP</sub>	2,7-14	1,15,16			I <sub>DN</sub>	1-5,7,8,11-13	14	
CD4055A	I <sub>DN</sub>	2-4,6-8	5,16	9	CD4075B	I <sub>DP</sub>	7	1-5,8,11-14	3
	I <sub>DP</sub>	2-8	16			I <sub>DN</sub>	2-5,7,9-12	14	
CD4056A	I <sub>DN</sub>	2-4,6-8	1,5,16	9	CD4078B	I <sub>DP</sub>	7	2-5,9-12,14	13
	I <sub>DP</sub>	2-8	1,16			I <sub>DN</sub>	2-5,9-12	14	
CD4057A	I <sub>DN</sub>	1-3,6,7,14,21 23,25,27,28	8,9,13,15,19, 22,26	24	CD4081B	I <sub>DP</sub>	7	1,2,5-9,12,13	3
	I <sub>DP</sub>	6,14,21,23 25,28	1-3,7-9,13,15, 19,20,22,26,27			I <sub>DN</sub>	2-5,7,9,12	14	
ZERO IND	I <sub>DN</sub>	1-3,6,14,21,23, 25,27,28	7-9,13,15,19 20,22,26	4	CD4082A	I <sub>DP</sub>	7	2-5,9-12,14	1
	I <sub>DP</sub>	1-3,6,7,14,21, 23,25,27,28	8,9,13,15,19, 20,22,26			I <sub>DN</sub>	1,2,5-9,11-13	10-14	
NEG IND	I <sub>DN</sub>	1-3-6,14,21,23, 25,27,28	6,13,15,20, 22,23,25,27,28	17	CD4085B	I <sub>DP</sub>	1,2,5-13	14	3
	I <sub>DP</sub>	1-3,6,7,14,21, 23,25,27,28	21,26			I <sub>DN</sub>	1,2,5-9,11,13	11,14	
OVERFLOW IND	I <sub>DN</sub>	1-3,5-7,9,14,19, 19,20,22,26,27	6,13,15,20, 21,26,27	17	CD4086B	I <sub>DP</sub>	1,2,5-10,12,13	11,14	10
	I <sub>DP</sub>	5,7-9,14,19,22, 23,25,28	1-3,6,13,15,20, 21,26,27			I <sub>DN</sub>	7	1,2,5,6,8,9, 12-14	
OTHER OUTPUTS	I <sub>DN</sub>	6,7,21,25	8,9,13,15,19,20, 22,23,26	1	CD4093B	I <sub>DP</sub>	1,2,5-9,12,13	14	11
	I <sub>DP</sub>	6,7,21,22,25	8,9,13,15,19,20, 23,26			I <sub>DN</sub>	2,3,12,21,22	1,2,3,24	
DATA OUT 1 & 3	I <sub>DN</sub>	6,7,21,25	8,9,13,15,19,20, 22,23,26	27	CD4514B	I <sub>DP</sub>	2,3,12,21-23	1,24	14
	I <sub>DP</sub>	6,7,21,22,25	8,9,13,15,19,20, 23,26			I <sub>DN</sub>	2,3,12,21,22	1,23,24	
CD4060A*	I <sub>DN</sub>	8,11	12,16	7	CD4515B	I <sub>DP</sub>	1,2,7-10,15	16	14
	I <sub>DP</sub>	8,12	16			I <sub>DN</sub>	1,2,7-10	15,16	
CD4061A*	I <sub>DN</sub>	1-4,6,7,9-12, 15,16	5	13	CD4518B*	I <sub>DP</sub>	1,2,7,8,10,15	16	14
	I <sub>DP</sub>	1-4,6,7,9-11, 15,16	5,12			I <sub>DN</sub>	1,2,7,8,10,15	16	

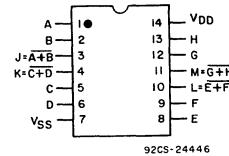
◆ M = Measurement

\* These types must be clocked into the proper state.

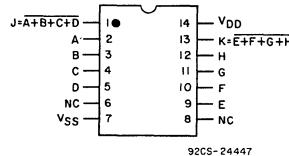
**TERMINAL ASSIGNMENT DIAGRAMS - Top View**



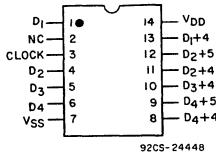
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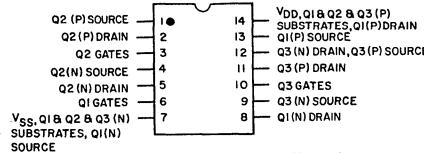
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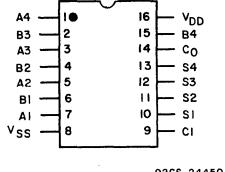
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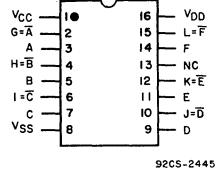
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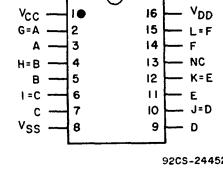
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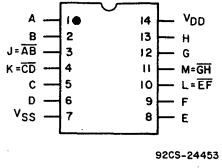
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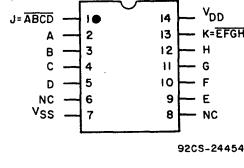
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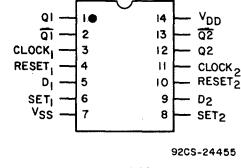
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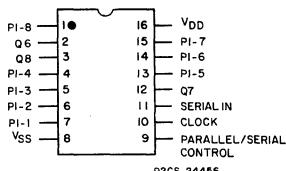
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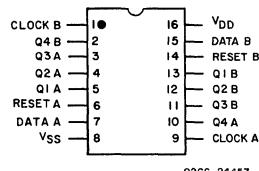
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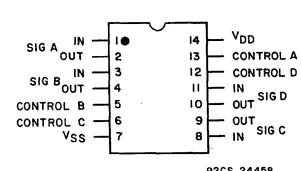
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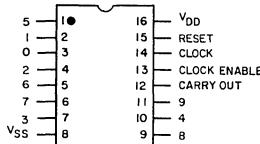


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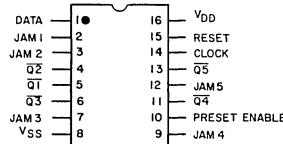


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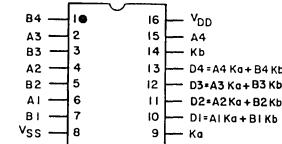
**TERMINAL ASSIGNMENT DIAGRAMS - Top View**



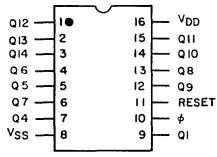
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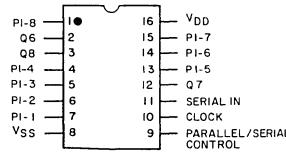
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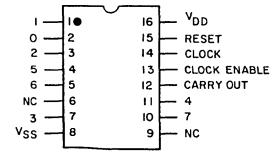
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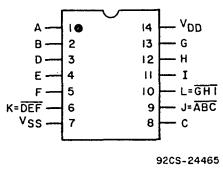
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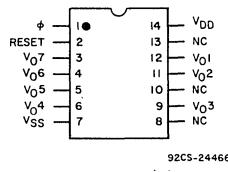


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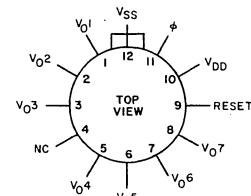


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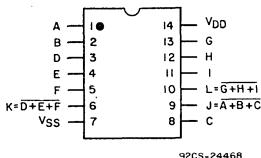


CD4024A (D, E, F, K)



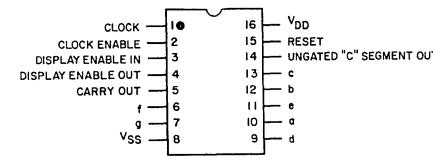
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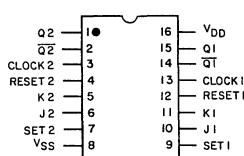
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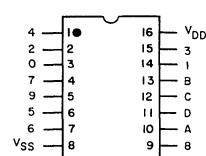
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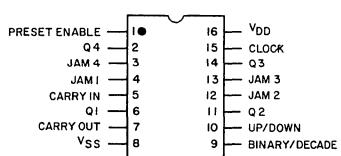
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CD4027A



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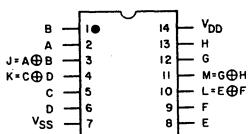
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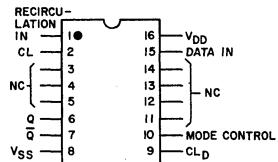
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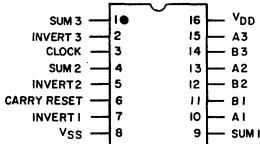
### TERMINAL ASSIGNMENT DIAGRAMS - Top View



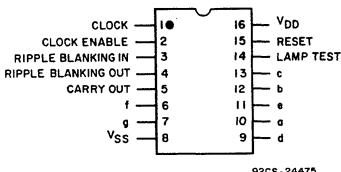
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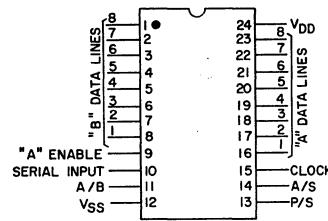
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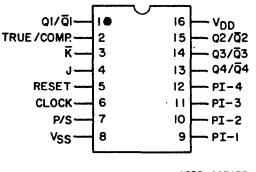
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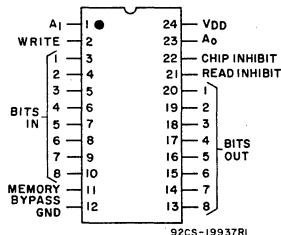
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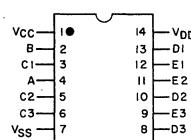
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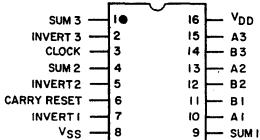
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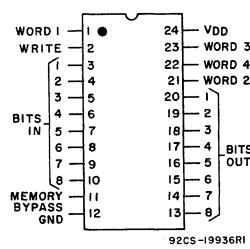
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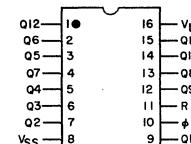
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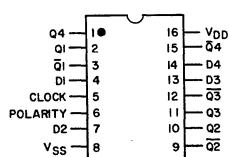
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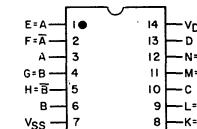
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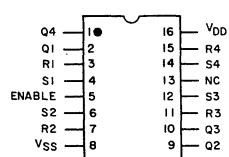
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92CS-20756RI

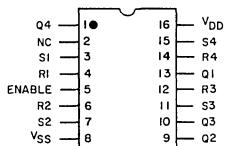


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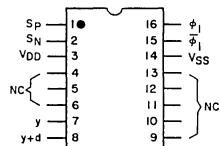


92CS-24476

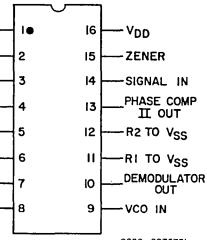
### TERMINAL ASSIGNMENT DIAGRAMS - Top View



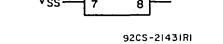
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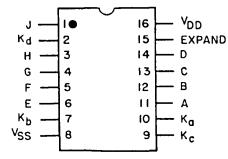
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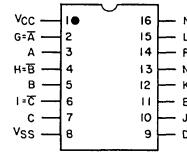
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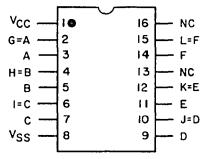
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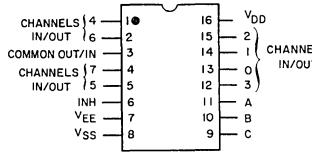
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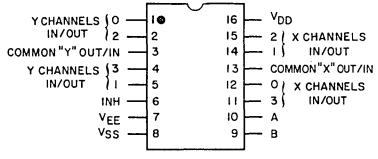
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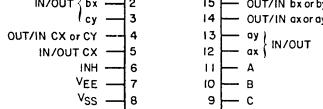
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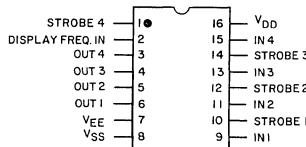
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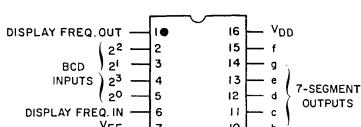
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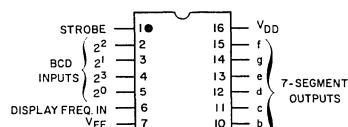
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92CS-24485



92CS-24486



92CS-24487

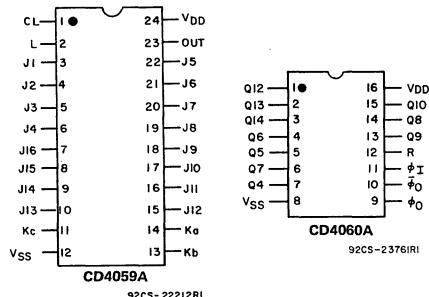
### TERMINAL ASSIGNMENT DIAGRAMS - Top View

PARALLEL DATA I	1 ●	28	RO2
PARALLEL DATA 4	2	27	PARALLEL DATA 3
PARALLEL DATA 2	3	26	* V <sub>DD</sub>
NEGATIVE INDICATOR	4	25	* V <sub>SS</sub>
ZI INPUT	5	24	ZERO INDICATOR OUTPUT
INPUT c	6	23	"DATA OUT" CONTROL
INPUT d	7	22	INPUT a
CONDITIONAL INPUT A	8	21	INPUT b
CONDITIONAL INPUT C	9	20	CLOCK
RIGHT SERIAL DATA LINE	10	19	CONDITIONAL INPUT B
BYPASS	11	18	LEFT SERIAL DATA LINE
NC	12	17	OVERFLOW INDICATOR
MODE-CONTROL INPUT LINE C1	13	16	OVERFLOW I/O
Ro I	14	15	MODE-CONTROL INPUT LINE C2

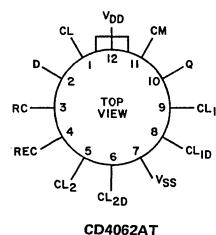
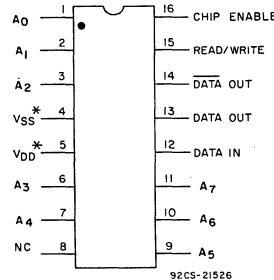
\* NOTE: NON-STANDARD TERMINAL LOCATIONS FOR V<sub>SS</sub> AND V<sub>DD</sub>. MOST OTHER COS/MOS TYPES USE CORNER TERMINALS FOR POWER-SUPPLY CONNECTIONS

92CS-20253RI

CD4057A

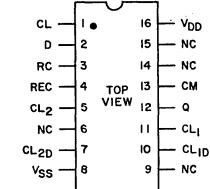


92CS-22212RI



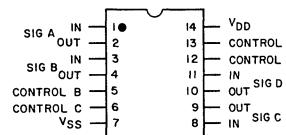
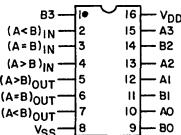
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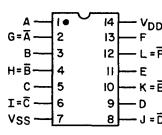
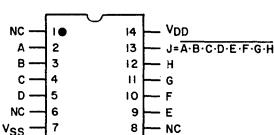
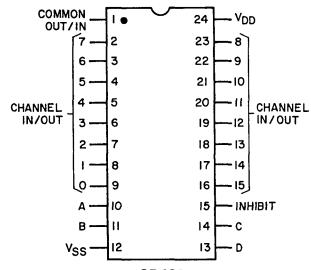


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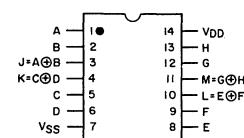
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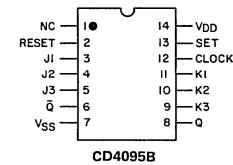
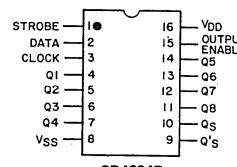
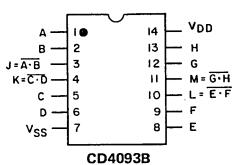
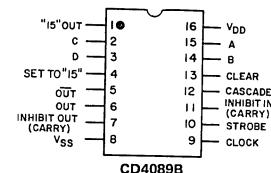
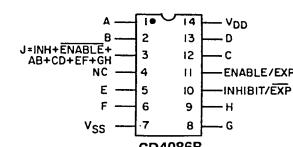
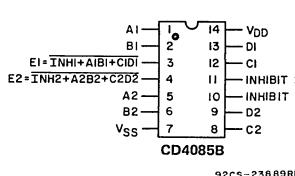
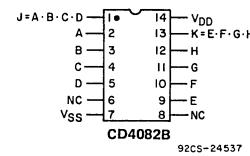
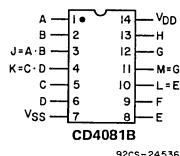
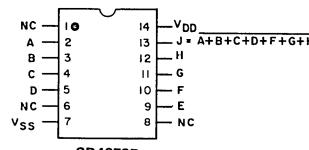
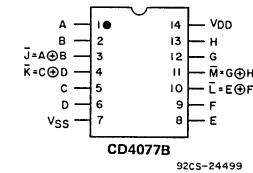
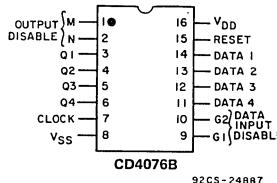
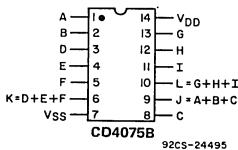
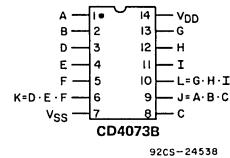
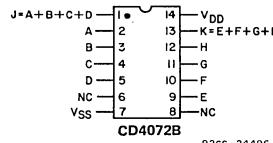
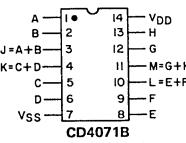
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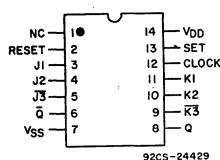
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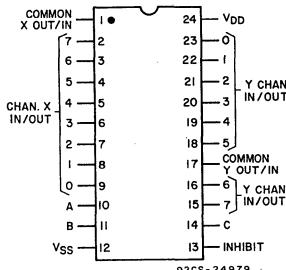
### TERMINAL ASSIGNMENT DIAGRAMS - Top View



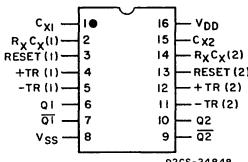
**TERMINAL ASSIGNMENT DIAGRAMS - Top View**



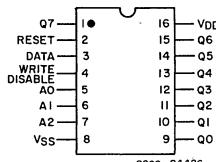
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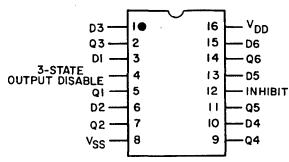
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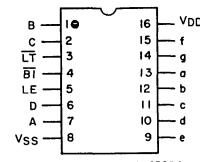
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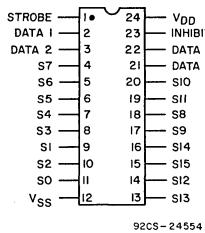
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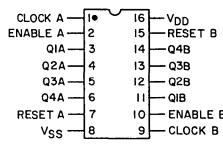
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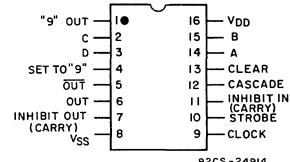
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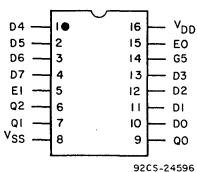
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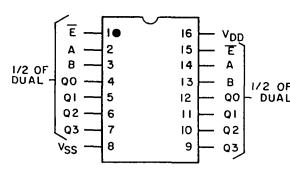
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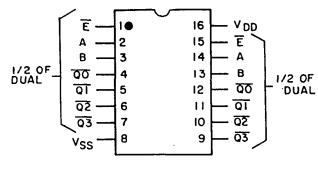
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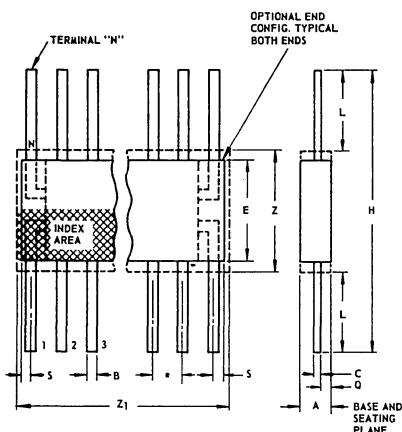
CD4532B



CD4555B



CD4556B

**DIMENSIONAL OUTLINES  
Ceramic Flat Packs**

**JEDEC MO-004-AF 14-LEAD**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006		0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z <sub>1</sub>	0.400		4	10.16	

92SS-4300RI

**JEDEC MO-004-AG 16-LEAD**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006		0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z <sub>1</sub>	0.400		4	10.16	

92CS-1727IRI

**24-LEAD**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z <sub>1</sub>	0.750		4	19.05	

92CS-19949

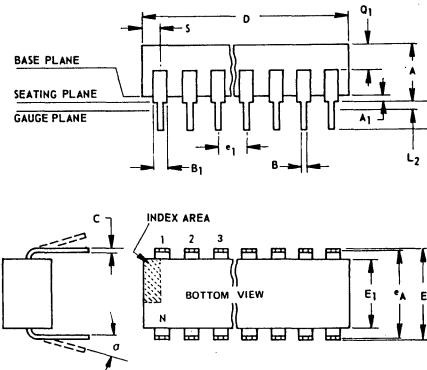
**28-LEAD**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	28		3	28	
Q	0.035	0.070		0.89	1.77
S	0	0.060	1	0	1.53
Z	0.700		4	17.78	
Z <sub>1</sub>	0.750		4	19.05	

92CS-20972

When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

**DIMENSIONAL OUTLINES**  
Ceramic Dual-in-Line Packages

**NOTES:**

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. eA applies in zone L2 when unit installed.
4. a applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N1 is the quantity of allowable missing leads.

**JEDEC MO-001-AD**  
14-Lead Welded-Seal

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A <sub>1</sub>	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B <sub>1</sub>	0.050	0.065		1.27	1.65
C	0.008	0.012		0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E <sub>1</sub>	0.240	0.260		6.10	6.60
e <sub>1</sub>	0.100 TP 0.300 TP		2	2.54 TP 7.62 TP	
e <sub>A</sub>			2, 3		
L	0.125	0.150		3.18	3.81
L <sub>2</sub>	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	14		5	14	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R1

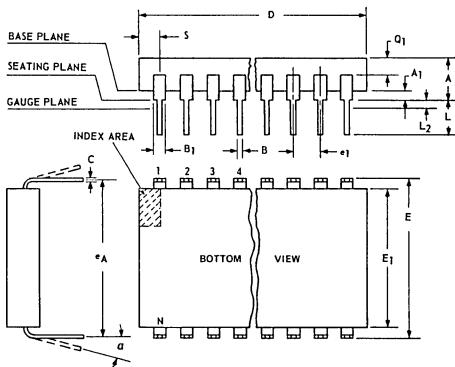
**JEDEC MO-001-AE**  
16-Lead Welded-Seal

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A <sub>1</sub>	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B <sub>1</sub>	0.035	0.065		0.89	1.65
C	0.008	0.012		0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E <sub>1</sub>	0.240	0.260		6.10	6.60
e <sub>1</sub>	0.100 TP 0.300 TP		2	2.54 TP 7.62 TP	
e <sub>A</sub>			2, 3		
L	0.125	0.150		3.18	3.81
L <sub>2</sub>	0.000	0.300		0.000	0.76
a	0°	15°	4	0°	15°
N	16		5	16	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R2

When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

**DIMENSIONAL OUTLINES**  
Ceramic Dual-in-Line Packages (Cont'd)

**NOTES:**

1. REFER TO RULES FOR DIMENSIONING (JEDEC PUBLICATION No. 13) AXIAL LEAD PRODUCT OUTLINES.
2. WHEN BASE OF BODY IS TO BE ATTACHED TO HEAT SINK, TERMINAL LEAD STAND-OFFS ARE NOT REQUIRED AND  $A_1 = 0$ . WHEN  $A_1 = 0$ , THE LEADS EMERGE FROM THE BODY WITH THE  $B_1$  DIMENSION AND REDUCE TO THE  $B$  DIMENSION ABOVE THE SEATING PLANE.
3.  $e_1$  AND  $a_1$  APPLY IN ZONE  $L_2$  WHEN UNIT INSTALLED. LEADS WITHIN .005" RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION.
4. APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
5.  $N$  IS THE MAXIMUM QUANTITY OF LEAD POSITIONS.
6.  $N_1$  IS THE QUANTITY OF ALLOWABLE MISSING LEADS.

**JEDEC MO-015-AH****28-Lead Welded-Seal**

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A <sub>1</sub>	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B <sub>1</sub>	0.045	0.055		1.143	1.397
C	0.008	0.012		0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E <sub>1</sub>	0.480	0.520		12.20	13.20
e <sub>1</sub>	0.100	TP	3	2.54	TP
e <sub>A</sub>	0.600	TP	3	15.24	TP
L	0.100	0.180		2.54	4.57
L <sub>2</sub>	0.000	0.030	3	0.00	0.76
a	0°	15°	4	0°	15°
N	24		5	24	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

92CS-19948

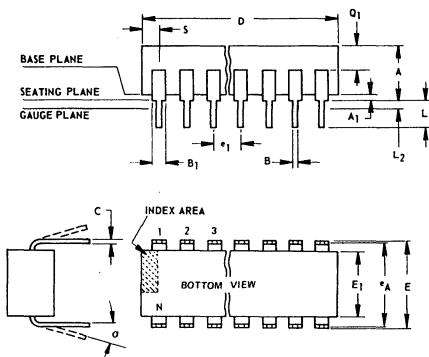
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	.100	.200		2.6	5.0
A <sub>1</sub>	.000	.070	2	0	1.77
B	.015	.020		.381	.508
B <sub>1</sub>	.015	.055		.39	1.39
C	.008	.012		.204	.304
D	1.380	1.420		35.06	36.06
E	.600	.625		15.24	15.87
E <sub>1</sub>	.485	.515		12.32	13.08
e <sub>1</sub>	.100	TP		2.54	TP
e <sub>A</sub>	.600	TP		15.24	TP
L	.100	.200		2.6	5.0
L <sub>2</sub>	.000	.030		0	.76
a	0	15		0°	15°
N	28			28	
N <sub>1</sub>	0			0	
Q <sub>1</sub>	.020	.070		.51	1.77
S	.040	.070		1.02	1.77

See Note 1

92CM-20250

When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

**DIMENSIONAL OUTLINES**  
Ceramic Dual-in-Line Packages (Cont'd)

**NOTES**

- Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
- Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
- $e_A$  applies in zone  $L_2$  when unit installed.
- $a$  applies to spread leads prior to installation.
- N is the maximum quantity of lead positions.
- $N_1$  is the quantity of allowable missing leads.
- $B_1$  applies to all leads except the four end leads which have one-half the normal width ( $B_1$  min. = 0.025 in.)

**JEDEC MO-001-AB**

14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A <sub>1</sub>	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B <sub>1</sub>	0.050	0.065		1.27	1.65
C	0.008	•0.012		0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E <sub>1</sub>	0.240	0.260		6.10	6.60
e <sub>1</sub>	0.100 TP		2	2.54 TP	
e <sub>A</sub>	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L <sub>2</sub>	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	14		5	14	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296RI

When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

**JEDEC MO-001-AC**

16-Lead

(except types CD4026AF, CD4029AF, CD4031AF, CD4033AF)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A <sub>1</sub>	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B <sub>1</sub>	0.035	0.065		0.89	1.65
C	0.008	•0.012		0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E <sub>1</sub>	0.240	0.260		6.10	6.60
e <sub>1</sub>	0.100 TP		2	2.54 TP	
e <sub>A</sub>	0.300 TP		2, 3	7.62 TP	
L	0.125	0.160		3.18	3.81
L <sub>2</sub>	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	16		5	16	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.050	0.080		1.27	2.03
S	0.010	0.060		0.254	1.52

92CM-15967RI

**JEDEC MO-001-AG**

16-Lead

(Types CD4026AF, CD4029AF, CD4031AF, CD4033AF)

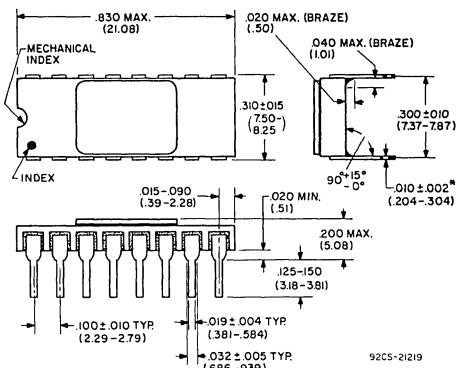
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.165	0.210		4.20	5.33
A <sub>1</sub>	0.015	0.045		0.381	1.14
B	0.015	0.020		0.381	0.508
B <sub>1</sub>	0.045	0.070	7	1.15	1.77
C	0.009	•0.011		0.229	0.279
D	0.750	0.795		19.05	20.19
E	0.295	0.325		7.50	8.25
E <sub>1</sub>	0.245	0.300		6.23	7.62
e <sub>1</sub>	0.100 TP		2	2.54 TP	
e <sub>A</sub>	0.300 TP		2, 3	7.62 TP	
L	0.120	0.160		3.05	4.06
L <sub>2</sub>	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	16		5	16	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.050	0.080		1.27	2.03
S	0.010	0.060		0.254	1.52

92CM-22284

This outline differs from the standard 16-Lead frit-seal ceramic package MO-001-AC as indicated by the values in italics shown in the chart above.

## Ceramic Dual-in-Line Welded Seal

## 16-Lead Side-Brazed

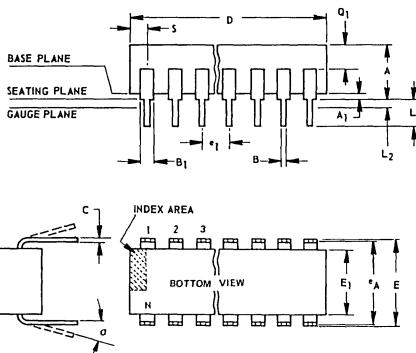


\* WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAX. LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED 0.013 (0.33mm).

NOTE: DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS AND ARE DERIVED FROM THE BASIC INCH DIMENSIONS

## DIMENSIONAL OUTLINES

## Plastic Dual-in-Line Packages



## NOTES:

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3.  $e_A$  applies in zone  $L_2$  when unit installed.
4.  $a$  applies to spread leads prior to installation.
5.  $N$  is the maximum quantity of lead positions.
6.  $N_1$  is the quantity of allowable missing leads.

## JEDEC MO-001-AB

## 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A <sub>1</sub>	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B <sub>1</sub>	0.050	0.065		1.27	1.65
C	0.008	• 0.012		0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E <sub>1</sub>	0.240	0.260		6.10	6.60
$e_1$	0.100 TP		2	2.54 TP	
$e_A$	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L <sub>2</sub>	0.000	0.030		0.000	0.76
$\alpha$	0°	15°	4	0°	15°
N	14		5	14	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296RI

## JEDEC MO-001-AC

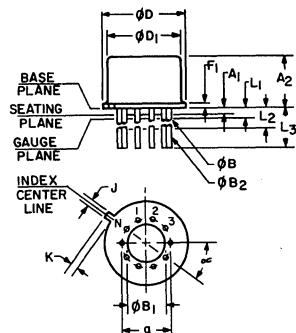
## 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A <sub>1</sub>	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B <sub>1</sub>	0.035	0.065		0.89	1.65
C	0.008	• 0.012		0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E <sub>1</sub>	0.240	0.260		6.10	6.60
$e_1$	0.100 TP		2	2.54 TP	
$e_A$	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L <sub>2</sub>	0.000	0.030		0.000	0.76
$\alpha$	0°	15°	4	0°	15°
N	16		5	16	
N <sub>1</sub>	0		6	0	
Q <sub>1</sub>	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967RI

When these devices are supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".

## TO-5-Style Package



## JEDEC MO-006-AG

## 12-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230	TP	2	5.84	TP
A1	0	0		0	0
A2	0.165	0.185		4.19	4.70
$\phi B$	0.016	0.019	3	0.407	0.482
$\phi B_1$	0	0		0	0
$\phi B_2$	0.016	0.021	3	0.407	0.533
$\phi D$	0.335	0.370		8.51	9.39
$\phi D_1$	0.305	0.335		7.75	8.50
F1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L1	0.000	0.050	3	0.00	1.27
L2	0.250	0.500	3	6.4	12.7
L3	0.500	0.562	3	12.7	14.27
$\alpha$	360 TP			360 TP	
N	12		6	12	
N1	1		5	1	

## NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Out-lines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3.  $\phi B$  applies between  $L_1$  and  $L_2$ .  $\phi B_2$  applies between  $L_2$  and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in  $L_1$  and beyond 0.500" (12.70 mm).
4. Measure from Max.  $\phi D$ .
5. N1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

92CS-19774

# **Application Notes**

## **Operating Considerations for RCA Solid State Devices**

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

### **GENERAL CONSIDERATIONS**

The design flexibility provided by these devices makes possible their use in a broad range of applications and under

many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

### **TESTING PRECAUTIONS**

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

## TRANSISTORS AND THYRISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operations to provide some slack or an expansion elbow in each lead to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

## TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange of a transistor be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device. Soldering is the preferred method for mounting thyristors; see "Rectifiers and Thyristors," below. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

## PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

### Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping.

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When

wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

#### Mounting

Recommended mounting arrangements and suggested hardware for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4142. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The package should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the device to become excessively high.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UJD Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.

4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiber-glass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term device life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with

respect to their component parts as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol is an acceptable solvent. Examples of specific, acceptable alcohols are isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44.

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliarios No. 320-33
2. Alpha Reliarios No. 346
3. Alpha Reliarios No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

#### RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the "modified TO-5" package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an epoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

#### MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applica-

tions, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB\* LD26" or equivalent.  
(NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

#### RF POWER TRANSISTORS

##### Mounting and Handling

Stripline rf devices should be mounted so that the leads are not bent or pulled away from the stud (heat sink) side of the device. When leads are formed, they should be supported to avoid transmitting the bending or cutting stress to the ceramic portion of the device. Excessive stresses may destroy the hermeticity of the package without displaying visible damage.

Devices employing silver leads are susceptible to tarnishing; these parts should not be removed from the original tarnish-preventive containers and wrappings until ready for use. Lead solderability is retarded by the presence of silver tarnish; the tarnish can be removed with a silver cleaning solution, such as thiourea.

The ceramic bodies of many rf devices contain beryllium oxide as a major ingredient. These portions of the transistors should not be crushed, ground, or abraded in any way because the dust created could be hazardous if inhaled.

##### Operating

**Forward-Biased Operation.** For Class A or AB operation, the allowable quiescent bias point is determined by reference to the infrared safe-area curve in the appropriate data bulletin. This curve depicts the safe current/voltage combinations for extended continuous operation.

**Load VSWR.** Excessive collector load or tuning mismatch can cause device destruction by over-dissipation or secondary breakdown. Mismatch capability is generally included on the data bulletins for the more recent rf transistors.

See RCA RF Power Transistor Manual, Technical Series RMF-430, pp 39-41, for additional information concerning the handling and mounting of rf power transistors.

\*Trade Mark: Emerson and Cumming, Inc.

## INTEGRATED CIRCUITS

### **Handling**

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6000, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

### **Mounting**

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.\* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

### **Operating**

#### **Unused Inputs**

All unused input leads must be connected to either V<sub>SS</sub> or V<sub>DD</sub>, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V<sub>SS</sub> or V<sub>DD</sub>. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

### **Input Signals**

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

### **Output Short Circuits**

Shorting of outputs to V<sub>SS</sub> or V<sub>DD</sub> can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handling considerations, refer to Application Note ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

### **SOLID STATE CHIPS**

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
  - A. Storage temperature, 40°C max.
  - B. Relative humidity, 50% max.
  - C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

\*Mil-M-38510A, paragraph 3.5.6.1 (a), lead material.

## **Handling and Operating Considerations for MOS Integrated Circuits**

by S. Dansky  
 R. E. Funk

This Note describes practices for handling and operating MOS integrated circuits that will guard against device damage and assure optimum performance.

### **Handling Considerations**

The input protection networks incorporated in all RCA COS/MOS devices are effective in a wide variety of device handling situations. To be totally safe, however, it is desirable to restate the general conditions for eliminating all possibilities of device damage.

Because MOS devices have extremely high input resistance, they are susceptible to damage when exposed to extremely high static electrical charges. To avoid possible damage to the devices during handling, testing, or actual operation, therefore, the following procedures should be followed:

1. The leads of devices should be in contact with a conductive material, except when being tested or in actual operation, to avoid build-up of static charge.
2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals should not be applied to the inputs while the device power supply is off.
5. All unused input leads must be connected to either V<sub>SS</sub> (ground) or V<sub>DD</sub> (device supply), whichever is appropriate for the logic circuit involved.

Table I indicates general handling procedures recommended to prevent damage from static electrical charges.

### **Handling of Unmounted Chips**

In handling of unmounted chips, care should be taken to avoid differences in voltage potential. A conductive carrier, or a carrier having a conductive overlay, should be used.

Another important consideration is the sequence in which bonds are made; the V<sub>DD</sub> (device supply) connection should always be made before the V<sub>SS</sub> (ground) bond.

### **Handling of Subassembly Boards**

After COS/MOS units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system

**Table I — General Handling Considerations**

	<b>Should be conductive</b>	<b>Should be grounded to common point</b>
Handling Equipment	X	
Metal Parts of Fixtures and Tools		X
Handling Trays	X	X
Soldering Irons		X
Table Tops	X	X
Transport Carts		(Static Discharge Straps)
Manufacturing Operating Personnel	● (Utilize grounded metal wrist straps)	
General Handling of Devices	● (Utilize grounded metal wrist straps)	

Total protection results when personnel and materials are all at the same or ground potential.

Dry weather (relative humidity less than 30%) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed above take on added importance and should be adhered to without exceptions.

- 1-megohm series resistor.

in which the proper voltages are applied, the board is no more than an extension of the leads of the device mounted on the board.

It is good practice to put conductive clips or conductive tape<sup>1</sup> on the circuit-board terminals. This precaution prevents static charges from being transmitted through the board wiring to the devices mounted on the board.

### **Automatic Handling Equipment**

When automatic handling equipment is used, static electricity may not always be eliminated through grounding

<sup>1</sup> See Table II for sources of anti-static materials.

techniques alone. Automatic feed mechanisms must be insulated from the devices under test at the point where the devices are connected to the test set. The device-insulated part of the automatic handling mechanism (anvil transport) can generate very high levels of static electricity which are developed by the continuous flow of devices sliding over and then separating from the anvil. Total control of these static voltages is critical because of the high throughputs associated with automatic handling.

Fortunately, the resolution of this problem is simple, practical, and inexpensive. Ionized-air blowers, which supply large volumes of ionized air to objects that are to be charge neutralized, are commercially available from many supply sources. Field experience with ionized-air techniques reveals this method to be extremely effective in eliminating static electricity when grounding techniques cannot be used.

#### **Lead Bending and Forming Considerations**

Other problems that can occur in handling COS/MOS devices relate to the proper handling of leads during mounting of devices. In any method of mounting integrated circuits that involves bending or forming of the device leads, it is extremely important that the leads be supported and clamped between the bend and the package seal, and that bends be made with extreme care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead flat-packaged integrated circuits, less than the lead thickness. It is also extremely important that the ends of the bent leads be perfectly straight and parallel to assure easy insertion through the holes in the printed-circuit board.

Bending, forming, and clinching of integrated-circuit leads produce stresses in the leads and can cause stresses in the seals if the above precautions are not taken. In addition, wide variations in temperature during normal use result in stresses in the device leads. Tests of 14-lead flat-pack integrated circuits, conducted under worst-case conditions in which the packages were rigidly attached to posts extending from the printed-circuit board, showed that over a temperature swing of 180°C (from -55°C to +125°C) the stress developed in the leads, the tensile pull on the leads, the shear stress introduced on the seal, and the tensile stress developed in the seal were all well within the limits for these materials. The use of thermal-stress-relief bends is, therefore, not necessary.

#### **Soldering Time and Temperature**

All device leads can withstand exposure to temperatures as high as 265°C for as long as ten seconds, and as close as  $1/16 \pm 1/32$  inch from the body of the device.

#### **Storing of COS/MOS Chips**

COS/MOS chips, unlike most packaged devices, are non-hermetic devices, fragile and small in physical size, and

therefore require the following special handling considerations:

1. Chips must be stored under proper conditions to assure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the storage temperature should not exceed 40°C and the environment should be clean, dust-free, and less than 50% relative humidity.
2. After mounting and bonding, these non-hermetic chips should not be subjected to moist or contaminated atmospheres that might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

For further information on COS/MOS chip handling, refer to File No. 517, "CD4000AH Series COS/MOS Chips".

#### **Storing of Printed-Circuit Boards**

Excessive humidity (greater than 60%) should be avoided during circuit-board check-out to prevent the false impression of excessive device internal leakage. High relative humidity may cause leakage paths between closely spaced elements of the circuit boards, such as the terminals and insulated metallized connection strips. Normally this added leakage is not significant in non-COS/MOS devices. However, when the nanoampere-leakage advantages of COS/MOS devices are desired, leakage currents on circuit boards or non-hermetic modules which are affected by high humidity become of major concern and must be controlled by coating, cleaning, or better environmental controls.

#### **Effects of Humidity on Static Electricity**

Dry weather (relative humidity less than 30%) tends to multiply the accumulation of static charges on any surface. Conversely, higher humidity levels tend to reduce the magnitude of the static voltage generated. In a low-humidity environment, the handling precautions listed in Table I take on added importance and should be adhered to without exceptions.

#### **Electrical Failure Modes Due To Improper Handling**

When the possibilities exist for appreciable static-energy discharge, and proper handling techniques are not used, electrical damage can result as follows:

- (a) shorted input protection diodes,
- (b) shorted or open gates,
- (c) opening in metal paths from the device input.

The presence of this type of device damage can be detected by curve-tracer checks of the input protection diodes of the gate-oxide protection circuits described on page 3, and also by a check of the device characteristics, especially mutual transconductance ( $gm$ ).

## Operating Considerations

	CD4000A Series
Maximum Ratings	
Storage-Temperature Range	-65 to +150°C
Operating-Temperature Range:	
Ceramic-Package Types	-55 to +125°C
Plastic-Package Types	-40 to + 85°C
DC Supply-Voltage Range:	
VDD - VSS	-0.5 to +15 V
VDD - VEE	-0.5 to + 15 V
VCC - VSS	-0.5 to +15 V
DC Input-Voltage Range	
for CD4009A, CD4010A	$V_{SS} \leq V_I \leq V_{DD}$
for CD4049A, CD4050A	$V_{SS} \leq V_I \leq V_{DD} \geq V_{CC}$
for CD4051A, CD4052A, CD4053A:	$V_{SS} \leq V_I \leq 15 \text{ V}$
Controls	$V_{SS} \leq V_I \leq V_{DD}$
Signals	$V_{EE} \leq V_I \leq V_{DD}$
Device Dissipation (per package)	200 mW
Lead Temperature (during soldering)	
at a distance $1/16 \pm 1/32$ inch	
( $1.59 \pm 0.79$ mm) from case for	
10 seconds maximum	+ 265°C

### Operating Voltage

When operating near the maximum supply-voltage range of 15 volts, care should be taken to avoid or suppress power-supply turn-on or turn-off transients, power-supply ripple or regulation, and ground noise; any of the above conditions must not cause ( $V_{DD} - V_{SS}$ ) to exceed the absolute maximum rating.

Power supplies should have a current compliance compatible with actual COS/MOS current drain.

Another good power-supply practice is to use a zener protection diode in parallel with the power bus. The zener value should be above the expected maximum regulation excursion, but should not exceed 15 volts. Fig. 1 illustrates a practical zener shunt circuit. A current-limiting resistor is included if the supply-current compliance is higher than the zener power-dissipation rating for a given zener voltage. The shunt capacitance value is chosen to supply required peak current switching transients.

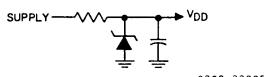


Fig. 1 – Zener-diode shunt circuit.

### Unused Inputs

All unused input leads must be connected to either  $V_{SS}$  or  $V_{DD}$ , whichever is appropriate for the logic circuit

involved. A floating input on a high-current type (such as the CD4009A, CD4010A, CD4041A, CD4049A, CD4050A) not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Another consideration with these high-current types is that a pull-up resistor from their inputs to  $V_{SS}$  or  $V_{DD}$  should be used if there is any possibility that the device may become temporarily unterminated (e.g., if the printed circuit board driving the high-current types is removed from the chassis). A useful range of values for such resistors is from 0.2 to 1 megohm.

### Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of typically less than 10 milliamperes. Input signal interfaces having the allowable 0.5 volt above  $V_{DD}$  or below  $V_{SS}$ , respectively, should be current-limited to typically 10 milliamperes or less.

Whenever the possibility of exceeding 10 milliamperes of input current exists, a resistor in series with the input is recommended. The value of this resistor can be as high as 10 kilohms without affecting static electrical characteristics. Speed, however, will be reduced due to the added RC delay. Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is

recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

### Interfacing with T<sub>2</sub>L Devices

The COS/MOS hex buffers (CD4009A, CD4010A, CD4049A, and CD4050A) are designed to drive two normal-power T<sub>2</sub>L loads. Other device types (such as the CD4041A, CD4048A, and CD4031A) can also directly drive at least one T<sub>2</sub>L load. Always consult the published data on the particular COS/MOS type for this capability. Most gates and inverters and some MSI types can drive one or more low-power T<sub>2</sub>L loads. To provide a good noise margin in the logic "1" state, T<sub>2</sub>L devices that drive COS/MOS devices require a pull-up resistor at the COS/MOS input. The COS/MOS hex buffers can also convert COS/MOS logic levels (5 to 15 volts) to T<sub>2</sub>L logic levels (5 volts), i.e., down-level conversion.

Rules for safe system design when COS/MOS interfaces with T<sub>2</sub>L and both logic systems have independent power supplies of the same voltage level but possibly on at different times are as follows:

- a) T<sub>2</sub>L driving COS/MOS -- use 1 kilohm in series with COS/MOS input
- b) COS/MOS driving T<sub>2</sub>L -- connect directly

### Interfacing with p-MOS Devices

COS/MOS devices can operate at V<sub>DD</sub> = 0 and V<sub>SS</sub> = -3 to -15 volts to interface directly with p-MOS devices with no degradation in noise immunity or other characteristics.

### Interfacing with n-MOS Devices

COS/MOS devices can be interfaced directly with n-MOS devices over the +3 to +15 volt range of power supplies.

### Fan-Out — COS/MOS to COS/MOS

All RCA COS/MOS devices have a dc fan-out capability of 50. The reduction in COS/MOS switching speed caused by added capacitive loading should, however, be consistent with high-speed system design. The input capacitance is typically 5 pF for most types; the CD4009A and CD4049A buffers have an input capacitance of typically 15 pF.

### Maximum Clock Rise and Fall Time

All COS/MOS clocked devices show maximum clock rise and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly.

### Parallel Clocking

When two or more different COS/MOS devices use a common clock, the clock rise time must be kept at a value less than the sum of the propagation delay time, the output transition time, and the setup time. Most flip-flop and shift-register types are included in this rule and are so noted in the individual data sheets.

### Noise Immunity

COS/MOS inputs normally switch at 30 to 70 per cent of the power-supply voltage. For example, for a 10-volt supply,

a logic "0" is 0 to 3 volts, and a logic "1" is 7 to 10 volts. For 5-volt operation, a logic "0" is 0 to 1.5 volts, and a logic "1" is 3.5 to 5 volts. COS/MOS noise immunity is 30 per cent of the supply voltage for the range from +3 to +15 volts.

The inherent 30-per-cent noise immunity of COS/MOS also permits a 1-volt noise margin when interfaced with T<sub>2</sub>L or DTL. For example, standard T<sub>2</sub>L and DTL interfacing with COS/MOS at a nominal V<sub>DD</sub> = V<sub>CC</sub> = 5 volts provides at least 1-volt noise margin; i.e., V<sub>OLmax(T2L)</sub> = 0.4 volt and V<sub>OLmin(DTL)</sub> = 0.45 volt; 30% of 5 volts = 1.5 volts.

This example applies typically to the 5400/7400 series, the 9000 series, and the 8000 series. HI NIL (300 series) can interface with COS/MOS at a nominal V<sub>DD</sub> = V<sub>CC</sub> = 12 volts with a worst-case noise margin of 2.1 volts.

Because COS/MOS voltage-transfer switching characteristics vary from 30 to 70 per cent of the supply voltage, system designers employing COS/MOS multivibrators, level detectors, and RC networks must consider this variation. Application Note ICAN-6267 illustrates an accurate multivibrator design technique which minimizes the switching-point variation.

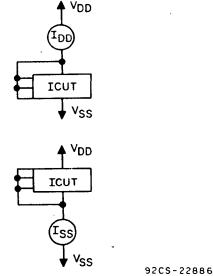
### Output Short Circuits

Shorting of outputs to V<sub>SS</sub> or V<sub>DD</sub> can cause the device power dissipation to exceed the safe value of 200 milliwatts for high-output-current types such as the CD4007A, CD4009A, CD4010A, CD4041A, CD4049A, and CD4050A. In general, outputs of these types can all be safely shorted when operated with V<sub>DD</sub> - V<sub>SS</sub> ≤ 5 volts, but may exceed the 200-milliwatt dissipation rating at higher power-supply voltages. For cases in which a short-circuited load, such as the base of a p-n-p or n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for safe operation below 200 milliwatts.

### COS/MOS Characteristics

#### Quiescent Device Leakage Current (I<sub>L</sub>):

Quiescent device leakage is measured for inputs tied high (I<sub>PD</sub>) and also for all inputs tied low (I<sub>SS</sub>), as illustrated below:



92CS-22886

#### Quiescent Device Dissipation (P<sub>D</sub>):

Quiescent device dissipation is given by

$$P_D = (V_{DD} - V_{SS}) I_L$$

where I<sub>L</sub> = I<sub>PD</sub> or I<sub>SS</sub>

## Output Voltage Levels (COS/MOS driving COS/MOS):

 $V_{OL}$  = Low-Level("0") Output = 10 mV\* at 25°C $V_{OH}$  = High-Level("1") Output =  $V_{DD}$  - 10 mV\* at +25°C

## Noise Immunity:

$V_{NL}$  = the maximum noise voltage that can be applied to a logic "0" input (added to  $V_{SS}$ ) before the output changes state.

$V_{NH}$  = the maximum noise voltage that can be applied to a logic "1" input (subtracted from  $V_{DD}$ ) before the output changes state.

## Output Drive Current:

Sink Current ( $I_{DN}$ ) = the output sink current provided by the n-channel transistor without exceeding a given output voltage ( $V_o$ ) as shown on each data sheet.

Source Current ( $I_{DP}$ ) = the output source current provided by the p-channel transistor without dropping below a given output voltage ( $V_o$ ) as shown on each data sheet.

Input Current ( $I_I$ ):

Input current is typically 10 picoamperes (3 to 15 volts) at  $T_A = 25^\circ\text{C}$ . Maximum input currents for COS/MOS devices are normally below 10 nanoamperes at 15 volts, and below 50 nanoamperes at  $T_A = +125^\circ\text{C}$ .

## AC (Dynamic) Characteristics:

Test parameters shown in the published data are measured at  $T_A = 25^\circ\text{C}$  with a 15-pF load and an input-signal rise or fall time of 20 nanoseconds. Actual system delays and transition times may be increased due to longer input rise and fall times. Graphs are included in the individual data sheets to illustrate typical variation of delays and transition times with capacitive loading. The designer should use a typical temperature coefficient of 0.3%/°C for estimating speeds at temperatures other than +25°C. Propagation delays and transition times increase with rising temperature; maximum clock input frequencies decrease with rising temperatures.

Dynamic power dissipation for each device type is shown graphically in the published data as a function of device operating frequency.

## Gate-Oxide Protection Circuits

Most COS/MOS gate inputs have the protection shown in Fig. 2. An exception to this statement is the input network for the CD4049A and CD4050A shown in Fig. 3. Figs. 4 and 5 illustrate the protection diodes inherently present at all transmission-gate input/output terminals and all inverter outputs. ICAN-6218 gives further information on protection circuits.

The protection networks can typically protect against 1-2 kilovolts of energy discharge from a 250-pF source.

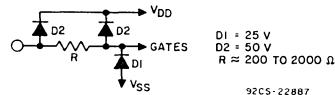


Fig. 2 – Normal gate-input-protection circuit.

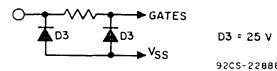


Fig. 3 – CD4049A/CD4050A gate-input-protection circuit.

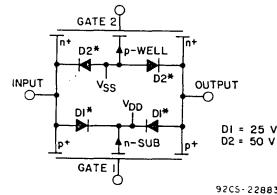


Fig. 4 – Transmission gate-input-output protection.

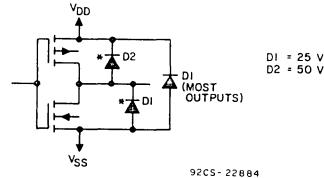


Fig. 5 – Active (inverter) output protection.

\* This voltage may be difficult to measure depending on accuracy, resolution, and offset voltage of test equipment used. Although device output "1" or "0" limits to which RCA tests in manufacture are 10 millivolts, a value of 50 millivolts may be used for customer measurements without compromise of device quality or system performance.

\* THESE DIODES ARE INHERENTLY PART OF THE MANUFACTURING PROCESS

**Table II – Partial List of Materials and Equipment Available  
for the Control of Static Charge**

Company	Conductive Foam	Conductive Envelopes	Static Neutralizing Air Blowers	Anti-Static Sprays	Conductive Tape
Custom Material Inc. Chelmsford, Mass.	Velofoam #7672	Velobags #1798M	TEC Dynastat DS120		P. C. Contab Shunt
3M Company St. Paul, Minn.			Ionized Air Blower #905	See Technical Bulletins	Scotch Shielding Tapes
Scientific Enterprises, Inc. Bloomfield, Colo.			Micro Stat 575 Portable Ionizer		
Emerson & Cuming, Inc. Canton, Mass.	ECCOSORB LD26			See Technical Bulletins	

## **Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC**

By O. H. Schade, Jr.

RCA COS/MOS integrated circuits have demonstrated outstanding performance in a wide variety of DIGITAL applications. Simplified circuitry, design flexibility, low power consumption, moderate speed, and high noise immunity of these devices can complement the high transconductance of bipolar IC's in an extension to LINEAR signal processing applications. This Note demonstrates the use of The RCA-CD4007A<sup>♦</sup> COS/MOS Dual Complementary Pair Plus Inverter as the Digital-to-Analog (D/A) switch; the op-amp output stage for a Digital-to-Analog Converter (DAC) uses COS/MOS and bipolar transistor-array IC's.

### **General Considerations**

In combination with a p-channel input pair (two p-channels of the CD4007A), a buffer-follower COS/MOS-bipolar op-amp has been designed with the capability to attain essentially the negative supply voltage at both the input and output terminals. Therefore, to consider inexpensive single-supply operation becomes possible without the sacrifice of speed and bandwidth that results with many monolithic bipolar IC op-amps. An additional advantage is the use of an MOS input stage to provide exceptionally high input resistance and low input current.

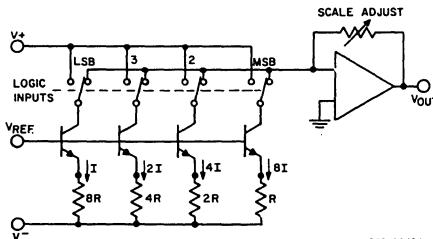
A 9-bit DAC is described in this Note to illustrate this design approach. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide film resistors, a COS/MOS-bipolar op-amp follower, and an inexpensive monolithic regulator in a simple single-supply system. An additional feature which complements the ever-increasing use of COS/MOS IC's for digital signal processing is the readily interfaced COS/MOS-DAC input logic.

Although the accuracy of a DAC system depends on many factors, it is the ladder network which must initiate properly-proportioned current or voltage outputs. Recognition of various ladder types and an appreciation of the design flexibility and constraints are paramount to a well executed DAC development.

### **Resistance Networks for DAC's**

Ladder networks for DAC's can take many forms, although three types are most generally encountered. Among the best-known variations is the current ladder shown in Fig. 1. This network is frequently used in combination with bipolar current switches which utilize a reference potential at the transistor base terminals to establish emitter currents having binary proportions. Because current summing is accomplished at the collectors of these transistors, the extent of  $V_{BE}$ - and beta-matching of these transistors depends on the degree of accuracy and temperature-range requirements. The use of a 10/20/40/80  $\text{k}\Omega$  network in conjunction with a "quad" switch, a follower amplifier, and dual power supplies is common.

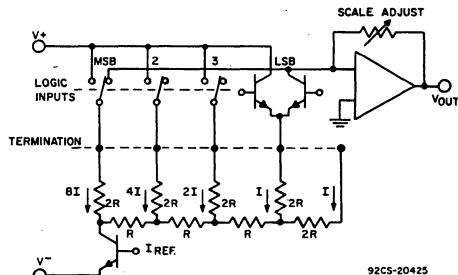
♦For data, see bulletin File No. 479.



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*Fig. 1— Current ladder-network for bipolar DAC.*

Fig. 2 shows an R/2R current ladder commonly employed in monolithic DAC's. Similar resistance values can simplify the problem of meeting ratio-match accuracy requirements. This ladder must be terminated in a single potential (or at least invariable values) to maintain proper current proportions. Although the *absolute* resistance values of the circuit in Fig. 1 must temperature track the summing resistor (or additional compensation must be employed), the R/2R current ladder must maintain only a resistance *ratio*; it is the current sink which must remain stable under external influences.



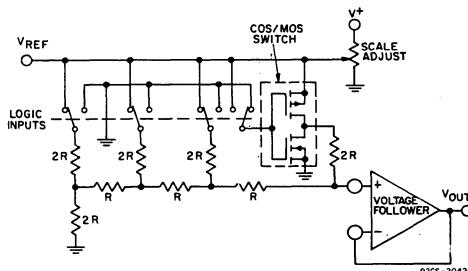
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Fig. 2— R/2R current ladder-network for monolithic DAC.

Fig. 3 shows a less common *voltage* ladder suitable for DAC's using COS/MOS switches. Output potentials are obtained directly by terminating the ladder arms at either the positive or the negative power supply. Each COS/MOS inverter output pair functions as a double-throw switch. If the switch (channel) resistance is kept small compared to the ladder-arm resistance value, accuracy becomes a function of ladder supply voltage and resistance ratios alone. Operation of this ladder is *dynamic*; the current in an arm reverses as the logic state changes. Therefore, stray capacitances (or the inductance of a wirewound resistor) can limit speed as a result of typical settling times of several microseconds.

However, the proper selection of parallel connection of switches for the most significant bit (MSB) to minimize channel resistance can result in COS/MOS-DAC speeds which approach those of the best bipolar systems, particularly when consideration is given to follower-amplifier speed limitations.

In the illustrative 9-bit application, a modified voltage-ladder design is employed. The use of 1%-tolerance metal-oxide film resistors can result in inexpensive networks suitable to about the 10-bit level. Such networks are readily constructed for system evaluations and may also prove to be suitable for production. Practical tolerance considerations call for variations from the "pure" R/2R configuration, as discussed later.



92CS-20426

Fig. 3— R/2R voltage ladder-network for COS/MOS DAC.

### The COS/MOS Switch

A typical COS/MOS switch (CD4007A) is shown in Fig. 4. A change in input logic level causes the output to swing to either the positive or the negative supply voltage. Power consumption is low, typically a few microwatts to a few milliwatts, depending on the ladder resistance and voltage choice. Large DAC ladder resistance values can be used to minimize the effects of switch resistance. Fig. 5 shows the minimum ladder resistance value for a given saturation resistance to produce an accuracy of 1/2 LSB (Least Significant Bit), with bit number as a parameter. For example, the CD4007A which has a channel resistance of approximately 250-ohms ( $V_{DD} = 10$  V), requires a minimum ladder resistance of 100 k $\Omega$  to maintain a 9-bit accuracy level. Reference to the dashed "settling time" line and the rightside ordinate shows that the approximate settling time of such a network having a 10-pF node capacitance is 6  $\mu$ s. This settling time has been based on six time constants for settling to 1/2 LSB, an *average* value for the bit range illustrated. If a faster settling time is required, circuits employing the RCA-CD4041A can be used.

The CD4041A<sup>o</sup> can drive (in a theoretical example) a 4-k $\Omega$ , 6-bit ladder network which has a settling time of approximately 250 ns. This is as fast as the *best* presently available monolithic bipolar switches. High-slew-rate voltage-follower amplifiers are needed to maintain these speed levels; when a COS/MOS bipolar op-amp is used, the slew rate is approximately 30 V/ $\mu$ s and the settling time is several hundred nanoseconds for a 10-V full-scale signal. This performance approaches the state-of-the-art for monolithic op-amps, especially in low-cost systems. In fact, high-speed op-amps capable of swinging to the negative supply have not generally been available.

### A Voltage-Follower Amplifier for Single-Supply Operation

It is practical to utilize commercially available COS/MOS and bipolar transistor-array IC's to provide a composite op-amp suitable for single-supply DAC systems. Fig. 6 shows a unity-gain follower amplifier having a COS/MOS p-channel input, an n-p-n second gain stage, and a COS/MOS inverter output. The IC building blocks are two CA3600E's<sup>a</sup> (COS/MOS Transistor Pairs) and a CA3046<sup>b</sup> n-p-n transistor array. A zener-regulated leg provides bias for a 400- $\mu$ A p-channel current source feeding the input stage, which is terminated in an n-p-n current mirror. Amplifier voltage-offset is nulled with the 10-k $\Omega$  balance potentiometer. The second-stage current level is established by the 20-k $\Omega$  load, and is selected to approximate the first-stage current level, to assure similar positive and negative slew rates. The COS/MOS inverter portion forms the final output stage and is terminated in a 2-k $\Omega$  load, a typical value used with monolithic op-amps. Voltage gain is affected by the choice of load resistance value. The output stage of this amplifier is easily driven to within 1 mV of the negative supply voltage.

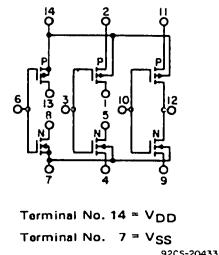


Fig. 4— CD4007A schematic diagram.

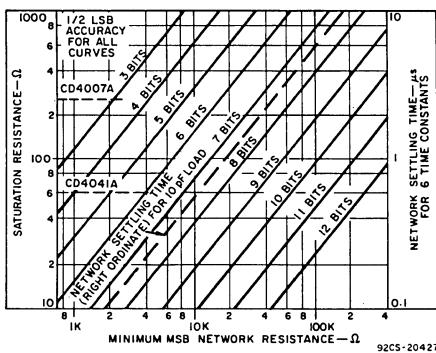


Fig. 5— COS/MOS-DAC voltage-network requirements.

<sup>a</sup>COS/MOS Quad True/Complement Buffer

<sup>b</sup>For data, see bulletin File No. 619.

<sup>c</sup>For data, see bulletin File No. 341.

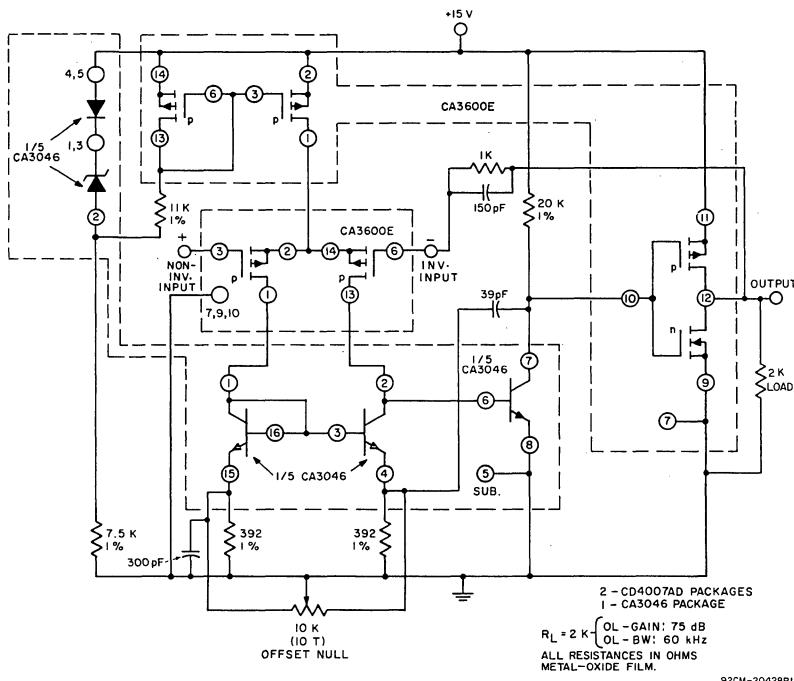


Fig. 6— Voltage-follower amplifier for single-supply operation.

Compensation for the unity-gain non-inverting mode is provided by Miller feedback of 39 pF and a 300-pF by-pass capacitor shunting one-half the driving current (1-2 MHz). Unity-gain bandwidth is just under 10 MHz and the open-loop gain is 75 dB. Fig. 7 shows the gain-bandwidth characteristics for this circuit. A potential latch situation at the bipolar mirror is avoided by use of resistor-capacitor network ( $R = 1 \text{ k}\Omega$ ,  $C = 150 \text{ pF}$ ), which limits the dc feedback through the p-channel gate-protective diode.

The amplifier response to 4-V input pulses is shown in Fig. 8. Although the slew rate is approximately  $30 \text{ V}/\mu\text{s}$ , the settling time is significantly prolonged (approximately  $2 \mu\text{s}$ ) as a result of the method of second-stage biasing when the output swings near the negative supply. For many applications, this speed loss is not significant. If a faster amplifier is desired, the load resistor can be replaced with a p-channel CA3600E current source similar to that used for the first stage. In fact, it may be desirable to change the current and resistance values to optimize the gain/speed trade-off for a particular application. For example, if higher gain is desired for less follower offset, the  $20\text{-k}\Omega$  resistance value can be increased. The choice of output load resistance also affects the gain/speed compromise.

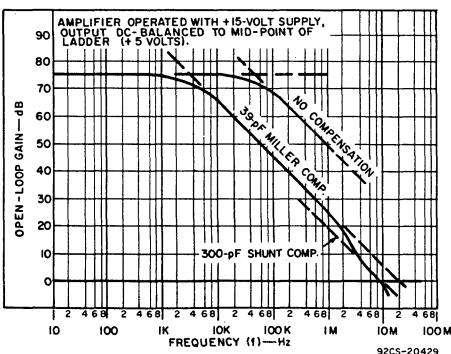


Fig. 7— Voltage-follower open-loop gain characteristics.

### A 9-Bit COS/MOS DAC

An example of a 9-bit DAC is shown in Fig. 9. Three CD4007A IC packages perform the switch function using a 10-V logic level. A single 15-V supply provides a positive bus for the follower amplifier and feeds the CA3085<sup>A</sup> voltage regulator. The "scale-adjust" function is provided by the regulator output control which is set to a nominal 10 V in this system. The line-voltage regulation (approximately 0.2%) permits 9-bit accuracy to be maintained with a variation of several volts in the supply. System power consumption ranges between 70 and 200 mW; a major portion is dissipated in the load resistor and op-amp. The regulated supply provides a maximum current of 440  $\mu$ A of which 370  $\mu$ A flows through the scale-adjust leg.

The resistor ladder is composed of 1-per-cent tolerance metal-oxide film resistors available from several manufacturers at modest cost. The five arms requiring the highest accuracy are built of series and parallel combinations of 806-k $\Omega$  resistors from the same manufacturing lot. The ratio match between resistance values is in the order of 0.2%, usually without need for special selection. The construction of a "standard" with eight parallel resistors assures a high probability that ratio matching will be satisfactory. If the usual assumption that tolerances can be improved with the square-root of the sample number is adopted, the loss of

tolerance is slower than the increase of resistance value toward the LSB. Once the most critical match has been attained, therefore, subsequent ratio matches should be more than adequate. An impedance-matching resistor is used between the fifth and sixth bits to permit ladder completion with individual resistors of the most desirable values where a 1% tolerance is adequate. This resistor value is chosen as R5-1/2R6, to terminate the first five bits in a fifth-bit value (the impedance is 1/2R6 looking into that node).

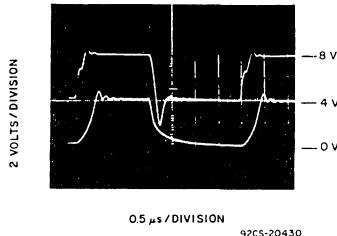


Fig. 8— Amplifier response to 4-V input pulses.

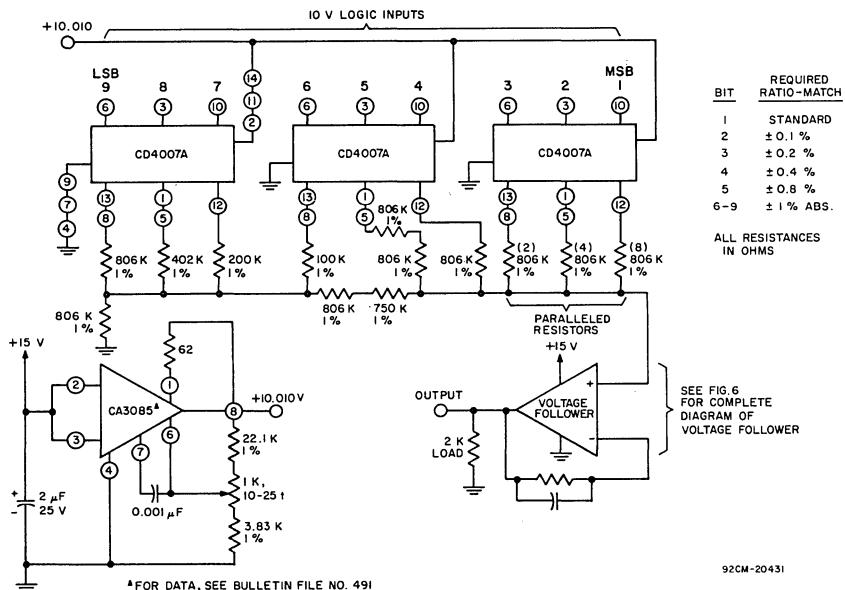


Fig. 9— 9-bit DAC using COS/MOS CD4007A.

The follower amplifier has the offset adjustment nulled at approximately a 1-volt output level. System operating potentials are shown in Table I, where each bit is set "low" individually to observe the progression of output values. The positive ladder-supply voltage was adjusted to 10.010 V to provide a small compensation for the MSB switch resistance. A high-impedance 5-digit multimeter, such as the DANA 5330 or equivalent, is needed for direct measurement of the ladder output, and is invaluable during system development and evaluation. Table I shows ideal potential values, system output, and ladder output and illustrates the sources of system inaccuracy. The system output maintains proportional accuracy within  $\pm 5.6$  mV, or  $\pm 1/4$  LSB.

Fig. 10 shows the system output response to a 4-V logic pulse. The ringing is caused by the voltage follower, and the more gradual transients are caused by voltage-follower and ladder time constants. Settling time to  $1/2$  LSB is 5  $\mu$ s.

This 9-bit COS/MOS-DAC demonstrates accuracy and simplicity with economical components and modest power-supply requirements. In addition, the design flexibility afforded by the COS/MOS building blocks simplifies the generation of DAC systems tailored to individual needs. COS/MOS switches used in conjunction with COS/MOS counters also find application in Analog-to-Digital Conversion Systems. The low-power and high noise-immunity features of these devices make them attractive A/D system components.

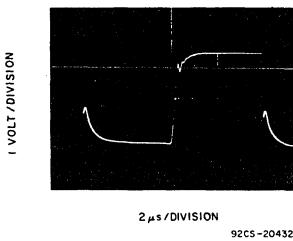


Fig. 10—System response to most-significant-bit logic pulse.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

Table I. Set Of Values For 10.010-V Regulated Supply Voltage

BINARY WORD	IDEAL POTENTIAL (V)	SYSTEM OUTPUT (V)	LADDER OUTPUT (V)	SYSTEM ERROR (mV)	VOLTAGE FOLLOWER OFFSET (mV)	LADDER & SWITCH ERROR (mV)	POSITIVE SWITCH DROP (mV)
000000000	9.9802	9.9856	9.9915	+ 5.4	- 5.9	+ 11.3	-
011111111	5.0000	4.9959	4.9997	- 4.1	- 3.8	- 0.3	14.8
101111111	2.5000	2.4996	2.5023	- 0.4	- 2.6	+ 2.3	11.0
110111111	1.2500	1.2554	1.2565	+ 5.4	- 1.0	+ 6.5	6.5
111011111	0.6250	0.6233	0.6226	- 2.7	+ 0.7	- 2.4	3.2
111101111	0.3125	0.3133	0.3113	+ 0.8	+ 2.1	- 1.2	1.7
111110111	0.1568	0.1603	0.1571	+ 3.5	+ 3.2	+ 0.3	14.0
111111011	0.0784	0.0826	0.0786	+ 4.2	+ 4.0	+ 0.2	11.8
111111101	0.0397	0.0439	0.0393	+ 4.2	+ 4.6	- 0.4	6.8
111111110	0.0198	0.0245	0.0195	+ 4.7	+ 5.0	- 0.3	3.6
111111111	0.0000	0.0056	0.0000	+ 5.6	+ 5.6	0.0	-



## Timekeeping Advances Through COS/MOS Technology

by S.S. Eaton

Most COS/MOS timing circuits consist of three basic parts: an oscillator, or main timing standard; some digital processing logic, usually in the form of frequency-dividing circuits; and logic-circuit drivers for mechanical or electrical output devices controlled by the digital processing logic. The oscillator is perhaps the most important because the accuracy of the total COS/MOS timing system is entirely dependent upon the accuracy of the oscillator. This Note discusses basic oscillator design considerations, practical COS/MOS oscillator circuits, and some typical COS/MOS timing-circuit applications.

### BASIC OSCILLATOR DESIGN CONSIDERATIONS

A basic oscillator circuit consists of an amplifier and a feedback section, as shown in Fig. 1. For oscillation to occur, the gain of the amplifier times the attenuation of the feedback network must be greater than one. In addition, the total phase shift through the amplifier and feedback network must be equal to  $n$  times 360 degrees, where  $n$  is an integer. These conditions imply that oscillations occur in any system in which an amplified signal is returned in phase to the amplifier input after being attenuated less than it was originally amplified. In such a system, any noise present at

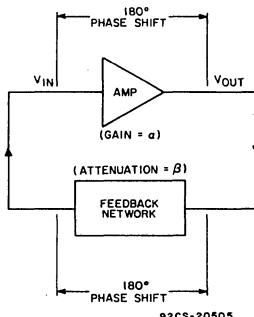


Fig. 1— Basic oscillator circuit.

the amplifier input causes oscillation to build up at a rate determined by the loop gain, or  $\alpha\beta$  product, of the over-all circuit.

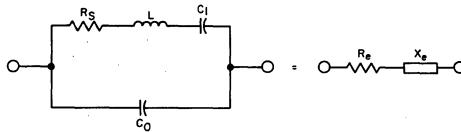
The frequency stability of an oscillator is primarily dependent upon the phase-changing properties of the feedback network. For high stability, quartz crystals and tuning forks are commonly used as feedback network elements. The quartz crystal is the more popular because of its higher Q or greater inherent frequency stability.

### Selection of Crystal Operating Mode

Fig. 2 shows the equivalent circuit of a quartz crystal, and Table I lists typical component values of the elements included in the equivalent circuit for different crystal cuts and operating frequencies. The basic circuit can be resolved into equivalent resistive ( $R_E$ ) and reactive ( $X_E$ ) components. Fig. 3 shows curves of these components as functions of frequency for a typical 32.768-kHz crystal. Fig. 3(b) shows two points at which the crystal appears purely resistive, (i.e., points at which  $X_E = 0$ ). These points are defined as the resonant ( $f_r$ ) and antiresonant ( $f_a$ ) frequencies. Series-resonant oscillator circuits are designed to oscillate at or near  $f_r$ . Parallel-resonant circuits oscillate between  $f_r$  and  $f_a$ , depending upon the value of a parallel loading capacitor, as discussed later. In contrast to series-resonant circuits, parallel resonant-circuits work best with amplifiers that have high input impedances. The parallel-resonant circuit, therefore, is most applicable to crystal oscillators that employ COS/MOS amplifiers.<sup>1</sup>

### Feedback-Circuit Configuration

A feedback circuit suitable for use with a parallel-resonant oscillator circuit is shown in Fig. 4. This circuit, known as a crystal pi network, is intended for use after an amplifier that provides a 180-degree phase shift. The pi network is designed to provide the additional 180-degree phase shift required for oscillation. The phase angle for this type of feedback circuit is extremely sensitive to a change in frequency, a condition necessary for stable oscillation. If the equivalent resistance of the crystal were in fact zero (infinite



**Fig. 2— Equivalent circuit for a quartz crystal.**

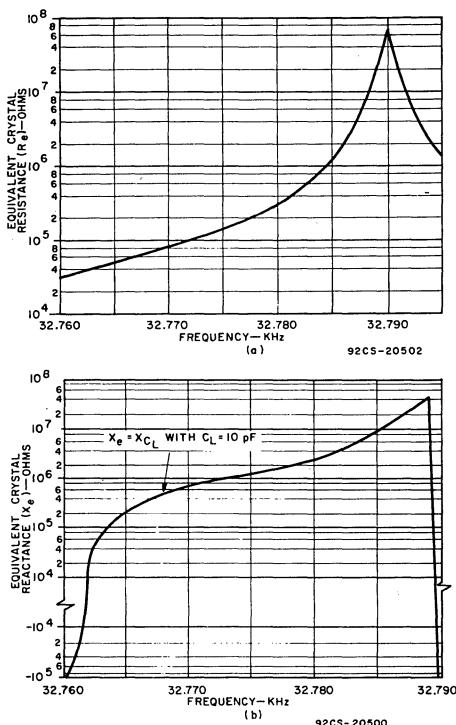
**Table I — Typical Component Values for Common Cuts of Quartz Oscillator Crystals**

FREQUENCY	32 kHz	280 kHz	525 kHz	2MHz
Cut	XY Bar	DT	DT	AT
R <sub>s</sub> (ohms)	40K	1820	1400	82
L (Hy)	4800	25.9	12.7	0.52
C <sub>1</sub> (pF)	0.00491	0.0125	0.00724	0.0122
C <sub>0</sub> (pF)	2.85	5.62	3.44	4.27
C <sub>0</sub> /C <sub>1</sub>	580	450	475	350
Q	25000	25000	30000	80000

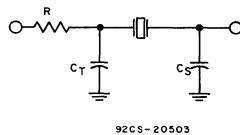
Q), a change in the phase angle of the feedback circuit would not cause any change in oscillator frequency; the frequency, therefore, would be insensitive to any phase change in the amplifier. Though practical crystals allow only a slight change in frequency for large variations in phase angle, the amplifier phase angle should, to the extent possible, be made independent of temperature and supply-voltage variations in order to minimize the phase compensation required of the feedback network. Any required phase compensation will, of course, dictate a corresponding change in the frequency of oscillation consistent with practical values of crystal Q. For this reason, the equivalent resistance of the crystal should be maintained as low as possible, and the amplifier should be designed to roll off at frequencies greater than the crystal frequency.

#### Oscillator Amplifier

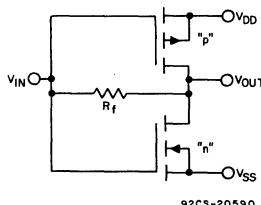
Fig. 5 shows a COS/MOS amplifier circuit that may be used to provide the amplification function in a crystal-controlled oscillator. The amplifier is biased so that the output voltage V<sub>OUT</sub> is equal to the input voltage V<sub>IN</sub> or typically is equal to one-half the supply voltage V<sub>DD</sub>, (i.e., V<sub>OUT</sub> = V<sub>IN</sub> = V<sub>DD</sub>/2). Biasing is accomplished by means of a resistor that has a value high enough to prevent loading of the feedback network, yet that is low in comparison to the amplifier input resistance. Resistor values of 10 to 500 megohms will satisfy these criteria; however, lower values in the order of 15 megohms are generally used to allow greater input leakage without any severe change in bias point. The gain of the amplifier varies with supply voltage, the size of the n- and p-channel MOS transistors, and the sum of the threshold voltages of the n- and p-channel transistors. When an oscillator amplifier is designed to roll off at frequencies greater than the crystal frequency, care must be taken to



**Fig. 3— Impedance characteristics of a quartz oscillator crystal: (a) equivalent crystal resistance as a function of frequency; (b) equivalent crystal reactance as a function of frequency.**



**Fig. 4— Crystal pi-type feedback network.**



**Fig. 5— COS/MOS amplifier.**

assure that the transistor sizes are large enough for the particular supply voltage used and range of threshold voltages expected. For any circuit, though, the sum of the threshold voltages of the n- and p-channel transistors must always be less than the supply voltage.

The oscillator amplifier governs, to a certain extent, the selection of the components for the feedback network. The amplifier current consumption is strongly dependent upon the attenuation across the feedback network. As the attenuation becomes greater, the signal at the amplifier input becomes smaller, which, in turn, increases the amplifier current consumption. Large voltage swings at the amplifier input cause little current to flow because the resistance of either the n- or p-channel transistor is high during a large portion of the cycle. On the basis of power considerations, it is best to design the feedback network for a small attenuation.

#### Equivalent Crystal Resistance

The equivalent resistance  $R_s$  of the crystal should be maintained as small as possible in order to obtain minimum attenuation across the feedback network. For any given circuit, the oscillator current always increases with a rise in crystal resistance. This factor and stability considerations provide strong arguments for the purchase of crystals that have low series resistance, although the usual cost tradeoffs prevail.

#### Crystal Load Capacitance

Another factor that influences the over-all power consumption is the size of the pi-network capacitor at the amplifier output. For minimum current consumption, this capacitor, obviously, should be kept small. This condition, however, does not always imply high frequency stability. The choice of the capacitor value first involves a determination of the over-all crystal load capacitance. The phase angle of the feedback network approaches 180 degrees when the crystal equivalent reactive component  $X_e$  is equal to the reactance ( $X_{CL}$ ) of a capacitor placed in parallel with the crystal. Fig. 4 shows that the effective capacitance across the crystal consists of the two pi-network capacitors in series. If the value of the equivalent reactance  $X_e$  at the crystal frequency, as may be determined from Fig. 3(b), is equal to the value of the crystal load capacitance  $C_L$ , then the equivalent value of the two series-connected pi-network capacitors can be calculated from the following relationship:

$$C_L = 1/\omega X_e \quad (1)$$

The value of the load capacitance  $C_L$ , in general, is chosen first, and the crystal manufacturer is required to cut the crystal to oscillate at the desired frequency for the specified value of load capacitance.

The choice of a load capacitance is important in terms of over-all power consumption and frequency stability. Higher values of  $C_L$  generally improve frequency stability, but also increase power dissipation. The timing industry presently seems to have standardized on values of  $C_L$  between 10 and 20 picofarads.

The choice of the total equivalent load capacitance  $C_L$  only fixes the series sum of the two pi-network capacitors. The individual capacitors themselves can be found from the following equations:

$$C_T = 4C_L/(1 - 5fR_eC_L) \quad (2)$$

$$C_S = 4C_L/(3 + 5fR_eC_L) \quad (3)$$

The actual value of  $C_S$  used in the feedback circuit should be about 3 picofarads less than the calculated value to allow for the amplifier input capacitance. The value of the amplifier output capacitor  $C_T$  should not normally be fixed. A trimmer capacitor should be placed in parallel with, or used in place of, a fixed output capacitor to allow for variations in stray capacitance and circuit components. The mid-range value of the output capacitor combination should be equal to the calculated value of  $C_T$ .

#### Frequency-Trimming Capability

The required capacitance range for the oscillator trimmer capacitor is determined by the variation in oscillation frequency with a change in load capacitance.<sup>2</sup> The total frequency-trimming range of a crystal-controlled oscillator circuit is mainly a function of the crystal characteristics, or more explicitly, is inversely proportional to the slope of the crystal reactance curve, shown in Fig. 3(b). The slope of this curve is a function of the difference between the resonant frequency  $f_r$  and the antiresonant frequency  $f_a$ . This frequency difference, in turn, is a function of the crystal capacitance ratio  $C_0/C_1$ , where  $C_0$  and  $C_1$  are the inherent shunt and series capacitances, respectively, of the crystal structure, as shown in Fig. 2. The slope of the reactance curve is also a function of the total external crystal load capacitance  $C_L$ . As shown in Fig. 3(b), this slope decreases as the equivalent reactance increases, (i.e., for smaller values of the capacitance  $C_L$ ). Fig. 6 and Table II show trimming-range data for a typical 32.768-kHz crystal that has a capacitance ratio  $C_0/C_1$  of 580. These data show that smaller values of load capacitance result in greater trimming-range capability.

#### Temperature Stability

Another important oscillator consideration is temperature stability. Most crystals have a negative parabolic temperature coefficient.<sup>2</sup> Fig. 7 shows a typical curve of the variation in crystal frequency as a function of temperature. The frequency of the total oscillator circuit also exhibits a similar temperature dependence. Temperature compensation of the over-all oscillator circuit can be achieved by use of a capacitor that has a positive parabolic temperature coefficient in the pi feedback network.<sup>3</sup> For comparison, Fig. 7 also shows a typical resultant curve for the over-all circuit.

The temperature characteristics of a crystal are determined to a large extent by the crystal cut. Popular low-frequency cuts include the NT and XY Bar. The XY Bar is the more popular of the two types because it can be made smaller for a given Q and is easier to trim. The disadvantage of a slightly lower shock resistance of XY Bar crystals is compensated by the superior aging characteristics of this type.

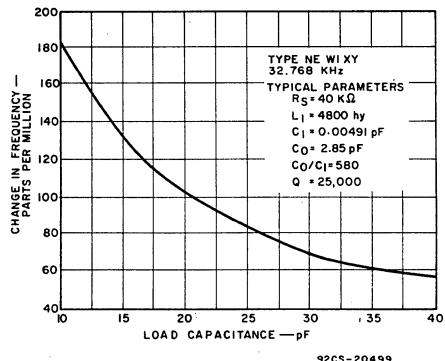


Fig. 6— Frequency as a function of load capacitance for a typical 32-kHz crystal.

AT-cut crystals, when used at frequencies greater than 1 MHz, are characterized by excellent temperature stability and ruggedness. Temperature characteristics for this type of crystal cut as well as for the XY Bar and NT types are shown in Fig. 8.

#### Crystal Dimensions

Size is also an important consideration in the design of oscillator crystals. The length of quartz required for any given cut is inversely proportional to the square root of frequency. Dimensions for a typical packaged 32-kHz, XY Bar crystal are 0.6 inch by 0.2 inch by 0.11 inch. The smallest XY Bar crystals currently available have dimensions in the order of 0.53 inch by 0.2 inch by 0.11 inch. A 1-MHz AT-cut crystal is significantly larger; however, dimensions again decrease with frequency. Crystal manufacturers are currently working to develop wristwatch-size AT-cut crystals with the anticipation of circuit improvements that will allow low-current operation at high frequencies.

#### Crystal Shock Resistance and Aging Rate

A prime concern of the timing industry today is that of crystal shock resistance and aging. The aging of a crystal results primarily from aging of the mounting material rather

Table II — Trimming Data for a Typical 32-kHz Quartz Oscillator Crystal

TRIM	LOAD CAPACITANCE, CL			
	5 pF	11.5 pF	20 pF	32 pF
± 20 PPM	-0.45 +0.51	-1.6 +2.0	-3.7 +5.5	-8.0 +14.7
± 25 PPM	-.55 +.65	-1.9 +2.6	-4.5 +7.3	-9.4 +20.5
± 30 PPM	-0.66 +0.79	-2.3 +3.3	-5.2 +9.3	-10.7 +27.9

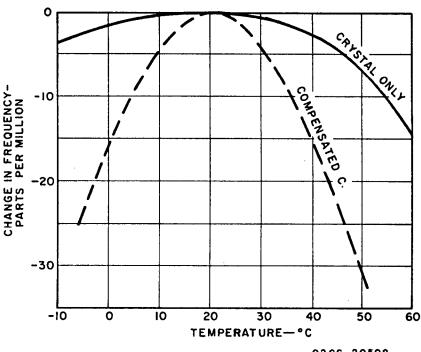


Fig. 7— Effect of temperature on crystal frequency.

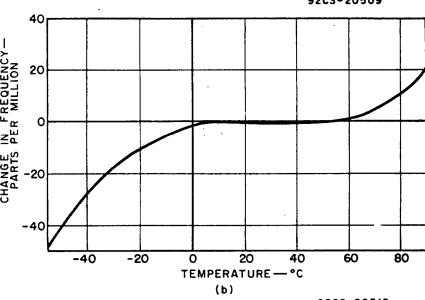
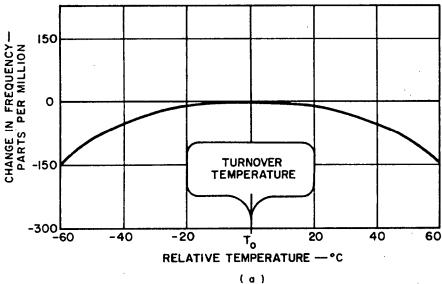


Fig. 8— Frequency-temperature characteristics for various crystal cuts: (a) XY-Bar and NT cuts; (b) AT cut.

than from aging of the quartz itself. The mounting material enters into the crystal equivalent circuit, and the slowest aging rate results when the mount consists of the least amount of supporting material. This condition of course, results in lower shock resistance, and an optimum trade-off must be achieved. At present, 32-kHz crystals can be made that can withstand a mechanical shock of about 1500 G's applied for 0.5 millisecond and that have aging rates that result in a frequency change of 2 to 5 parts per million for

the first year and essentially no aging thereafter. Any mechanical or thermal shock, however, will interrupt the normal aging process. The aging rate of 2 to 5 parts per million presently appears acceptable to the timing industry, although shock resistances of 3,000 to 5,000 G's are desired. This shock level corresponds approximately to the shock experienced by dropping the crystal from a height of one meter onto a hardwood floor.

### PRACTICAL OSCILLATOR CIRCUITS

The basic amplifier, feedback-network, and crystal considerations discussed in the preceding paragraphs can be combined in the design of COS/MOS oscillator circuits. In the circuits, the crystal selected has an equivalent resistance  $R_e$  of 50 kilohms and is cut to operate at a frequency of 32.768 kHz with a load capacitance  $C_L$  of 10 picofarads. The values of pi feedback-network capacitors  $C_T$  and  $C_S$  can be calculated by use of Eqs. (2) and (3) as  $C_T = 43$  picofarads and  $C_S = 13$  picofarads. The value of the feedback-network resistance  $R$  can be calculated as follows:

$$R = \frac{(3X_e + 0.27 R_e)(X_e - 0.8 R_e)}{16 R_e}$$

$\approx 1 \text{ M}\Omega$

This value is the maximum value of resistance allowed for a minimum feedback-network attenuation of 0.75, a value chosen on the basis of power and stability considerations.<sup>1</sup> The calculated value of  $R$  includes any fixed resistance plus the amplifier output resistance. Because the output resistance is often appreciable and varies with supply voltage, transistor size, and threshold voltages, it is generally best to add resistance experimentally until the desired power consumption and frequency stability are reached. The effect of this resistance on operating current and frequency stability can be predicted from data given in Table III for the three different COS/MOS crystal oscillator circuits shown in Fig. 9. In each circuit, the pi-network capacitors  $C_T$  and  $C_S$  are 39 picofarads and 10 picofarads, respectively. These capacitances are slightly less than the calculated values because of stray and amplifier capacitances.

The circuit shown in Fig. 9(a) combines the amplifier and feedback circuits shown in Fig. 4 and 5. Although theory predicts that an increase in the values of the feedback-network resistor  $R$  will result in increased frequency stability, the circuit performance data given in Table III show no significant improvement in this characteristic. This result indicates that the circuit instability can be attributed almost entirely to phase instabilities of the amplifier. This assumption is verified by data taken from the circuits shown in Figs. 9(b) and 9(c) in which the required feedback-network resistance is incorporated into the amplifier as a fixed value. The resistors essentially fix the amplifier phase shift so that greater stability results. As the data show, use of these resistors also results in a decrease in the total current consumption. Because of the two fixed resistors, the circuit of Fig. 9(b) shows the least current consumption and also the greatest stability.

Table III – Typical Oscillator Data

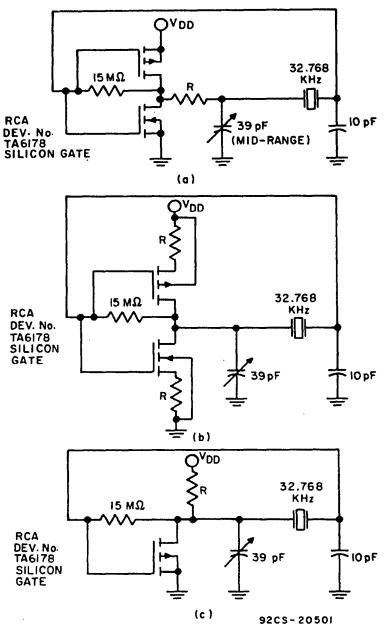
Circuit	Value of R ( $\Omega$ )	V <sub>DD</sub> (Volts)	Current ( $\mu\text{A}$ )	Frequency Stability V <sub>DD</sub> = 1.45V to 1.6V
9(a)	0	1.60	4.0	2.8
	0	1.45	3.1	
	100K	1.60	3.1	
	"	1.45	2.4	
	200K	1.60	2.9	2.6
9(b)	"	1.45	2.1	
	100K	1.60	2.3	.3
	"	1.45	2.0	
	"	1.1	1.5	
	150K	1.60	1.8	
	"	1.45	1.6	.2
	"	1.1	.95	
9(c)	200K	1.60	5.0	.6
	"	1.45	4.4	
	300K	1.60	3.5	
	"	1.45	3.0	.5

As mentioned previously, the amplifier feedback resistor should not significantly load the crystal feedback network. The resistor value at which loading begins to occur can be determined from a curve of circuit operating frequency as a function of feedback resistance. Fig. 10 shows such a curve for the circuit shown in Fig. 9(b). This curve indicates that 15 megohms is a suitable value for the feedback resistor.

### FREQUENCY DIVIDERS

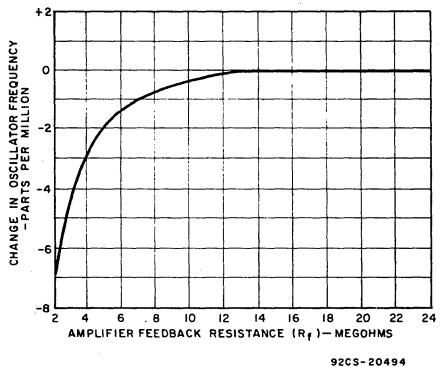
Because of restrictions on crystal size and cost, oscillator frequencies of 8192 Hz, or higher, are generally used for electronic timing circuits. The use of such high crystal frequencies usually requires division of the oscillator frequency to a more convenient value. Synchronous motors, for example, are often driven by frequencies between 0.5 Hz and 64 Hz. Numeric readouts for digital clocks or wristwatches require pulses at least every second, minute, and hour. The necessity for frequency division becomes clear if one considers the wide variety of timing intervals that may be required for certain applications.

The basic frequency-dividing circuit, shown in Fig. 11, consists of a master-slave D-type flip-flop connected as a binary counter stage.  $N$  stages may be cascaded with the final output frequency equal to  $2^{-N}$  times the input frequency. Division by integers other than powers of 2 can also be accomplished by use of gating techniques. For example, a divide-by-60 counter implemented as shown in Fig. 12, can be used to obtain minutes from seconds.

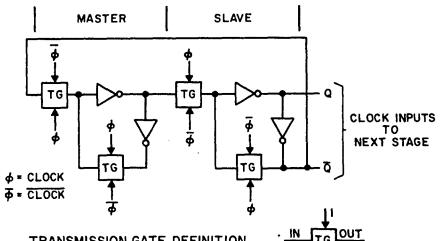


*Fig. 9— Typical COS/MOS crystal-oscillator circuits.*

A basic block diagram of a typical digital clock that employs divide-by-60 counters is shown in Fig. 13. The display for the clock is designed to be multiplexed in that new information is provided to only one of the six readout characters, while the eye itself holds the previous state of the other five. The multiplexing unit consists of COS/MOS transmission gates controlled by a six-stage ring counter that also addresses each character sequentially. This type of



*Fig. 10—Oscillator frequency as a function of amplifier feedback resistance.*



*Fig. 11—Basic frequency-dividing stage.*

circuit is particularly applicable for driving light-emitting diode displays.

Light-emitting diodes, as well as other readout devices, require some form of driving circuitry which is often unique to the driven device. Other typical readout devices include stepping motors, balance-wheel motors, tuning-fork motors, and liquid-crystal displays.

Motors are frequently driven by low-impedance MOS transistor drivers. The waveforms required depend upon the particular type of motor. Rotary stepping motors require a pulsed waveform such as that shown in Fig. 14(a). The motor advances one position (for example 180 degrees) on each pulse. Fig. 14(b) shows a COS/MOS circuit that may be used to generate this type of waveform. The crystal frequency and the number of countdown stages for this circuit determine the pulse frequency. The duty factor is controlled by two resettable flip-flops that are clocked inversely by the last counting stage and reset by an intermediate stage. The output waveform from this circuit will have a duty factor that is exactly given by  $2^I - 1 - N$  where I is the number of the intermediate stage used to reset the shaping flip-flops and N is the total number of frequency-divider stages.

A tuning-fork motor consists of two coils wired in series and wound on either side of the fork. A subdivision of the crystal frequency drives the coils which electromagnetically vibrate the fork. The fork can be linked to an index wheel that, in turn, can drive the hands of a watch.

A balance-wheel motor consists of a coil fixed near the periphery of a pivoted balance wheel. Permanent magnets are attached to one side of the wheel and counterweights to the other. The coil can be energized by pulses supplied to the gate of an n-channel MOS transistor with the coil connected between the drain and the supply voltage of the transistor. When the coil is energized, the balance wheel swings toward the coil. The momentum of the wheel moves it beyond the coil, and spring action then forces it back. Repeated cycles generate a back-and-forth type motion which can be linked to a wheel for driving the hands of a watch or clock.

Seven-segment liquid-crystal numerals can be driven as shown in Fig. 15. An ac voltage is required across each

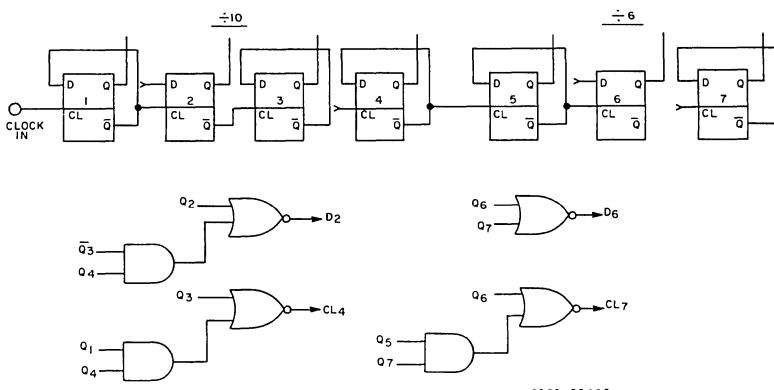


Fig. 12—COS/MOS divide-by-60 counter.

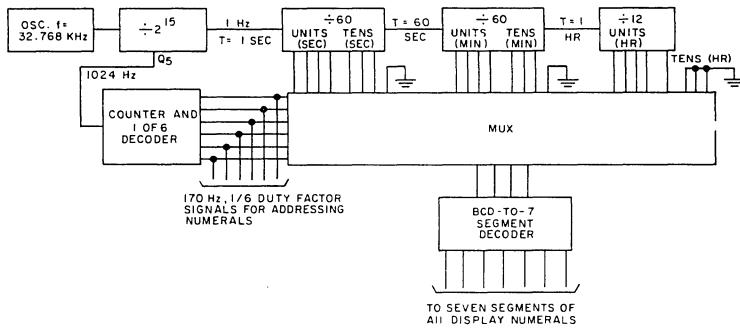


Fig. 13—Typical COS/MOS digital clock.

segment of the display to assure long life. For this purpose, a 60-Hz square wave is applied to one input of each of seven exclusive-OR gates. The logic state present at the other input determines whether the segment will transmit or scatter light.

Liquid-crystal displays can be made for operation in either transmissive or reflective modes. The transmissive-mode type requires a light source behind the display. The light will either be transmitted or not depending upon the voltage across the segment. In the reflective-mode type, ambient light can be scattered by the liquid crystal material, or reflected from a mirrored surface placed behind the numeral. If displayed correctly, excellent contrast between "on" and "off" segments can be obtained when reflecting or scattering only ambient light.

The light scattering property of liquid-crystal displays offers two major advantages. First, the problem of washout in high intensity light is prevented. Washout has always been a problem with light generating displays. Second, because the displays do not generate light, they require negligible power.

In fact, liquid crystals require the least amount of power of any currently available type of display.<sup>4</sup>

Light-emitting diodes are somewhat simpler to drive than liquid crystals because signals to individual segment and/or numerals can be easily multiplexed. Fig. 16 shows a typical multiplexed driving circuit. The n-p-n transistor, which is common to the cathode of all segments in each numeral, can be turned on to address only one particular numeral. The eye will hold the reading from all off segments long enough for at least six numerals to be multiplexed.

#### COS/MOS TIMING-CIRCUIT APPLICATIONS

The choice of a readout device depends, of course, upon the application involved and to a certain extent upon the individual characteristics of the device itself. Special considerations for readout devices are perhaps best treated in a discussion of special requirements for three important timing-circuit applications, namely, wristwatches, wall clocks, and automobile clocks.

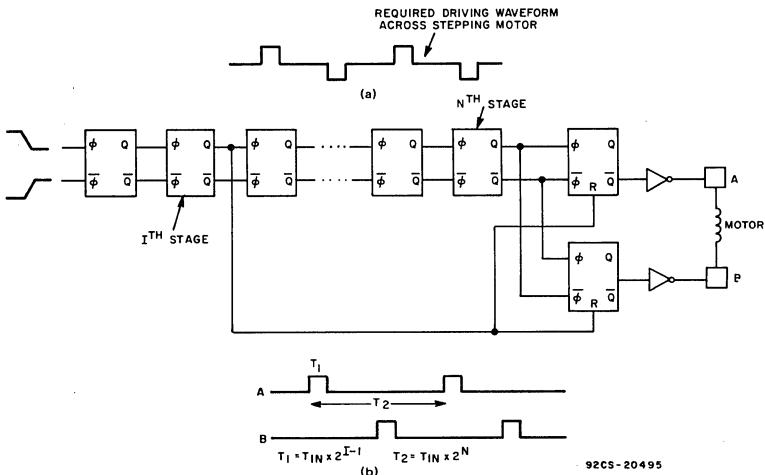


Fig. 14—Generation of required stepping-motor waveforms: (a) required driving waveform across stepping motor; (b) COS/MOS driving circuit and output waveforms applied to motor control winding.

#### Wristwatches

In any wristwatch application, size and total operating current are perhaps the two most important considerations. The total timing circuitry, together with the battery and readout device, must fit into a relatively fixed size and have a current consumption small enough to allow at least one year of life. Size and power considerations also become important in crystal selection. The size and cost of a crystal decreases with increases in frequency up to about 1 MHz. The power consumption of the oscillator and counter increases with frequency. On the basis of these considerations, the most

popular crystal frequency for wristwatches at present is 32.768 kHz. Typical packaged sizes for this crystal and various available crystal oscillator circuits were discussed in an earlier section of this Note.

The choice of a readout device also involves considerations of size and power as well as, of course, marketing considerations. If conventional-hand movements are chosen, a motor type of drive must be selected. No great size advantage exists over any of the various motor types used in this type of application. In addition, all types can be designed to operate from 1.1 to 1.6 volts with average

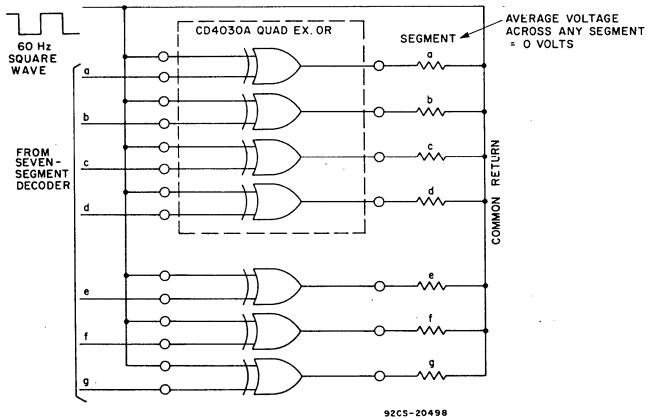


Fig. 15—COS/MOS liquid-crystal driving circuit.

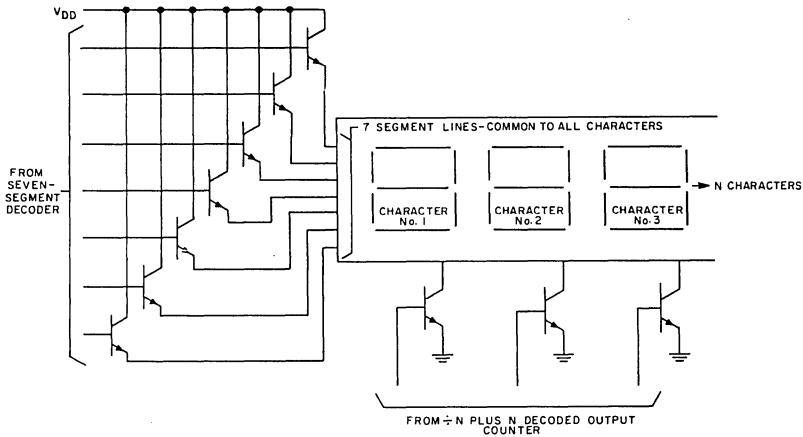


Fig. 16—Multiplexing driving circuit for light-emitting diodes.

current consumptions of about 10 microamperes. Sensitivity to vibration, however, is one separating characteristic. Although balance-wheel motors can be designed to compensate to a certain extent for speed variations produced by vibrations, the stepping motor, which is insensitive to vibration, remains superior in this respect. At present, however, the stepping motor is the more expensive of the two types.

Light-emitting diodes require a minimum of two battery cells for proper operation. The required current can be kept to about 2 milliamperes per segment when the diodes are pulsed from a six-stage ring counter, as shown in Fig. 13. A duty factor of 16 per cent is achieved with this arrangement. Because of the high current, however, a continuously operating battery-powered display is not possible, and a "readout on demand" watch is then necessary.

Continuously operating liquid-crystal displays are possible and practical. RCA wristwatch displays employ liquid-crystal material having resistivities of about  $5 \times 10^9$  ohms per centimeter, which at a 0.5-mil spacing results in a resistance of 6.3 megohms per square centimeter. With all segments energized, the display consumes only about 1 microampere of current at 15 volts. Liquid crystals, however, require a minimum supply of 12 volts to assure good contrast between on and off segments. For single-cell operation, a dc-to-dc converter must be used to step the voltage up to the required 12-to-15-volt level. Transformer and capacitor voltage-doubling circuits with conversion efficiencies of about 75 per cent are typically used for this purpose.

Because current consumption is such an important consideration for wristwatch circuits, the careful consideration given to the choice of a battery is easily understood. Small silver-oxide and mercury cells are presently popular for wristwatch use. Pertinent information on these types of

Mallory cells is shown in Table IV. Most of the cells listed will last at least one year with a motor current of 10 microamperes and a total oscillator and divider current less than 5 microamperes at an oscillator frequency of 32.768 kHz. The voltage for both types of cells is relatively constant during the active life listed and falls off rapidly thereafter. Typical end-of-life voltages at 1.1 volts for mercury cells and 1.45 volts for silver-oxide cells. Either type of cell works equally well with RCA silicon-gate COS/MOS circuits which operate from supply voltages as low as 1.1 volts.

#### Wall Clocks

Size and power limitations for clocks are not as restrictive as those for wristwatches. For this reason, lower-cost, higher-frequency crystals may be used. The optimum range of crystal frequencies presently appears to be from 131 kHz to 524 kHz. All the oscillator considerations given previously for operation at 32 kHz apply equally well to this higher frequency range. The oscillator circuit configuration shown in Fig. 9(b) is still the optimum type; however, the value of the source resistors must be decreased to assure adequate gain at the higher frequencies. Source resistors are often best chosen experimentally by gradually increasing the resistance until an output voltage swing of 30 to 70 per cent of the supply voltage  $V_{DD}$  is reached. Data taken from a typical 262-kHz oscillator circuit that employs two 10-kilohm source resistors and a DT-cut, 262-kHz crystal are shown in Table V. The table also shows typical counter current.

The most popular readout devices for clocks are conventional-hand movements and liquid-crystal displays. Continuously operating light-emitting-diode numerals consume too much current even for long life of C- and D-size batteries. In contrast, a typical RCA four-digit liquid-crystal

Table IV – Typical Data for Mallory Watch Cells

Type	Voltage	Capacity μA yrs.	Height (in.)	Diameter (in.)
WH3	1.35	25	0.208	0.455
WS 14 Type A	1.55	19	0.210	0.455
W4	1.35	11	0.139	0.455
WS11	1.55	11	0.164	0.455
10 R 101 (EXP)	1.35	36	0.190	0.610
10 L 19 (EXP)	1.55	27	0.190	0.610
WD4	1.36	14	0.149	0.594
WD5	1.36	23	0.110	1.003

display having a 0.4-inch-by-0.6-inch numeral consumes only 100 microamperes of current with all segments energized.

Motors for driving the clock hands are typically of the balance-wheel or continuously rotating synchronous types. Sensitivity to vibration is usually not a restriction; hence, the balance wheel motor can be successfully used in place of the more expensive stepping motor. Clock motors typically require about 300 to 450 microwatts of power, or average currents of 200 to 300 microamperes at 1.5 volts.

These currents, together with the oscillator and counter currents given in Table V, can now be compared with typical battery capacities. Battery information extrapolated from published Eveready data on popular AA-, C-, and D-size cells is listed in Table VI.<sup>5</sup> Most of the battery current is consumed by the motor, and if a total current of 250 microamperes is assumed, the data show a carbon-zinc C cell as the minimum size battery required for one year of life.

#### Auto Clocks

Auto clock circuits are somewhat unique in that power considerations are not nearly as restrictive as in other portable applications. Although the low-power feature of COS/MOS circuits is helpful, the main advantages obtained

Table V – Typical Data for 262-kHz Oscillator and Counter Circuits

Product	V <sub>DD</sub> (Volts)	Oscillator Current (μA)	Counter Current (μA)	Freq. Stability (ppm)
Silicon-Gate	1.1V	7	7	2.0 ppm 1.4 1.2
"	1.3V	9.5	9	
"	1.5V	11.5	10	
"	1.6V	12.5	11	
Low-Voltage	2.2V	21	10	1.8
"	3.0V	35	13	

Table VI – Life Data for Typical Batteries

Eveready Type #	Mallory Type #	Size	Type	Life (Days)
915	M15F	AA	Carbon-Zinc	150
E91	MN1500	AA	Alkaline	200
935	M14F	C	Carbon-Zinc	385
E93	MN1400	C	Alkaline	575
950	M13F	D	Carbon-Zinc	800
E95	MN1300	D	Alkaline	1100

All life data assumes a continuous drain of 250 μA and an end-of-life voltage of 1.1V.

from the use of COS/MOS in automobile clocks, or in any automotive application, are those of wide operating voltage and temperature range and high noise immunity.

With little restriction on power, the choice of a crystal depends mainly on cost. Crystals typically used for automobile timing applications are AT-cut types that operate at frequencies between 1 MHz and 4.2 MHz. The oscillator considerations discussed earlier also apply to these frequencies; however, as the frequency increases, it becomes increasingly difficult to maintain a low starting voltage at a low current. At high frequencies, the starting voltage and current are inversely proportional and are controlled mainly by the values of the capacitors on the pi-type feedback network and the size of the COS/MOS amplifier transistors. For minimum starting voltage, relatively small capacitors should be used in the pi-feedback network, and no source resistors should be added to the amplifier. As indicated by data taken on the circuit shown in Fig. 9(b) and shown in Table VII, low power can still be maintained even when the source resistors are not used.

The upper limit of the crystal frequency depends not so much on power consumption as on the minimum supply voltage allowed for circuit operation. The minimum automobile battery voltage is generally considered to be 5 volts; however, the supply voltage for the timing circuit can be considerably less than this value depending upon the design of the transient protection circuit, as discussed later. Table VIII lists minimum COS/MOS supply voltages for typical oscillator circuits. The values shown permit design at two temperatures. The lower temperature is often considered adequate by auto companies with the opinion that the minimum battery voltage of 5 volts rarely, if ever, occurs at high temperatures.

The oscillator in a typical auto clock circuit is followed by a number of frequency-dividing stages, the last stage of which is frequently used to drive a motor. Long counter chains are required because of the high oscillator frequency; however, the power dissipation of COS/MOS circuits is so low that the number of stages is only restricted by chip size

**Table VII — Typical High-Frequency Data for COS/MOS Oscillator and Counter Circuits (Low-Voltage Product)**

V <sub>DD</sub> (Volts)	Freq. (MHz)	Oscillator Current (mA)	Counter Current (mA)	Motor Current (mA)
5	1	0.28	0.125	5V 2.5 mA
12	1	1.3	0.275	12V 5-10 mA
5	2	0.37	0.250	
12	2	1.5	0.550	
5	3	0.40	0.375	5V 3.8 mA
12	3	1.9	0.825	
5	4	0.43	0.500	12V 8-20 mA
12	4	2.3	1.1	

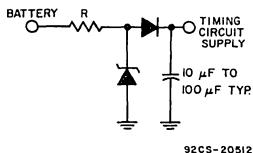
limitations. Because COS/MOS circuits consume current only during switching transitions, each counter stage averages one-half the current of the previous stage. The first counter stage, therefore, consumes as much current as all of the following stages combined for a counter of infinite length. Little difference, then, exists between the power consumption of a ten-stage or thirty-stage COS/MOS counter. Table VII lists, in addition to the oscillator current, typical values of counter current, as well as some typical ranges of peak and average motor currents.

Current data, such as that shown in Table VII, are necessary for a proper design of the transient protection circuit, an essential part of any automobile digital logic system. Automobile manufacturers disagree on the maximum amplitude and decay of transient voltage; however, values often used are maximum transients of +120 volts and -90 volts, each decaying exponentially with a maximum time constant of 45 milliseconds. Because standard COS/MOS circuits are rated for a maximum supply of 15 volts, a protection circuit must be included between the battery and the COS/MOS logic.

Fig. 17 shows a transient-voltage protection circuit that is frequently used. The zener diode regulates the voltage supply

**Table VIII — Minimum Operating Voltages for COS/MOS Integrated Circuits**

Freq. (MHz)	Low-Voltage Product				Silicon-Gate Product			
	1	2	3	4	1	2	3	4
Min. Voltage at 25°C	2.9	3.1	3.5	4.0	1.6	2.0	2.6	3.0
Min. Voltage at 82°C 180°F	3.0	3.3	4.0	5.0	1.8	2.6	3.4	4.0



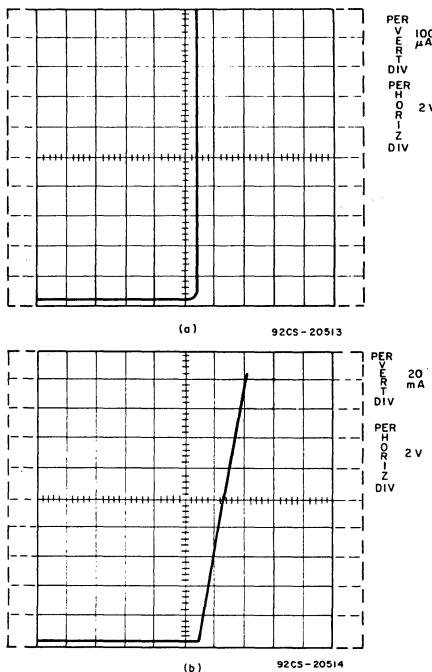
**Fig. 17— Automobile transient-protection circuit.**

for the clock circuits, and the capacitor and series diode prevent timing losses during negative transients. For minimum zener current during transients, the maximum value of R should be based on the minimum circuit operating voltage and the peak current drawn by the logic circuit and motor at the minimum battery voltage. The minimum zener breakdown voltage is then determined by subtraction of the product of the minimum current drain at the normal battery voltage and the value of R just chosen from the battery voltage. A zener breakdown greater than this voltage assures that no unnecessary current will be drawn by the zener during normal automobile operation.

Another important zener characteristic is dynamic impedance. During a current surge, the voltage across the zener must not rise to a damaging level. A value of 22 volts for the 45-millisecond time constant appears safe for standard COS/MOS circuits.

In the design of a typical transient-voltage protection circuit, it is assumed that the minimum battery voltage is 5 volts, that the minimum circuit operating voltage is 3.5 volts at a crystal frequency of 3.145728 MHz, and that a peak current of 3 milliamperes is obtained at 5 volts. The value of the resistance R is then found as  $(5 - 3.5 + 0.7)/3 \approx 250$  ohms. With a minimum current of 5 milliamperes at 12 volts, the minimum zener voltage becomes  $12 - 5(0.250) = 11.75$  volts. For a +120-volt transient, the zener could then consume a peak current of  $(120 - 11.8)/250 = 0.4$  ampere. For a maximum zener voltage of 13 volts, the dynamic impedance of the zener must be less than  $(22V - 13V)/.4A = 22$  ohms. Components chosen in this manner will provide adequate protection for anticipated transients.

Both protection-circuit diodes can be integrated onto the COS/MOS chip. When located as shown in Fig. 17, the series diode need only have a breakdown rating of about 12 volts. Zener diodes that have breakdown ratings of 4.5 to 6.0 volts or any multiple thereof can also be integrated onto the COS/MOS chip. The breakdown rating can also be increased in 0.7-volt steps by addition of forward-biased diodes in series. Characteristics of two typical zener diodes integrated in series are shown in Fig. 18. Fig. 18(a) shows the area around the "knee" of the breakdown region, and Fig. 18(b) shows the higher-current region useful for determining the dynamic resistance. From the slope of the line, the typical dynamic resistance for two diodes is found to be 17.6 ohms total, or 8.8 ohms per diode. The diodes are rated to withstand a 0.5-ampere surge current that decays with an 80-millisecond time constant. The zener diode, then, is compatible with present automobile protection requirements,



*Fig. 18—Oscillograph tracings showing characteristics of an integrated zener diode: (a) low-current region; (b) high-current region.*

and integration of this component should represent a considerable cost saving, especially when integrated with the series diode.

#### Other Applications

Although wristwatches and clocks of various types are important applications of COS/MOS timing circuits, they are certainly not the only timing applications which can benefit from the unique features of COS/MOS logic. Applications such as fuze timers, feeding systems, automatic sprinklers,

incubator timers, and other similar systems can be designed from information provided on the oscillator and counter with only the output device unique to the particular application. Automobile applications for COS/MOS circuits are almost endless. One can think of speed controllers, digital speedometers, miles per gallon indicators, and perhaps even estimated-time-of-arrival indicators that, on the basis of the given total mileage, would update the time on a dynamic basis from information provided by the speedometer, odometer, and clock.

#### CONCLUSIONS

The primary advantage of electronic timing circuits over conventional mechanical methods of timekeeping lies in the greatly increased accuracy permitted by the highly stable crystal-controlled oscillator circuit. Although crystal oscillator circuits have existed for some time, their usefulness in portable applications has been somewhat limited because of the high current consumption required by the following digital logic. The advent of COS/MOS integrated circuits now permits the design of complete low-power timing systems. The impact of COS/MOS on timing applications is perhaps equalled by the recent development of liquid-crystal displays and dc-to-dc converters that allow low-power continuously operating digital displays. Certainly, no great technological barriers now exist for the use of electronic timing circuits in a wide variety of applications. The search, no doubt, will always continue for the ideal timekeeping device; however, it should be apparent from the information presented that the ideal timekeeping unit can now be more closely approached than ever before.

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## The RCA COS/MOS Phase-Locked-Loop A Versatile Building Block for Micro-Power Digital and Analog Applications

by David K. Morgan

### INTRODUCTION

Phase-locked-loops (PLL's), especially in monolithic form, are finding significantly increased usage in signal-processing and digital systems. FM demodulation, FSK demodulation, tone decoding, frequency multiplication, signal conditioning, clock synchronization, and frequency synthesis are some of the many applications of a PLL. The PLL described in this Note is the COS/MOS CD4046A, which consumes only 600 microwatts of power at 10 kHz, a reduction in power consumption of 160 times when compared to the 100 milliwatts required by similar monolithic bipolar PLL's. This power reduction has particular significance for portable battery-operated equipment. This Note discusses the basic fundamentals of phase-locked-loops, and presents a detailed technical description of the COS/MOS PLL as well as some of its applications.

### REVIEW OF PLL FUNDAMENTALS

The basic phase-locked-loop system is shown in Fig. 1; it consists of three parts: phase comparator, low-pass filter, and voltage-controlled oscillator (VCO); all are connected to form a closed-loop frequency-feedback system.

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage,  $V_d(t)$ , from the low-pass filter is also zero, which causes the VCO to operate at a set frequency,  $f_0$ , called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the VCO frequency and generates an error voltage proportional to the phase and frequency

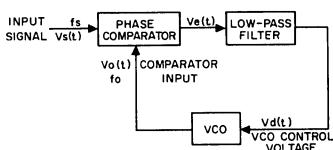


Fig. 1—Block diagram of PLL.

difference of the input signal and the VCO. The error voltage,  $V_e(t)$ , is filtered and applied to the control input of the VCO;  $V_d(t)$  varies in a direction that reduces the frequency difference between the VCO and signal-input frequency. When the input frequency is sufficiently close to the VCO frequency, the closed-loop nature of the PLL forces the VCO to lock in frequency with the signal input; i.e., when the PLL is in lock, the VCO frequency is identical to the signal input except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the lock range of the system. The lock range is always larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the capture range of the PLL system.

### TECHNICAL DESCRIPTION OF COS/MOS PLL

Fig. 2 shows a block diagram of the COS/MOS CD4046A, which has been implemented on a single

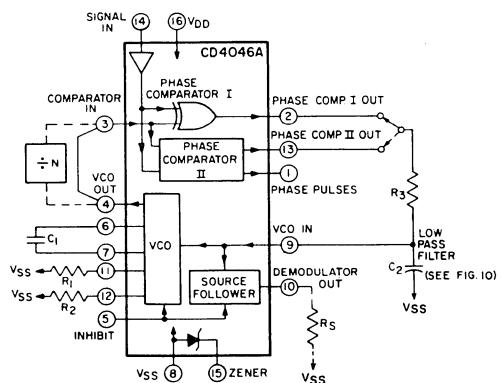


Fig. 2—COS/MOS PLL block diagram.

monolithic integrated circuit. The PLL structure consists of a low-power, linear, voltage-controlled oscillator (VCO), and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-volt zener is provided for supply regulation if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The low-pass filter is implemented through external parts because of the radical configuration changes from application to application and because some of the components are non-integrable. The CD4046A is supplied in a 16-lead, dual-in-line, ceramic package (CD4046AD); a 16-lead, dual-in-line, plastic package (CD4046AE); or a 16-lead flat-pack (CD4046AK). It is also available in chip form (CD4046AH).

#### Phase Comparators

Most PLL systems utilize a balanced mixer composed of well-controlled analog amplifiers for the phase-comparator section. Analog amplifiers with well-controlled gain characteristics cannot easily be realized using COS/MOS technology. Hence, the COS/MOS design shown in Fig. 3 employs digital-type phase comparators. Both phase comparators are driven by a common-input amplifier configuration composed of a bias stage and four inverting-amplifier stages. The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic  $0 \leq 30\%$  (VDD-VSS), logic  $1 \geq 70\%$  (VDD-VSS)]. For smaller input signal swings, the signal must be capacitively coupled to the self-biasing amplifier at the signal input to insure an over-driven digital signal into the phase comparators.

**Phase-comparator I** is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator input frequencies must have 50-percent duty cycle. With no signal or noise on the signal input, this phase comparator has

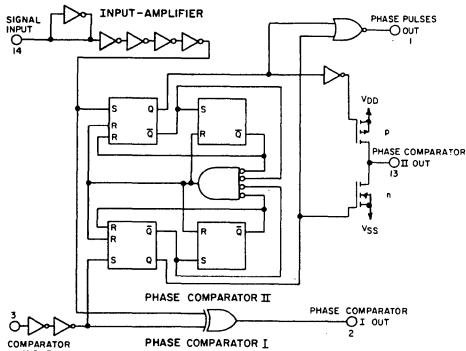


Fig. 3— Schematic of COS/MOS PLL phase-comparator section.

an average output voltage equal to  $VDD/2$ . The low-pass filter connected to the output of phase-comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency ( $f_0$ ). With phase-comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between  $0^\circ$  and  $180^\circ$ , and is  $90^\circ$  at the center frequency. Fig. 4 shows the typical, triangular, phase-to-output, response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase-comparator I in locked condition of  $f_0$  is shown in Fig. 5.

**Phase-comparator II** is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p and n drivers having a common output node as shown in Fig. 3. When the p-MOS or n-MOS drivers are ON, they pull the output up to  $VDD$  or down to  $VSS$ , respectively. This type of phase comparator acts only on the positive edges of the signal-and comparator-input signals. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-MOS output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-MOS output driver is maintained ON continuously. If the signal-and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-MOS output driver is maintained ON for a time corresponding to the phase difference. If the signal-and comparator-input frequencies are the same, but the signal input leads the comparator input in phase, the p-MOS output driver is maintained ON for time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this type of phase comparator is adjusted until the signal and comparator input are equal in both phase and frequency. At this stable operating point, both p- and n-MOS output drivers remain OFF, and thus the phase-comparator

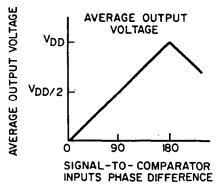


Fig. 4— Phase-comparator I characteristics at low-pass filter output.

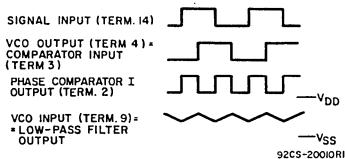


Fig. 5 – Typical waveforms for COS/MOS phase-locked loop employing phase-comparator I in locked condition of  $f_o$ .

output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover, the signal at the "phase pulses" output is at a high level, and can be used for indicating a locked condition. Thus, for phase-comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-MOS output drivers are OFF for most of the signal-input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase-comparator II. Fig. 6 shows typical waveforms for a COS/MOS PLL employing phase-comparator II in a locked condition.

Fig. 7 shows the state diagram for phase-comparator II; each circle represents a state of the comparator. The number at the top inside each circle represents the state of the comparator, while the logic state of the signal and comparator inputs, represented by a 0 or a 1, are given by the left and right numbers, respectively, at the bottom of each circle. The transitions from one state to another result from either a logic change on the signal input (I) or the comparator input (C). A positive transition and a negative transition are shown by an arrow pointing up or down, respectively. The state diagram assumes that only one transition on either the signal input or the comparator input occurs at any instant. States 3, 5, 9, and 11 represent the condition at the output of phase-comparator II when the p-MOS driver is ON, while states 2, 4, 10, and 12 determine the condition when the n-MOS driver is ON. States 1, 6, 7, and 8 represent the condition when the output of phase-comparator II is in its high impedance state; i.e., both p- and n-devices are OFF, and the phase-pulses output (terminal 1) is high. The condition at the phase-pulses output for all other states is low.

As an example of how one may use the state diagram shown in Fig. 7, consider the operation of phase-comparator II in the locked condition shown in Fig. 6. The waveforms shown in Fig. 6 are broken up into three sections: section I corresponds to the condition in which the signal input leads the comparator input in phase, while section II corresponds to a finite phase difference. Section III depicts the condition when the comparator input leads the signal input in phase. These three sections all correspond to a locked condition for the COS/MOS PLL; i.e., both signal- and comparator-input

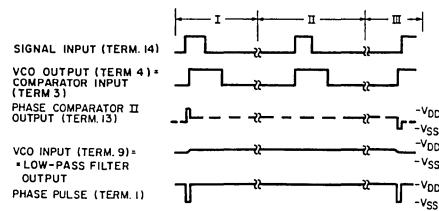


Fig. 6 – Typical waveforms for COS/MOS phase-locked loop employing phase-comparator II in locked condition.

signals are of the same frequency but differ slightly in phase. Assume that both the signal inputs begin in the 0 state, and that phase-comparator II is initially in its high-impedance output condition (state 1), as shown in Figs. 7 and 6, respectively. The signal input makes a positive transition

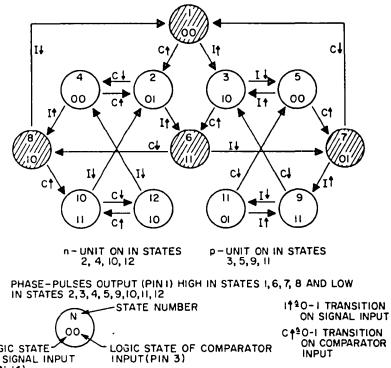


Fig. 7 – State diagram of phase-comparator II.

first, which brings phase-comparator II to state 3. State 3 corresponds to the condition of the comparator in which the signal input is a 1, the comparator input is a 0, and the output p-device is ON. The comparator input goes high next, while the signal input is high, thus bringing the comparator to state 6, a high-impedance output condition. The signal input goes to zero next, while the comparator input is high, which corresponds to state 7. The comparator input goes low next, bringing phase-comparator II back to state 1. As shown for section I, the p-device stays on for a time corresponding to the phase difference between the signal input and the comparator input. Starting in state 1 at the beginning of section III, the comparator input goes high first, while the signal input is low, bringing the comparator to state 2. Following the example given for section I, the comparator proceeds from state 2 to states 6 and 8 and then back to 1. The output of phase-comparator II for section III corresponds to the n-device being on for a time corresponding to the phase difference between the signal and comparator inputs.

The state diagram of phase-comparator II completely describes all modes of operation of the comparator for any input condition in a phase-locked-loop.

### Voltage-Controlled Oscillator

Fig. 8 shows the schematic diagram of the voltage-controlled oscillator (VCO). To assure low system-power dissipation, it is desirable that the low-pass filter consume little power. For example, in an RC filter, this requirement dictates that a high-value R and a low-value C be utilized. The VCO input must not, however, load down or modify the characteristics of the low-pass filter. Since the VCO design shown utilizes an n-MOS input configuration having practically infinite input resistance, a great degree of freedom is allowed in selection of the low-pass filter components.

The VCO circuit shown in Fig. 8 operates as follows: when the inhibit input is low,  $P_3$  is turned full ON, effectively connecting the sources of  $P_1$  and  $P_2$  to  $V_{DD}$ ; and gates 1 and 2 are permitted to function as NOR-gate flip-flops.  $N_1$  together with external-resistor  $R_1$  form a source-follower configuration. As long as the resistance of  $R_1$  is at least an order of magnitude greater than ON resistance of  $N_1$  (greater than 10 kilohms), the current through  $R_1$  is linearly dependent on the VCO input voltage. This current flows through  $P_1$ , which, together with  $P_2$ , forms a current-mirror network. External resistor  $R_2$  adds an additional constant current through  $P_1$ ; this current offsets the VCO operating frequency for VCO input signals of 0 volts. In the current-mirror network, the current of  $P_2$  is effectively equal to the current through  $P_1$  independent of the drain voltage at  $P_2$ . (This condition is true provided  $P_2$  is maintained in saturation; in the circuit shown,  $P_2$  is saturated under all possible operating conditions and modes). The set/reset flip-flop composed of gates 1 and 2 turns ON either  $P_4$  and  $N_3$ , or  $P_5$  and  $N_2$ . One side of the external capacitor  $C_1$  is, therefore, held at ground, while the other side is charged by the constant current supplied by  $P_2$ . As soon as  $C_1$  charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. The

charged side of the capacitor is now pulled to ground. The other side of the capacitor goes negative, and discharges rapidly through the drain diode of the OFF n-device. Subsequently, a new half-cycle starts. Since inverters 1 and 5 have the same transfer points, the VCO has a 50-percent duty-cycle. Inverters 1 through 4 and 5 through 8 serve several purposes: (1) they shape the slow-input ramp from capacitor  $C_1$  to a fast waveform at the flip-flop input stage, (2) they maintain low power dissipation through the use of high-impedance devices at inverters 1 and 5 (slow-input wave-forms), and (3) they provide four inverter delays before removal of the set/reset flip-flop triggering pulse to assure proper triggering action.

In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided (demodulated output). If this output is used, a load resistor ( $R_s$ ) of 10 kilohms or more should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the VCO and the source follower, while a logic 1 turns off both to minimize stand-by power consumption.

### Performance Summary of COS/MOS PLL

The maximum ratings for the CD4046A COS/MOS PLL, as well as its general operating-performance characteristics are outlined in Table I. The VCO and comparator characteristics are shown in Tables II and III, respectively. Table IV summarizes some useful formulas as a guide for approximating the values of external components for the CD4046A in a phase-locked-loop system. When using Table IV, one should keep in mind that frequency values are in kilohertz, resistance values are in kilohms, and capacitance values are in microfarads. The selected external components must be within the following ranges:

$$\begin{aligned} 10 \text{ k}\Omega &\leq R_1, R_2, R_s \leq 1 \text{ M}\Omega \\ C_1 &\geq 100 \text{ pF at } V_{DD} \geq 5 \text{ V} \\ C_1 &\geq 50 \text{ pF at } V_{DD} \geq 10 \text{ V} \end{aligned}$$

In addition to the given design information, refer to Fig. 9 for  $R_1$ ,  $R_2$ , and  $C_1$  component selections. The use of Table IV in designing a COS/MOS PLL system for some familiar applications is discussed below.

### APPLICATIONS OF THE COS/MOS PLL

The COS/MOS phase-locked-loop is a versatile building block suitable for a wide variety of applications, such as FM demodulators, frequency synthesizers, split-phase data synchronization and decoding, and phase-locked-loop lock detection.

#### FM Demodulation

When a phase-locked-loop is locked on an FM signal, the voltage-controlled oscillator (VCO) tracks the instantaneous frequency of that signal. The VCO input voltage, which is the filtered error voltage from the phase detector, corresponds to the demodulated output. Fig. 11 shows the connections for the COS/MOS CD4046A PLL as an FM demodulator. For this example, an FM signal consisting of a 10-kilohertz carrier frequency was modulated by a 400-Hz audio signal. The total

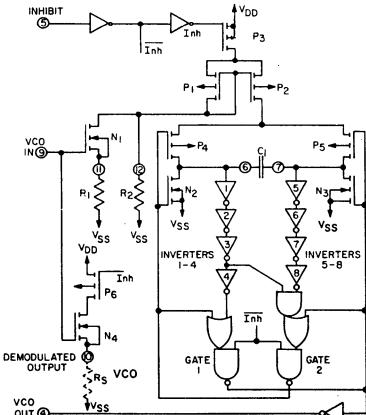


Fig. 8— Schematic of COS/MOS VCO section.

**Table I— Maximum ratings and general operating characteristics**

MAXIMUM RATINGS, <i>Absolute-Maximum Values:</i>			
Storage Temperature Range . . . . .	-65°C to +150	°C	
Operating Temperature Range:			
Ceramic Package Types . . . . .	-55°C to +125	°C	
Plastic Package Types . . . . .	-40°C to +85	°C	
DC Supply Voltage Range			
( $V_{DD} - V_{SS}$ ) . . . . .	-0.5 V to +15	V	
Device Dissipation (Per Pkg.) . . . . .	200	mW	
All Inputs . . . . .	$V_{SS} \leq V_I \leq V_{DD}$		
Recommended			
DC Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . .	5 to 15	V	
Recommended			
Input Voltage Swing . . . . .	$V_{DD}$ to $V_{SS}$		
General Characteristics (Typical Values at $V_{DD} - V_{SS} = 10$ V and $T_A = 25^\circ\text{C}$ )			
Operating Supply Voltage ( $V_{DD} - V_{SS}$ ) . . . . .	5 to 15 V		
Operating Supply Current:			
Inhibit = "0" $f_0 = 10 \text{ kHz}, V_{DD} = 5 \text{ V} \dots 70 \mu\text{W}$ @ $C_1 = 0.0001 \mu\text{F}$			
$R_1 = 1 \text{ M}\Omega$ $f_0 = 10 \text{ kHz}, V_{DD} = 10 \text{ V} \dots 600 \mu\text{W}$			
Inhibit = "1" . . . . .	25 $\mu\text{A}$		

**Table II— VCO electrical characteristics**

VCO Characteristics (Typical Values at $V_{DD} - V_{SS} = 10$ V and $T_A = 25^\circ\text{C}$ )			
Maximum Frequency . . . . .	1.2 MHz		
Temperature Stability . . . . .	600 ppm/ $^\circ\text{C}$		
Linearity ( $V_{VCO \text{ in}} = 5 \text{ V} \pm 2.5 \text{ V}$ ) . . . . .	1%		
Center Frequency . . . . .	Programmable with $R_1$ and $C_1$		
Frequency Range . . . . .	Programmable with $R_1, R_2$ , and $C_1$		
Input Resistance . . . . .	$10^{12} \Omega$		
Output Voltage . . . . .	10 V p-p		
Duty Cycle . . . . .	50%		
Rise & Fall Times . . . . .	50 ns		
Output Current Capability			
"1" Drive @ $V_O = 9.5 \text{ V}$ . . . . .	-1.8 mA		
"0" Sink @ $V_O = 0.5 \text{ V}$ . . . . .	2.6 mA		
Demodulated Output:			
Offset Voltage			
$(V_{VCO \text{ in}} - V_{DEMOD \text{ out}}) @ 1 \text{ mA}$	1.5 V		

**Table III— Comparator electrical characteristics**  
Comparator Characteristics (Typical Values at  $V_{DD} - V_{SS} = 10$  V and  $T_A = 25^\circ\text{C}$ )

Signal Input:	
Input Impedance . . . . .	400 K $\Omega$
Input Sensitivity:	
ac coupled . . . . .	400 mV
dc coupled . . . . .	$\begin{cases} "0" \leq 30\% (V_{DD} - V_{SS}) \\ "1" \geq 70\% (V_{DD} - V_{SS}) \end{cases}$
Comparator Input Levels (term. 3):	$\begin{cases} "0" \leq 30\% (V_{DD} - V_{SS}) \\ "1" \geq 70\% (V_{DD} - V_{SS}) \end{cases}$
Output Current Capability	
Comparator I (term. 2) and Comparator II (term. 13):	
"1" Drive @ $V_O = 9.5 \text{ V}$ . . . . .	-1.8 mA
"0" Sink @ $V_O = 0.5 \text{ V}$ . . . . .	2.6 mA
Comparator II Phase Pulses (term. 1):	
"1" Drive @ $V_O = 9.5 \text{ V}$ . . . . .	-0.5 mA
"0" Sink @ $V_O = 0.5 \text{ V}$ . . . . .	1.4 mA

FM signal amplitude is 500 millivolts, therefore the signal must be ac coupled to the signal input (terminal 14). Phase-comparator I is used for this application because a PLL system with a center frequency equal to the FM carrier frequency is needed. Phase comparator I lends itself to this application also because of its high signal-input-noise-rejection characteristics.

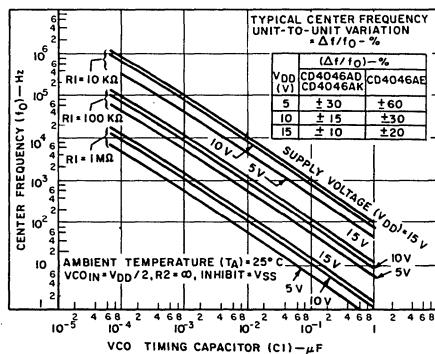
The formulas shown in Table IV for phase-comparator I with  $R_2 = \infty$  are used in the following considerations. The center frequency of the VCO is designed to be equal to the carrier frequency, 10 kHz. The value of capacitor  $C_1$ , 500 pF, was found by assuming an  $R_1 = 100 \text{ k}\Omega$  for a supply voltage  $V_{DD} = 5$  volts.

These values determined the center frequency:

$$f_0 = 10 \text{ kHz}$$

The PLL was set for a capture-range of

$$f_C \approx \pm \frac{1}{2\pi} \frac{2\pi f_1}{R_3 C_2} = \pm 0.4 \text{ kHz}$$

**Fig. 9(a)— Typical center frequency vs.  $C_1$  for  $R_1 = 10 \text{ k}\Omega, 100 \text{ k}\Omega$ , and  $1 \text{ M}\Omega$ .**

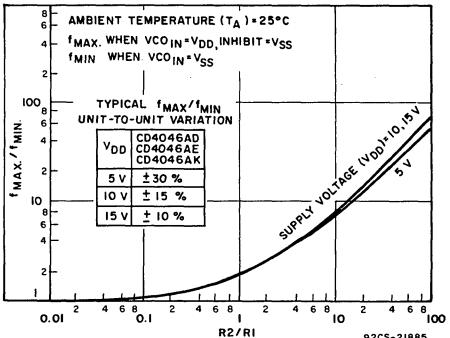
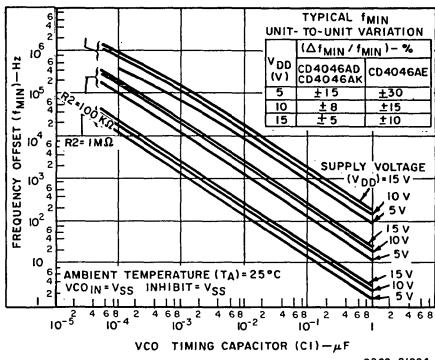


Fig. 9(b) – Typical frequency offset vs.  $C_1$  for  $R_2 = 10 \text{ k}\Omega$ ,  $100 \text{ k}\Omega$ , and  $1 \text{ M}\Omega$ .

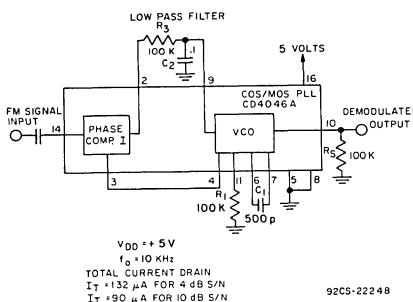
Fig. 9(c) – Typical  $f_{\text{max}}/f_{\text{min}}$  vs.  $R_2/R_1$ .

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, $f_0$		VCO in PLL system will adjust to lowest operating frequency, $f_{\text{min}}$	
Frequency Lock Range, $2f_L$		$2f_L = \text{full VCO frequency range}$	$2f_L = f_{\text{max}} - f_{\text{min}}$	
Frequency Capture Range, $2f_C$		$(1), (2) \quad 2f_C \approx \frac{1}{\pi \sqrt{R1L1}}$		$f_C = f_L$
Loop Filter Component Selection		For $2f_C$ , see Ref. (2)		
Phase Angle between Signal and Comparator	$90^\circ$ at center frequency ( $f_0$ ), approximating $0^\circ$ and $180^\circ$ at ends of lock range ( $2f_L$ )		Always $0^\circ$ in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	<ul style="list-style-type: none"> <li>Given: <math>f_0</math></li> <li>Use <math>f_0</math> with Fig.9a to determine <math>R_1</math> and <math>C_1</math></li> </ul>		<ul style="list-style-type: none"> <li>Given: <math>f_{\text{max}}</math></li> <li>Calculate <math>f_{\text{min}}</math> from the equation <math>f_{\text{min}} = f_0 - f_L</math></li> <li>Use <math>f_{\text{min}}</math> with Fig.9b to determine <math>R_2</math> and <math>C_1</math></li> <li>Calculate <math>f_{\text{max}}</math> from the equation <math>f_{\text{max}} = \frac{f_0 + f_L}{2}</math></li> <li>Use <math>f_{\text{max}}</math> with Fig.9a to determine <math>R_1</math> and <math>C_1</math></li> </ul>	

For further information, see

(1) F. Gardner, "Phase-Lock Techniques", John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniatuerized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.



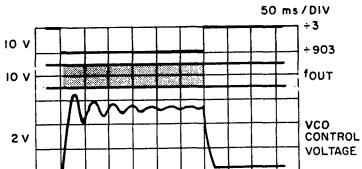


Fig. 13—Frequency-synthesizer waveforms.

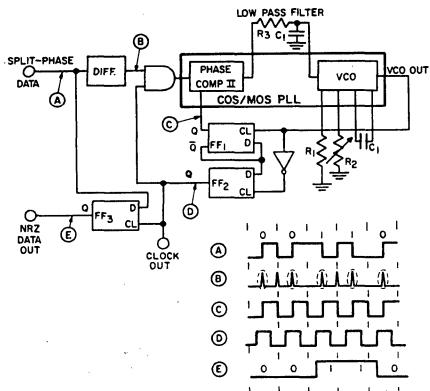


Fig. 14—Split-phase data synchronization and decoding.

As shown in Fig. 14, the split-phase data-input (A) is first differentiated to mark the locations of the data transitions. The differentiated signal, (B), which is twice the bit rate, is gated into the COS/MOS PLL. Phase-comparator II in the PLL is used because of its insensitivity to duty cycle on both the signal and comparator inputs. The VCO output is fed into the clock input of FF1 which divides the VCO frequency by two. During the ON intervals, the PLL tracks the differentiated signal (B); during the OFF intervals the PLL remembers the last frequency present and still provides a clock output. The VCO output is inverted and fed into the clock input of FF2 whose data input is the inverted output of FF1. FF2 provides the necessary phase shift in signal (C) to obtain signal (D), the recovered clock signal from the split-phase data transmission. The output of FF3, (E), is the recovered binary information from the phase information contained in the split-phase data. Initial synchronization of this PLL system is accomplished by a string of alternating 0's and 1's that precede the data transmission.

#### Phase-Locked-Loop Lock Detection

In some applications that utilize a PLL, it is sometimes necessary to have an output indication of when the PLL is in lock. One of the simplest forms of lock-condition indicator is

a binary signal. For example, a 1 or a 0 output from a lock-detection circuit would correspond to a locked or unlocked condition, respectively. This signal could, in turn, activate circuitry utilizing a locked PLL signal. This detection could also be used in frequency-shift-keyed (FSK) data transmissions in which digital information is transmitted by switching the input frequency between either of two discrete input frequencies, one corresponding to a digital 1 and the other to a digital 0.

Fig. 15 shows a lock-detection scheme for the COS/MOS PLL. The signal input is switched between two discrete frequencies of 20 kHz and 10 kHz. The PLL system uses phase-comparator II; the VCO bandwidth is set up for an  $f_{\min}$  of 9.5 kHz and an  $f_{\max}$  of 10.5 kHz. Therefore, the PLL locks and unlocks on the 10-kHz and 20-kHz signals, respectively. When the PLL is in lock, the output of phase-comparator I is low except for some very short pulses that result from the inherent phase difference between the signal and comparator inputs; the phase-pulses output (terminal 1) is high except for some very small pulses resulting from the same phase difference. This low condition of phase comparator I is detected by the lock-detection circuit shown in Fig. 15. Fig. 16 shows the performance of this circuit when the input signal is switched between 20 and 10 kHz. It can be seen that after about five input cycles the lock detection signal goes high.

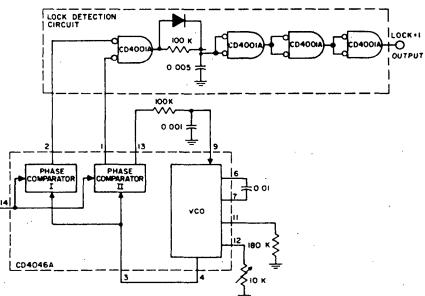


Fig. 15—Lock-detection circuit.

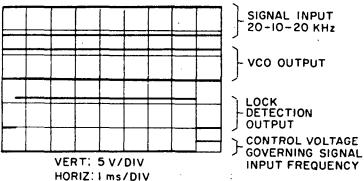


Fig. 16—Lock-detection-circuit waveforms.

## COS/MOS MSI Counter and Register Design and Applications

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COS/MOS (Complementary-Symmetry Metal-Oxide-Semiconductor) technology offers economical MSI (Medium-Scale Integration) arrays on a single monolithic silicon chip. Added performance benefits are derived from micropower quiescent power dissipation; moderately fast operation; excellent dc and dynamic noise immunity; high dc fanout; stable performance over wide ranges of supply voltage, temperature, and device parameter variation; simple circuit and subsystem design; and compatible logic and memory circuitry from simple gates and flip-flops to complex MSI circuits.

In the COS/MOS MSI area, RCA has several counter and register types presently available commercially. These devices are available in both plastic and ceramic packages intended for military, commercial and industrial uses. Devices with the suffix "E" are plastic package types; suffix "D" are ceramic package types.

CD4006A — Eighteen-Stage Static Shift Register

CD4014A — Eight-Stage Synchronous Parallel-Input/Serial-Output Static Shift Register

CD4015A — Dual Four-Stage Serial-Input/Parallel-Output Static Shift Register

CD4017A — Decade Counter/Divider Plus 10 Decoded Decimal Outputs

CD4018A — Presetable Divide-by-“N” Counter

CD4020A — Fourteen-Stage Ripple-Carry Binary Counter

CD4021A — Eight Stage Asynchronous Parallel-Input/Serial-Output Static Shift Register

CD4022A — Divide-by-8 Counter Plus 8 Decoded Outputs

CD4024A — Seven-Stage Ripple-Carry Binary Counter

This Note shows logic and schematic diagrams for each of the counter and register types listed above, outlines circuit designs, and discusses device-design tradeoffs. Performance criteria are summarized, and applications by type are outlined by logic or subsystems diagrams and waveform photographs. Possible extensions of design into other areas of application are given.

The applications shown also utilize other RCA COS/MOS family types such as the CD4000A-CD4002A “NOR” gate types; CD4013A Dual-D Flip-Flop type; CD4007A Dual

Complementary Pair Plus Inverter; CD4009A and CD4010A Hex-Buffer/Logic-Level Converter types; and the CD4011A and CD4012A Quad-2 and Dual-4 “NAND” gate types.

### General COS/MOS Design

The COS/MOS counter and register types described consist of between 100 and 300 MOS devices, supporting interconnect tunnels and metal runs, and bond pads, all on a single monolithic pellet.

Table I summarizes the major operating characteristics of the counter and register types. A complete description of the advantages and operating characteristics of the RCA COS/MOS line is given in Refs. 1, 2, 3 and 4. The applications shown in this Note for each type are not intended to be all-inclusive, but rather to highlight sample uses.

Fig. 1 illustrates the basic static master-slave flip-flop

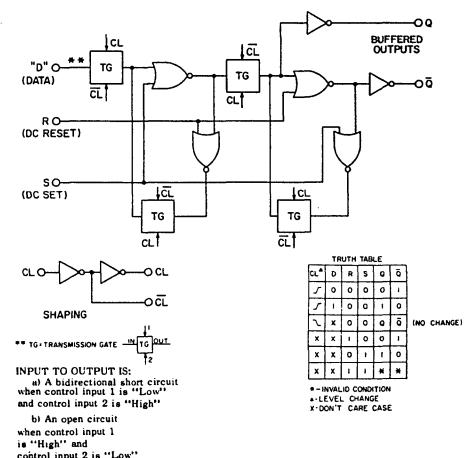


Fig. 1 - Basic COS/MOS master-slave flip-flop stage.

circuit configuration utilized in all the designs described. The logic level present at the "D" (Data) input is transferred to the "Q" output during the positive-going transition of the clock pulse. DC "Reset" or "Set" is accomplished by a high level at the respective input.

loosely specified input waveshape requirement. As shown in Table I, the basic flip-flop configuration operates from a non-critical single-phase clock input signal. Both "1" and "0" clock-pulse durations can go to infinity, and rise and fall times of 5 microseconds or less are permissible.

**Table I - Typical Features and Characteristics of COS/MOS Counters and Registers – All Types.**

#### FEATURES:

Operating Temperature Range                    -55 to +125°C (Ceramic)  
     -40 to + 85°C (Plastic)  
     3.5 to 15V

Operating Voltage Range  
 Full MOS Gate Oxide Protection at all Terminals  
 Output Buffers Provided  
 Full Static Operation

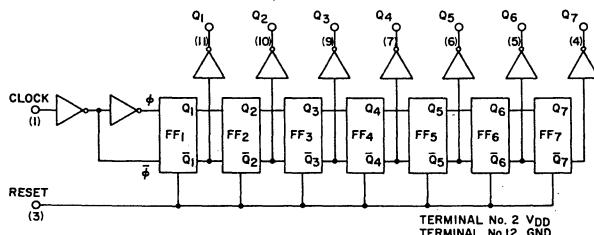
#### TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

	$V_{DD} = 10\text{V}$	$V_{DD} = 5\text{V}$
Clock Pulse Frequency	5MHz	2.5MHz
Clock Rise & Fall Times	$\leq 5\ \mu\text{s}$	$\leq 5\ \mu\text{s}$
Quiescent Power Dissipation/Package	5 $\mu\text{W}$	1.5 $\mu\text{W}$
Noise Immunity — All Inputs	45% of $V_{DD}$	
Drive Capability	$I_D = 0.5$ to $3\text{mA}$ @ $V_I = 7\text{V}$	$I_D = 0.1$ to $1\text{mA}$ @ $V_I = 4\text{V}$
Sink Capability	$I_D = 0.5$ to $3\text{mA}$ @ $V_O = 3\text{V}$	$I_D = 0.1$ to $1\text{mA}$ @ $V_O = 1\text{V}$

Both "Reset" and/or "Set" functions are easily omitted, as shown for some of the designs. Output lead isolation at the "Q" and/or "Q̄" outputs is realized by use of inverters. These inverters eliminate all possibility of MOS gate oxide damage at the output leads, and also improve circuit speed, noise immunity, and drive capability. The sizes of the p-channel and n-channel MOS devices in the output inverters are tailored to meet the desired drive and sink current requirements. The internal clock shaping shown permits a

#### CD4024A Seven-Stage Ripple-Carry Binary Counter

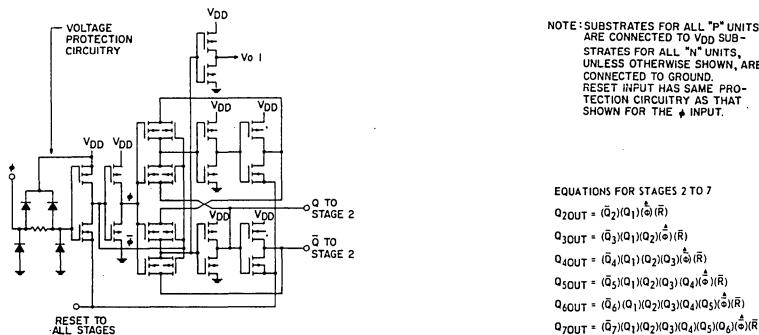
Fig. 2 shows the logic diagram of the CD4024A, a 7-stage ripple-carry binary counter. Fig. 3 illustrates in more detail the schematic and logic diagrams for one of the seven counter stages. Operation is similar to that of the basic master-slave flip-flop, with the following exceptions: the "D"-line connection is derived from the Q output of that stage so that it complements the stage at the negative clock-pulse transition. The clocking of a stage is derived from



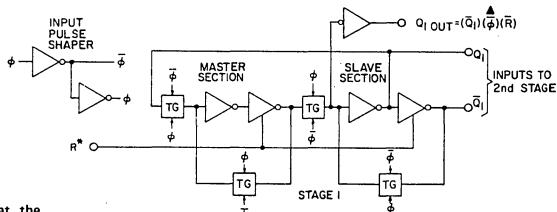
**Fig. 2 - Logic diagram of CD4024A binary counter.**

the previous counter stage (ripple-carry). The dc "Reset" function is realized by raising the ground return path of the  $\bar{Q}$  outputs of all seven stages (both master and slave sections). This mode of resetting saves four devices and associated interconnections per counter stage.

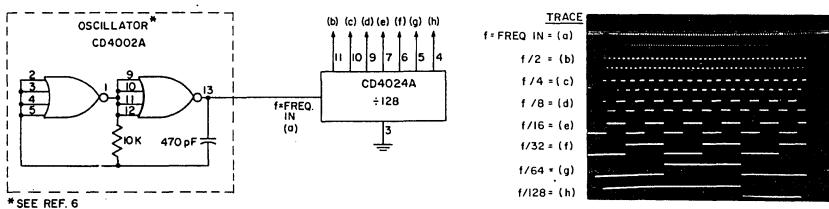
Fig. 4 illustrates the use of the CD4024A as a binary frequency-divider. Multiple CD4024A units can be stacked for added frequency division. The clock input of a subsequent CD4024A is derived directly from the last output stage of the previous CD4024A.



**Note:** Reset line drive impedance must be such that the specified conditions are met. For example, with  $V_{DD} = 10$  V the reset line voltage must not exceed 1 volt. For a typical peak current of 2 mA this requires that the drive impedance be  $< 500 \Omega$ .



*Fig. 3 - Schematic and logic diagrams for one of the seven counter stages in the CD4024A.*



*Fig. 4 - CD4024A "Binary frequency-divider" application.*

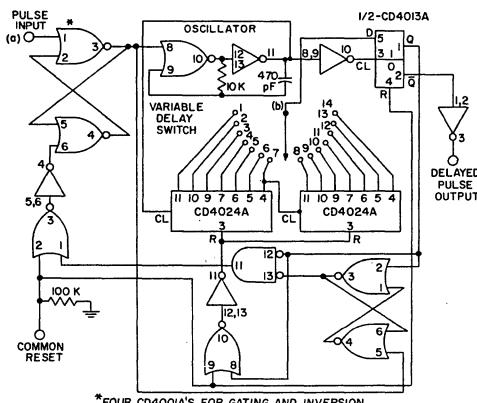
Fig. 5 shows how the CD4024A is used to derive a desired pulse-output delay time. Varied delay times can be realized by detecting different CD4024A outputs. A finer control of delay time is possible if more than one CD4024A output is detected. Extremely long and accurate delay times can be realized by use of an accurate oscillator\* and multiple CD4024A units.

Fig. 6 illustrates the use of the CD4024A to derive various divide-by-N counter configurations. Fig. 6a & 6b illustrate 2 reliable reset methods for counting to the number N, (N=60). Reset mode 1 is shown in Fig. 6a. The type D-Flip-Flop is set at the coincidence of count 59 and the positive clock transition. At the next negative clock transition, a reset pulse is generated, whose duration is

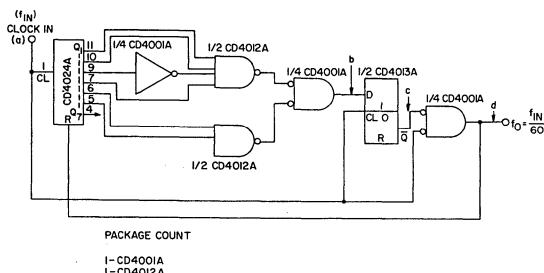
one-half the clock cycle time. This resets the CD4024A to zero. Note that only count 59 needs to be detected for the reset operation, and no N+1 count occurs.

Reset mode 2 is shown in Fig. 6b. The N+1 count (60) is detected, sets the R-S Flip-Flop, which in turn resets the CD4024A to the zero state. The reset pulse width is one-half the clock cycle time, and is removed by gating count zero with the positive clock transition to reset the R-S Flip-Flop.

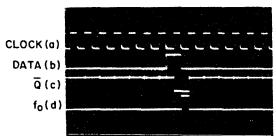
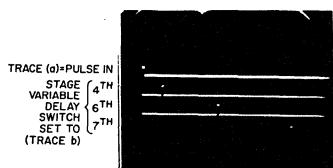
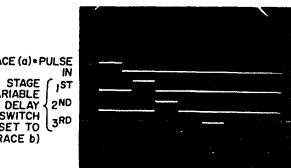
Fig. 6c illustrates a divide-by-60, divide-by-60 and divide-by-24 timer system using the reset scheme (mode 1) of Fig. 6a. Similar use of one CD4024A unit permits any divide-by-N from 2 to 128. In applications where decimal display outputs are required, the RCA type CD4017A can be used to advantage, as described later in this Note.



*Fig. 5 - CD4024A "Pulse-delay-control" application*

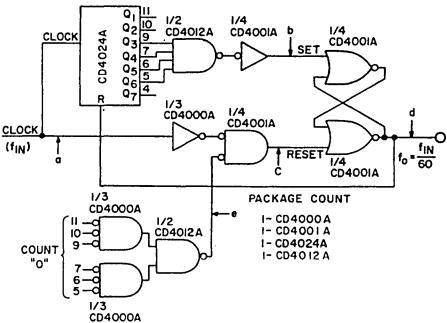


*Fig. 6a - Counter of 60 using reset mode 1.*



*Fig. 6 - CD4024A used to derive various divide-by-N counter configurations.*

\* See Ref. 5



*Fig. 6b - Counter of 60 using reset mode 2.*

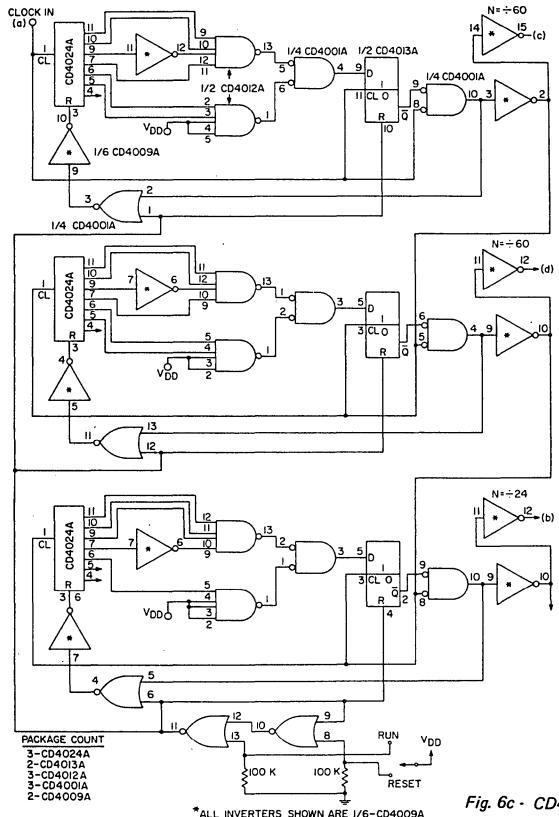
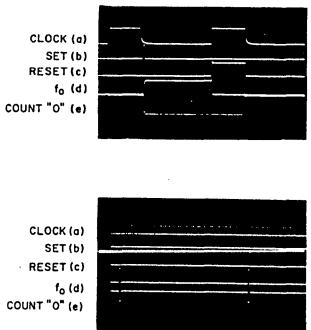


Fig. 6c - CD4024A "Divide-by-N counter" configuration; diagram shows divide-by-60, divide-by-60 and divide-by-24 configurations.

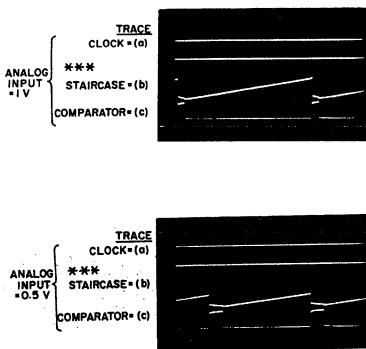
Fig. 7a shows how the CD4024A is used with a weighted resistor network to realize analog to digital conversion (A to D). The CD4010A (Hex-Buffer, Non-Inverting) is used to reduce the more significant counter output "1" level impedances (which have poor tolerances) to well below the precision resistor network values.

Variied ranges of analog signals can be handled by control of the resistor network and comparator.

As the CD4024A counter advances, the voltage input to the comparator rises until it equals the analog input. The comparator then switches and inhibits further counter advancement, thus holding the digital representation of the analog signal in the counter. Because the CD4024A can

count to  $2^7$ , or 128, division of an analog voltage range into 100 parts is easily realized. (The example shows a 1-volt range broken into 10-millivolt steps.)

Fig. 7b shows the CD4024A used with an R-2R ladder network for A to D conversion. The R-2R network, while requiring added resistors, utilizes only 2 resistor values, permits ready expansion to greater than 7 stages, and provides better resistor temperature tracking and allows elimination of the CD4010A's. The photographs, for the R-2R network, show a stepping input from zero to 12.8 volts, divided into 100-millivolt steps. The CD4010A Buffers may be used to permit lower R-2R values, if desired.



\*TISTER RESET ON COMPARATOR TO PERMIT REPETITIVE OPERATION FOR SCOPE DISPLAY.

\*\*DIFFERENT ANALOG VOLTAGE RANGES CAN BE REALIZED BY DIFFERENT RESISTOR, COMPARATOR ARRANGEMENTS.

\*\*\*1 VOLT/DY Vertical Scale.

Fig. 7a - Weighted resistor network.

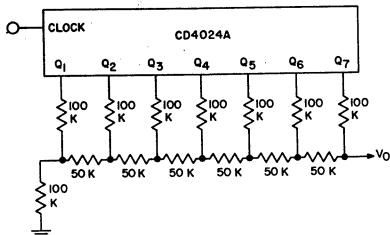
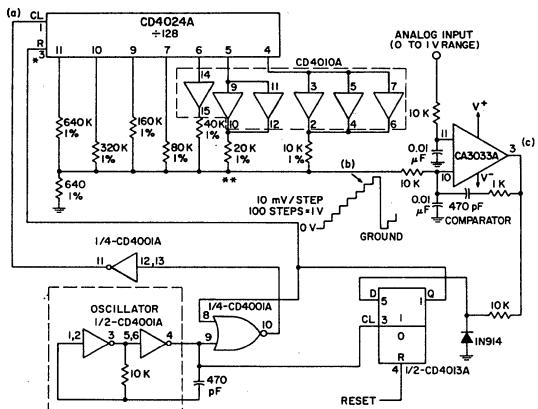


Fig. 7b - Analog-to-digital conversion-resistor ladder network.

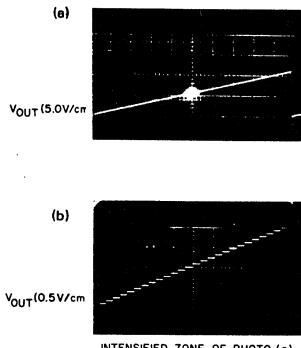


Fig. 7 - CD4024A "Analog-to-digital conversion" application.

Fig. 8 shows the Logic Diagram of the CD4020A, a 14-Stage Binary Counter. Applications are similar to the CD4024A.

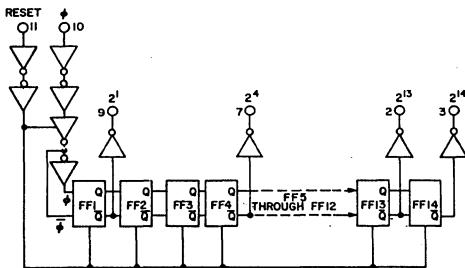


Fig. 8 - Logic diagram of CD4020A 14-stage binary counter.

#### RCA CD4017A Decade Counter/Divider

##### Plus 10 Decoded Decimal Outputs

Fig. 9 shows the logic diagram of the CD4017A, a decade counter plus 10 decoded decimal outputs. A five-stage "Johnson Counter" configuration is used to implement the decade counter. The basic flip-flop stages are similar to that described in Fig. 1. "Clock", "Reset", "Inhibit", and "Carry Out" signals are provided. The decade counter advances one count at the positive clock-signal transition provided the inhibit signal is low. Counter advancement by way of the clock line is inhibited when the inhibit signal is high. A high

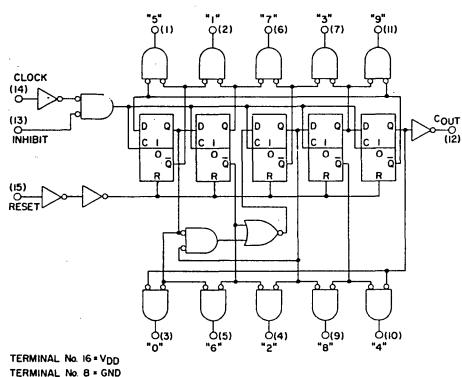


Fig. 9 - Logic diagram of CD4017A-decade counter.

reset signal clears the decade counter to its zero count. Use of the "Johnson" decade counter configuration permits high-speed operation, two-input decimal decode gating, and spike-free decoded output. Anti-lock gating is provided to permit only the proper counting sequence. The ten decimal outputs are normally low and go high only at their respective decoded decimal time slot. Each decimal output remains high for one full clock cycle. The carry-out signal completes one cycle for every ten clock input cycles, and is used to clock the following decade directly in any multi-decade application.

Fig. 10 shows the use of the CD4017A in a "Multi-Decade Counter/Decimal Display" application. Two typical lamp-driver interface circuits are shown. When one-sixth of a CD4009A is used as the lamp driver, current ranges up to 20-milliampères and 7.5-milliampères can be realized for COS/MOS supply voltages of 10 volts and 5.0 volts, respectively.

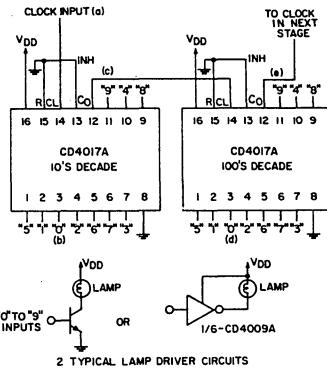


Fig. 10 - CD4017A "Multi-decade counter/decimal display" application.

Fig. 11 illustrates the use of the CD4017A in a "Multi-Decade Frequency Division" application; decimal display is optional. Fig. 12 shows the use of the CD4017A to obtain various divide-by-N counter configurations. Figs. 12a & 12b illustrate two reset methods in counting to the number 60. Fig. 12c shows an example of divide-by-60, divide-by-60 and divide-by-24. The CD4017A permits easy decimal display of each divide-by-N section. The CD4017A can also be used in applications requiring multiplexing, de-multiplexing and commutation of signals.

**RCA CD4022A Divide-by-8 Counter Plus 8 Decoded Outputs**

Fig. 13 shows the logic diagram of the CD4022A, a divide-by-8 counter and 8 decoded outputs. A four-stage "Johnson Counter" is used to implement the divide-by-8 counter. The basic flip-flop stages are similar to that described in Fig. 1. "Clock", "Clock-Enable", "Reset" and "Carry-Out" signals are provided on the divide-by-8 counter.

The divide-by-8 counter is advanced one count at the positive clock-signal transition. A high reset signal returns the divide-by-8 counter to its zero count. Use of the "Johnson" divide-by-8 counter configuration permits high-speed operation, two-input decode gating, and spike-free decoded output. Anti-lock gating is provided to permit only the proper counting sequence. The eight decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. The carry-out signal completes one cycle for every eight clock input cycles, and is used to clock the following counter stage directly, in multi-stage applications.

Fig. 14 shows the CD4022A used in a "Divide-by-8 Counter/Decoder" application. One CD4022A unit provides the counting as well as the decoding function.

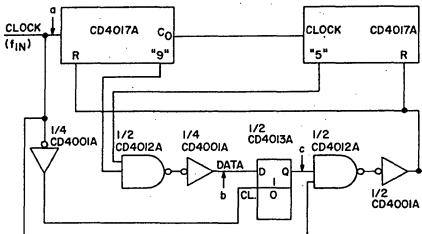


Fig. 12a - Counter of 60-using reset mode 1.

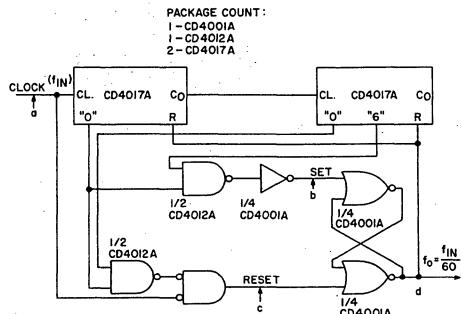


Fig. 12b - Counter of 60-using reset mode 2.

Fig. 12 - CD4017A "Divide-by-N counter" configurations.

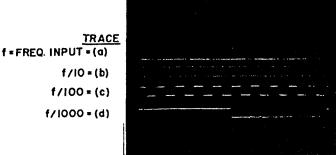
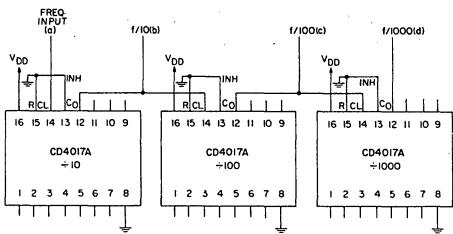
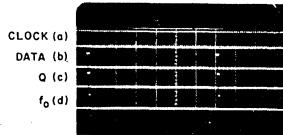
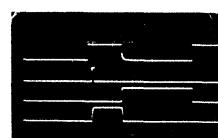
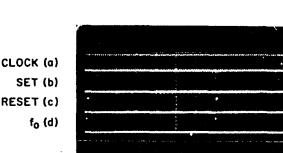
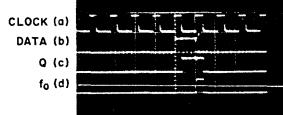
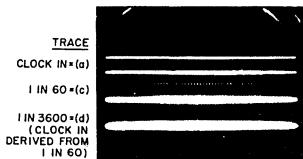
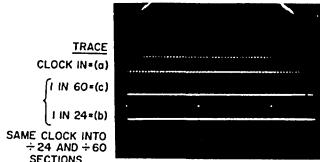
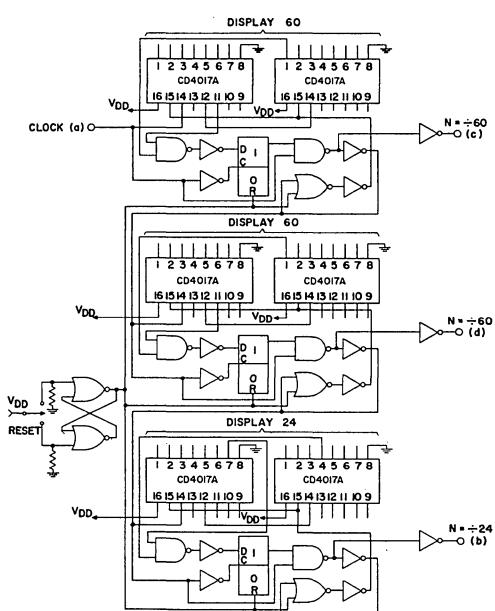


Fig. 11 - CD4017A "Multi-decade frequency division" application.

PACKAGE COUNT:  
1 - CD4017A  
1 - CD4012A  
2 - CD4001A

"DIVIDE BY N COUNTER WITH DECIMAL DISPLAY"  
(EXAMPLE SHOWN  $\div 60$ ,  $\div 60$ ,  $\div 24$ )



## PACKAGE COUNT

6-CD4017A  
2-CD4011A  
2-CD40101A  
2-CD4013A  
2-CD4009A

Fig. 12c - Divide-by-60, divide-by-60 and divide-by-24 configuration.

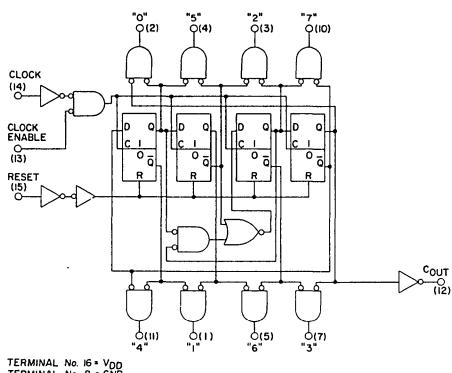


Fig. 13 - Logic diagram of the CD4022A-divide-by-8 counter.

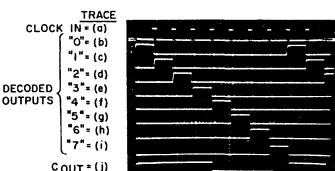
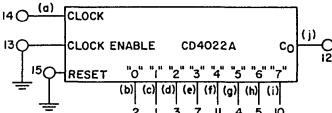


Fig. 14 - CD4022A "Divide-by-8 counter/decoder" application.

Fig. 15 shows a "Divide-by-64 Counter/Decoder" application. The partial decode function performed by the CD4022A significantly simplifies the external gating to complete the 1-in-64 decode function. Other binary counter/decoder applications can also be realized.

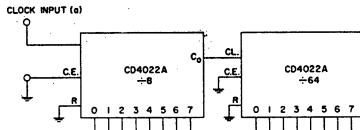


Fig. 15a - Block diagram.

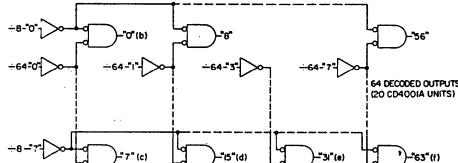


Fig. 15b - Logic diagram.



Fig. 15c - Waveforms.

Fig. 15 - CD4022A "Divide-by-64" counter/decoder" application.

#### RCA CD4018A Presettable Divide-by-N Counter

Fig. 16 shows the logic diagram of the CD4018A, a presettable divide-by-N counter. The CD4018A consists of five flip-flops which can be configured as a 5-, 4-, 3-, or 2-stage Johnson counter with buffered  $\bar{Q}$  outputs from each stage, and counter preset control gating. "Clock", "Reset", "Data", "Preset", and 5 "Jam" inputs are provided.  $\bar{Q}$  outputs are provided from each of the five counter stages. The basic flip-flop stages are similar to that shown in Fig. 1.

Divide-by-10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the  $\bar{Q}_5$ ,  $\bar{Q}_4$ ,  $\bar{Q}_3$ ,  $\bar{Q}_2$ , or  $\bar{Q}_1$  signals, respectively, back to the data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by use of the CD4011A gate package to gate the proper feedback connection to the data input. Divide-by-functions greater than 10 can be achieved by use of multiple CD4018A packages. The counter configuration is advanced one count at the positive clock-signal transition. A high reset signal clears the counter to an all-zero condition. A high preset

signal allows information on the Jam inputs to preset the counter configuration. Anti-lock gating is provided to assure the proper counting sequence.

Fig. 17 shows the CD4018A utilized in constructing fixed counters of divide-by-9, 7, 5 or 3. Operation in a divide-by-7 configuration is shown in detail in Fig. 18.

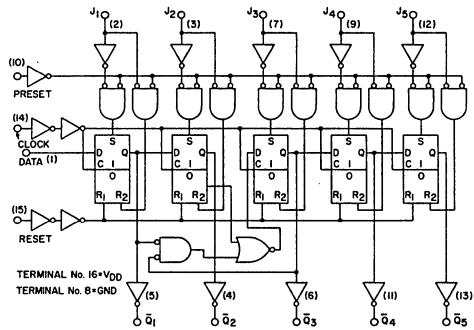


Fig. 16 - Logic diagram of the CD4018A-presettable divide-by-N counter.

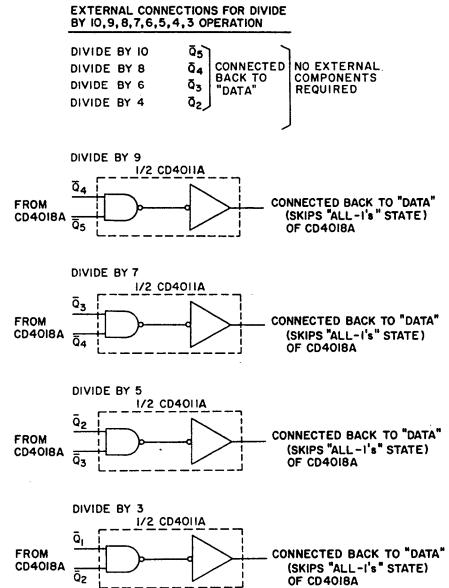
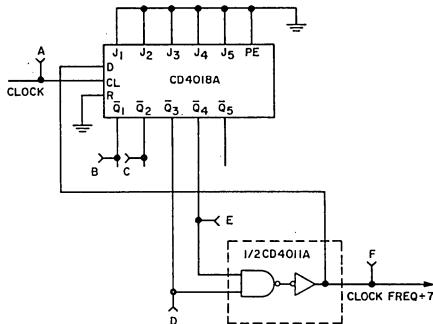


Fig. 17 - External connections for divide-by-10, 9, 8, 7, 6, 5, 4, 3 operation.



TEST POINT

CLOCK	A
$\bar{Q}_1$	B
$\bar{Q}_2$	C
$\bar{Q}_3$	D
$\bar{Q}_4$	E
	F
	DATA

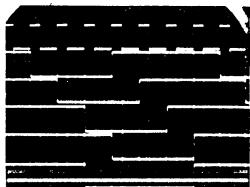
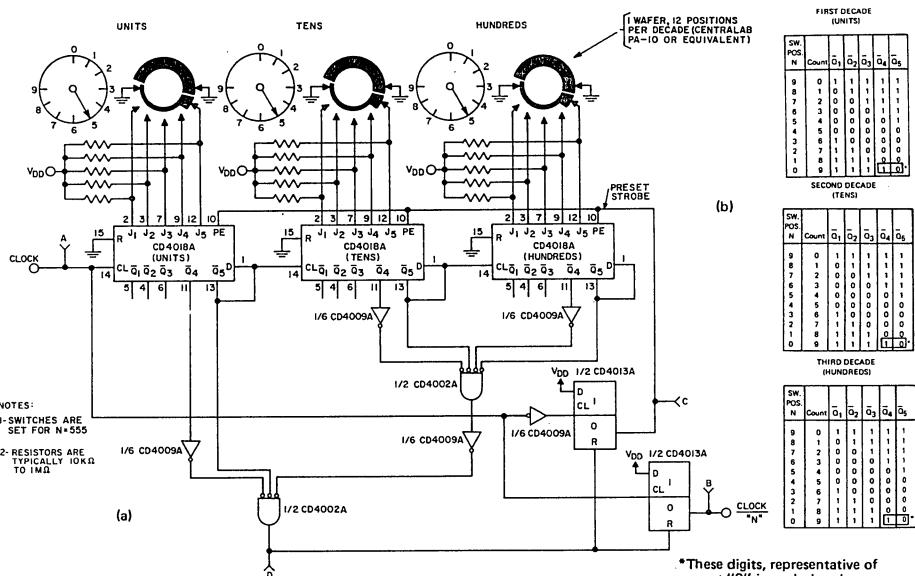


Fig. 18 - CD4018A "Fixed divide-by-7" configuration.



(b)

FIRST DECADE (UNITS)					
SW.	POS.	N	Count	$\bar{Q}_1$	$\bar{Q}_2$
9	0	1	1	1	1
8	2	0	0	1	1
7	5	3	0	0	1
6	4	4	0	0	0
5	3	6	1	0	0
4	2	7	1	1	0
3	1	8	1	1	1
2	0	9	1	1	1
1		0			

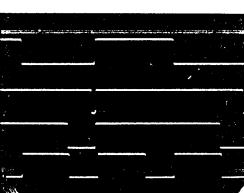
SECOND DECADE (TENS)					
SW.	POS.	N	Count	$\bar{Q}_1$	$\bar{Q}_2$
9	0	1	1	1	1
8	2	0	0	1	1
7	5	3	0	0	1
6	4	4	0	0	0
5	3	6	1	0	0
4	2	7	1	1	0
3	1	8	1	1	1
2	0	9	1	1	1
1		0			

THIRD DECADE (HUNDREDS)					
SW.	POS.	N	Count	$\bar{Q}_1$	$\bar{Q}_2$
9	0	1	1	1	1
8	2	0	0	1	1
7	5	3	0	0	1
6	4	4	0	0	0
5	3	6	1	0	0
4	2	7	1	1	0
3	1	8	1	1	1
2	0	9	1	1	1
1		0			

\*These digits, representative of count "9" in each decade, are decoded to give the preset strobe.

(c) FIG. 19 a TEST POINT



(d) CLOCK-[TP "A", FIG. 19 a]

JAM-IN FOR SWITCHES PROGRAMMED FOR "N" EQUALS:  
[TP "B", FIG. 19 c]

009
019
050
090
099

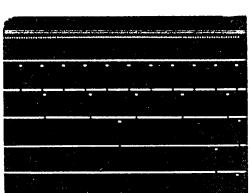


Fig. 19 - Three-decade, programmable, divide-by-N counter with frequency division from 2 to 999: (a) logic diagram; (b) counting sequence; (c) timing waveforms at various points in the circuit; (d) divide-by-N output for various values of N;

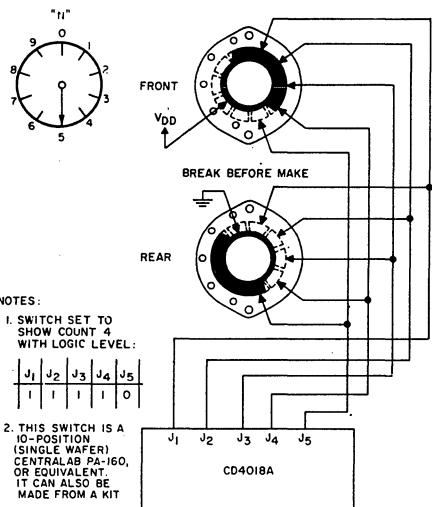


Fig. 19 (e) alternative decade switch configuration.

Fig. 19 illustrates the use of the CD4018A in a programmable divide-by-N counter, where N is any number from 2 to 999 for the example shown. Extension to higher N ranges is realized by use of additional CD4018A units. The Johnson-counter configuration of the CD4018A permits simpler switch arrangements at the Jam inputs controlling the programmable preset state. The programmable divide-by-N configuration can be utilized in frequency-synthesis applications.

The CD4018A can also be utilized as a five stage parallel input/output holding register. "Holding Register" parallel entry can be controlled by means of the "Preset Enable Line", resulting in a five stage latch operation.

#### CD4006A 18-Stage Static Shift Register

Fig. 20 shows the logic diagram of the CD4006A, an 18-stage static shift register. The register stages are similar to those shown in Fig. 1. The CD4006A consists of four separate shift-register sections, two four-stage sections and two five-stage sections with output taps at the fourth stage. Each register section has independent "Data" inputs to the first stage. The clock input is common to all 18 register stages. Through appropriate connection of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one CD4006A. Longer shift-register sections can be assembled by use of more than one CD4006A.

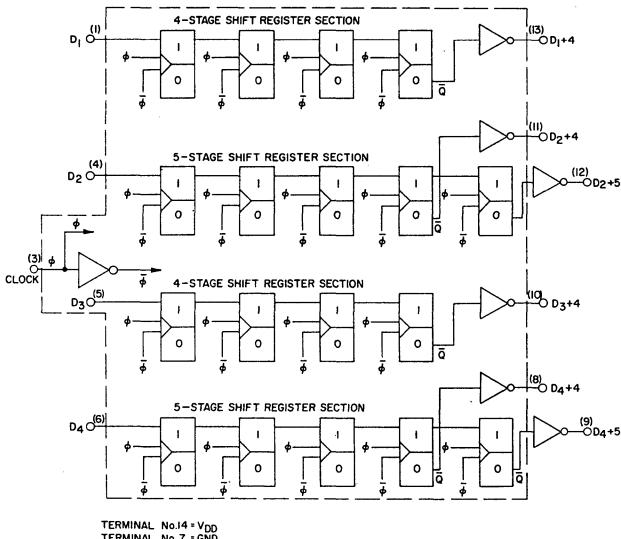


Fig. 20 - Logic diagram of the CD4006A - 18-stage static shift register.

Fig. 21 shows in more detail the schematic and logic diagrams for one of the 18 register stages. Register shifting occurs on the negative clock-pulse transition.

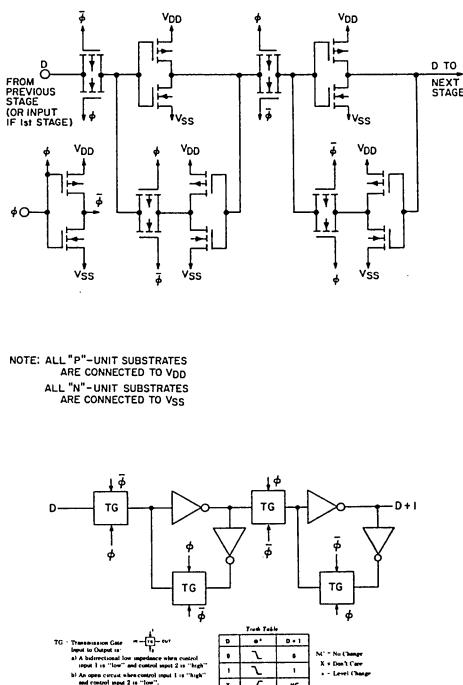


Fig. 21 - Schematic and logic diagrams for one of the 18 register sections of the CD4006A.

#### RCA CD4015A Dual 4-Stage Serial-Input/Parallel-Output Static Shift Register

Fig. 22 shows the logic diagram of the CD4015A. The CD4015A consists of two identical, independent, four-stage serial-input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs, as well as a serial "Data" input. "Q" outputs are available from each of the four stages on both registers. All register stages are similar to that shown in Fig. 1. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive clock transition. Reset of a four-stage section is accomplished by a high level on the reset line. Register expansion to 8 stages with one CD4015A or to more than 8 stages with multiple CD4015A packages, is possible.

Fig. 23 shows the use of the CD4015A in an 8-stage serial-input/parallel-output register application. This circuit operates as follows: The CD4015A connected as an 8-stage register is reset and "1's" are shifted through the register. The scope trace shows the "1" pattern loading into the register until a "1" reaches the eighth stage and initiates reset. After two clock pulses, the reset is removed and "1's" again shift into the register. Low-speed-to-high-speed data queueing and serial/parallel data conversion are typical applications.

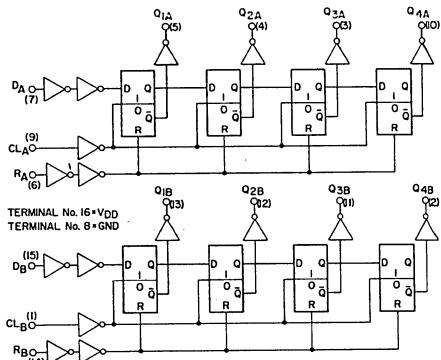


Fig. 22 - Logic diagram of the CD4015A - dual 4-stage serial-input/parallel-output register.

#### RCA CD4014A 8-Stage Synchronous Parallel-Input/Serial-Output Static Shift Register

Fig. 24 shows the logic diagram of the CD4014A, an 8-stage synchronous parallel-input/serial-output register. A "Clock" input and a single serial "Data" input along with individual parallel "Jam" inputs to each register stage and a common "Parallel/Serial" control signal are provided. "Q" outputs from the 6th, 7th, and 8th stages are available. All register stages are similar to that shown in Fig. 1, except that extra transmission gates permit parallel or serial entry. Parallel or serial entry is made into the register synchronous with the positive clock transition and under control of the parallel/serial input. When the parallel/serial input is low, data is serially shifted into the 8-stage register synchronous with the positive clock transition. When the parallel/serial input is high, data is jammed into the 8-stage register by way of the parallel input lines and synchronous with the positive clock transition. Register expansion with multiple CD4014A packages is possible.

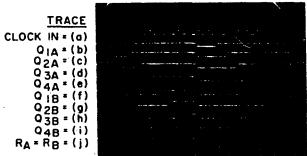
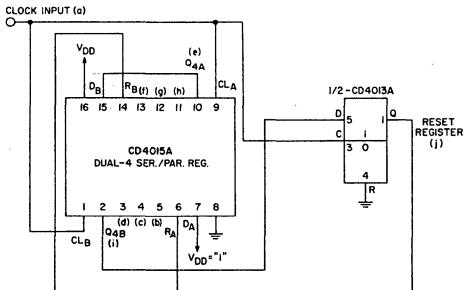


Fig. 23 - CD4015A 8-stage serial-input/parallel-output register application.

Fig. 25 shows the use of the CD4014A in an 8-stage synchronous parallel-input/serial-output register application. In this configuration, the CD4013A allows a parallel transfer to be made into the CD4014A register once every 8 clock pulses. Use of the divide-by-2 outputs of the CD4013A as parallel inputs to alternate CD4014A stages permits change-over from a 10101010 to a 01010101 parallel input pattern every 8 pulses. The scope trace shows the parallel transfer of the 01010101 pattern into the register followed by eight shift pulses and subsequently another parallel transfer of 10101010 and eight shift pulses. High-speed-to-low-speed data queueing and parallel/serial data conversion are typical applications.

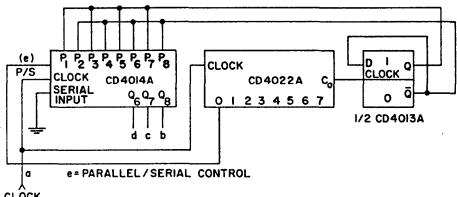


Fig. 25 - CD4014A 8-stage synchronous parallel-input/serial-output register application.

The CD4014A can be utilized in pseudo-random-code generation applications via combined control of the parallel input conditions and gating of the 6th, 7th, and 8th stage register feedback to the serial input. Fig. 26 shows the photomicrograph of the CD4014A pellet.

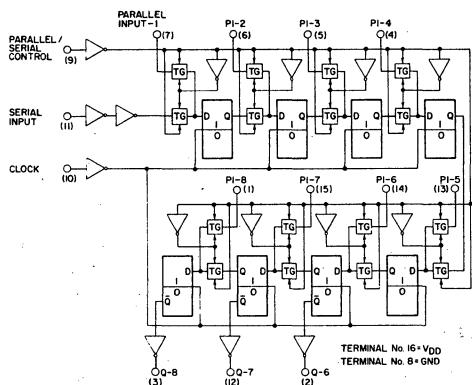


Fig. 24 - Logic diagram of the CD4014A 8-stage synchronous parallel-input/serial-output register.

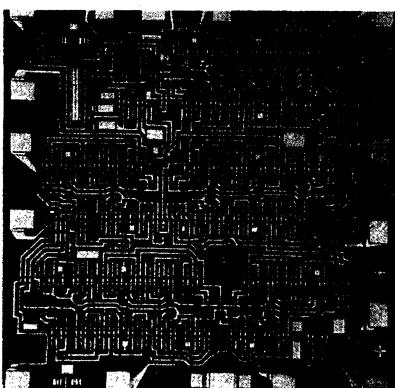


Fig. 26 - Photomicrograph of the CD4014A pellet.

### RCA CD4021A 8-Stage Asynchronous Parallel-Input/Serial-Output Static Shift Register

Fig. 27 shows the logic diagram of the CD4021A 8-stage asynchronous parallel-input/serial-output register. Operation is basically the same as that of the CD4014A except that parallel transfers are made as soon as the parallel/serial control input goes high. Parallel transfers are thus made asynchronous with the clock input. Serial shifting is still performed synchronously with the clock input. The CD4014A thus permits the parallel transfer to be synchronized with a different clocking signal than that of the serial transfer. Thus, in high-speed-to-low-speed data queueing, for example, an externally gated high-speed clock may control the parallel transfer while the low-speed clock may control the serial shifting.

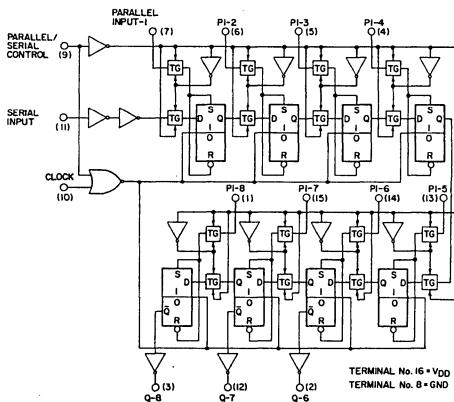


Fig. 27 - Logic diagram of the CD4021A 8-stage asynchronous parallel-input/serial-output register.

Fig. 28 shows the use of the CD4021A in an 8-stage asynchronous high-speed parallel-input/low-speed serial-output application. For the example shown, the high-speed portion of the system is simulated by simplified control logic. A 10kHz slow-speed clock and 1MHz high-speed clock are assumed. Signal lines "a" and "b", as well as the eight data lines, are representative of the information transfer requirements, between the high-and-low-speed systems. At the slow-speed output sections, the CD4021A shifts out stored information at a 10kHz clock rate. The CD4022A

counts to eight at the 10kHz rate and at count zero, sends a high "Flag" signal to the high-speed system over line "a", indicating that the low-speed section is ready to accept eight bits on the data lines.

In the simulated high-speed section, a high on line "a", allows Flip-Flop "A" to set on the positive transition of the 1MHz clock. The Q output of Flip-Flop "A" is gated with the 1MHz clock to form a gated 1MHz clock signal on line "b". This clock signal along with count zero at the slow speed section puts a single 1MHz gated clock pulse at the Parallel/Serial Control of the CD4021A to permit an eight bit parallel transfer of data from the high-speed system to the low-speed system.

R-S Flip-Flops 1 & 2 remove the "Flag" signal "a" after a 1MHz gated clock pulse on line "b" has generated the parallel transfer signal. These flip-flops also prevent any further activation of line "a" (and line "b") and subsequent parallel transfers until the CD4022A counts back to zero. Thus, the eight bits transferred into the CD4021A are shifted out at the 10kHz clock rate before a new set of data is transferred into the CD4021A. Note that the extra pulse edge generated at line "b" (one clock pulse after the gated 1MHz clock pulse) is ignored. (See the Logic of the slow-speed section.) For Scope Display purposes, Flip-Flop B, in the high-speed system is used to change the pattern transferred every eight 10kHz clock pulses from a 10101010 to a 01010101 pattern.

In an actual system the high signal at line "a" would represent a "Flag" bit, enabling the high-speed system to transfer eight bits of new data, any time during the count zero. (10kHz clock cycle duration.) This allows the high-speed system time to service its many other input and output lines and to satisfy internal process requirements at the 1MHz rate. At the same time, the high-speed system is still conditioning the eight transfer lines (just prior to activation of line "b") with a pulse to enable the parallel transfer of data. The re-sync Flip-Flop in the slow-speed section helps avoid any gap in the output data due to the variable delay possible in line servicing between the eighth shifted bit out of the CD4021A and the next parallel transfer of the eight valid bits of information.

### Conclusions

This note has shown the use of several COS/MOS MSI counters and static shift registers in systems designs. The designs described are useful in a variety of applications.

The availability of an increasing number of standard low-cost COS/MOS devices now permits the systems designer greater freedom and versatility as well as increased reliability in his designs.

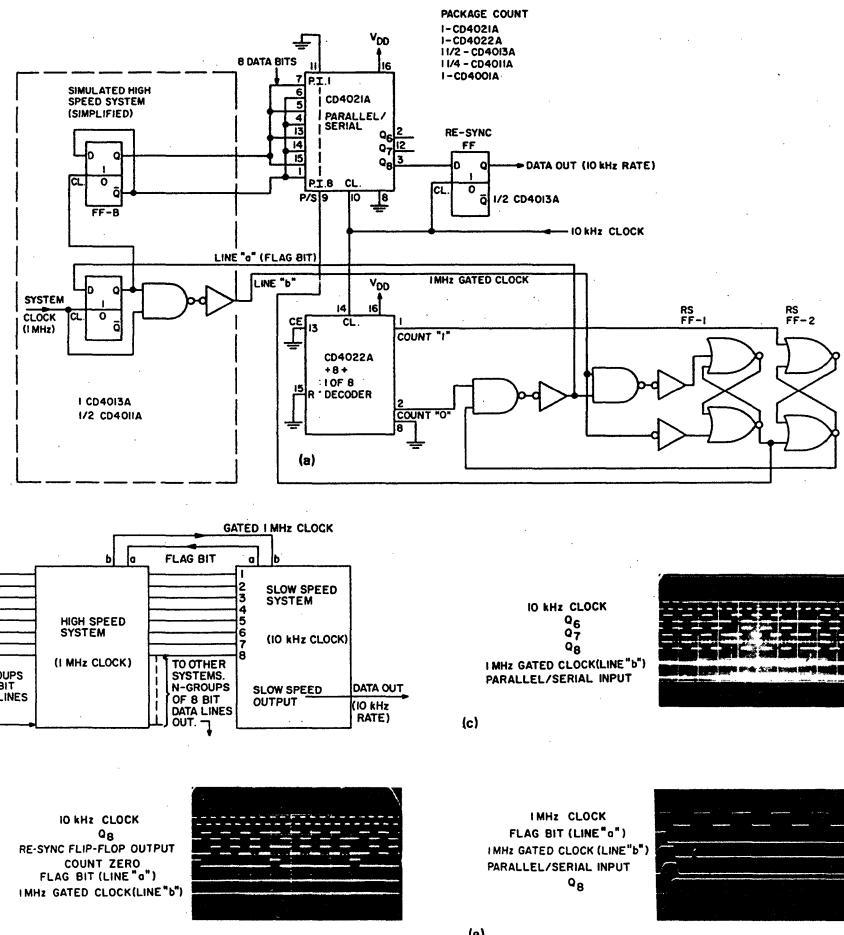


Fig. 28 – CD4021A “8 bit asynchronous high-speed parallel-input/low-speed serial-output” application; (a) logic diagram, (b) block diagram; (c) slow-speed system waveforms; (d) slow-speed system waveforms; (e) high-speed system (expanded scale) waveforms.

#### References:

1. RCA COS/MOS Commercial Data Sheets, CD4000A series and Developmental Data Sheets by “TA” Number
2. “Power Supply Considerations For RCA COS/MOS IC’s” by H. Pujol, ICAN-6576
3. “Design of Fixed and Programmable Counters Using the RCA CD4018A COS/MOS Presettable Divide-by-N Counter”, by J. Litus, Jr., ICAN-6498
4. “Complementary MOS Transistor Logic Integrated Circuits”, ICAN-5593
5. “Micropower Crystal-Controlled Oscillator Design using RCA-COS/MOS Inverters”, by S.S. Eaton, ICAN-6539
6. “Astable and Monostable Oscillators Using RCA COS/MOS Digital IC’s”, by J.A. Dean and J.P. Rupley, ICAN-6267



# Digital Integrated Circuits

## Application Note

ICAN-6176

### Noise Immunity of COS/MOS Integrated-Circuit Logic Gates

by S.S. Eaton

The immunity of a COS/MOS integrated-circuit logic gate to noise signals is a function of many variables, such as individual chip differences, fan-in and fan-out, stray inductance and capacitance, supply voltage, location of the noise, shape of the noise signal, and temperature. Moreover, the immunity of a system of gates usually differs from that of any individual gate. Because of the many variables involved, a generalized analysis of the noise immunity of a logic circuit is a complex process. In general, it is more practical to analyze immunity of a system for a specific set of conditions and then to generalize or extrapolate the results to make them applicable to other sets of conditions.

This Note describes the types of noise usually encountered in a logic system and evaluates the noise immunity of a COS/MOS integrated-circuit logic-gate test setup in relation to system variables. The evaluation is performed on a setup that includes a CD4000A dual 3-input gate plus inverter and a CD4001A quad 2-input gate connected in cascade to drive a CD4013A flip-flop. Measurement of the voltage required at various gate leads to switch the flip-flop defines the noise-immunity threshold of the gate circuits.

#### TYPES OF NOISE

The following listing indicates and briefly explains the types of noise usually encountered in logic systems:

1. **External noise** – noise that is generated externally by electric motors, arcing relay contacts, circuit breakers, and other similar types of devices. Such noise is usually inductively coupled into the logic system.

2. **Crosstalk** – noise that results from coupling (usually capacitive) between adjacent signal lines.
3. **Transmission-line reflections** – noise introduced into the logic system when an impedance mismatch exists at the receiving end of the line. The energy reflected back along the line causes ringing, and voltage levels produced may exceed the noise-immunity threshold of the receiving gate. This type of noise is most prevalent when the switching time of the gate is short in comparison to the time delay of the line.
4. **Power-line noise** – noise that results from transient currents produced in the supply line by coupling from external sources or by stray or junction capacitances at the gate outputs.
5. **Ground-line noise** – noise that is produced on the ground line because of improper ground returns.

This Note evaluates the noise immunity of the CD4000A and CD4001A COS/MOS integrated-circuit logic gates with respect to each type of noise listed above with the exception of that produced by transmission-line reflections. Because this type of noise is specifically a function of the transmission line, a generalized analysis is not as effective as in the case of the other types of noise. However, transmission-line reflections are not significant in COS/MOS circuit systems because the switching speed of a COS/MOS circuit is generally slow in comparison to the time delay of a line. The schematic and logic diagrams of the CD4000A and CD4001A gates are shown in Figs. 1 and 2, respectively.

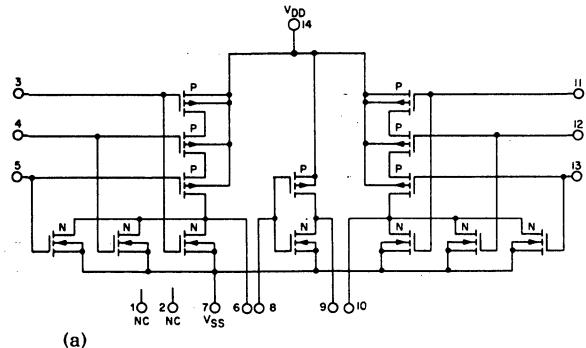
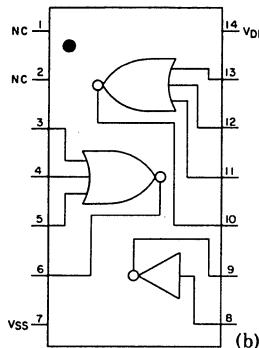
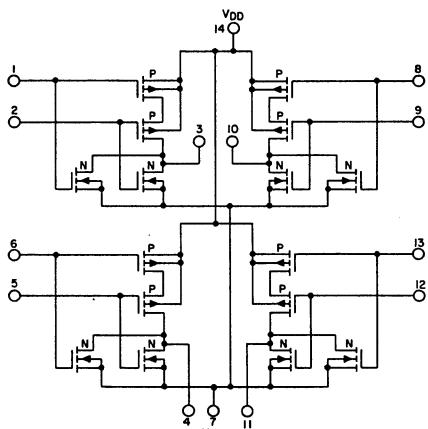


Fig. 1 - Schematic and logic diagrams of the CD4000A dual 3-input gate plus inverter.

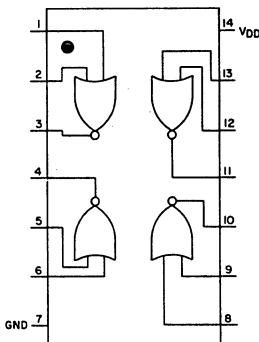


(a)

(b)



(a)



(b)

Fig. 2 - Schematic and logic diagrams of the CD4001A quad 2-input gate.

## SIGNAL-LINE EXTERNAL NOISE IMMUNITY

The following analysis was used to determine the immunity of a COS/MOS gate to noise on the input line at both the "0" (low-level) and "1" (high-level) states.

### "0"-State Analysis

The signal-line noise immunity of COS/MOS gates was evaluated by use of the test circuit shown in Fig. 3(a). The COS/MOS gate under test was the inverter section of a CD4000A. Fig. 3(b) shows the results obtained. The test setup

is designed to measure the voltage required at the input of the inverter to trigger a CD4013A flip-flop. The logic diagram of the CD4013A is shown in Fig. 4.

During test, a noise pulse is introduced on the signal line of the CD4000A inverter. At some voltage level, depending on the width of the pulse and the gate thresholds, this pulse causes the flip-flop to be "set" because of the rising voltage on the set input that results from the decreasing voltage at the output of the inverter. This level defines the permissible input range for a logical "0." The measured value for a supply voltage of 10 volts was 4.4 volts. For a supply voltage

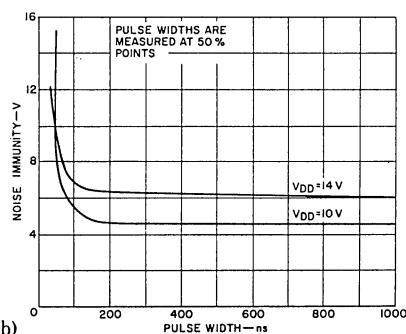
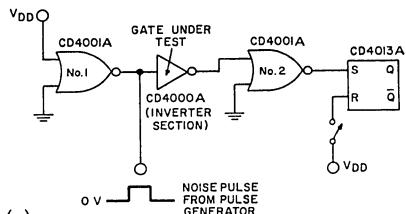


Fig. 3 - (a) Test circuit and (b) measured results for "O"-state signal-line noise-immunity test.

of 14 volts, the measured value of the voltage required to trigger the flip-flop was approximately 6.2 volts.

A dc analysis of the transfer characteristics of the components included in the test setup, shown in Fig. 5, can also be used to determine the noise level required to set the flip-flop. Fig. 5(a) shows that an input of 5.5 volts is required

to trigger the CD4013A flip-flop at a supply voltage V<sub>DD</sub> of 10 volts. Fig. 5(b) shows that a signal of 5.45 volts is required at the input to the CD4001A gate to produce an output of 5.5 volts.

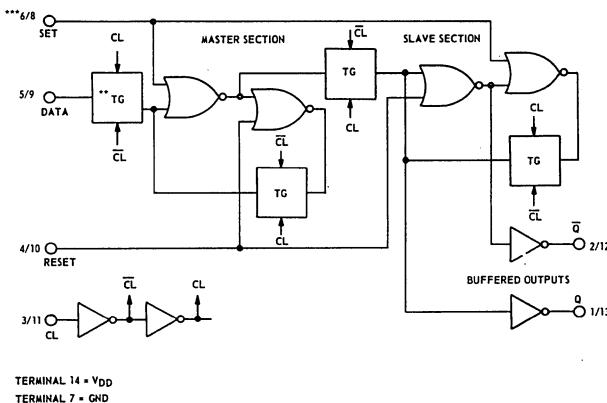
Similarly, Fig. 5(c) shows that the CD4000A inverter requires an input of 4.45 volts to provide 5.45 volts to the input of the CD4001A gate. An input of 4.45 volts to the CD4000A inverter, therefore, should trigger the CD4013A flip-flop. The actual measured value of the voltage required to trigger the flip-flop, as shown in the curve for V<sub>DD</sub> = 10 V in Fig. 3(b), is 4.4 volts. (All measured values shown on all graphs are typical, obtained from measurements on gates that have typical threshold switching characteristics.)

#### "1"-State Analysis

Fig. 6 shows the test setup used and the results obtained from noise-immunity measurements on the COS/MOS logic gates when the input to the CD4000A inverter gate is high and a negative-going pulse is superimposed on the signal line. As in the case of the "O"-state evaluation, a dc analysis of the component transfer characteristics may be made to verify the measured noise immunity. Fig. 5(c) shows that the input to the CD4000A must decrease from 10 volts to 4.5 volts (a margin of 5.5 volts) to provide the 5.5-volt output required to trigger the flip-flop. The measured value of the required decrease in voltage, as shown in Fig. 6(b), is 5.3 volts.

#### POWER-SUPPLY NOISE IMMUNITY

The test configuration shown in Fig. 7(a) measures the ability of the CD4000A inverter to withstand a negative-going noise pulse on the supply line without a change in state. A pulse of sufficient amplitude causes the output of the gate to decrease so that, at some point, the CD4013A flip-flop will be



* = INVALID CONDITION																																										
** TG = TRANSMISSION GATE																																										
 INPUT TO OUTPUT IS: a) A BIDIRECTIONAL LOW IMPEDANCE WHEN CONTROL INPUT 1 IS "LOW" AND CONTROL INPUT 2 IS "HIGH" b) AN OPEN CIRCUIT WHEN CONTROL INPUT 1 IS "HIGH" AND CONTROL INPUT 2 IS "LOW"																																										
*** = FF1/FF2 TERMINAL ASSIGNMENTS																																										
<b>TRUTH TABLE</b> <table border="1"> <thead> <tr> <th>CL<sup>a</sup></th> <th>D</th> <th>R</th> <th>S</th> <th>Q</th> <th><math>\bar{Q}</math></th> </tr> </thead> <tbody> <tr> <td>/</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>x</td> <td>0</td> <td>0</td> <td>Q</td> <td><math>\bar{Q}</math></td> <td>NO CHANGE</td> </tr> <tr> <td>x</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>x</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>*</td> </tr> <tr> <td>x</td> <td>1</td> <td>1</td> <td>*</td> <td>*</td> <td>*</td> </tr> </tbody> </table>	CL <sup>a</sup>	D	R	S	Q	$\bar{Q}$	/	0	0	0	0	1	/	1	0	0	1	0	x	0	0	Q	$\bar{Q}$	NO CHANGE	x	1	0	0	1	0	x	0	1	1	0	*	x	1	1	*	*	*
CL <sup>a</sup>	D	R	S	Q	$\bar{Q}$																																					
/	0	0	0	0	1																																					
/	1	0	0	1	0																																					
x	0	0	Q	$\bar{Q}$	NO CHANGE																																					
x	1	0	0	1	0																																					
x	0	1	1	0	*																																					
x	1	1	*	*	*																																					

Fig. 4 - Logic diagram and truth table for the CD4013A COS/MOS integrated circuit flip-flop.

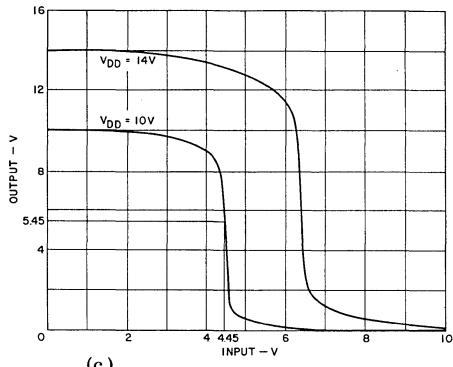
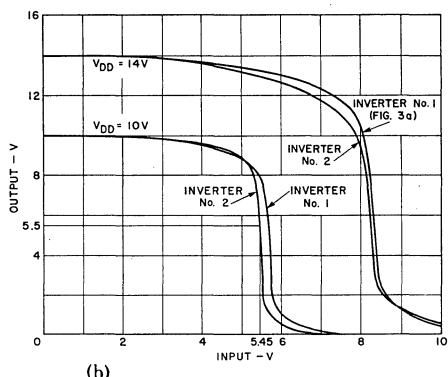
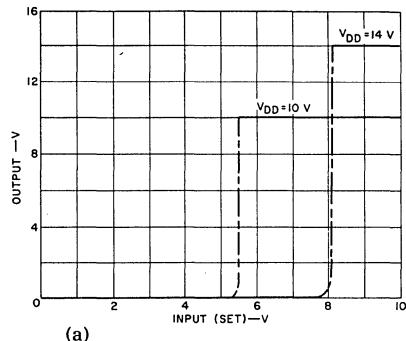
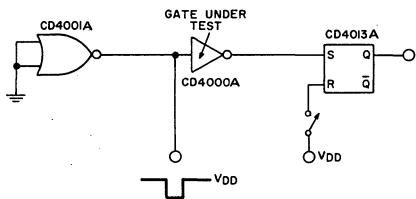


Fig. 5 - Transfer characteristics for (a) the CD4013A flip-flop, (b) the CD4001A quad 2-input NOR gates, and (c) the CD4000A inverter gate.



(a)

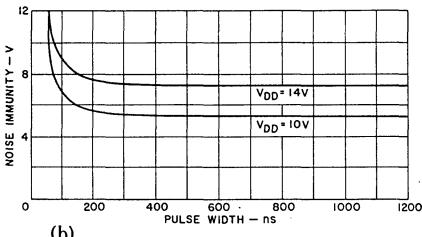
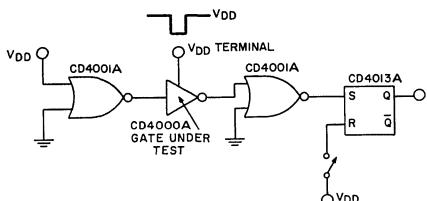


Fig. 6 - (a) Test circuit and (b) measured results for the "1"-state signal-line noise immunity test.

triggered from the rising voltage at the output of the driving inverter stage. The curves in Fig. 7(b) show the noise immunity level for noise pulses on the power supply to be 4.2 volts at 10 volts and 5.7 volts at 14 volts.



(a)

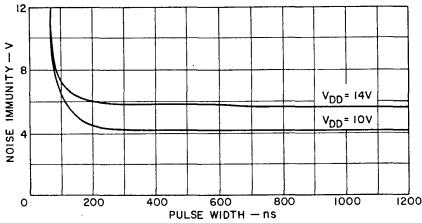


Fig. 7 - (a) Test circuit and (b) measured results for the power-line noise-immunity test.

### GROUND-LINE NOISE IMMUNITY

Noise on the power line may be effectively reduced or eliminated by use of decoupling capacitors; ground-line noise, however, cannot be reduced so easily and, therefore, is more objectionable. Fig. 8(a) shows the test circuit used to measure the ground-line noise immunity of the COS/MOS gate, and Fig. 8(b) shows curves of the measured results

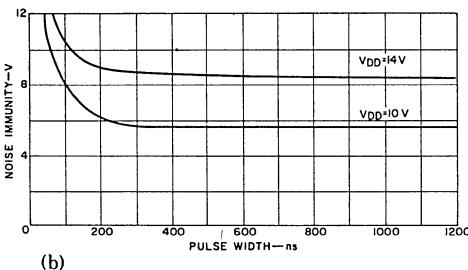
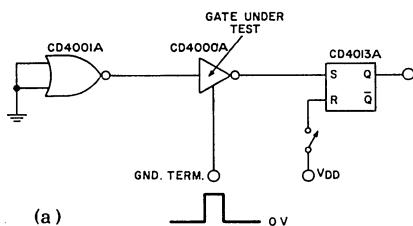


Fig. 8 - (a) Test circuit and (b) measured results for the ground immunity test.

obtained. The noise pulse introduced on the ground line of the CD4000A inverter raises the potential of the output of the gate until the flip-flop is triggered. The close similarity of the COS/MOS flip-flop switching curves shown in Fig. 9(b) and the noise-immunity curves shown in Fig. 8(b) confirms a volt-for-volt change at the gate output with a change in ground potential for the COS/MOS circuit.

### CROSSTALK NOISE IMMUNITY

A test circuit that may be used to evaluate crosstalk is shown in Fig. 10. A noise pulse from a pulse generator is coupled to the signal line of the CD4000A gate through a capacitor. The noise voltage necessary to trigger the flip-flop is then measured for different values of capacitance under "high" and "low" input conditions. Fig. 11 shows the results of these tests. As expected, the noise amplitudes required to trigger the flip-flop are higher for lower capacitance values. A more meaningful evaluation of the circuit is provided by the curves in Fig. 12, which show the noise amplitude as a percentage of the supply voltage. Because crosstalk is caused

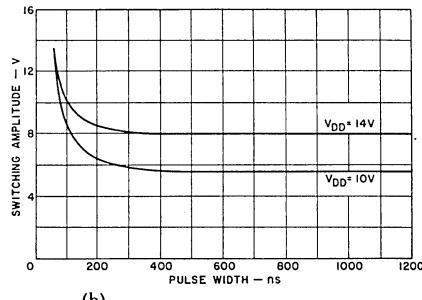
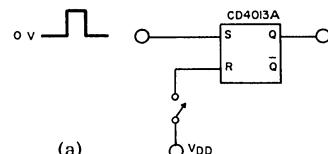


Fig. 9 - Switching curves for the CD4013A COS/MOS flip-flop.

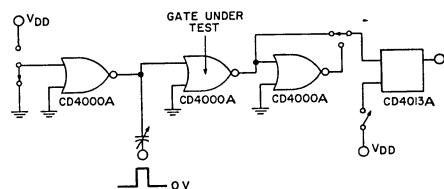


Fig. 10 - Circuit used for test of noise voltage as a function of coupling capacitance.

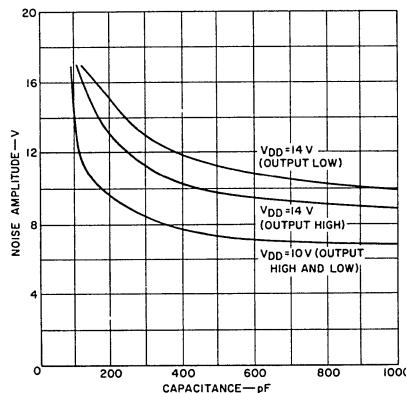


Fig. 11 - Noise immunity as a function of coupling capacitance.

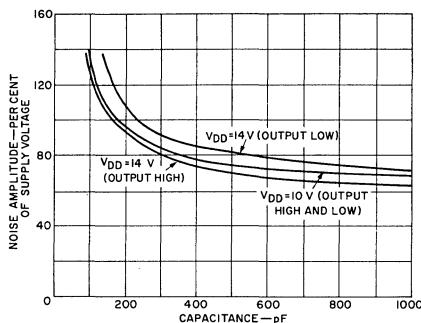


Fig. 12 - Noise immunity in terms of percentage of supply voltage.

by varying signals coupled from adjacent lines and the logic swing of these signals is limited and approaches the supply voltage, the percentage of the supply voltage coupled at the time when the flip-flop is set is a more meaningful value than the actual value of the voltage at this instant. For example, if the amplitude of crosstalk noise required to trigger the CD4013A flip-flop at a supply voltage of 10 volts is less than that required at a supply voltage of 14 volts, this condition does not imply that a COS/MOS logic circuit operated at 14 volts is more immune to crosstalk than a similar circuit operated at 10 volts because of the different logic swings involved.

The results shown in Figs. 11 and 12 also provide a meaningful comparison between low- and high-state operation of the COS/MOS gates. In general, a greater noise immunity is achieved in the low state.

Although the test circuit shown in Fig. 10 yields reliable data, the measured values are not entirely representative of actual operating conditions. The circuit shown in Fig. 13

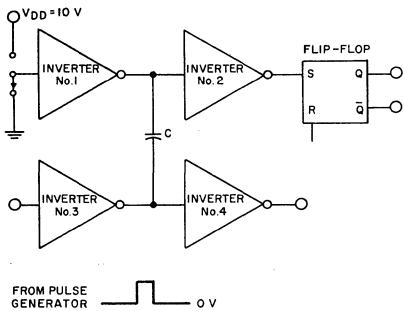


Fig. 13 - Test circuit used to determine crosstalk noise susceptibility.

more closely approximates crosstalk caused by adjacent signal lines. In this circuit, CD4001A gates are used as the driving inverters for the CD4013A flip-flop. The output of inverter No. 1 can be made either high or low for crosstalk tests in both logic states. The response of this test circuit to a noise pulse may be explained by analysis of the response of a high-pass RC circuit to a ramp input of  $V_i = at$ . The output voltage  $V_o$  may be expressed by the following equation:

$$V_o = \alpha \cdot RC \left( 1 - e^{-t/RC} \right) \quad (1)$$

The equivalent circuit for the part of the test configuration used in this analysis is shown in Fig. 14. On the basis of this equivalent circuit, Eq. (1) may be rewritten as follows:

$$V_{o_{\max}} \approx \alpha \left( Z_o // Z_{in} \right) C \left[ 1 - e^{-t/ \left( Z_o // Z_{in} \right) C} \right] \quad (2)$$

If  $V_i$  is assumed to be  $at$  (where  $t$  is the rise time) during the period in which the output voltage switches from 10 to 90 per cent of its total value, this change in output voltage can be expressed as follows:

$$\Delta V_{o_{\max}} \approx \frac{V_i \left( Z_o // Z_{in} \right) C}{t} \left[ 1 - e^{-t/ \left( Z_o // Z_{in} \right) C} \right] \quad (3)$$

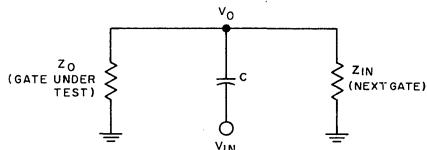


Fig. 14 - Equivalent circuit for noise analysis of the test configuration shown in Fig. 13.

The results of this analysis may be applied to the various crosstalk waveforms obtained. Fig. 15 shows photographs of  $V_o$  with the output of inverter No. 1 in the high state. Fig. 15(a) shows the crosstalk pulses obtained for the CD4001A COS/MOS gate for a capacitance  $C$  of 100 picofarads. Noise pulses are obtained only at certain time intervals which correspond to the rising and falling edges of the voltage  $V_i$ . Only the falling pulses are considered in the following analysis because they are responsible for triggering the flip-flop.

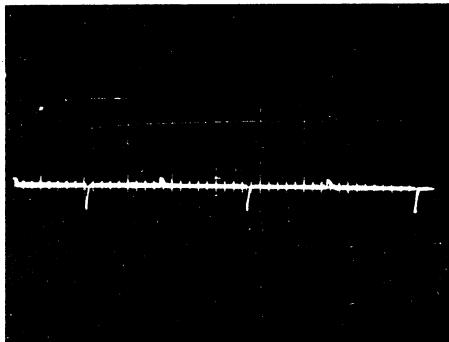
Eq. (3) may be used to calculate the amplitude of the pulses. The noise pulse introduced to the test circuit switches from 90 to 10 per cent of its final value in 17 nanoseconds (fall time). Because of the 100-picofarad capacitance  $C$  at the output of inverter No. 3, the fall time at this point should be somewhat greater than 17 nanoseconds. The actual measured value is 130 nanoseconds. In Eq. (3), therefore,  $t = 130$  nanoseconds,  $\Delta V_i = (0.090)(10) - (0.10)(10) = 8$  volts,  $Z_{in} \approx 10^12 \text{ ohms}$ ,  $Z_o \approx 550 \text{ ohms}$  (for the COS/MOS

integrated-circuit gate used), and  $C = 100$  picofarads. The output voltage swing  $\Delta V_{o\max}$  is then calculated as follows:

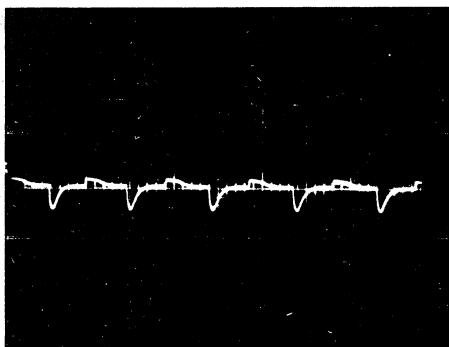
$$\Delta V_{o\max} \approx \frac{(8 \text{ V}) (550 \Omega) (10^{-10} \text{ F})}{130 \times 10^{-9} \text{ s}}$$

$$[1-e^{-\frac{130 \times 10^{-9} \text{ s}}{(550 \Omega) (10^{-10} \text{ F})}}] \\ = 3.1 \text{ V}$$

Fig. 15(a) shows that the measured value of the fall voltage (about 2.9 volts) is in close agreement with the calculated value. Fig. 15(b) shows the crosstalk pulse for the same COS/MOS circuit with a noise pulse rate of 500 kHz rather than 54 kHz. As Eq. (3) implies, the pulse rate does not seem to change the noise amplitudes.



(a)



(b)

Fig. 15 - "1"-state crosstalk waveforms: (a) frequency = 54 kHz, pulse width = 5  $\mu\text{s}/\text{cm}$ , and pulse amplitude = 5 V/cm; (b) frequency = 500 kHz, pulse width = 1  $\mu\text{s}/\text{cm}$  and pulse amplitude = 5 V/cm.

In the low state, the output impedances of the COS/MOS logic circuit are low enough (550 ohms) and the rise times sufficiently slow that the flip-flop could not be triggered at any value of capacitance used (up to 10 microfarads).

Crosstalk measurements that simulate actual operation are made by use of the test circuit shown in Fig. 16. In this

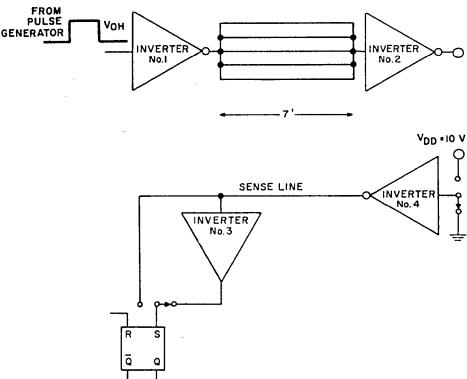


Fig. 16 - Crosstalk test circuit which uses tightly coupled cable to simulate actual operating conditions.

circuit, a sense line is placed tightly within five surrounding wires (No. 22 gauge) to form a 7-foot-long cable which has a capacitance of 30 picofarads per foot (determined by measurement). The cable is used to simulate a worst-case cable with 5 gates switching on lines adjacent to one wire. The results of this test are shown by the photographs in Figs. 17 and 18. Fig. 17 shows the effect of the capacitive loading

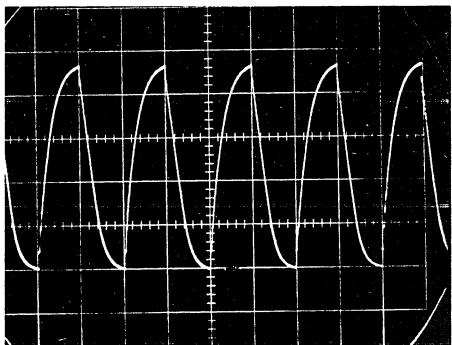
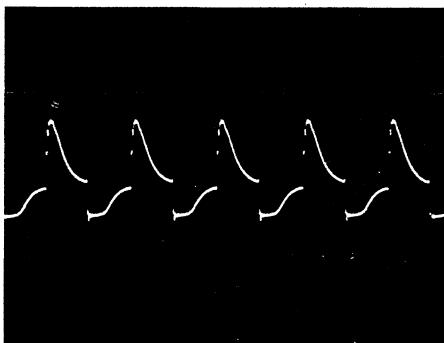
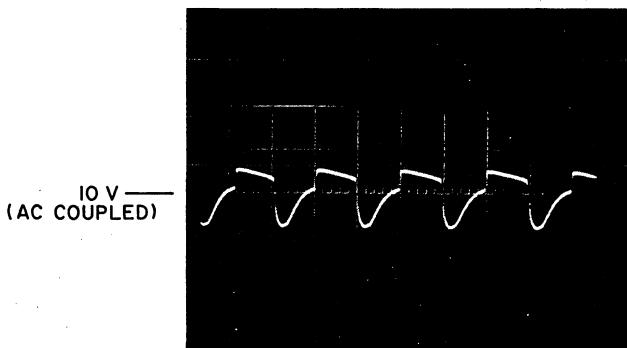


Fig. 17 - Crosstalk waveform showing effect of load capacitance (output of CD4001A inverter No. 3; frequency = 500 kHz, pulse width = 1  $\mu\text{s}/\text{cm}$ , and pulse amplitude = 2 V/cm).



(a)



(b)

*Fig. 18 - Crosstalk waveforms for (a) "0" state and (b) "1" state (frequency = 500 kHz, pulse width = 1  $\mu$ s/cm, and pulse amplitude = 1 V/cm for "0" state waveforms or 0.2 V/cm for "1"-state waveforms).*

on the fall time of the inverted output waveform. Fig. 18 shows the "0"-and "1"-state crosstalk coupled to the sense line. In both cases, the forward crosstalk, or noise, at the receiver end of the cable (the input to inverter No. 2 in Fig. 16) matched back crosstalk, or noise at the driver end of the cable (the output of inverter No. 1). The crosstalk does not trigger the flip-flop in either the "0" or "1" state. Even with a tightly coupled 7-foot cable, the COS/MOS gate does not change state falsely.

## CONCLUSIONS

The results of all tests show exceptionally high noise immunity for COS/MOS integrated-circuit gates. Typical noise-immunity values range from 4.5 to 5.5 volts for a supply voltage  $V_{DD}$  of 10 volts, and 5.5 to 8.5 volts for a

$V_{DD}$  of 14 volts. These high values are achieved with gate power consumptions in the microwatt range, as compared with much higher (milliwatt) consumptions and much lower noise immunities (about 1 volt) for saturated bipolar logic. Factors contributing to the high noise immunity of COS/MOS gates are the relatively slow speeds and relatively low (500 ohms) output impedances.

Because it is impossible to study all cases of noise immunity, the cases chosen are meant only to be representative. Noise pulses are certainly not all rectangular in shape, and the same type of integrated circuit may have widely differing characteristics. It is hoped, however, that enough information is presented to permit generalization to other cases not specifically studied.

## A Typical Data-Gathering & Processing System Using CD4000A-Series COS/MOS Parts

by D. Block

### INTRODUCTION

The broad line of COS/MOS standard parts in the CD4000A series,<sup>1</sup> including many MSI functions not available in other logic families, provides the design engineer with the tools to implement a large number of digital functions. The well-known characteristics of COS/MOS circuits,<sup>2</sup> such as low power dissipation, wide supply-voltage range, high noise immunity, and excellent temperature stability, can make possible cost-effective systems for a variety of applications, and have opened up new areas where electronic controls were not previously suitable for a variety of reasons.

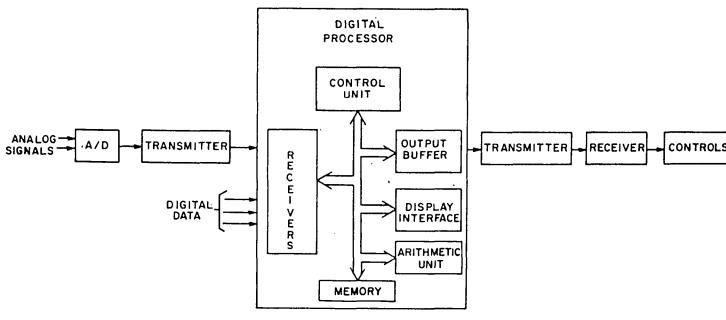
This Note considers the area of data gathering and processing, and is developed in terms of a typical system for process controls. Emphasis is placed on applications of the newer parts in the CD4000A line. Also stressed are the flexibility of system design and common data-bus architecture made possible by the three-state outputs and bidirectional input/outputs incorporated in many COS/MOS circuits and the ease of system design for data handling in increments of 4 bits made possible by the careful planning of the CD4000A family.

The implementation of the system described is shown in terms of the COS/MOS standard parts which can be used to perform the desired system functions. Specific details, such as pin numbers, are not provided; rather attention is focused on the multiplicity of applications which can be handled by a single product and the scope of information processing which can be covered by standard parts.

The fine points of circuit design, which would have to be dealt with in any real-world design, are not treated here. The approach adopted is one of "filling in the blocks" to show which COS/MOS standard parts can be used to implement a particular function, and how these blocks tie together to create a system.

### SYSTEM DESCRIPTION

The over-all system described is one which accepts asynchronous inputs of analog or digital data and operates on that data; the output is display and control information. Fig. 1 shows a block diagram of the entire system. It is assumed that the input signals from remote sensors are digitally encoded and transmitted to the central Processor Unit for data manip-



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Fig. 1 – Block diagram of the Data-Gathering and Processing System.

lation. It is also assumed that the controlled functions are at a distance from the **Processor** and that data is transmitted from the **Processor** to the **Controller** by frequency-modulation techniques. At the **Controller**, data is reconstructed to an NRZ data-word format which can then be used for direct digital control or converted to an analog voltage for proportional control of servos, etc.

The display output at the **Processor** is a 4-digit, liquid-crystal display located in reasonable proximity to the rest of the logic. Thus, the areas to be considered for COS/MOS implementation include A/D and D/A conversion, data transmission and reception, and data processing. Serial-to-parallel and parallel-to-serial conversion are included since a common data bus architecture is assumed in the **Processor Unit**.

Two power supplies, +10 volts and -5 volts, are used in the system. All COS/MOS parts require only a single power supply and single-phase clock, and logic levels in the system will be from  $V_{SS} = 0$  volts to  $V_{DD} = 10$  volts. However, the negative supply can be used to advantage, as examples in this Note will show, to permit transmission of signal levels above and below ground, and to develop 15 volts across the liquid-crystal display for good readability.

#### INPUT SIGNAL CONDITIONING AND TRANSMISSION

Fig. 2 shows the conversion of analog input voltages to a serial-data stream. The CD4051A's are used as multiplexers to connect, one at a time, each of the 16 analog input voltages to the A/D converter. When the conversion is completed, a signal from the converter gates an oscillator ON which causes the 8-bit result of the A/D conversion to be multiplexed into a serial-data stream. This data, along with a clock, is transmitted to the **Processor Unit**. A CD4047A used in the negative-trigger, astable mode provides a reset pulse to the A/D converter on the negative transition of Q3. The pulse indicates that the 8-bit data stream has been transmitted and that the input multi-

plexer has been stepped to the next address. By taking advantage of the capability of the CD4051A's to operate from two power supplies, analog voltages above and below ground can be switched by control-signal inputs of 0 to 10 volts. Note that the CD4051A is suitable for both analog and digital multiplexing applications and that, because of the Inhibit input, which entirely disconnects the common outputs, two or more units can be wire-OR'ed.

The A/D converter can also be assembled with COS/MOS standard parts, as shown in Fig. 3(a). The CD4040A binary counter, used in conjunction with an R/2R resistor ladder network, generates a staircase ramp at the negative input to the comparator as shown in Fig. 3(b). When the ladder voltage matches the analog input, the comparator output goes low. This signal is inverted by the CD4007A and becomes a logic 1 latched into the flip-flop. This action inhibits additional clocks to the counter and indicates that the conversion is complete. The output of the counter, which is buffered by high-current CD4041A's to minimize switch impedance effects on the resistor ladder, is the digital equivalent of the analog input voltage. A reset clears the flip-flop and resets the counter so that the next conversion can begin.

To generate a staircase from -5 volts to 10 volts, one end of the resistor ladder is connected to -5 volts, and the counter is connected with a  $V_{DD}$  of 10 volts and a  $V_{SS}$  of -5 volts. Since the clock and reset signals to the counter must then swing from -5 volts to 10 volts, a CD4054A is used as a level translator.

A micropower op-amp, the CA3080A, is used as a voltage comparator for the D/A converter. The op-amp is gated off after the conversion is completed by turning off a p-device of the CD4007A supplying bias current to the unit. In this way, power dissipation is reduced to a few microwatts in the standby state during those times in which a conversion is not actually being performed. With the active bias current ( $I_{abc}$ ) set at 15 microamperes, typical power dissipation for the CA3080 is

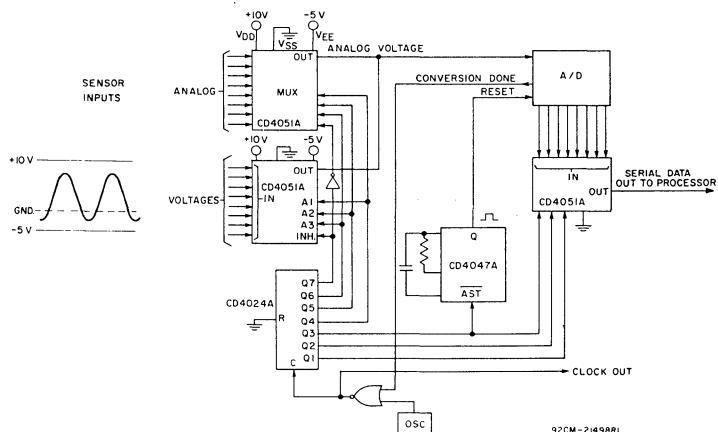


Fig. 2 – The conversion of analog input voltages to a serial-data stream.

about 500 microwatts with a  $V_+$  of 10 volts and a  $V_-$  of -5 volts. Dissipation during a conversion would be approximately 20 milliwatts at a clock rate of 100kHz for the circuit shown in Fig. 3. Standby dissipation, however, would typically be less than 50 microwatts. Care must be taken not to exceed the common-mode input voltage of the op-amp.

#### DIGITAL PROCESSOR UNIT

A block diagram of the Processor Unit is shown in Fig. 4. Four internal bus systems are used. The Control Bus carries discrete control and timing signals from the Control Unit to the various sub-units; the other three bus systems are 8-bit, parallel transfer buses. The Memory Bus (M) carries memory

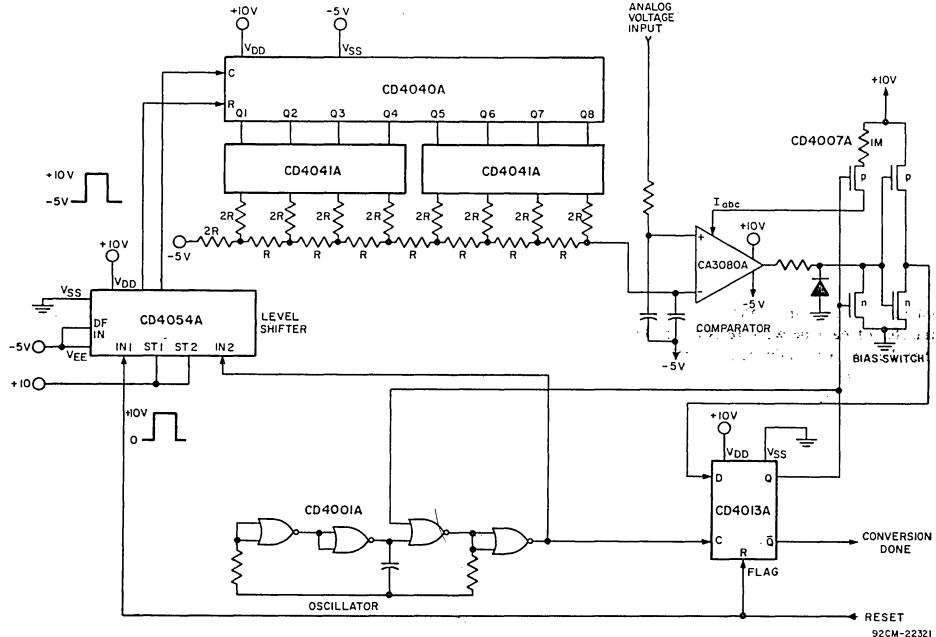


Fig. 3 – (a) The A/D converter assembled with COS/MOS standard parts, (b) staircase ramp generated by the CD4040A binary counter.

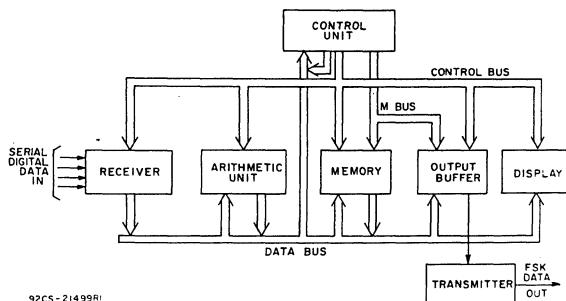


Fig. 4 – Block diagram of the Processor Unit.

address information from the **Control Unit** to the **Memory** and **Output Buffer**, while the **Data Bus** (D) is used for common data transfers between all subsystems. The third parallel bus is internal to the **Arithmetic Unit** and is used for high-speed transfer of data between registers in that unit. It is assumed that, because of bandwidth limitations, data input and output rates are asynchronous with respect to the system internal clocking and, therefore, that the I/O's are interfaced with the D bus under command of the **Control Unit**.

#### RECEIVER

Fig. 5 shows the **Receiver** portion of the **Processor**. A CD4034A is used in the serial-in/parallel-out mode for data serial-to-parallel conversion, and also functions as a holding register for input data until the **Control Unit** calls for it to be strobed onto the D bus. A CD4017A associated with each register counts input clocks and, when output number "8" goes high, indicates that its associated register is full. A scanner, consisting of a CD4052A dual-4-channel multiplexer,

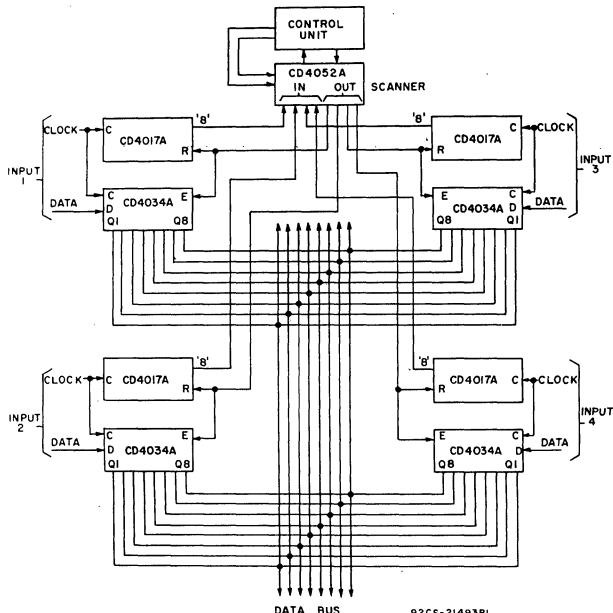


Fig. 5 – Receiver portion of the Processor.

sequentially examines each counter and reports to the Control Unit when any register is ready to be read out. A pulse from the Control Unit back through the CD4052A resets the counter and strobes the appropriate register onto the D bus.

## MEMORY

The Memory portion of the Processor is shown in Fig. 6(a). Eight CD4061A's are paralleled to form the 8-bit

structure required for the D bus. A chip enable feature allows the Data Input and Data Output terminals of these units to be tied together since both are disconnected when the Chip Enable input is high. (The Chip Enable input must be high prior to any change of address.) The Read/Write control determines whether parallel data will be written from or read onto the Data Bus when the memory is enabled. With reasonable capacitive loading, read access times of about 400 nano-

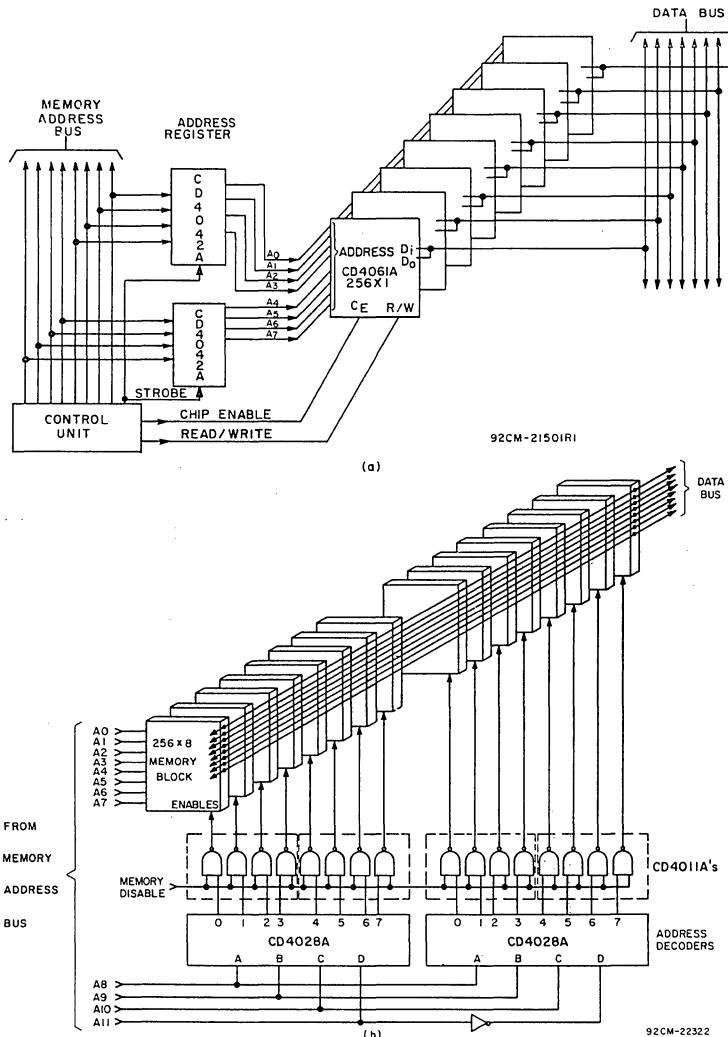


Fig. 6 – (a) Memory portion of the Processor, (b) an expanded memory organization to 4096 words.

seconds are achievable. The CD4042A's, which are quad-coded latches, are used as a memory address register.

An expanded memory organization to 4096 words is shown in Fig. 6(b). Here the eight-package organization of Fig. 6(a) is taken as a basic building block and repeated 16 times. Four more address bits on the M Bus can be decoded into 16 discrete block-enabling signals by using a CD4028A. The decoded outputs must be inverted to provide the "low" enabling signal required by the CD4061A memories. The entire memory can be disabled, i.e., effectively disconnected from the D Bus, by maintaining the Memory Disable signal low.

The memory could be used in this system to store programming instructions for the **Control Unit**, parameter limits against which new inputs are to be compared, instruction words which are to be sent to the remote controller, etc.

### ARITHMETIC UNIT

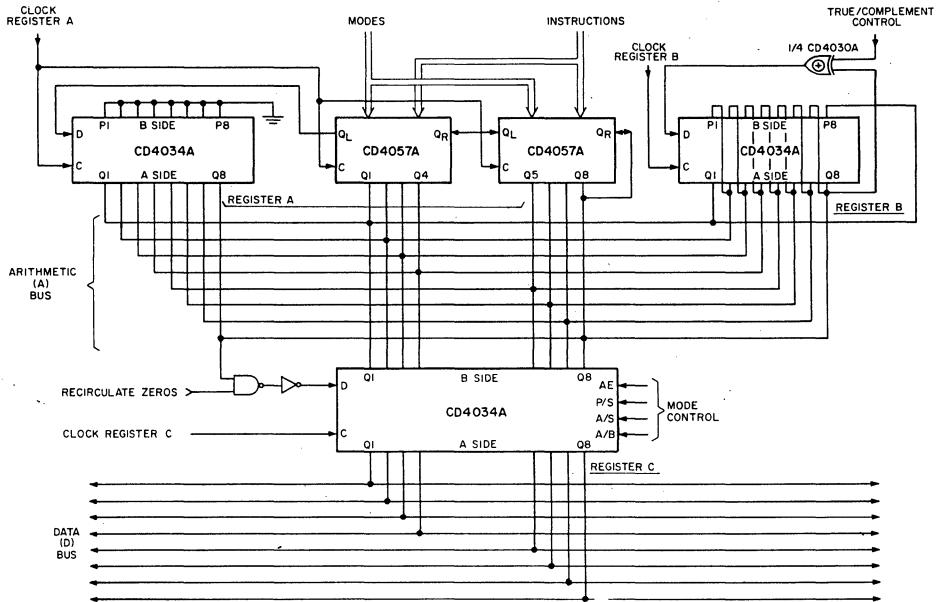
An extremely flexible **Arithmetic Unit** can be configured by using two CD4057A 4-bit arithmetic arrays and three CD4034A shift registers, as shown in Fig. 7. The CD4057A's have a 16-instruction repertoire, as shown in Table I. The addition of four operational modes which control transfer of information, either serial data or arithmetic carries, and the I/O control, makes the CD4057A a powerful tool for arithmetic operations. The results of these operations are fed back to the **Control Unit** of the D bus and overflow indicator, and are used to determine the next sequence of operations.

The bidirectional data input/output capability of the CD4057A's and CD4034A's enables units to be arrayed on their own **Arithmetic Bus A** and to communicate directly with all other subsystems.

Register A contains two CD4057A's for arithmetic operations and a CD4034A to allow left shifting of results as

**Table I — The 16-Instruction Repertoire of the CD4057A**

- NO-OP (Operational Inhibit)
- AND
- Count down
- Count up
- Subtract from zero (SMZ) (Stored number)
- Subtract from memory (SM) (Stored number from memory)
- Add (AD)
- Subtract (SUB) (Memory from stored number)
- Set to one
- Clear to zero
- Exclusive-OR
- OR
- Input Data (From parallel data lines)
- Left shift
- Right shift
- Rotate (cycle) right



**Fig. 7 — The Arithmetic Unit.**

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would be required in a multiplication algorithm. Parallel data entry or access to the A bus is possible for the shift register from the A side of the CD4034A. When all inputs on the B side are grounded, the shift register can be reset by performing a parallel-input operation on the B side.

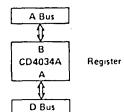
Register B is a general-purpose register which could be used to hold intermediate results, a multiplicand, or for shift-right expansion of register A. With the configuration shown, i.e., with the output of Q8 connected to the input of Q7 and so forth, register B can be made to shift left as well as right, its normal mode of shifting. Left shifting is accomplished by enabling synchronous data entry on the B side and clocking the register. The addition of a CD4030A exclusive-OR gate causes the register to be complemented when the True/Complement Control signal is high and data is right shifted around once. With the control signal low, data is recirculated without modification. Here again, the three-state outputs on the A side of the B register allow parallel or serial data transfer to and from the A bus.

The C register is used as an interface buffer between the A and D buses and for data storage or right-hand expansion of the A register. Table II shows the modes of operation for buffering and the required control-signal levels. The one mode which is not realizable directly from Table II could be accomplished by putting two CD4016A transmission-gate packages between the B side of the CD4034A and the A bus. Register C can be cleared by setting the Recirculate-Zeros control-line low and shifting data around once. Of course, a parallel entry of zeros from either the A or D bus would also serve as a reset for this register.

## DISPLAY OUTPUT

The display unit for numerical outputs is shown in Fig. 8. The CD4056A is used as interface with a 4-digit liquid-crystal display, the TA8054R. Each CD4056A contains a 4-bit latch, a BCD-to-7-segment decoder, level shifters, and display drivers. When a square wave is applied to the Display-Frequency input of the CD4056A and as a common to one side of the display, the selected segment outputs consist of a square wave  $180^\circ$

**Table II — Modes of Operation for Buffering and the Required Control-Signal Levels for the C Register**



	Control Lines				
	AE	A/B	A/S	P/S	C
1. Input from D, disconnect from A*	-	-	-	-	-
2. Input from D, connect to A	H	H	H	H	L
3. Disconnect from D, connect to A	L	H	H	H	
4. Disconnect from D, disconnect from A	L	L	L	X	
5. Input from A, disconnect from D	L	L	H	H	
6. Input from A, connect to D	H	L	H	H	
7. Disconnect from A, connect to D	H	L	L	H	
8. Disconnect from A, disconnect from D	L	L	L	X	

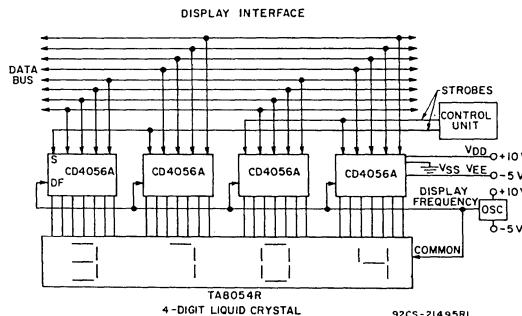
\*Note:

These "A's" refer to the A (Arithmetic) Bus, not to the "A side" of the CD4034A.

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out of phase with the common. The signal causes the appropriate segment to become visible. Unselected outputs are in phase with the common, and the appropriate segment is then not visible. The two voltage-supply terminals of the CD4056A permit a higher voltage to be used across the display than appears on the control inputs to the device and allows for maximum contrast ratio on the display. At 15 volts and a frequency of 60 Hz, typical operating current for the display is only 125 microamperes.

Assuming that the normal data-bus information is in standard binary notation, conversion to BCD for the display can be handled in the Arithmetic Unit by using the Couleur 3 technique or hard-wired, IC-implemented schemes.<sup>4,5</sup> Since the D bus is 8 bits, two transfers are necessary to display all 4 digits.



**Fig. 8 — Display unit for numerical outputs.**

## OUTPUT BUFFER

The **Output-Buffer** circuitry, shown in Fig. 9, is realized by using a memory in a parallel-write/serial-read mode. The CD4051A is used as a multiplexer to enable one CD4061A memory circuit at a time when the Read/Write control line is low (for Read) and the Inhibit input of the CD4051A is also low. If the Inhibit input were high in the read mode, then all multiplexer outputs would be off since, with both inputs low to each gate, all NOR outputs will be high, and the memory will be disabled. Note that pull-down resistors are used to define a logic 0 level to the NOR gate since the tri-state outputs of the CD4051A would otherwise leave those inputs floating. Whenever the Read/Write control line goes high, all NOR gate outputs will be forced low and a parallel Write operation will be enabled.

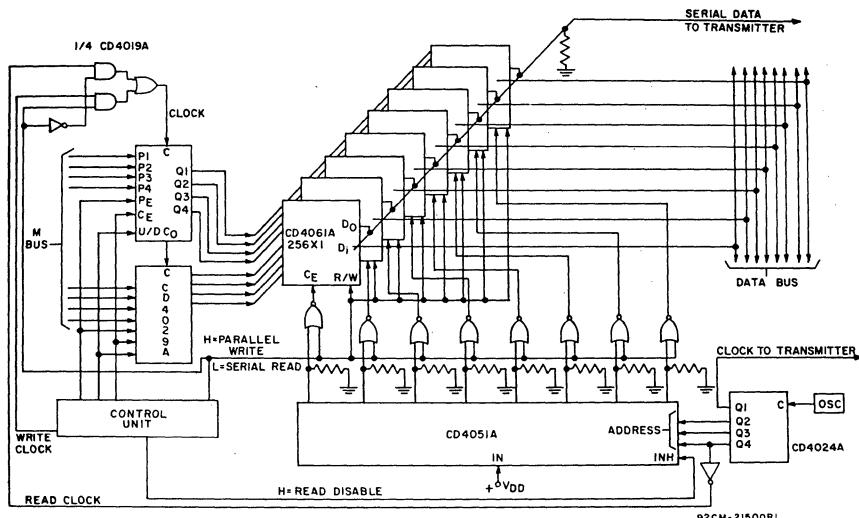
For the greatest flexibility in this buffer application, CD4029A up/down presetable counters have been used for the address register. A starting address is strobed into the register by using the Preset Enable inputs of the CD4029A's. The clock is then enabled to provide a serial-memory readout where the address is automatically advanced or decremented at a rate suitable for the transmission medium. A faster clock can be used to fill the memory initially from the D Bus in the Write Mode. A CD4019A AND/OR select gate is used to switch between the two clocks. By disabling the clock entirely, the CD4029A can be made to perform as a simple, 4-bit latch to randomly access any particular memory location.

As an example of the use and operation of the entire Control Unit, consider the case where one of the system

analog inputs represents water pressure being monitored in a pipe. The digitized pressure reading would be entered into the **Arithmetic Unit** and then subtracted from a maximum or minimum limit number brought from memory. In addition, the present reading could be compared against the last reading stored in memory and the result compared with yet another stored parameter to determine whether the difference in two readings lay within expected bounds. A rapid pressure drop, for instance, could indicate a leak in the line and would require a warning message to be generated and special action to be taken by the controls.

## OUTPUT TRANSMITTER

The Transmitter portion of the system, shown in Fig. 10(a), consists of an NRZ-to-biphase data converter (CD4037A) and a VCO (CD4046A), so that output data will be in the form of biphase FSK. This type of modulation is preferred in many applications since one zero-crossing is generated during each bit period; this arrangement simplifies clock recovery. However, this technique is relatively wasteful of bandwidth. The CD4037A generates biphase data, as shown in Fig. 10(b), when supplied with a clock and clock at twice the bit rate. The output of the circuit is used to control a transmission gate (CD4016A) which switches R3 in parallel with R2, thus changing the input voltage to the VCO. The VCO output, then, is two discrete frequencies determined by the ratios of R1 and R2 for a logic 1 and R1 to R2/R3 for a logic 0.



*Fig. 9 – Output-Buffer circuit.*

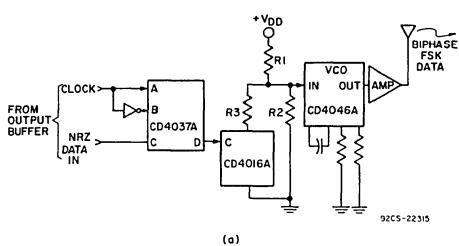


Fig. 10 – (a) Transmitter, (b) biphase data generated by the CD4037A.

## RECEIVER

The block diagram of the **Receiver** is shown in Fig. 11(a). After amplification, the FSK signal is detected in a phase-locked loop using the CD4046A and a threshold detector (Fig. 11(b)). Clock and data reconstruction is accomplished by the circuit shown in Fig. 11(c).

The flexibility of COS/MOS devices is demonstrated in Fig. 12 in which an op-amp circuit that can be used to amplify the incoming signal to the **Receiver** is configured. The op-amp consists of two CA3600E packages, which are CD4007A units specially tested for linear applications, and one CA3046 bipolar-transistor array. This circuit is unusual in that it is responsive to small-signal, ground-referenced inputs, and the output stage can easily be driven to within 10 millivolts of  $V_{DD}$  or  $V_{SS}$  when  $R_L$  is very high.

In Fig. 11(b), the phase-locked loop locks onto the incoming frequency. The voltage controlling the VCO then assumes two discrete values corresponding to whether the loop is locked onto  $f_1$ , representing a binary 1, or  $f_2$ , representing a binary 0. A Schmitt trigger, constructed of a CD4007A and used here for threshold detection, discriminates between the two voltages and produces a clean 1 or 0 output. This action completes the demodulation of FSK into a biphase data stream.

The next step is to reconvert the data in the biphase data stream to the original NRZ and recover the clock signal; Fig. 11(c) shows how this can be done. The biphase data (A) is

differentiated to mark the locations of data transitions. This differentiation provides a reference frequency at twice the bit rate of the phase-locked loop. However, some of the pulses will be missing where transitions occurred in the original data stream (B). To provide a reliable clock, the VCO is forced to

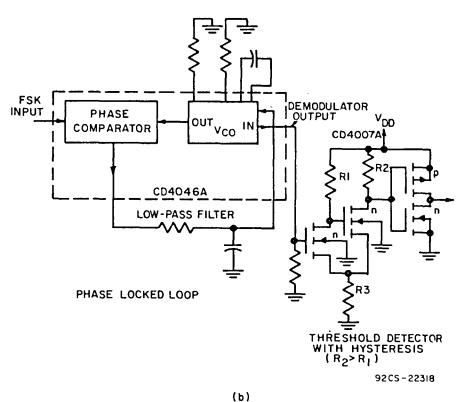
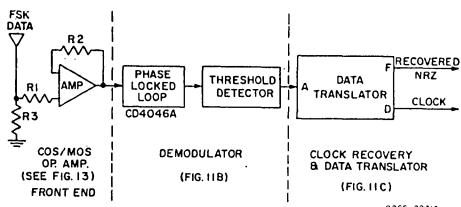


Fig. 11 – (a) Receiver, (b) phase-locked loop consisting of a CD4046A and a threshold detector, (c) circuit for clock and data reconstruction.

run at twice the bit rate by FF1, which divides the VCO output by two before returning it to the phase comparator (D). The differentiated signal is gated such that only every other pulse is permitted through to the phase comparator (C). In this way, the PPL does not see the missing pulses, and the VCO output remains constant at twice the bit rate. FF2 provides the necessary 90° phase shift to generate a clock signal for incoming data (E). The output of FF3 is the recovered binary information (F). Initial synchronization of the system is accomplished by preceding actual data transmission with a string of alternating 0's and 1's.<sup>6</sup>

Typical data rates up to 600 kHz can be realized within the frequency range of the VCO incorporated in the CD4046A with the VCO operating at 10 volts.

### CONTROL UNIT

Binary information recovered at the **Control Unit** can be used directly to control on/off functions by a particular bit in the data word, or a complete word can be converted to an equivalent analog voltage for proportional control of servos, for example. An A/D converter realizable with COS/MOS standard parts is shown in Fig. 13. In a configuration analogous to the **Receiver** portion of the **Control Unit**, a data word is clocked into a CD4034A register and, after all 8 bits have

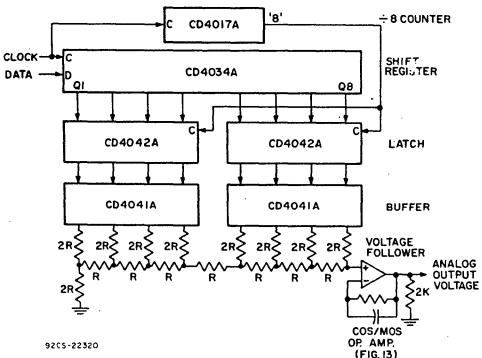
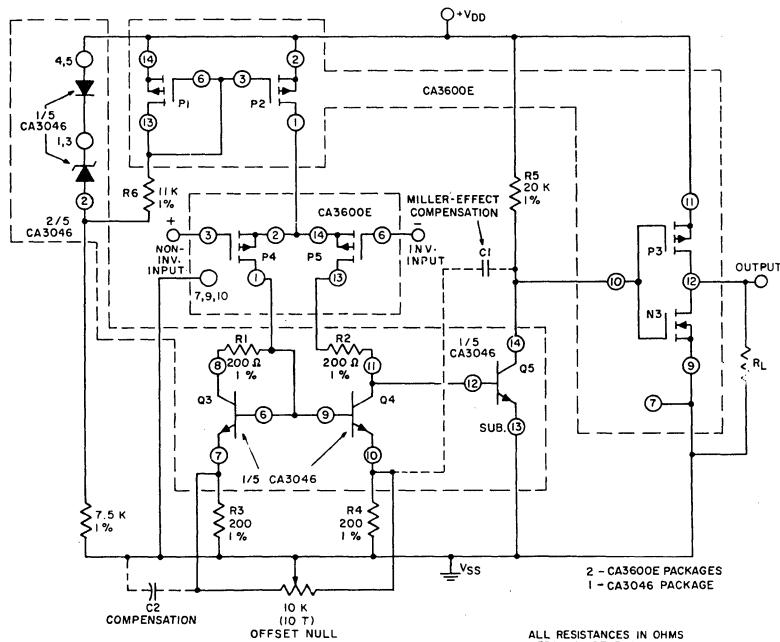


Fig. 13 - A D/A converter that can be made up of COS/MOS standard parts.

been received, the output of a CD4017A (connected in a divide-by-8 mode) strobes the word into a CD4042A holding register. Register outputs are buffered by CD4041A's to an R/2R resistor ladder and a voltage follower. The COS/MOS op-amp shown in Fig. 12 can be used as the follower.



## SUMMARY

The wide range of logic functions available as standard parts in the ever-expanding CD4000A line provides the design engineer with the building blocks for a wide variety of digital functions. Complex logic functions realized on a single IC permit the designer to think in large-scale system terms. The flexibility of design made possible by such features as bi-directional inputs and outputs and three-stage logic results in a minimum package count, even for complex systems. These features, coupled with the well-known advantages of COS/MOS circuits in the areas of noise immunity, low power, high fanout, power-supply tolerance, temperature stability, and off-the-shelf availability of parts for both bread-boarding and production, make a very attractive combination for the designer.

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## Gate-Oxide Protection Circuit in RCA COS/MOS Digital Integrated Circuits

by R.R. Painter

One of the most frequently encountered handling and testing problems with early MOS devices was failure of the gate oxide. Although this problem existed during handling and testing of devices prior to their installation in a circuit (because normal circuit impedances and voltages make damage of this nature less likely), a solution to the problem was necessary to reduce failure of MOS devices and integrated circuits during manufacture, reliability testing, shipping, incoming inspection, and assembly by equipment designers.

The breakdown voltage of an MOS gate oxide is generally in the order of 70 to 100 volts, and the dc resistance is in the order of  $10^{12}$  ohms. In contrast to other semiconductor diodes, in which the breakdown can be tested any number of times without damage, the MOS gate oxide will be shorted as a result of only one voltage excursion to the breakdown limit. Because of the extremely high resistance of the gate oxide, even a very-low-energy source (such as a static charge) is capable of developing this voltage.

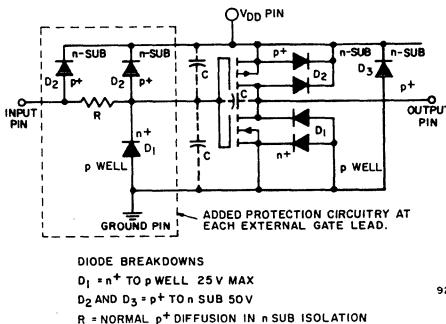
Fig. 1 shows a protection circuit developed by RCA which is incorporated in COS/MOS integrated circuits to minimize this problem. The results to date have shown that this approach is effective in minimizing occurrences of gate-oxide

failure; when the handling guidance contained in ICAN-6000\* is followed, the problem is eliminated.

A value of 200 to 2000 ohms (depending on design and process variations) is used for the input resistor R in Fig. 1. This value is chosen, in conjunction with the capacitance of the gate and the associated protective diodes, to integrate and clamp the device voltages at a safe level. The diagrams shown in Fig. 2 demonstrate that the input circuit limits extraneous voltages to safe levels for all operating conditions. Because of its low RC time constant, this network has no noticeable effect on circuit speed.

Because of the presence of this integral protection circuit, the  $V_{DD}$  power supply should not be turned off while a signal from a low-impedance generator is applied at an input of a COS/MOS integrated circuit. If the  $V_{DD}$  supply is turned off while a low-impedance pulse generator is connected to an input, the  $V_{DD}$  line is essentially grounded and a positive voltage from the pulse generator is impressed across diode  $D_2$ . This voltage of up to 15 volts can cause permanent damage to the diode or can burn out the  $V_{DD}$  metallization. If any input excursion exceeds  $+V_{DD}$  or goes below  $-V_{SS}$ , the current through the input diodes should be limited to 10 milliamperes for safe operation.

\* "Handling Considerations for MOS Integrated Circuits"



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Fig. 1 - Gate-oxide protection circuit used in COS/MOS integrated circuits.

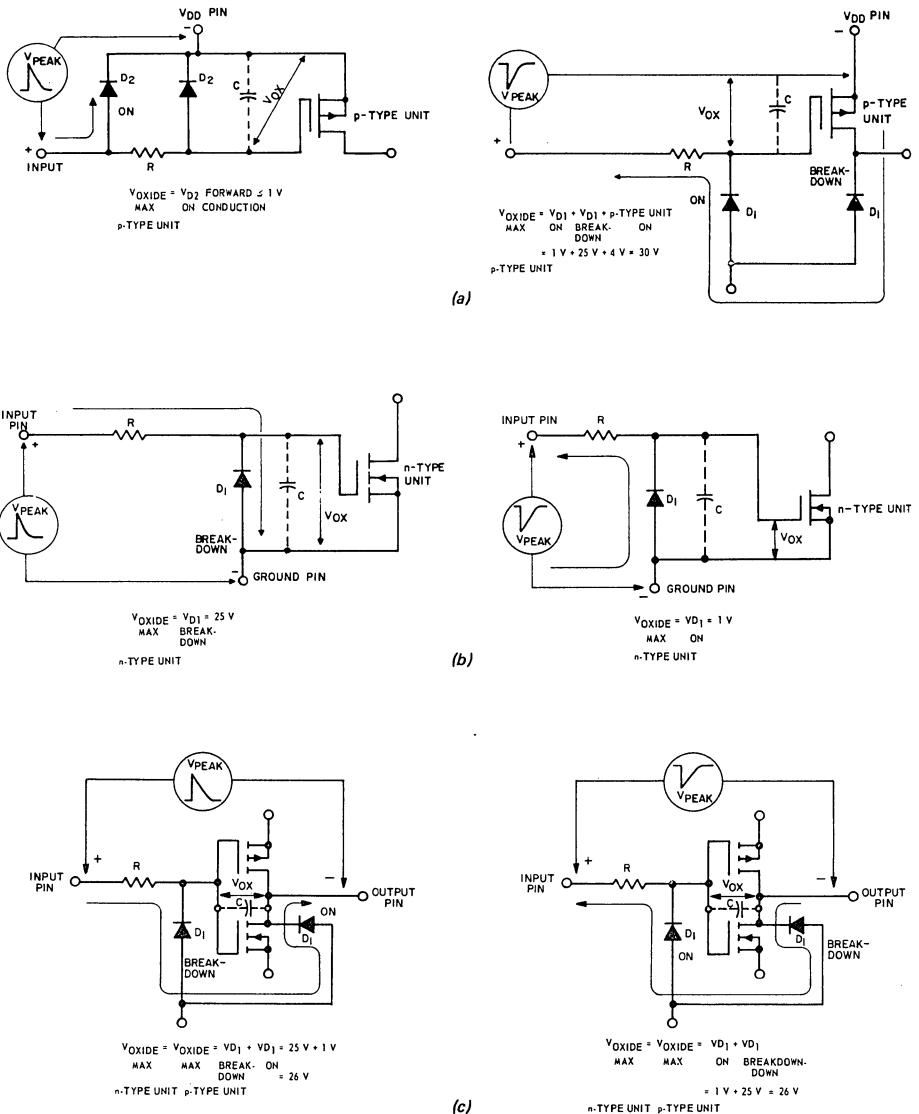


Fig. 2 - Circuits used to provide: (a) protection between input pin and  $V_{DD}$  pin;  
(b) protection between input pin and ground pin; (c) protection between input pin and output pin.

## Radiation Resistance of the COS/MOS CD4000A Series

by M. N. Vincoff

Complementary MOS (COS/MOS) integrated circuits possess many advantages which recommend their use in radiation-susceptible space and military environments. Several of the most significant of these advantages are: ultra-low standby-power consumption, high noise immunity,<sup>1</sup> extremely high packaging density, and inherently high reliability.<sup>2</sup> These advantages, along with the improved radiation resistance of the RCA CD4000A series over the CD4000 series described in earlier radiation studies,<sup>3</sup> exhibit the maturity reached by the MOS technology since 1971.

A number of studies of the radiation resistance of complementary MOS devices by NASA, the Navy and various companies in the space industry have revealed two areas of prime concern.<sup>4-15</sup> The first, *permanent* radiation exposure, as experienced in a space environment, causes a shift in threshold or switching voltage and a possible increase in leakage current,  $I_L$ . The second, *transient* radiation exposure, as experienced in an atomic environment, causes the output-voltage levels to respond to a pulse of ionizing radiation; this effect could change the state of the logic circuitry and require resetting of that circuitry for proper equipment or system operation.

### Permanent-Radiation Resistance

The CD4000 series was resistant to permanent radiation levels of  $2 \times 10^4$  rads (approximately  $10^{12}$  e/cm<sup>2</sup>). Now, however, RCA CD4000A-series devices without special shielding have been found to be resistant to radiation levels up to  $2 \times 10^5$  rads (approximately  $10^{13}$  e/cm<sup>2</sup>), as shown in Fig. 1.<sup>3</sup> In this figure the change in switching voltage  $\Delta V_S$  is plotted as a function of dose. The value of  $\Delta V_S$  was calculated from the average value of  $\Delta V_{TN}$  and  $\Delta V_{TP}$  for the devices mentioned. The new radiation level of the CD4000A series represents a significant improvement over the CD4000 series. In addition, with minimal shielding (for example, 1/16-inch of aluminum) the CD4000A series can be used in application with levels of radiation up to  $3 \times 10^6$  rads (approximately  $10^{14}$  e/cm<sup>2</sup>).

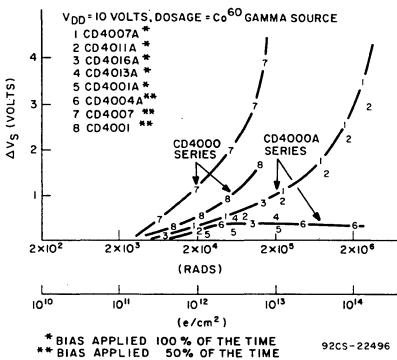


Fig. 1 – Permanent radiation resistance of CD4000A- and CD4000-series devices.

### Transient-Radiation Resistance

The resistance of the CD4000A series to transient radiation is expected to be ten times better than that of the CD4000 series, which can withstand pulses of radiation of approximately  $10^{10}$  rads/s.<sup>5</sup>

### Design Considerations

The resistance of the CD4000A-series devices to either permanent- or transient-radiation exposure can be increased by providing either minimal shielding through the design of the equipment enclosure containing the devices or by locating the devices deep within the equipment in which they are used. In any case, the action taken will depend on the constraints dictated by the radiation environment imposed by the system or program. Each application must be tested and the results analyzed with the data in this Note as criteria. Test items to be considered are radiation environment, which

will vary greatly depending on dosage rate; time of exposure; amount of normal shielding; distance of the device from the radiation source; shielding afforded by the atmosphere; power-supply voltage selection; and switching cycles used during exposure. For example, consider the effects of permanent radiation on two spacecraft in 90-degree orbits at 600 and 1500 nautical miles from the earth, respectively. The dose-depth is determined as shown in the curves of Fig. 2. In these curves the dose in rads(A<sub>1</sub>)/day is plotted as a function of the thickness of spacecraft aluminum required to shield the devices from trapped electrons and protons.<sup>4</sup>

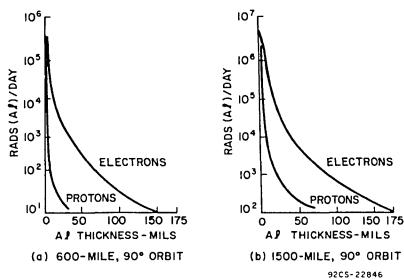


Fig. 2 – Dose-depth curves for trapped electrons and protons in space-craft in orbit.

### Conclusion

The RCA COS/MOS CD4000A series exhibits improved radiation resistance over the CD4000 series, and is well suited for use in many applications in which permanent and transient radiation effects are factors. When stringent radiation requirements are imposed, additional shielding can be employed to increase the radiation life of COS/MOS CD4000A-series devices to any desired level, i.e., to make their radiation resistance equivalent to that of bipolar devices.

Custom COS/MOS devices that can resist a radiation level of  $10^6$  rads are now being developed by means of an aluminum implantation process which requires one additional masking step in the production line.<sup>11-14</sup>

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## Using the CD4047A in COS/MOS Timing Applications

by J. Paradise

Many applications exist today for COS/MOS multivibrators—both oscillators and one-shots—in analog and digital circuits. The requirements for these applications vary widely in such parameters as voltage range, temperature stability, power dissipation, drive capability, and external-component cost. No design is optimum for all of the above considerations. However, the RCA-CD4047A Monostable/Astable Multivibrator fulfills the needs of most applications in this timing area. It can function as either an oscillator or one-shot with many additional features, and will meet the power dissipation, stability, and speed requirements of most COS/MOS systems.

This Note compares some simpler types of oscillator circuits with the CD4047A in both theoretical and actual performance, and provides application information on the CD4047A which should prove useful to COS/MOS circuit and system designers.

### COS/MOS DISCRETE RC OSCILLATOR

The simplest type of RC-oscillator is shown in Fig. 1. It consists of two inverters (which may be taken from standard

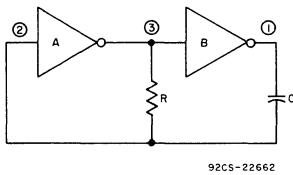
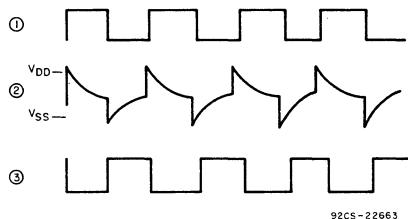


Fig. 1 — Simplest COS/MOS RC oscillator.

RCA COS/MOS parts, i.e., CD4007A, CD4001A, CD4011A, etc.) and a single resistor and capacitor. The operating waveforms for this circuit are shown in Fig. 2.

The circuit operates as follows: depending on the output levels of inverters A and B, at any instant C will be charging or discharging through R. When the waveform at point (2) in the circuit passes through the transfer voltage of inverter A, this inverter will switch and cause inverter B to switch. Subsequently, the waveform at point (2) would be exponentially



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Fig. 2 — RC-oscillator operating waveforms.

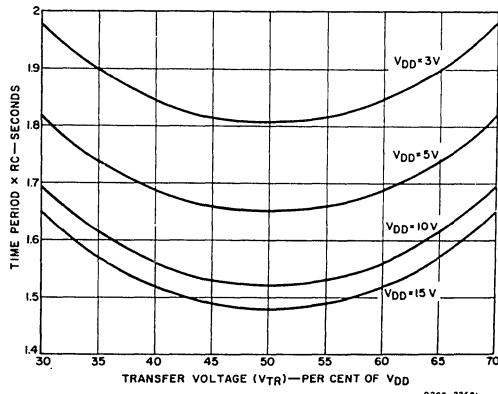
increasing or decreasing with discontinuities equal in magnitude to  $V_{DD}$  during the instant of switching. However, since point (2) is protected by a standard input-protection circuit common to COS/MOS devices, the waveform is clamped at one diode voltage drop above  $V_{DD}$  and below  $V_{SS}$ . (Refer to waveforms in Figs. 2 and A1). The calculations for the period of this multivibrator circuit are shown in Appendix A; the final equation for the period T is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \quad (1)$$

where  $V_{TR}$  is the switching or transfer point of the inverter, and  $V_D$  is the diode forward voltage drop.

Equation (1) shows that the period of the multivibrator, T, is sensitive to changes in  $V_{DD}$ , as illustrated by the graph of time period, T, vs transfer voltage as a function of  $V_{DD}$  in Fig. 3. In addition to the strong dependence of actual time period on the  $V_{DD}$  chosen, the graph also illustrates that, for a given  $V_{DD}$ , a full transfer voltage spread of 30 to 70 per cent of  $V_{DD}$  (unit-to-unit worst-case variations) yields a change in time period of about 10 per cent from the nominal 50-per-cent transfer-voltage percentage values.

The above analysis is valid only at low frequencies (i.e., less than 50 kHz). As the multivibrator frequency approaches this value, other considerations must be taken into account:



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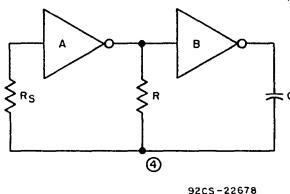
1. The input protection circuit has a  $V_{DD}$  diode with a finite resistance and capacitance; the diode will discharge at the rate associated with this small time constant.

2. In the negative direction, there is a diode as well as a series protection resistor (1 to 3 kilohms); the time constant of this diode is even longer than that of the  $V_{DD}$  diode.

3. The propagation delay of the inverters used is added to the time period during each charge and discharge cycle. Since the delay is a function of  $V_{DD}$ , small changes in  $V_{DD}$  at high frequencies will cause the time period to vary.

4. There is a finite output impedance associated with the inverter which is in series with the external timing resistor. Since this output impedance also changes with  $V_{DD}$ , at high frequencies where the external resistor becomes small, the multivibrator stability decreases with small variations in  $V_{DD}$ .

The negative features of the input protection circuit can be partially compensated for by the addition of a resistor,  $R_S$ , in series with the input protection circuit, as shown in Fig. 4. Although the input inverter A is still clamped at one diode drop above  $V_{DD}$  or one diode drop below  $V_{SS}$ , the waveform at point (4) is allowed to swing well above  $V_{DD}$  and below  $V_{SS}$ . The larger swing reduces the dependency of transfer-voltage variations upon stability; the variable characteristics of the input protection circuit and their effect upon stability are greatly reduced. An analysis of this circuit is presented in

Fig. 4 - RC-oscillator with the addition of  $R_S$ .

Appendix B; the equation for the period, T, for this circuit is shown in Eq. 2.

When  $K = \frac{R_S}{R}$ , T is:

$$\left. \begin{aligned} T &= -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2} \\ &= \frac{(K)}{(K+1)} RC \ln \frac{K[V_{DD} + V_D]}{K[V_{DD} + V_{TR}] + [V_{TR} - V_D]} \\ &= \frac{(K)}{(K+1)} RC \ln \frac{K[V_{DD} + V_D]}{K[2V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]} \end{aligned} \right\} (2)$$

In this form it is easy to see that when K approaches zero, the circuit and associated waveforms are equivalent to those of Fig. A-1. On the other hand, as K approaches infinity, the variation in period as a function of  $V_{DD}$  is reduced to zero. This result is shown in Fig. 5, where period as a function of trans-

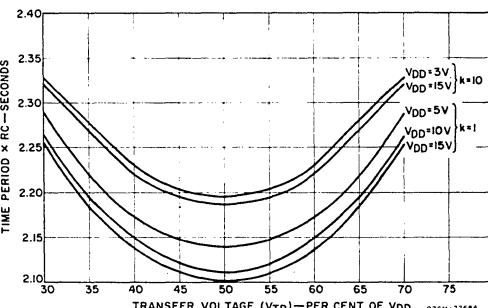


Fig. 5 - Discrete RC-oscillator time period as a function of transfer voltage.

fer voltage is plotted for different value of  $V_{DD}$  and K, and Fig. 6, which shows period as a function of K for different values of  $V_{DD}$ . Variation in period with transfer voltage is also reduced as K increases. This variation decreases from 10 per cent for K = 0 to about 5 per cent as K gets large.

There are some obvious limitations in the value of  $R_S$  that can be used. Besides the disadvantages in this circuit if R is to

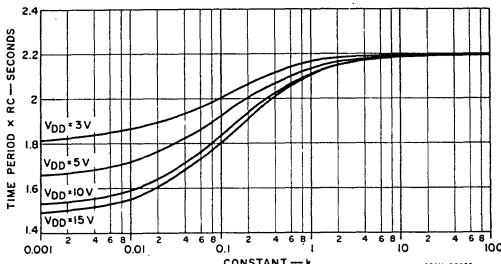


Fig. 6 - Discrete RC-oscillator time period as a function of constant, k.

be made adjustable, the user must be careful with component layout, if  $R_S$  is made very large, to take advantage of the improvement in stability. A time constant and phase shift is produced by  $R_S$  and stray wiring and breadboard capacitance, see Fig. 7. This shift creates a switching delay in the circuit which changes the time period and, in addition, may cause spurious oscillations and glitches in the multivibrator circuit. A reasonable value for K would be anywhere from 2 to 10, with maximum and minimum values for  $R_S$  determined by the above considerations.

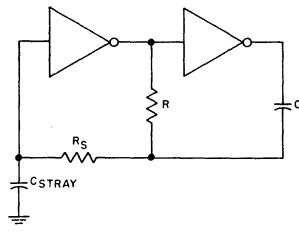


Fig. 7 — RC-oscillator circuit with stray capacitance.

#### COS/MOS INTEGRATED RC OSCILLATORS

The RCA-CD4047A is an integrated RC oscillator that eliminates most of the disadvantages of the discrete circuits previously discussed. The primary reason for this improved performance is the special input-protection circuit which allows the capacitor charging waveform to swing above  $V_{DD}$  and below  $V_{SS}$  without the need for an external resistor. This circuit, shown in Fig. 8, has the same time period and stability as the circuit in Fig. 4 for the case where the value of  $R_S$  is infinite. However, a resistor is eliminated, as well as the disadvantages of a time constant caused by the resistor.

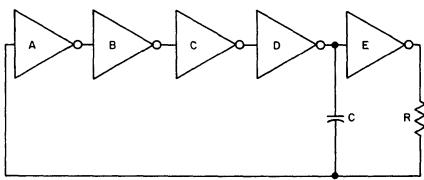


Fig. 8 — CD4047A oscillator section

There are two additional reasons for expected improvement with the CD4047A. First, the transfer-voltage point of the input inverter, A, is tested between 33 and 67 per cent of  $V_{DD}$  instead of between 30 and 70 per cent; this narrower test range improves stability by reducing unit-to-unit variations. In addition, large buffers are used for inverters D and E; this practice reduces the effect of changes of device output impedance with period stability. A derivation of period, T, for this circuit is presented in the Appendix C; the final equation for T becomes:

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})} \quad (3)$$

Figure 9 shows a graph of stability as a function of transfer voltage based on this equation.

The graph of Fig. 9 shows a maximum variation of 5 per cent between minimum (2.197 RC) and maximum (2.307 RC) time periods. A value of 2.25 RC yields a  $\pm 2.5$  per-cent variation. Typical values of period variations at high frequencies and temperature extremes are included in the published data for the CD4047A.<sup>1</sup>

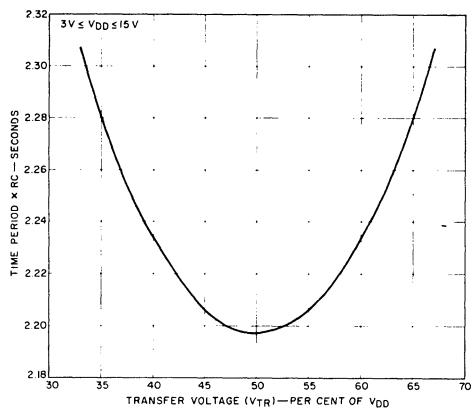


Fig. 9 — CD4047 time period as a function of transfer voltage.

An additional advantage of the CD4047A is a reduction in power dissipation as compared to the discrete multivibrators discussed previously. Inverter A in Fig. 8 is designed with high-impedance components that limit power dissipation during the time that the inverter operates in the middle of its transfer region. Four additional inverters are used to gradually shift from a very-high-impedance inverter at the input to a very-low-impedance driver in series with the external timing resistor. Calculations for power dissipation and a comparison of  $P_{diss}$  for the CD4047A and a discrete oscillator are presented in Appendix D; the result is

$$P_{diss} = 2CV^2 f \quad (4)$$

This equation specifies the power dissipated in the external components only. At low frequencies, where most of the power will be dissipated in R, power can be minimized by using a small value of C, since the formula shows the power is a function of C and not R.

Additional power is consumed in the CD4047A chip as a function of frequency. Fig. 10 shows curves for theoretical minimum power dissipation, actual CD4047A oscillator-power dissipation, and discrete oscillator-power dissipation as a function of frequency.

#### CMOS DISCRETE ONE-SHOTS

Fig. 11 illustrates one of several simple monostable circuits which can be employed in non-critical timing circuits.<sup>2</sup> The

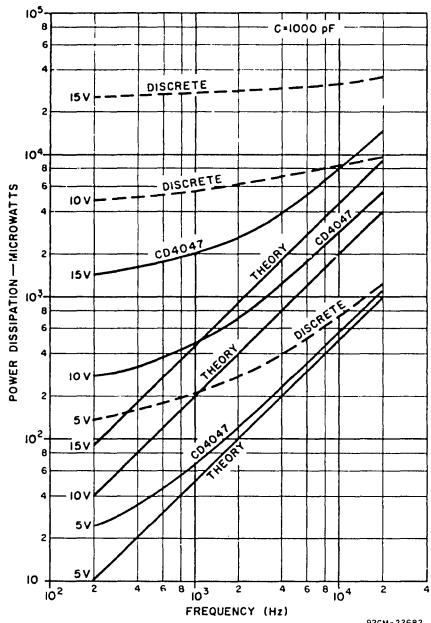


Fig. 10 – Comparison of  $P_{diss}$  for discrete oscillator and CD4047 with theory.

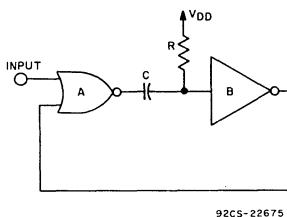


Fig. 11 – COS/MOS monostable circuit.

circuit pulse width is dependent upon the transfer voltage of inverter B as time constant RC charges to  $V_{DD}$  from  $V_{SS}$ . The pulse width is defined as

$$T = -RC \ln \frac{(V_{DD} - V_{TR})}{(V_{DD})} \quad (5)$$

Fig. 12 shows the variation in pulse width as a function of transfer voltage for this device.

There are several alternatives to the circuit shown in Fig. 12.<sup>2</sup> These alternatives have the advantage of greater stability, but at the expense of two time constants required in circuit and, in some cases, the addition of a diode.

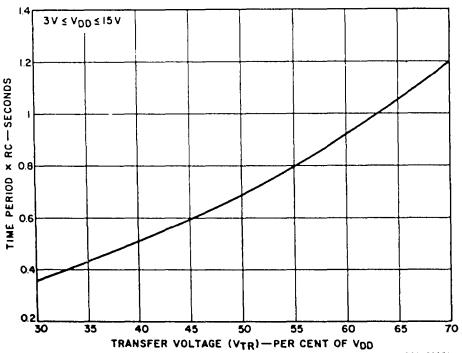


Fig. 12 – Simple one-shot time period as a function of transfer voltage.

### COS/MOS INTEGRATED ONE-SHOTS

The CD4047A, when used in the monostable mode, again has several advantages over discrete designs. A high degree of accuracy can be achieved with one time constant, and power dissipation is lower than with discrete designs. Fig. 13 shows that many functions can be achieved with the CD4047A, including leading and trailing-edge triggering, and retrigging.

The pulse width,  $T_M$ , is expressed below: its derivation is given in Appendix E.

$$T_M = -RC \ln \frac{(V_{TR})(V_{DD}) - V_{TR}}{(2V_{DD})(2V_{DD} - V_{TR})} \quad (6)$$

Fig. 14 is a graph of pulse width versus transfer voltage based on the above equation.

The equations for monostable-mode power dissipation are also derived in Appendix E. For a repetitive output on the CD4047A, power dissipation can be expressed by the following equation:

$$P_{diss} = \frac{2.875 CV_{DD}^2}{T_M} \times (\text{duty cycle}) \quad (7)$$

### USING THE CD4047A – SPECIAL CONSIDERATIONS

A number of circuit considerations are explained below which will aid the user of the CD4047A.

A clamping circuit is provided on the chip to reduce the recovery time ( $t_r$ ) that would normally exist in other monostable circuits; see Figs. 15 and 16. Fig. 17 shows a plot of monostable-pulse-width stability as a function of duty cycle for specific R and C external components. Note that there is no appreciable change in pulse width until the duty cycle approaches 100 per cent. A disadvantage to the clamping circuit is that it introduces additional capacitance at the RC common node (Fig. 16), which may be noticeable for short pulse widths in the monostable mode only. Some diffusion capacitance present at the base of the n-p-n transistor is used to quickly

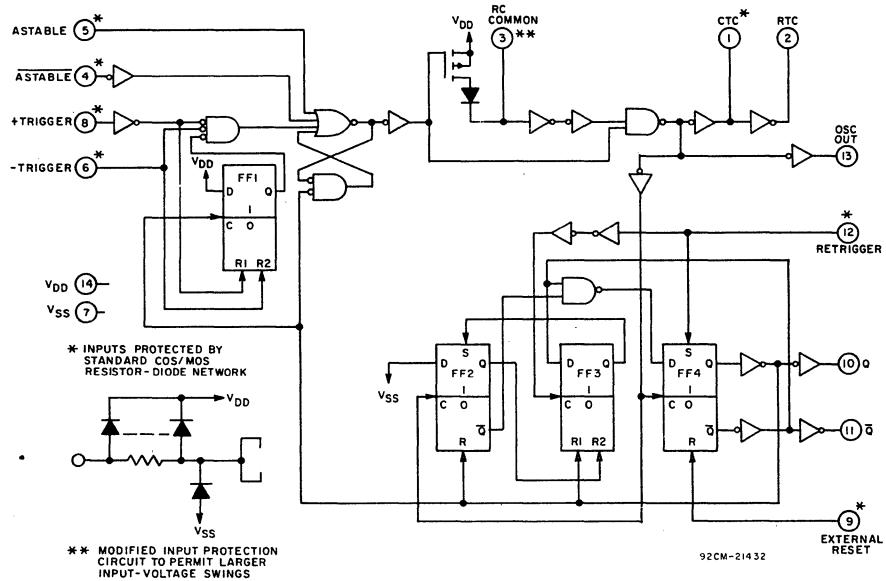


Fig. 13 - CD4047A logic diagram.

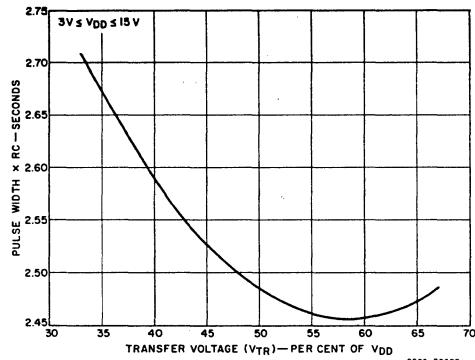


Fig. 14 - CD4047A one-shot pulse width as a function of transfer voltage.

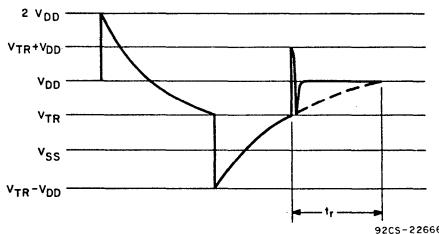


Fig. 15 - CD4047A one-shot RC waveform.

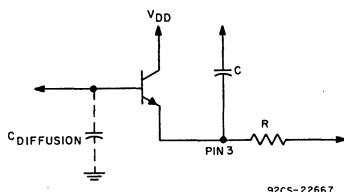


Fig. 16 - CD4047A clamping circuit.

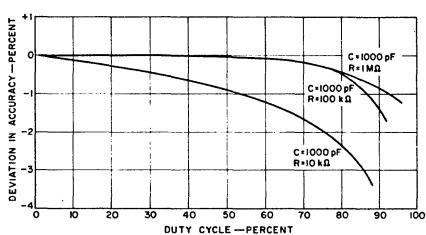


Fig. 17 - CD4047A monostable accuracy as a function of duty cycle.

charge C to  $V_{DD}$  after the one-shot cycle has terminated. This capacitance is multiplied by the beta of the transistor, and is in parallel with the external C during the time interval that the transistor is on ( $(V_{DD} - V_{BE}) < t < V_{BE}$ ). Thus, when values of C less than 1000 picofarads are used, the actual width will be longer than that predicted by the formula. Fig. 18 is a graph of actual, typical pulse widths as a function of external C used under these conditions. Note that the minimum values of C used in the graph are the smallest that can be used in the CD4047A to assure proper operation of the circuit.

The waveform in Fig. 15 shows that two positive transitions are encountered by the control circuitry in the CD4047A. These transitions are necessary to make the output flip-flop at pin 10 toggle properly to produce the single pulse needed in monostable operation. However, at pin 13, the waveform of

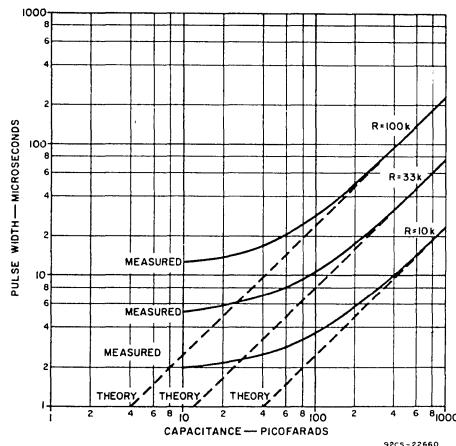


Fig. 18 — CD4047A pulse width as a function of capacitance.

Fig. 19 results; the pulse width of the spike is equivalent to the propagation delay of the circuit. This spike will normally prevent the user from using pin 13 in the monostable mode. In the astable mode, however, pin 13 can be used whenever a 50-per-cent duty cycle and higher drive capability are not



Fig. 19 — CD4047A one-shot output at pin 13.

required. The advantage to the use of pin 13 under these conditions is that the frequency of the waveform at pin 13 is twice that of pin 10 for the same external timing components.

When the CD4047A is used in the retrigger mode, the retrigger input is connected directly to the set input of FF4,

as shown in Fig. 13. This connection means that the output at pin 10 will be high during the time that a high level is present on pin 12. Thus, if normal one-shot operation is required at any time that the circuit is in the retrigger mode, the input pulse should be shorter than the expected pulse at the output. Note that in the retrigger mode the output pulse width is not referenced to the last positive-going edge produced at the input because of the asynchronous nature of the circuit. The output actually terminates when two internal oscillator leading edges have been received by FF4, after the high level present on pin 12 has been removed. The output width variation will then be between one and two time constants referenced to the trailing edge of the input at pin 12, see Fig. 20.

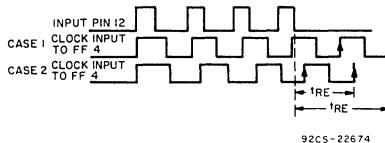


Fig. 20 — CD4047A retrigger-mode waveforms.

A section on timing-component limitations is presented in the CD4047A data sheet.<sup>1</sup> It should be emphasized that it is desirable to use a small value of capacitance wherever possible. The circuit will work well even when the value of R approaches or exceeds 1 megohm. For very low frequencies, where a large value of capacitance is needed, the selection of the capacitor is very important. It must be nonpolarized because there is no reference ground at either of the two pins to which C is connected. The capacitor parallel resistance (i.e., leakage) must also be at least an order of magnitude higher than the external R used. This criterion generally eliminates electrolytic capacitors and those made of materials which could produce greater leakage current than that permitted for proper circuit operation.

Because of the internal circuit construction, there is no guarantee as to what dc level will be present on the output at pin 10 or 11 when power is first turned on. If this condition must be guaranteed, a system-power-on pulse input to pin 9 can be made to assure that pin 10 will initially be at a low logic level. The pulse can be generated from one of the circuits shown in Fig. 21.

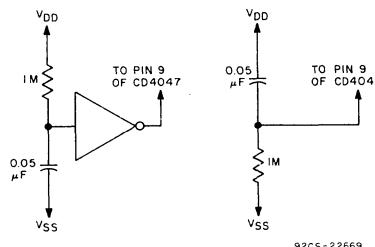


Fig. 21 — CD4047A power-up reset circuits.

Although the CD4047A data sheet calls for a minimum input pulse duration of 200 nanoseconds at 10 volts and 500 nanoseconds at 5 volts, shorter pulses (due to transients, etc.) occur frequently in system applications where the CD4047A is used. Such narrow pulses may not be ignored by the CD4047A, but may instead cause Q to go high permanently or until a reset input occurs. The circuit shown in Fig. 22 eliminates this problem by essentially "lengthening" the trigger pulse by feeding back through  $R_A$  and  $C_A$  a current pulse when Q goes from 0 to a 1. The particular values shown have been tried and found to work well, even for extremely short input pulses (less than 20 nanoseconds).

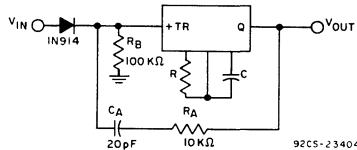


Fig. 22 - Input-pulse stretcher circuit.

## APPLICATIONS

### NOISE DISCRIMINATOR

Fig. 23 illustrates an application of the CD4047A in a noise-discriminator circuit. By adjusting the external time constant, a pulse width narrower than that determined by the time constant will be rejected by the circuit. The output pulse will

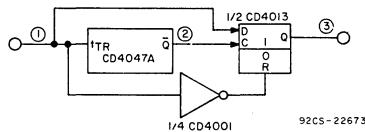
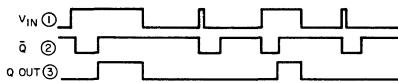


Fig. 23 - Noise-discriminator circuit.

follow the desired input, but the leading edge will be delayed by the selected time constant. Fig. 24 shows typical waveforms with the circuit in operation.

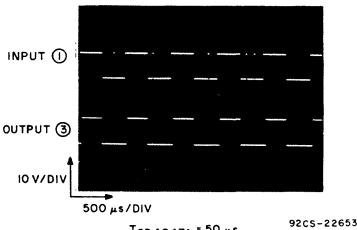


Fig. 24 - Noise-discriminator circuit waveforms.

### FREQUENCY DISCRIMINATOR

The CD4047A can be used as a frequency-to-voltage converter, as shown in Fig. 25. A waveform of varying frequency is applied to the +TR input. The one-shot will produce a pulse of constant width for each positive transition on the input. The

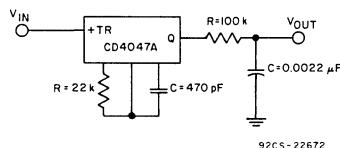


Fig. 25 - Frequency-discriminator circuit.

resultant pulse train is integrated to produce a waveform whose amplitude is proportional to the input frequency. The waveforms of Fig. 26 were taken with the circuit in operation.

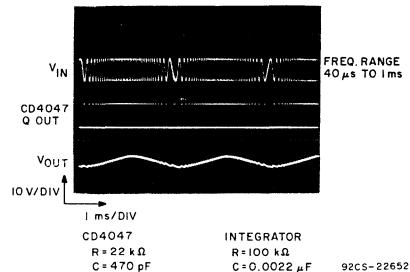


Fig. 26 - Frequency-discriminator-circuit waveforms.

### LOW-PASS FILTER

A simple circuit using the CD4047A as a low-pass filter is shown in Fig. 27. The time constant chosen for the multivibrator will determine the upper cutoff frequency for the filter. The circuit essentially compares the input frequency

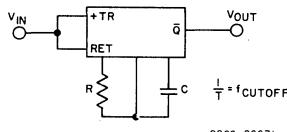


Fig. 27 - Low-pass filter circuit.

with its own reference, and produces an output which follows the input for frequencies less than  $f_{cutoff}$ , and a low output for frequencies greater than  $f_{cutoff}$ . Figs. 28 and 29 show waveforms with the low-pass filter circuit in operation.

### BANDPASS FILTER

Two CD4047A low-pass filters can be employed to construct a bandpass filter, as illustrated by the circuit in Fig. 30.

The pass band is determined by the time constants of the two filters. If the output of filter No. 2 is delayed by  $C_1$ , the CD4013A flip-flop will clock high only when the cutoff frequency of filter No. 2 has been exceeded; this point is illustrated in the timing diagram in Fig. 30. The Q output of the CD4013A is gated with the output of filter No. 1 to produce

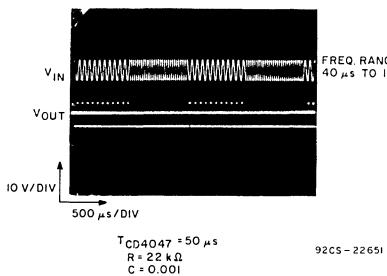


Fig. 28 — Low-pass filter-circuit waveforms.

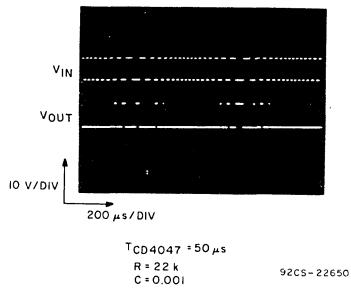


Fig. 29 — Low-pass-circuit waveforms.

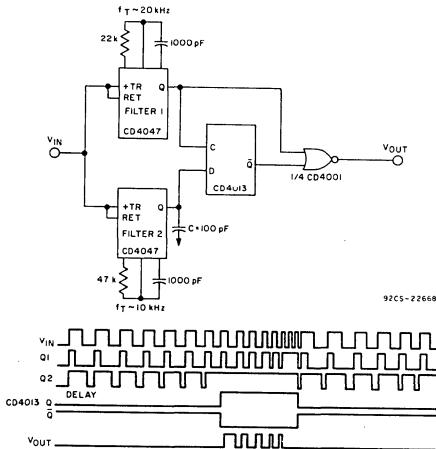


Fig. 30 — Bandpass filter circuit and waveforms.

the desired output. Typical operation of the circuit is shown in Fig. 31, where the input frequency is swept through the pass band.

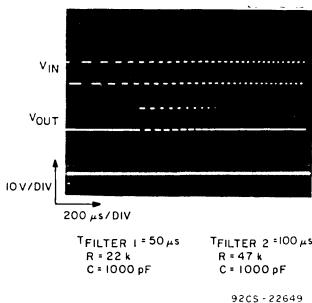


Fig. 31 — Bandpass-filter-circuit waveforms.

### ENVELOPE DETECTOR

The CD4047A can be used as an envelope detector by employing it in the retrigger mode, as shown in Fig. 32. The time constant is selected so that the circuit will retrigger at the



Fig. 32 — Envelope-detector circuit.

frequency of the input pulse burst. A dc level appears at the output for the duration of the input pulse train. Fig. 33 shows waveforms taken with the circuit in operation.

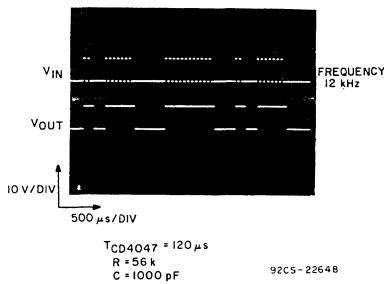
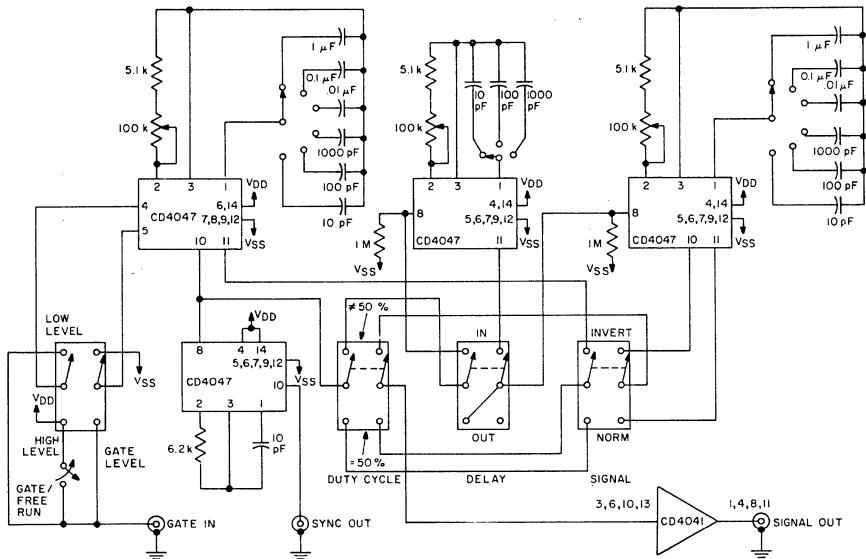


Fig. 33 — Envelope-detector-circuit waveforms.

### PULSE GENERATOR

Several CD4047A units can be connected together to produce a general-purpose laboratory pulse generator, as shown in Fig. 34. The circuit shown has variable-frequency and pulse-width control, as well as gating and delayed sync capability.



92CM-22556

Fig. 34 — Pulse-generator circuit.

Gating can be controlled from a high- or low-level input. Automatic 50-per-cent duty-cycle capability is included, as normal or inverted output.

CD4047A No. 1 is connected as a gated, astable multivibrator, and, with the RC values shown, can produce overlapping ranges of frequencies from 2 Hz to 1 MHz. For free-running operation, the Gate/Free-Run switch is closed, and the Gate Level switch is placed in the **high-level** position. Standby operation can be achieved with the Gate Level switch in the **low-level** position. When gating, the Gate/Free-Run switch is open, and the Gate Level switch is set to the appropriate position. The gate signal is applied to the Gate In jack.

CD4047A No. 2 is triggered from the gated, astable multivibrator, and produces a narrow sync pulse which can trigger an oscilloscope or generator. The sync pulse is obtained from the Sync Out jack.

If a 50-per-cent duty cycle is desired, the Duty Cycle switch is set in the 50-per-cent position, and the output is obtained from CD4047A No. 1. The Signal Polarity switch determines whether the Q and Q̄ output is used.

CD4047A No. 3 produces a variable, delayed (from 1.5 microseconds to 250 milliseconds) output with respect to the sync pulse when the Delay switch is in the IN position. This

one-shot is bypassed when the Delay switch is in the OUT position (the inherent delay is approximately 400 nanoseconds).

CD4047A No. 4 is a monostable multivibrator which receives trigger pulses from CD4047A No. 1 or No. 3. It can produce overlapping ranges of pulse widths from 1.5 microseconds to 200 milliseconds with the values shown.

The signal output is buffered with the CD4041A to allow the pulse generator to drive any required load. The circuit shown has the advantages of being compact, battery-powered, and COS/MOS compatible. In addition, it is capable of being run from the same power supply as the device under test to assure that the input levels are the same as V<sub>DD</sub> when the power-supply voltage is varied.

#### MISCELLANEOUS APPLICATIONS

The basic properties of good stability in the astable mode, and stable pulse delay and width control in the monostable mode, make the CD4047A a useful building block in many systems, such as PMOS clock generation, audio tone generation, semiconductor memory systems, semiconductor memory exercisers, and general-purpose functional-testing systems. This Application Note will serve as a guideline in incorporating the CD4047A in a system design.

**Appendix A –**  
**Calculation of the Period of an Astable Multivibrator Using a Single RC Time Constant**

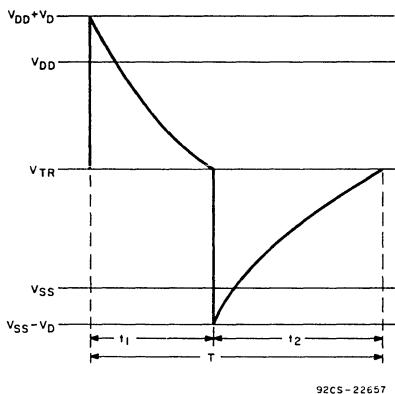


Fig. A-1 – RC oscillator waveform for the circuit of Fig. 1.

In Fig. A-1:

$$t_1: V_{TR} = (V_{DD} + V_D) e^{-t_1/RC}$$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_D) e^{-t_2/RC}$$

$$t_2 = RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

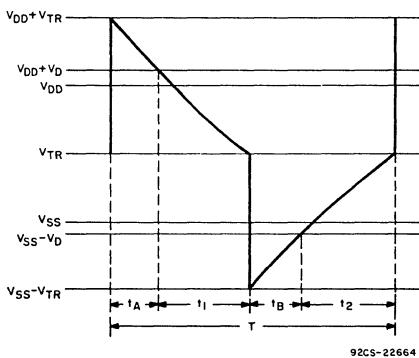
And the period of an astable multivibrator using a single RC time constant is:

$$T = t_1 + t_2 = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2}$$



**Appendix B –**

**Analysis of Circuit Shown in Fig. 4**



In Fig. B-1:

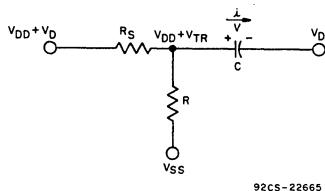
$$t_1: V_{TR} = (V_{DD} + V_D) e^{-t_1/RC}$$

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_D}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_D) e^{-t_2/RC}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{V_{DD} + V_D}$$

Fig. B-1 – RC waveform for the circuit of Fig. 4.

t<sub>A</sub>Fig. B-2 – Initial conditions for solving period  $t_A$ .

Circuit initial conditions are shown in Fig. B-2. In the figure

$$-C \frac{dv}{dt} = \frac{V + V_{DD}}{R} + \frac{V + V_{DD} - (V_{DD} + V_D)}{R_S} \quad (B-1)$$

Eq. (B-1) is solved for V; the final voltage across the capacitor is

$$V = C_1 e^{-K_1 t_A} + \frac{K_2}{K_1} \quad (B-2)$$

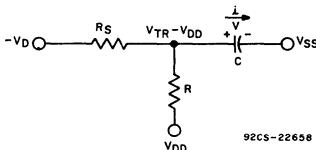
where  $C_1 = V_{TR}$  = initial voltage across capacitor

$$K_1 = \frac{R_S + R}{R_S R C}$$

$$K_2 = \frac{V_D R - R_S V_{DD}}{R_S R C}$$

By inserting these values into Eq. (B-2) and setting the final voltage across the capacitor, V, to  $V_D$ ,  $t_A$  becomes

$$t_A = -\left[ \frac{R_S R C}{R_S + R} \right] \ln \frac{R_S [V_{DD} + V_D]}{R_S [V_{DD} + V_{TR}] + R [V_{TR} - V_D]}$$

t<sub>B</sub>Fig. B-3 – Initial conditions for solving period  $t_B$ .

Circuit initial conditions as shown in Fig. B-3. In the figure

$$C \frac{dv}{dt} = \frac{V_{DD} - V}{R} - \frac{V_D + V}{R_S} \quad (B-3)$$

Solving Eq. (B-3) for V the final voltage across the capacitor, yields

$$V = C_2 e^{-K_1 t_B} - \frac{K_2}{K_1} \quad (B-4)$$

where  $C_2 = V_{TR} - V_{DD}$  = initial voltage across capacitor

$K_1$ ,  $K_2$  are same values as for above for  $t_A$ .

Insertion of these values into Eq. (B-4), with  $V = -V_D$  yields

$$t_B = \left[ \frac{R_S R C}{R_S + R} \right] \ln \frac{R_S [V_{DD} + V_D]}{R_S [2 V_{DD} - V_{TR}] + R [V_{DD} - V_{TR} - V_D]}$$

and  $T = t_1 + t_2 + t_A + t_B$

The equations for  $t_A$ ,  $t_B$ , and T can be simplified by expressing  $R_S$  as a multiple of R. Let

$R_S = \frac{R}{R}$  and combining the expressions for  $t_1$  and  $t_2$ . The resulting expression for T is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_D)^2}$$

$$-\left( \frac{K}{K+1} \right) RC \ln \frac{K [V_{DD} + V_D]}{K [V_{DD} + V_{TR}] + [V_{TR} - V_D]}$$

$$-\left( \frac{K}{K+1} \right) RC \ln \frac{K [V_{DD} + V_D]}{K [2 V_{DD} - V_{TR}] + [V_{DD} - V_{TR} - V_D]}$$

**Appendix C —**  
**Calculation for Period of Astable Multivibrator Using Integrated Techniques**

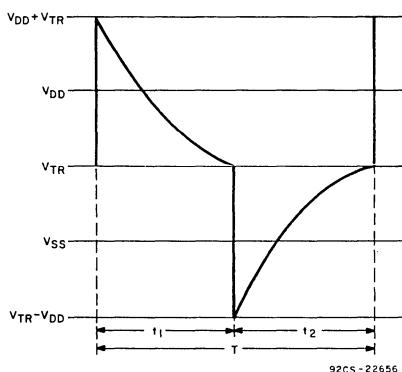


Fig. C-1 — CD4047A RC oscillator waveform.

In Fig. C-1

$$t_1: V_{TR} = (V_{DD} + V_{VTR}) e^{-t_1/RC}$$

$$t_1 = RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2: V_{DD} - V_{TR} = (V_{DD} + V_{VTR}) e^{-t_2/RC}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2(V_{DD} - V_{TR})}$$

And the period of the astable multivibrator using integrated techniques is

$$T = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

**Appendix D —**

**Power Needed for Charge and Discharge of an External Capacitor During One Cycle**

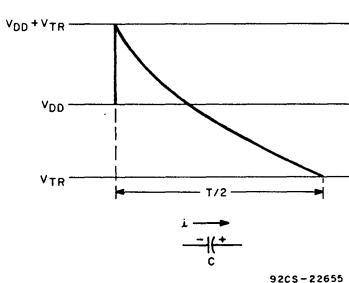


Fig. D-1 — Waveform for calculating power dissipation.

Assume for this calculation that  $V_{TR} = 50\text{-per-cent } V_{DD}$ , and that  $T = 2.2 \text{ RC}$ . Since charge and discharge cycles are symmetrical, the calculation can be performed by analyzing a discharge cycle only. See Fig. D-1.

$$V = 1.5 V_{DD} e^{-t/RC}$$

$$\frac{dV}{dt} = -\left(\frac{1}{RC}\right)(1.5 V_{DD}) (e^{-t/RC})$$

$$\begin{aligned} P &= \frac{1}{(T/2)} \int_0^{T/2} CV \frac{dv}{dt} dt \\ &= \frac{2C}{T} \int_0^{T/2} (1.5 V_{DD} e^{-t/RC}) \left(\frac{1}{RC}\right) (1.5 V_{DD}) e^{-t/RC} dt \\ &= \frac{4.5C}{T} \frac{V_{DD}^2}{RC} \int_0^{T/2} e^{-2t/RC} dt \\ &= \frac{2.25C}{T} V_{DD}^2 e^{-2t/RC} \Big|_0^{T/2} \end{aligned}$$

Substituting  $T = 2.2 \text{ RC}$

$$P = -\frac{C}{T} (2.25) V_{DD}^2 [e^{-2.2} - 1] = \frac{2.0C}{T} V_{DD}^2$$

$$P = 2CV^2f$$

## Appendix E —

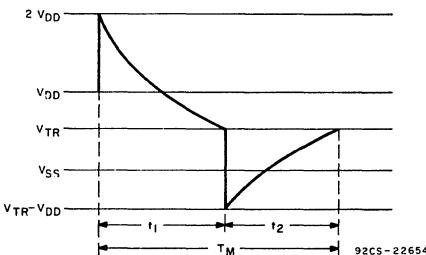
Equations for Pulse Width  $T_M$  of CD4047A in Monostable Mode

Fig. E-1 — CD4047A RC waveform, monostable mode.

Note that the waveform in Fig. E-1 is not symmetrical because the timing capacitor is initially charged to  $V_{DD}$ . In the monostable mode, the circuit goes through one cycle only.

## Monostable Power Dissipation

To calculate the power dissipation for the circuit in the monostable mode, refer to Fig. E-1. If it is assumed that  $V_{TR} = 50\text{-per-cent } V_{DD}$ , Fig. 14 shows that  $T_M = 2.485 \text{ RC}$ .  $t_2$  is the same as in the astable calculation, i.e.,  $t_2 = 1.10 \text{ RC}$  and  $P_{t2} = CV^2 f$  for  $V_{TR} = 50\text{-per-cent } V_{DD}$ . Thus,  $t_1$  in the monostable mode =  $2.485 \text{ RC} - 1.10 \text{ RC} = 1.385 \text{ RC}$ .

$$P = \frac{1}{T_M} \left[ \int_0^{t_1} CV \frac{dv}{dt} dt + \int_{t_1}^{t_2} CV \frac{dv}{dt} dv \right]$$

$$= \frac{1}{T_M} \int_0^{t_1} CV \frac{dv}{dt} dt + \frac{1}{T_M} CV^2$$

where  $V = 2 V_{DD} e^{-t/RC}$  and

$$\frac{dv}{dt} = -\left(-\frac{1}{RC}\right)(2 V_{DD}) e^{-t/RC}$$

$$t_1: V_{TR} = 2 V_{DD} e^{-t_1/RC}$$

$$t_1 = -RC \ln \frac{V_{TR}}{2 V_{DD}}$$

$$t_2: V_{DD} - V_{TR} = (2 V_{DD} - V_{TR}) e^{-t_2/RC}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2 V_{DD} - V_{TR}}$$

And the equation for the pulse width,  $T_M$ , of a CD4047A in the monostable mode is:

$$T_M = t_1 + t_2 = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2 V_{DD})(2 V_{DD} - V_{TR})}$$

$$Pt_1 = \frac{C}{T_M} \int_0^{t_1} \left( 2 V_{dd} e^{-t/RC} \right) \left( \frac{1}{RC} \right) \left( 2 V_{dd} e^{-t/RC} \right) dt$$

$$= \frac{C}{T_M} \frac{4 V_{dd}^2}{RC} \int_0^{t_1} e^{-2t/RC} dt$$

$$= -\frac{C}{T_M} 2 V_{dd}^2 e^{-2t/RC} \Big|_0^{t_1}$$

Substituting  $t_1 = 1.385 \text{ RC}$

$$P_{t1} = -\frac{C}{T_M} 2 V_{dd}^2 [e^{-2.77} - 1] = \frac{1.875 C V_{dd}^2}{T_M}$$

$$P = P_{t1} + P_{t2} = (1.875 + 1) \frac{C V_{dd}^2}{T_M} = 2.875 \frac{C V_{dd}^2}{T_M}$$

For a repetitive output from the CD4047A

$$P = \frac{2.875 C V_{dd}^2}{T_M} \times \text{duty cycle}$$

## REFERENCES

- “CD4047A COS/MOS Low-Power Monostable/Astable Multivibrator,” RCA Data Bulletin, File No. 623
- “Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits,” by J. A. Dean and J. P. Rupley, RCA Application Note ICAN-6267

## ACKNOWLEDGMENTS

The assistance of R. Vaccarella in the designing of some of the application circuits shown and in obtaining laboratory measurements used in plotting the curves shown in this Note is acknowledged.

## Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits

by J. A. Dean and J. P. Rupley

COS/MOS integrated logic circuits are being widely used in digital and other applications because of their inherent advantages of high noise immunity, extremely low power dissipation, and tolerance to wide variations in power-supply voltages and operating-temperature ranges. In addition to these features, COS/MOS gates and inverters can provide cost and size reductions in multivibrator circuits because their high input impedance makes it possible to obtain large time constants without the use of large capacitors. This Note describes several techniques which may be used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits for operation at frequencies up to 1 MHz. The circuits shown can be formed by use of COS/MOS inverters and NAND or NOR gates connected in an inverter configuration. NAND and NOR gates perform the inverter function when all of the gate inputs are tied together. This Note also describes various applications for COS/MOS multivibrator circuits, (i.e., voltage-controlled oscillators, voltage controlled-pulse-width circuits, phased-locked voltage controlled oscillators, frequency multipliers, and modulator/demodulator (envelope detectors). (Note: COS/MOS Hex Buffers CD4009A and CD4049A and Quad Buffer CD4041A are not recommended for use as multivibrators because of the very high power consumption in the linear mode for long time constants. In addition, the Hex Buffers have large imbalance between source and sink current capability which makes oscillator start-up more unpredictable. The COS/MOS General-Purpose Hex Inverter CD4069B is recommended for use in the multivibrator applications illustrated in this Note. The CD4069B is well adapted to MV applications, having balanced output drive capability of  $\pm 0.4$  milliamper for 5 V operation at an output voltage level of  $\pm 0.4$  volt. Specific data in this Note relate to the use of "A" series gates as shown; performance using the CD4069B may differ slightly from the data shown herein.

### ASTABLE CIRCUITS

Fig. 1(a) shows an astable multivibrator circuit that uses two COS/MOS inverters, and Fig. 1(b) shows the related waveforms. This simple circuit requires only two resistors and one capacitor, and operates in the following manner. When the waveform 1 at the output of inverter B is in a high or "one" state, capacitor  $C_{tc}$  becomes charged positive. As a result, the input to inverter A is high and its output is low or "zero". Resistor  $R_{tc}$  is returned to the output of inverter A to provide a path to ground for discharge of capacitor  $C_{tc}$ .

As long as the output of A is low, the output of inverter B is high. As capacitor  $C_{tc}$  discharges, however, the voltage generated [waveform 2 in Fig. 1(b)] approaches and passes through the transfer voltage point of inverter A. At the instant that this crossover occurs, the output of A becomes high; as a result, the output of B becomes low and the capacitor  $C_{tc}$  is charged negative (or low). The resistor  $R_{tc}$  connected to the output of A then provides a charge path to a supply voltage. Capacitor  $C_{tc}$  begins to charge to this voltage, and again the voltage approaches and passes through the transfer voltage point of inverter A. At that instant, the circuit again changes state (the output of A becomes low and that of B high) and the cycle repeats.

Because of the input-diode protection circuits included in the COS/MOS IC, shown in Fig. 2, the generated drive waveform

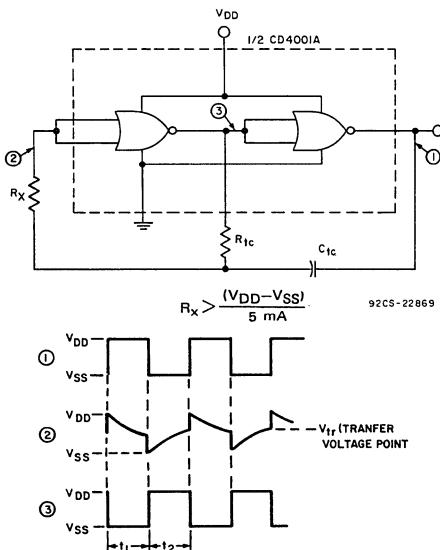


Fig. 1 - Circuit diagram and voltage waveforms for astable multivibrator circuit that uses two COS/MOS inverters.

is clamped between  $V_{DD}$  and  $V_{SS}$ . Consequently, the time to complete one cycle is approximately 1.4 times the RC time constant because one time constant is used to control the switching of both states of the multivibrator circuit. Resistor  $R_X$  (Fig.1) limits the current through D1 (Fig.2) to a safe level. Switching occurs when the charge or discharge reaches the transfer voltage level, or when the time period reaches 70.7 per cent of its discharge. As shown in waveform 2 of Fig.1(b), the transfer voltage point  $V_{tr}$  is the same for  $t_1$  and  $t_2$ . The time period T for one cycle can be computed as follows:

$$\begin{aligned} T &= t_1 + t_2 \\ t_1 &= -RC \ln \frac{(V_{DD} - V_{tr})}{V_{DD}} \\ t_2 &= -RC \left[ \ln \frac{V_{tr}}{V_{DD}} \right] \\ T &= -RC \left[ \ln \frac{(V_{DD} - V_{tr})}{V_{DD}} + \ln \frac{V_{tr}}{V_{DD}} \right] \quad (1) \end{aligned}$$

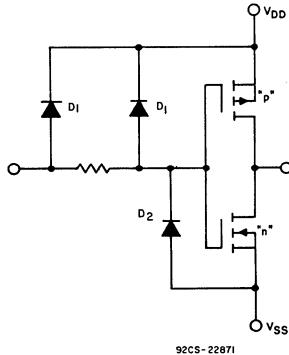


Fig. 2 - Diode protection circuit.

If the time constant is assumed to be  $1 \times 10^{-6}$  second and the transfer voltage  $V_{tr}$  is allowed to vary from 33 to 67 per cent of  $V_{DD}$ , the period T varies from 1.4 microseconds at a value of  $V_{tr}$  equal to half of  $V_{DD}$  to 1.5 microseconds at either the 33 or 67 per cent value of  $V_{DD}$ . Therefore, the maximum variation in the time period T is only 9 per cent with a  $\pm 33$ -per-cent variation in transfer voltage from unit to unit.

The oscillator can be made independent of supply-voltage variations by use of a large resistance in series with the input lead to inverter A, shown in Fig.3(a). This resistor  $R_S$  should be at least twice as large as the resistor  $R_{tc}$  of the time constant to allow the voltage waveform generated at the junction of  $R_S$ ,  $R_{tc}$ , and  $C_{tc}$  to rise to  $V_{DD} + V_{tr}$ . The waveform is still clamped at the input between  $V_{DD}$  and  $V_{SS}$ , as shown by the waveforms in Fig. 3(b). The use of resistor  $R_S$

provides several advantages in the circuit. First, because the RC time constant controls the frequency, the over-all maximum variations in the time period are reduced to less than 5 per cent with variations in transfer voltage, as determined by the following equation:

$$T = -RC \left[ \ln \frac{V_{tr}}{(V_{DD} + V_{tr})} + \ln \frac{(V_{DD} - V_{tr})}{2V_{DD} - V_{tr}} \right] \quad (2)$$

The resistor  $R_S$  also makes the frequency independent of supply-voltage variations. Table I shows data measured on typical units with and without the resistor

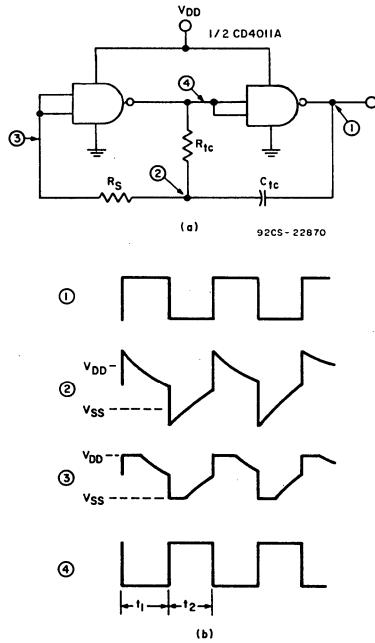


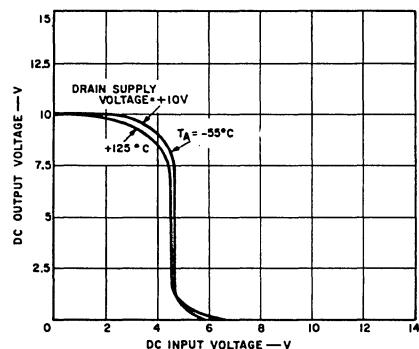
Fig. 3 - Addition of resistor in series with input to one COS/MOS inverter to make oscillator circuit independent of supply-voltage variations: (a) circuit diagram; (b) voltage waveforms.

Fig. 4 shows a typical transfer characteristic as a function of temperature. It can be seen that there is very little change in the characteristic from low to high temperature. Because the oscillator can also tolerate changes in the transfer characteristic without frequency instability, it requires no thermal compensation. The frequency at  $-55^{\circ}\text{C}$  is the same as at  $+125^{\circ}\text{C}$ . Table II shows data measured on typical units at temperature extremes.

**Table I - Frequency variations of astable multivibrator with and without series resistor.**

Unit No.	$V_{tr} @$ $V_{DD} = 10V$ (V)	Period Without $R_s$ - (ms)			Period With $R_s$ - (ms)		
		$V_{DD} = 6V$	$V_{DD} = 10V$	$V_{DD} = 14V$	$V_{DD} = 6V$	$V_{DD} = 10V$	$V_{DD} = 14V$
2	4.77	0.735	0.66	0.645	1.04	1.00	1.02
6	5.78	0.715	0.665	0.63	1.06	1.04	1.03
11	5.58	0.695	0.66	0.625	1.03	1.02	1.03
13	5.00	0.70	0.665	0.64	1.03	1.01	1.02
20	5.56	0.70	0.665	0.64	1.04	1.03	1.03

$R_{tc} = 0.4$  megohm,  $C_{tc} = 1000\text{pF}$ ,  $R_s = 0.8$  megohm

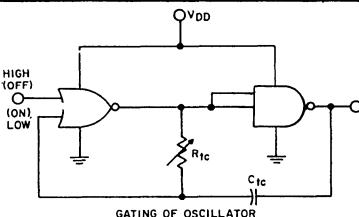
**Fig. 4 - Transfer characteristic as a function of temperature.**

The astable multivibrator shown in Fig. 1 can be gated on/off by use of a NOR gate as the first inverter, as shown in Fig. 5.

**Table II - Frequency variations of astable multivibrator at temperature extremes.**

Unit No.	Period - (ms)					
	$V_{DD} = 6V$		$V_{DD} = 10V$		$V_{DD} = 14V$	
	-55°C	+125°C	-55°C	+125°C	-55°C	+125°C
2	1.04	1.04	1.02	1.01	1.03	1.02
6	1.06	1.07	1.06	1.04	1.04	1.03
11	1.03	1.03	1.04	1.02	1.04	1.01
13	1.02	1.02	1.02	1.02	1.03	1.01
20	1.04	1.03	1.04	1.03	1.04	1.02

$R_{tc} = 0.4$  megohm,  $C_{tc} = 1000\text{pF}$ ,  $R_s = 0.8$  megohm

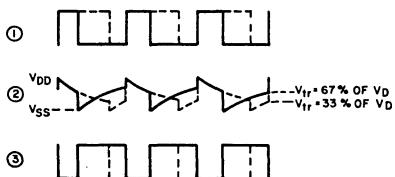


**Fig. 5 - Astable multivibrator in which a NOR gate is used as the first inverter to permit gating of the multivibrator. The NOR and NAND gates can also be reversed with suitable change in control polarity.**

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#### COMPENSATION FOR 50-PER-CENT DUTY CYCLES

The variation in transfer voltage described above affects the output-pulse duty cycle, as shown in Fig. 6. A true square-wave pulse is obtained only when the transfer voltage

**Fig. 6 - Waveforms showing effects of transfer voltage on multivibrator frequency.**

occurs at the 50-per-cent point. However, the duty cycle can be controlled if part of the resistance in the RC time constant is shunted out with a diode, as shown in Fig. 7. Because adjustment of this diode shunt to obtain a specific pulse duty factor causes the frequency of the circuit to vary, a frequency control  $R_3$  is added to compensate for this variation. It may also be necessary to reverse the diode to obtain the desired duty factor. The frequency of any of the circuits shown can be made variable by use of a potentiometer for resistor  $R_{tc}$ .

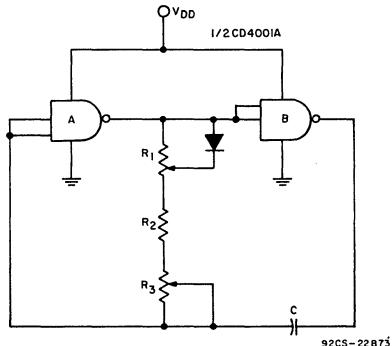


Fig. 7 - Astable multivibrator in which a duty-cycle control is added.

## MONOSTABLE CIRCUITS

**Basic Configuration.** Fig. 8(a) shows a basic "one-shot" circuit that uses a single RC time constant. This circuit operates well provided it is adjusted to the particular COS/MOS unit used. If no adjustment is made, however, the period T can vary from unit to unit by as much as -40 per cent to +60 per cent if the transfer voltage varies by  $\pm 33$  per cent, as shown by the waveforms in Fig. 8(b).

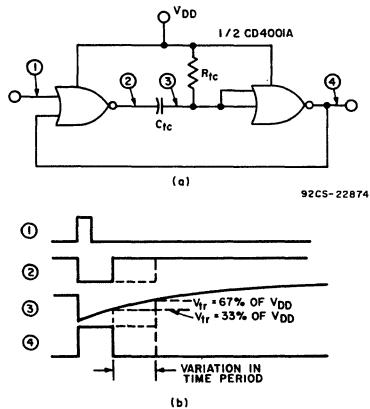


Fig. 8 - Basic one-shot multivibrator circuit: (a) circuit diagram; (b) waveforms.

**Compensated Monostable Circuit.** Fig. 9 shows a compensated monostable multivibrator type of circuit that can be triggered with a negative-going pulse ( $V_{DD}$  to ground). In the quiescent state, the input to inverter A is high and the output low; therefore, the output of inverter B is high. When a negative-going pulse or spike is introduced into the circuit, as

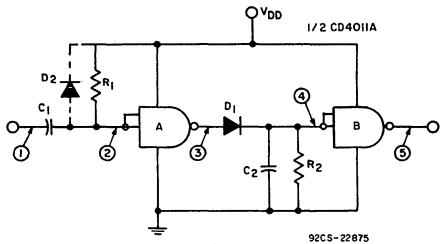


Fig. 9 - Compensated monostable multivibrator circuit.

shown in the waveforms of Fig. 10, capacitor C<sub>1</sub> becomes negatively charged to ground and the output of inverter A becomes high. Capacitor C<sub>2</sub> then charges to  $V_{DD}$  through the diode D<sub>1</sub> and inverter A, and the output of inverter B becomes low. As capacitor C<sub>1</sub> discharges negatively, it charges through resistor R<sub>1</sub> to  $V_{DD}$  (waveform 2). The output of inverter A remains high until the voltage waveform generated by the charge of C<sub>1</sub> passes through the transfer voltage of inverter A; at that instant its output becomes low. Diode D<sub>1</sub> temporarily prevents the discharge of capacitor C<sub>2</sub>, which was charged when inverter A was high (waveform 3). Capacitor C<sub>2</sub> then commences to discharge to ground through resistor R<sub>2</sub> (waveform 4). The output of inverter B remains low until the waveform generated by the discharge of C<sub>2</sub> passes through the transfer voltage point of inverter B; at that point the output returns to its high state (waveform 5).

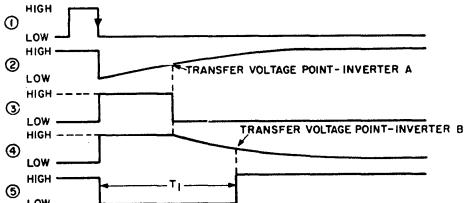


Fig. 10 - Voltage waveforms for monostable multivibrator circuit when a negative-going trigger pulse is applied.

The advantage of using two gates connected as inverters fabricated on the same chip is that they have similar transfer voltages. When two equal RC time constants are used ( $R_1C_1$  equals  $R_2C_2$ ), the effects of variations in transfer voltage from device to device are effectively cancelled out, as shown in Fig. 11. By use of Eq.(1) derived for the astable oscillator, it can be shown that the maximum variation in the time period T is less than 9 per cent. The total time for one period T<sub>1</sub> is approximately 1.4 times the  $R_1C_1$  time constant.

Unlike the astable circuit, which shows no variation in frequency over the temperature range from  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,

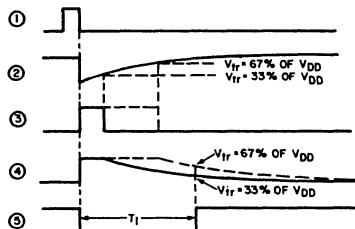


Fig. 11 - Waveforms showing the cancelling effects of transfer-voltage variations of the two COS/MOS inverters when two equal time constants are used.

the monostable multivibrator shows some change in time period. The variation is less than 10 per cent. Table III shows data measured on five units over the temperature range. At 25°C, the variation in the time period  $T$  from unit to unit is quite small, usually less than 5 per cent at a  $V_{DD}$  of 10 volts.

The output from inverter B can be held in the low or zero state as long as the  $R_2 C_2$  time constant is recharged by another triggering pulse before the discharge waveform it generates passes through the transfer voltage of inverter B.

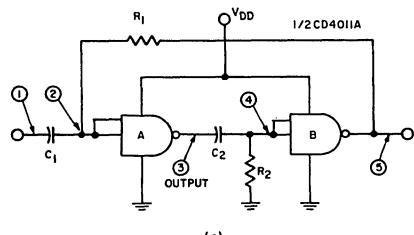
Table III - Frequency variations of monostable multivibrator at three temperatures.

Unit No.	Period @ $V_{DD} = 10V$ - (ms)		
	-55°C	+25°C	+125°C
2	1.06	1.08	1.00
6	1.015	1.03	0.99
11	1.00	1.02	0.98
13	1.01	1.03	0.97
20	1.02	1.02	0.99

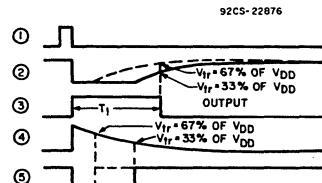
$$R_1 = R_2 = 1 \text{ megohm}, C_1 = C_2 = 0.001\mu\text{F}$$

Diode  $D_2$  in Fig. 9 is internal to the COS/MOS-circuit. As discussed for the astable oscillator, it is part of the input protection circuit shown in Fig. 2, and serves to clamp the input at  $V_{DD}$ .

Figs. 12 and 13 show two variations of the monostable circuit, together with their associated waveforms. The circuit of Fig. 12 triggers on the negative-going excursions of the input pulse, in the same manner as the circuit of Fig. 9. The output pulse is positive-going and is taken from the first inverter. This circuit does not need an external diode. The circuit of Fig. 13 triggers on the positive-going excursion of the input pulse, and then locks back on itself until the RC time constants complete their discharge. The circuits of Figs. 12 and 13 cannot be retriggered until they return to their quiescent states.

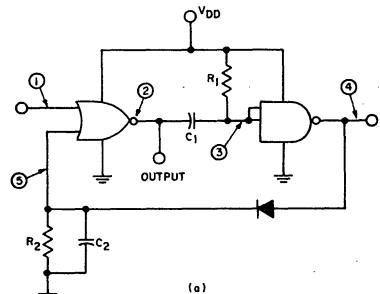


(a)

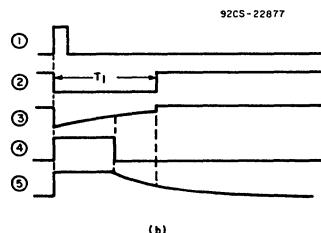


(b)

Fig. 12 - Monostable multivibrator that is triggered by a negative-going input pulse: (a) circuit diagram; (b) waveforms.



(a)



(b)

Fig. 13 - Monostable multivibrator that is triggered by a positive-going input pulse: (a) circuit diagram; (b) waveforms.

**Low-Power Monostable Circuit.** The monostable circuits discussed thus far dissipate some power because one or both of the inverters are on during the charging or discharging of the RC time constants. This power dissipation will be extremely low provided the "one-shot" pulse width is short compared to the over-all cycle time. Fig. 14 shows the current waveform associated with the circuit of Fig. 9. This

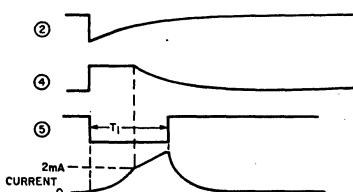


Fig. 14 - Current waveforms for the diode-compensated multivibrator shown in Fig. 9.

waveform is quite wide at the base, and some current flows for approximately twice the time period. Fig. 15(a) shows a circuit using the CD4007A which dissipates much less power than the other circuits shown, but does not have the same stability. This circuit operates as shown by the waveforms in Fig. 15(b). In the quiescent state, the p-channel transistor of the first inverter is biased off, while the n-channel transistor (which derives its control from the output of the second inverter) is biased on. Therefore, the output at C is low, and that at D is high. When a negative-going pulse is introduced into the circuit through capacitor  $C_1$ , the  $R_1C_1$  time constant becomes negatively charged, and the p-channel device is turned on. Capacitor  $C_2$  then charges to  $V_{DD}$ , the output at D becomes low, and the n-channel device of the first inverter is turned off. Capacitor  $C_1$  immediately begins to charge to  $V_{DD}$  through  $R_1$  (waveform B). The p-channel transistor remains on, keeping capacitor  $C_2$  charged to  $V_{DD}$ , until the waveform generated passes through its threshold voltage level and turns it off. The n-channel transistor of the first inverter is still off because the output of the second inverter (waveform D) is still low. When the p-channel device of the first inverter turns off, capacitor  $C_2$  begins to discharge through resistor  $R_2$  (waveform C) to ground. As it discharges, it passes through the threshold voltage of the second p-channel transistor so that it begins to turn on. The voltage waveform at D then begins to rise, and the n-channel device of the first inverter turns on and provides a second discharge path for the capacitor  $C_2$ . As a result, the output waveform changes state from low to high quite rapidly to complete the cycle.

The major advantage of the circuit of Fig. 15 is its low power dissipation. Because the circuit depends on the p-channel transistor threshold, the time period T varies from unit to unit or with temperature variations. Some compensation can

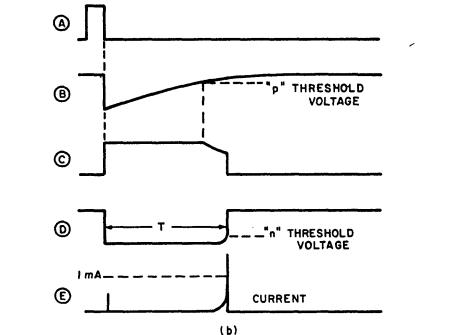
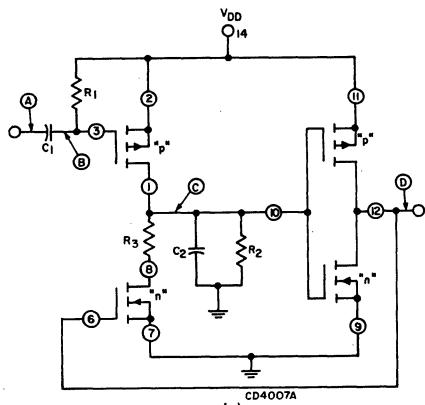


Fig. 15 - Low-power monostable multivibrator: (a) circuit diagram; (b) waveforms.

be provided if the  $R_2C_2$  time constant is made approximately 3 times larger than the  $R_1C_1$  time constant, as shown in Table IV.

Table IV - Frequency variations of monostable multivibrator with temperature when  $R_2C_2$  time constant is increased.

Unit No.	Period with $V_{DD} = 10V$ ( $\mu s$ )		
	-55°C	+25°C	+125°C
553	1090	1120	1160
554	1060	1090	1120
810	1030	1030	1020
900	1000	1020	990
939	1080	1100	1050

$$R_1 = 0.35 \text{ megohm}, C_1 = 0.001 \mu\text{F}$$

$$R_2 = 1 \text{ megohm}, C_2 = 0.001 \mu\text{F}$$

$R_2C_2$  is approximately 3 times the time constant  $R_1C_1$   
 $R_3 = 4700 \text{ ohms}$

For minimum current in the circuit of Fig. 15, capacitor  $C_2$  can be removed so that only stray capacitance is present at the input of the second inverter. A comparison of time-period variations under this condition is shown in Table V. Again, the variations from unit to unit are caused by differences in p-channel transistor threshold.

**Table V - Frequency variations of monostable multivibrator with temperature when  $C_2$  consists of stray capacitance only.**

Unit No.	Period with $V_{DD} = 10V$ (μs)		
	-55°C	+25°C	+125°C
553	870	940	1020
554	900	970	1050
810	900	1000	1080
900	810	880	960
939	780	850	920

$$R_1 = 0.82 \text{ megohm}, C_1 = 0.001 \mu\text{F}$$

$$R_2 = 1 \text{ megohm}, C_2 = \text{strays}$$

### Applications

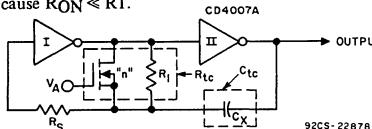
Fig. 16 shows a circuit similar to the circuit in Fig. 3a.  $C_{tc}$  is variable (by adjustment of  $C_X$ ) and  $R_{tc}$  is variable (by adjustment of  $V_A$ ). The value of  $R_{tc}$  varies from  $\approx 1k\Omega$  to  $10k\Omega$ . These limits are determined by the parallel combination of  $R_1$  ( $10k\Omega$ ) and the n-channel device resistance. This varies from  $1k\Omega$  ( $R_{ON}$ ) to  $\approx 10^9\Omega$  ( $R_{OFF}$ ).

When  $V_A = V_{SS}$ , the n-channel device is "OFF" and  $R_{tc} = R_{OFF}/R_1 \approx R_1 = 10k\Omega$

because  $R_{OFF} \gg R_1$ .

When  $V_A = V_{DD}$ , the n-channel device is fully "ON.. and  $R_{tc} = R_{ON}/R_1 \approx R_{ON} = 1k\Omega$

because  $R_{ON} \ll R_1$ .



NOTE :  
INVERTERS AND n-CHANNEL DEVICE ARE AVAILABLE IN  
A SINGLE COS/MOS PACKAGE :  
CD4007A\*

#### TYPICAL VALUES :

$$R_1 = 10k\Omega \quad C_X = 0.001 - 0.004 \mu\text{F}$$

$$R_S = 100k\Omega \quad 0 \leq V_A \leq V_{DD}$$

\* USE PROPER SUFFIX TO DENOTE PACKAGE  
REQUIRED - SEE APPENDIX

**Fig. 16 - Voltage-controlled oscillator.**

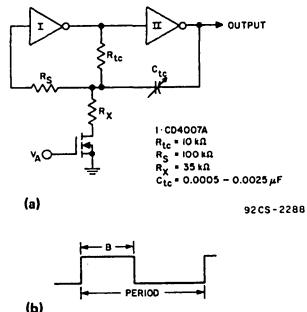
The oscillator center frequency is varied by adjustment of  $C_X$ . Table VI shows a comparison of the period of the output waveform as a function of  $V_{DD}$  and  $V_A$ .

**Table VI - Period of Output as a function of  $V_A$  and  $V_{DD}$  - V.C.O. of Fig. 16.**

Period (μsec)			
$V_A$	$V_{DD} = 5V$	$V_{DD} = 10V$	$V_{DD} = 15V$
0	120	54	48
5	115	45	41
10	--	32	30
15	--	--	24

### Voltage-Controlled Pulse-Width Circuit

Fig. 17a shows a further modification of the circuit of Fig. 3a which modulates the pulse width (by varying  $V_A$ ) only if  $R_X$  is sufficiently high. As an example; if  $C = 0.0022\mu\text{F}$ , then  $R_X \approx 35k\Omega$ . Lower values of  $R_X$  cause the frequency to be affected. If  $R_X < 10k\Omega$ , there is a value of  $V_A$  which will cause the oscillator to cut off. Table VII lists values of pulse width (B in Fig. 17b) for various values of  $V_A$  and  $V_{DD}$ . Fig. 17b shows the output waveform for the circuit described.



**Fig. 17 - (a) V.C. pulse-width circuit; (b) output waveform.**

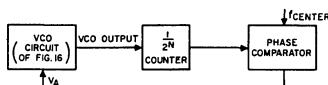
**Table VII - Pulse Width as a Function of  $V_A$  and  $V_{DD}$ .**

$V_A$	Pulse Width (B) μsec		
	$V_{DD} = 5V$ Period=41.5	$V_{DD} = 10V$ Period=35	$V_{DD} = 15V$ Period=33
0	23	19.3	17
5	20	17.7	16.2
10	--	16.2	15.5
15	--	--	14.3

$C_{tc} = 0.001\mu\text{F}$

### Phase Locked VCO

The voltage controlled oscillator can be operated as a phase locked oscillator by the application of a frequency controlled voltage to the gate of the n-channel device. Fig. 18 shows the block diagram of an FM discriminator using the phase locked VCO. Block A is the same circuit as Fig. 16. The output of the phase comparator is fed to the gate of the n-channel device ( $V_A$ ). If the two inputs to the phase comparator are different, the change of  $V_A$  causes the output frequency of the VCO to change. This change is divided by  $2^N$  and fed back to the phase comparator.



**Fig. 18 - VCO used in phase-locked loop.**

**Frequency Multipliers**

Fig. 19a shows frequency doubler. A  $2^N$  multiplier can be realized by cascading this circuit with  $N-1$  other identical circuits. The leading edge of the input signal is differentiated by  $R_1$  and  $C_1$ , applied to the input No. 1 of the NAND gate, and produces a pulse at the output. The trailing edge of the input pulse, after having been inverted, is differentiated, applied to the input No. 2 of the NAND gate, and produces the second output pulse from the NAND gate. The waveforms for 5 points in the circuit are shown in Fig. 19b.

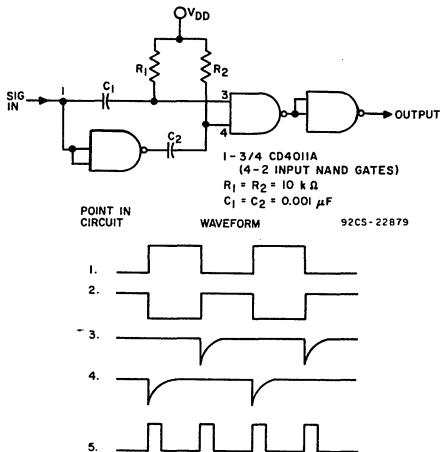


Fig. 19 - (a) Frequency doubler schematic; (b) waveforms.

**Modulation/Demodulation (Envelope Detection).**

Pulse modulation may be accomplished by use of the circuit shown in Fig. 20a. This circuit is a variation of Fig. 3. The oscillator is gated ON or OFF by the signal input No. 1 to the NAND gate. The waveforms are shown in Fig. 20b.

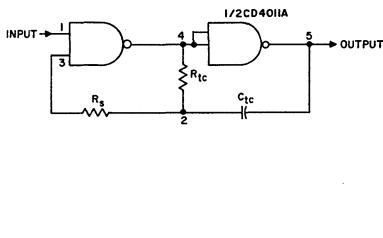


Fig. 20 - (a) Modulator circuit; (b) waveforms.

Demodulation or envelope detection of pulse modulated waves is performed by the circuit shown in Fig. 21a. The carrier burst is inverted (by Inverter A), and its first negative transition at point 2, turns on the diode (D) to provide a charging path for  $C_{TC}$  through the n-channel resistance to ground. On the positive transition of the signal (at point 2), the diode is cut off and  $C_{TC}$  discharges through  $R_{TC}$ . The discharge time constant ( $R_{TC} C_{TC}$ ) is much greater than the time of the burst duration. Point 3, therefore, never reaches the switch point of inverter B until the burst has ended. The waveforms for 4 points in the circuit are shown in Fig. 21b.

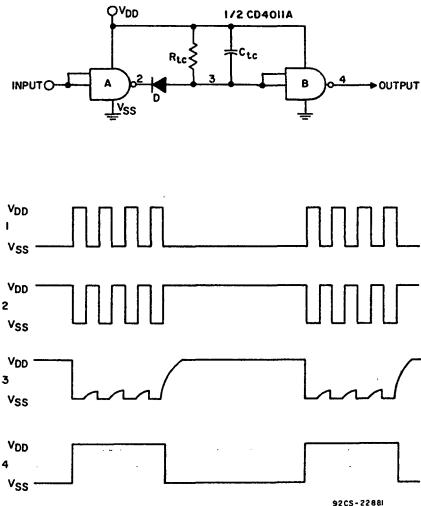


Fig. 21 - (a) Demodulator circuit; (b) waveforms.

## A COS/MOS PCM Telemetry and Remote Data Acquisition Design

by A. Young and D. Block

### Introduction

The data explosion has brought with it a tremendous demand for acquisition stations capable of providing information to a central location for recording and processing. A particular challenge to designers is remote stations for geologic, oceanographic, and space applications where high reliability of data must be combined with low power dissipation to conserve power supplies.

Pulse code modulation (PCM) and COS/MOS are an excellent combination for these applications since COS/MOS devices have inherently low standby and operational power requirements. The wide range of supply voltages (3 to 15 volts) from which COS/MOS circuits can operate reduces power-supply regulation requirements and, in addition, permits emergency power sourcing from convenient alternate supplies. PCM telemetry systems designed to work in severe electrical-noise environments can also benefit from the inherently high noise immunity of COS/MOS devices (typically 45 percent of the supply voltage). Finally, both analog and digital data can be switched through COS/MOS devices; this feature allows convenient multiplexing and interfacing of the telemetry logic with the external world.

The wide range of circuits from simple gates to complex multiplexers and arithmetic units available as standard parts in the COS/MOS CD4000 family allows the realization of the functional elements of PCM telemetry systems with a minimum number of components. The ease of system design resulting from the availability of MSI functions and the tolerant nature of the COS/MOS devices can result in reduced design time and reliable system operation. For critical applications, COS/MOS parts are also available in Hi-Rel versions processed to MIL-STD-883 or MIL-STD-38510.

This note contains descriptive background material on telemetry systems plus examples of typical systems for both immediate and remote data conversion and transmission. Parts from the CD4000 family are used to show how various sections of the system may be realized in the general case. The exact configuration of any specific system would, of course, depend on the unique requirements of the application.

### GENERAL CONCEPTS

#### Format

The order in which data channels are sampled is of fundamental importance to the operation of the systems. This ordering of data is called the "format." The smallest unit of digital data is a "bit" (either a logic 1 or logic 0) and the smallest number of bits handled as a single entity is called a "word." The word length or number of bits in each word is determined by the accuracy with which analog information is to be converted to an equivalent digital word; the greater the accuracy the more bits required. Two types of words are used in a telemetry system: control words containing synchronization or parity bits and data words containing the actual information to be transmitted. Words are grouped together into frames. A frame contains one control word and an integral number of data words. The format, then, refers to the sequence of words within a frame. Fig. 1 shows a typical format of N words grouped into a frame.

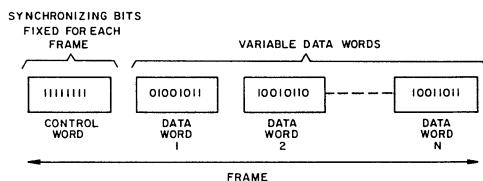


Fig. 1—Basic data format. 92CS-23356

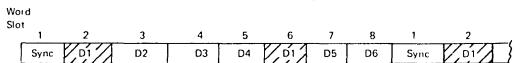
### Information Transmission Rates

To accurately reconstruct at the receiver end of a telemetry system events occurring at the transmitting end, data must be sampled at a rate at least as fast as the fastest changing bit in the data word. Once this rate is determined, the bit rate to be transmitted can be found from the following expression:

$$\text{Bit Rate} = (\text{Word Length}) (\text{Frame Length}) (\text{Sampling Rate}) \quad (1)$$

Thus, for a sampling rate (SR) of 100 samples per second (SPS), a frame length of 10 words, and a word length of eight bits, the bit rate (BR) is 8 kilobits per second (kBPS).

A disadvantage of the format in Fig. 1 is that it requires the sampling rate to be the same for each input. However, many applications have inputs which change at different rates, and for maximum efficiency a range of sampling rates is desirable. There are two techniques which may be used to accomplish sampling rate variation: subcommutation and supercommutation.



BR = 6.4 kBPS  
SR = 100 SPS Word Slot (8-bit words)

(a)

Word Slot	1	2	3	4	5	6	7	8	9	10
Sync	D1	Subframe Sync	D2	D3	D4a	D1	D5	D6		

BR = 6.4 kBPS  
SR = 100 SPS Word Slot (8-bit words)

(b)

Main Frame	1	2	3	4	5	6	7	8	Frame Number
Subframe	Sync	D1	Subframe Sync	D3	D4a	D1	D5	D6	1
Subframe	Sync	D1	D2a	D3	D4b	D1	D5	D6	2
Subframe	Sync	D1	D2b	D3	D4a	D1	D5	D6	3
Main Frame	Sync	D1	Subframe Sync	D3	D4b	D1	D5	D6	4

BR = 6.4 kBPS  
SR = 100 SPS Word Slot (8-bit words)

(c)

92CS - 23357

Fig. 2-(a) Supercommutation of channel D1 in word slots 2 and 6;  
(b) subcommutation of word slots 3 and 5; (c) shorthand representation of (b).

In supercommutation, as shown in Fig. 2(a), data channels are repeatedly sampled within the same frame to obtain sampling rates that are multiples of the fundamental rate. For the format parameters shown, D1 is sampled at 200 samples per second, twice the fundamental rate. The process of supercommutation is equivalent to dividing the frame-length term of Eq. (1) by the number of repetitions of a given channel. Proper supercommutation requires that the word slots be evenly spaced in a frame.

Subcommutation, Fig. 3(b), is an alternate sampling of data channels from frame to frame to obtain sampling rates that are less than the fundamental rate. In Fig. 2(b), channel D2a is sampled every fourth frame, as are channels D2b, D2c, and the subframe sync channel. Channels D4a and D4b are sampled every other frame. Fig. 2(c) is a shorthand notation of this format. The process of subcommutation is equivalent to multiplying the frame-length term of Eq. (1) by the subcommutation length.

The entire data cycle (the smallest number of words that repeat periodically) is called a "subframe" and includes the main frame and subsequent frames. Subcommutation can be applied to more than one main frame word, but the number of subcommutations must have an integral relationship to all other subcommutation lengths. For example, subcommutation lengths of 2, 4 and 16 in the same format are acceptable, but lengths of 2, 8 and 10 are not because 10 is not an integral multiple of 8. The maintenance of integral relationships in subcommutation assures the synchronization of subcommutated channels required for decommutation.

## A DESIGN EXAMPLE

### Format

Manipulation of the bit-rate, frame-length, and subframe-length parameters is required to obtain an optimum format from sampling rate requirements. Consider, for example, the requirements for transmitting 8 channels of analog information, identified as A1 through A8 in Fig. 3(a), and one

Word Slot	1	2	3	4	5	6	7	8	9	10
Sync	A1	A2	A3	A4	A5	A6	A7	A8		D1

BR = 8x10x200 = 16 k BPS for 8-bit words

A = Analog Data Channels  
D = Digital Data Channels

(a)

Word Slot	1	2	3	4	5	6	7	8
Sync	A1 (200)	Subframe Sync (100)	A3 (50)	A4a (50)	A1 (200)	D1 (100)	A5 (100)	
		D2a (25)		A4b (50)				
		D2b (25)						
		D2c (25)						

(Numbers in parentheses are sampling rates)

BR = 8x100x8 = 6.4 kBPS for 8-bit words

(b)

92CS - 23358

Fig. 3-(a) Format configuration 1; (b) format configuration 2.

channel of digital information (D1) where the required sampling rates are:

- (a) 200 samples per second (SPS) for one analog channel
- (b) 100 SPS for two analog and one digital channel
- (c) 50 SPS for two analog channels
- (d) 25 SPS for three analog channels

One solution would be to sample all channels at 200 SPS. This sampling rate meets the requirement of the most active channel at the cost of over-sampling the others. The resultant ten-word frame shown in Fig. 3(a) would require a bit rate of 16 kBPS for an eight-bit word length. This format is inefficient and results in having to record and process redundant data.

An alternate format, shown in Fig. 3(b), consists of eight 100-SPS main frame words with supercommutation and subcommutation used to generate alternate sampling rates. Supercommutation of word slots 2 and 6 produces a 200-SPS channel. Subcommutation of word slot 5 twice and slot 3 four times produces 50- and 25-SPS channels, respectively. The bit rate required by this format is 6.4 kBPS or roughly one-third of that required by the previous format. The reduction is accomplished with only a small increase in programming hardware.

### System Hardware

A block diagram of the functions needed for the telemetry system of the design example above is shown in Fig. 4. The system includes both analog and digital multiplexers, an analog-to-digital converter and digital data-signal conditioner, a programmer, and an output formatter, synchronizer and serializer. The following sections discuss the implementation of these functions with standard COS/MOS CD4000-family parts.

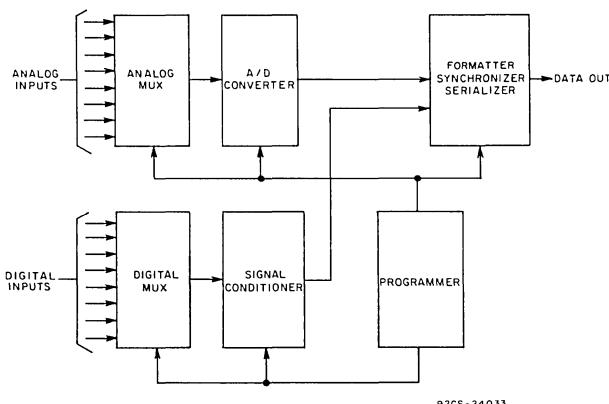


Fig. 4—PCM telemetry system.

## Programmer

The Programmer provides basic timing and system synchronization by reducing the bit-rate clock timing to words, frames, and subframes. In general, counters and decoders are required to generate the format matrix column and row dimensions. The COS/MOS IC family includes several devices that aid in the design of format counters and decoders; one such device is the CD4018A, Presettable Divide-by-N Counter. One or more CD4018A's can provide a large selection of frame and subframe

lengths. The CD4017A (Decade Counter plus Ten Decoded Outputs) or the CD4022A (Divide-by-Eight Counter with Eight Decoded Outputs) may be used instead to generate 8 or 10 decoded states. The internal decoding of these devices greatly reduces the number of IC's required in the Programmer. The CD4024A, CD4040A, and CD4020A, 7, 12, and 14-stage binary counters, respectively, can be used to generate longer binary frame/subframe lengths. Decoding of these counters can be performed by standard COS/MOS gates. The Programmer of Fig. 5 has been designed with six COS/MOS IC's.

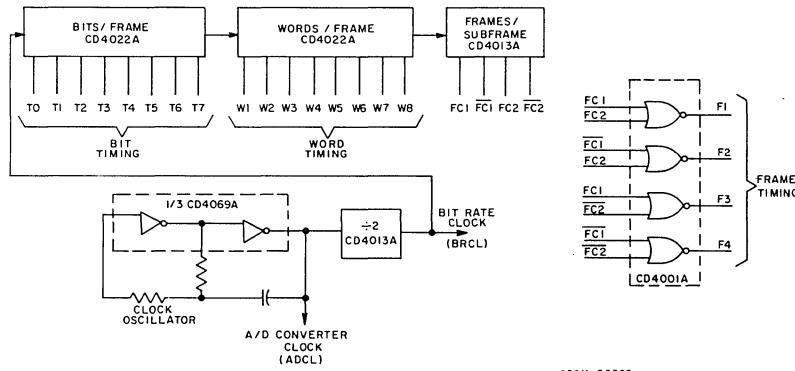


Fig. 5—Programmer timing generation.

### Handling Analog Inputs

Analog input channels to the PCM system of Fig. 4 are switched to an A/D converter, and the resultant digital word transferred to a parallel-to-serial converter for serial readout. Synchronization of the A/D operation is explained below. Analog switching can be done with CD4066A transmission gates, as shown in Fig. 6. Switching of the gates is controlled by the word and frame counters properly decoded to generate the format of Fig. 3(b).

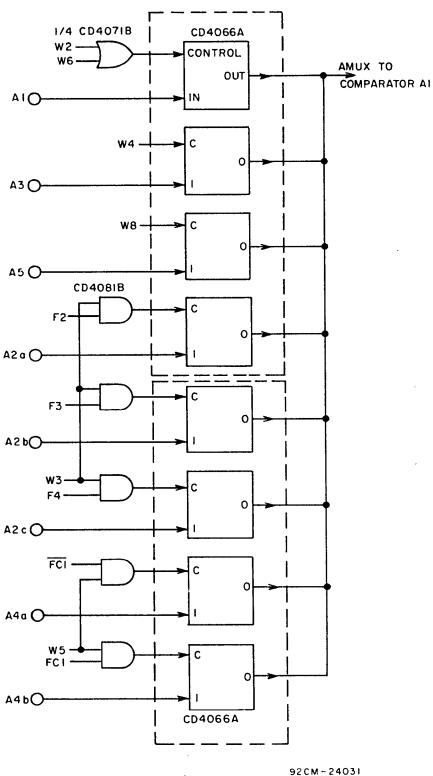


Fig. 6—Analog multiplexer.

The accurate conversion of analog inputs to digitally coded words is a major function of PCM systems. The logic required to control conversions using the successive approximation technique can be implemented with standard COS/MOS circuits. Also, the analog portion of the A/D converter can be simplified by the use of COS/MOS devices, depending upon the accuracy and speed required.

A COS/MOS A/D converter design using the successive approximation technique is shown in Fig. 7. A timing sequence to encode an analog input of 1.480 volts is given in Fig. 8. The converter works as follows. Operation is initiated by the programmer when the next word-slot is assigned to an analog input. At that time (SO) the A/D holding register is set to 1000000 (half scale). This action generates a reference voltage ( $V_R$ ) of 2.5 volts which is applied to comparator A1. The comparator output is zero if  $V_R$  is greater than AMUX (AMUX is the sampled input voltage from the multiplexer), hence the D inputs to the register elements are zero. At time S1 the first flip-flop is clocked to zero and the second flip-flop is set to the one state. The resulting reference voltage (1.25 volts) is less than AMUX this time, and the comparator output goes to the one state. At time S2, the second flip-flop is clocked to one, and the third flip-flop is set to the one state. This procedure continues until all the bit weights have been considered for inclusion in the encoded word. For an 8-bit system with a 5-volt reference, the lowest discrete level of quantization is 19.6 millivolts, and the maximum theoretical accuracy is 0.4 percent. However, for the system shown in Fig. 7 where COS/MOS flip-flops drive a 200-kilohm resistor ladder directly, an accuracy of 1.5 to 2 percent can be expected with conversion rates of approximately 10 kBPS. This encoder can handle the data requirements of most operational and surveillance applications as well as some experimental applications. The system can be made to operate more accurately if the impedance of the most significant bit (MSB) switches is reduced. This can be done by using CD4041A low-impedance buffer units between the flip-flop outputs and the resistor ladder on the first two flip-flops. The CD4041A's have output impedances of less than 200 ohms at 5 volts, either sourcing or sinking current, and permit construction of an 8-bit converter with a relative accuracy of one percent or less.

An alternate method of constructing the A/D converter so that analog signals both above and below ground can be handled is shown in Fig. 9. Here the CD4054A's are used as level shifters to convert the 0- to +5-volt levels from the holding register to -5- to +5-volt signals to the resistor ladder. By connecting one end of the ladder to -5 volts,  $V_R$  is allowed to range between -5 volts and +5 volts. By judicious choice of power supplies, analog voltages between  $\pm 7$  volts could be accommodated using this scheme. (Another scheme for A/D conversion is given in reference 2.) The entire telemetry system could have been run with  $V_{DD} = 5$  V and  $V_{SS} = -5$  V; level translators would not then be necessary. However, to minimize overall dissipation (dynamic power is proportional to  $V^2$ ) the system was designed to operate with  $V_{DD} = 5$  V and  $V_{SS} = 0$  V.

A/D converters are subject to numerous error sources, many of which are rather subtle. Temperature variation is one of the major causes of error. Changes as small as  $10^\circ\text{C}$  can cause an output variation equivalent to a quantizing level. Other sources of error which must be considered in a practical design include such parameters as sampling-rate variations, aperture time, interpolation errors, source impedance, and multiplexer leakage. Trade-offs between cost, size and power must also be made in determining the optimum system for a given application.

A timing diagram showing bit-timing assignments in relation to the A/D conversion cycle is shown in Fig. 8.

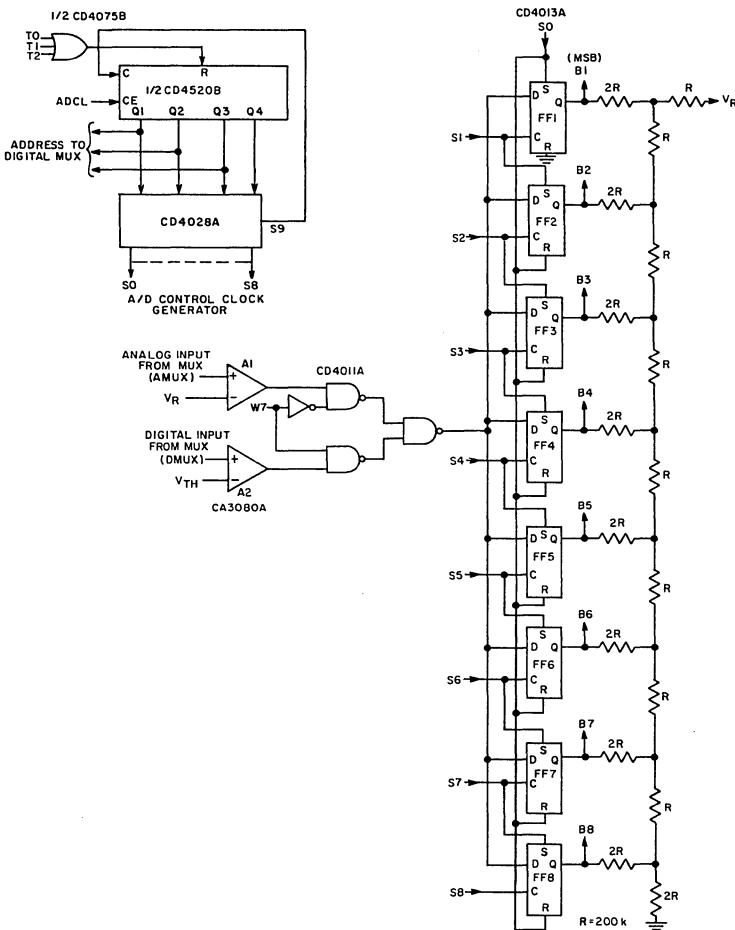
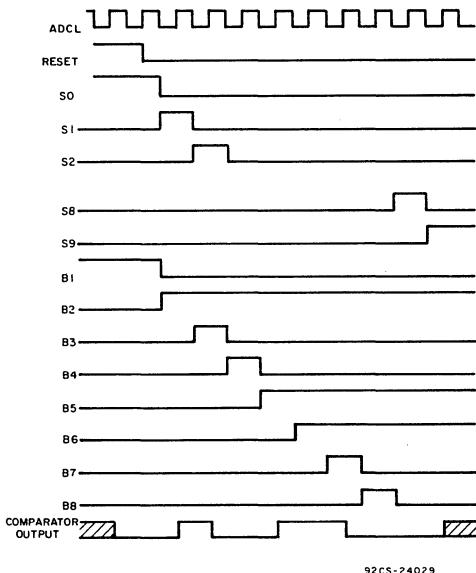


Fig. 7—Successive-approximation A/D converter.

### Handling Digital Inputs

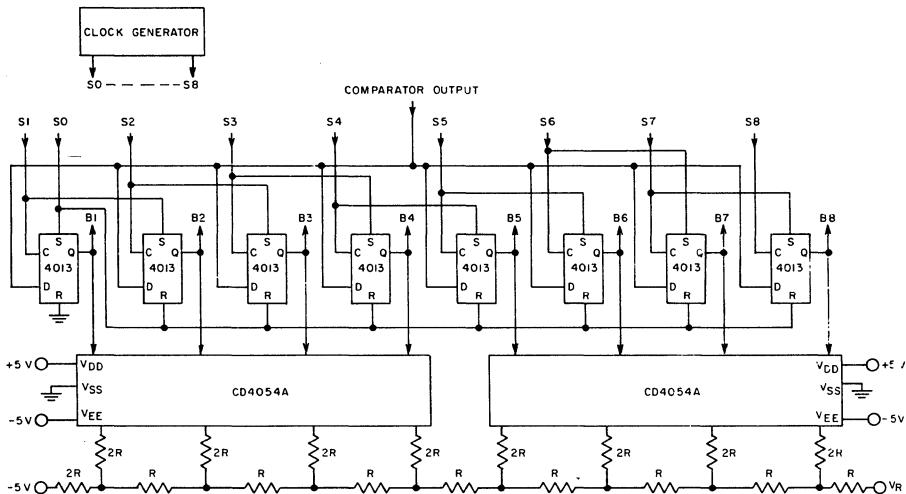
In the most general case, the digital-word input to the PCM system could have logic levels degraded as the result of noise, offsets, or other causes, or it could consist of simple analog voltages to be quantized to single-bit resolution. In the latter case, the concern is only that the input voltage is above or below a given threshold. In the former case, comparison of the in-

put-voltage level against a reference would be used to re-establish solid logic one and zero-voltage levels. This process is referred to as "signal conditioning." Thus, Fig. 7 shows digital inputs being put through comparator A2 for conditioning and being stored in the A/D holding register. In the case of digital data, the ladder network hanging on the register is superfluous. Digital data is simply stored in this register for convenience (to avoid having to create a separate register and controls) and to keep timing and synchronization constant.



92CS-24029

Fig. 8—A/D timing for encoding an analog input of 1.480 volts.



92CM-24030

Fig. 9—Alternate A/D analog section.

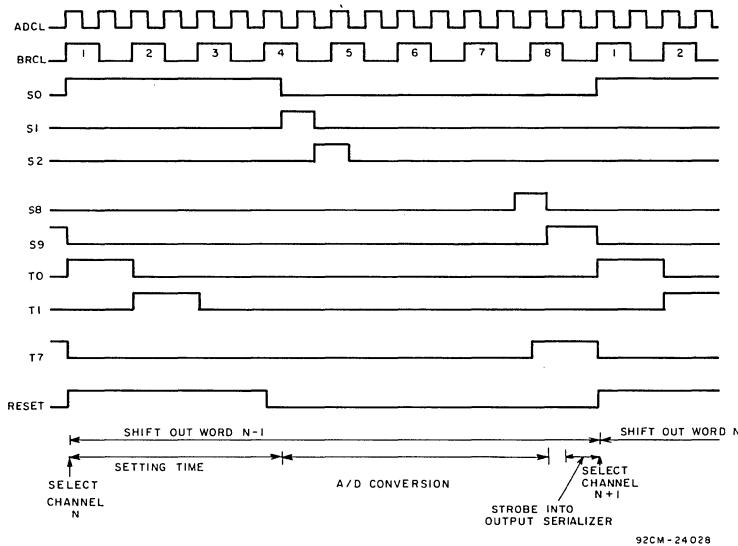


Fig. 10—Bit timing assignment.

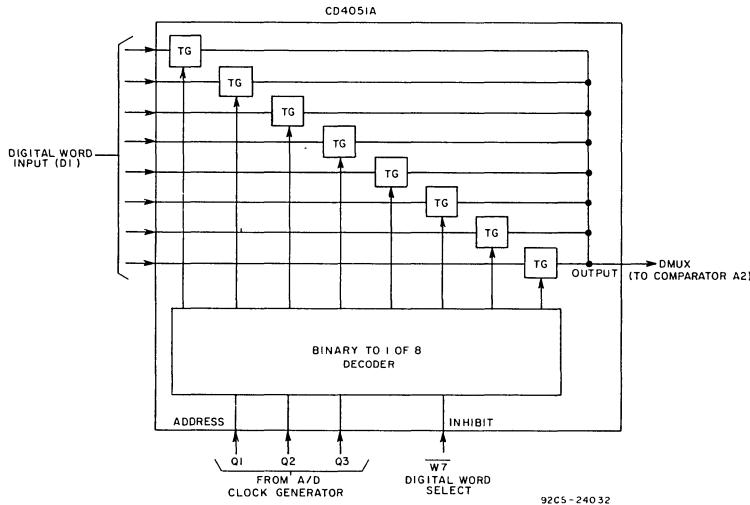


Fig. 11—Digital multiplexing.

The digital input word is first multiplexed into a serial data stream using the CD4051A, as shown in Fig. 11. At time SO, the first flip-flop of the holding register is set to the 1 state, and will be conditionally reset depending on the output of comparator

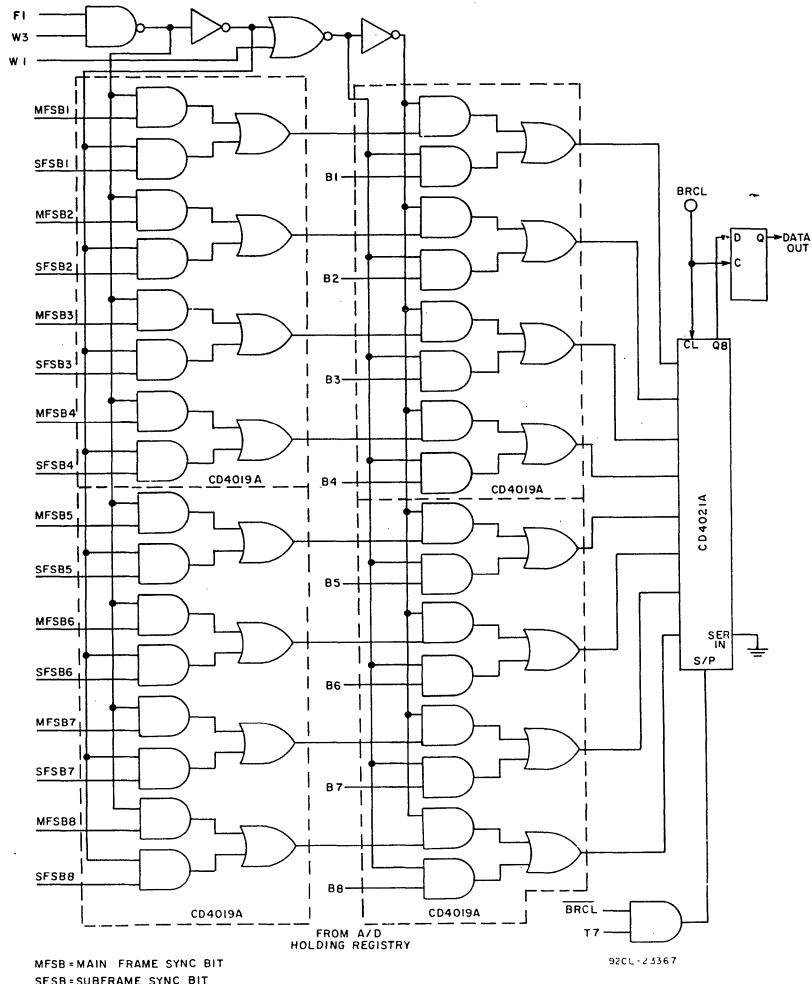
A2 at the end of time SO. (Refer to the description of operation of the A/D converter for a more detailed explanation of this cycle.) The sequence is repeated for each bit until the entire word has been entered into the holding register.

## Data Output

At the appropriate time determined by the format, the output serializer gathers data from one of three sources: a data word from the A/D holding register, or control words from the main frame-sync word generator or the subframe-sync word generator. The 8-bit parallel word is loaded into a CD4021A shift register, as shown in Fig. 12, at the end of bit period T7.

and then clocked out at the bit rate. To preserve the symmetry of the last bit period, a flip-flop is added to the end of the register. Selection of data to the register can be performed by a double rank of CD4019A's. Sync-bit patterns are normally fixed for a given system, and the bit lines are hand-wired to  $V_{DD}$  or  $V_{SS}$  in correspondence with the ones and zeros of the chosen sync pattern.

The output data can feed a computer directly or can modulate an rf carrier for telemetering to a distant data sink.<sup>2</sup>



*Fig. 12—Sync and subframe sync word generator, output data formatter, and serializer.*

## System Integration

A diagram of the entire PCM telemetry system of Fig. 4 is shown in Fig. 13; system timing is shown in Fig. 10.

## Remote Data Acquisition

Many industrial-control and data-management systems are not efficiently served by fixed-format PCM systems. Their requirements are better satisfied by slaved-data acquisition subsystems in which data and control is provided on request, a method that substantially reduces redundant data and transmission rates and that provides control capability at remote locations. The PCM telemetry system previously described is adaptable to this form of operation. The implementation of the

logic of remote slaved-data acquisition systems with COS/MOS devices is desirable because the power consumption of the system is reduced significantly as the switching activity of the circuit decreases.

A slaved Programmer must include a channel address-register, data-request recognition logic, and output transfer-control logic. The format is defined by an external programming source and is not constrained by the acquisition system except for maximum channel capacity; format words-per-frame and frames-per-subframe counters are not necessary. The interface can range from a single wire to several parallel buses; Figure 14 shows block diagram of a typical interface scheme. There are five control lines in the system: CLOCK, DATA REQUEST, REQUEST ACCEPTED, BUSY and DATA READY. A single, bi-directional line is used to send the desired channel address to the slaved programmer and to return the requested data.

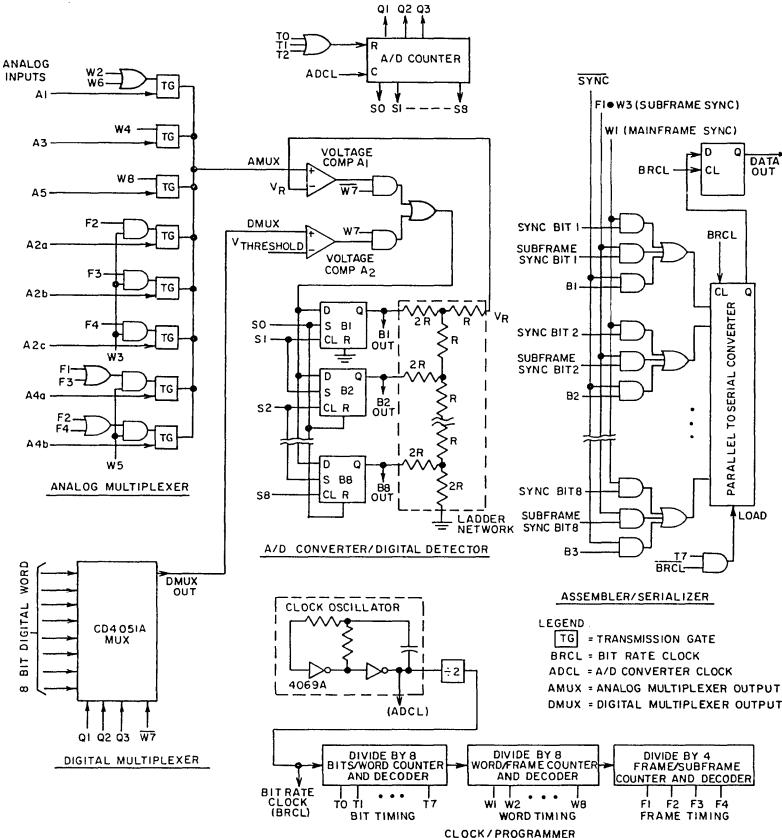
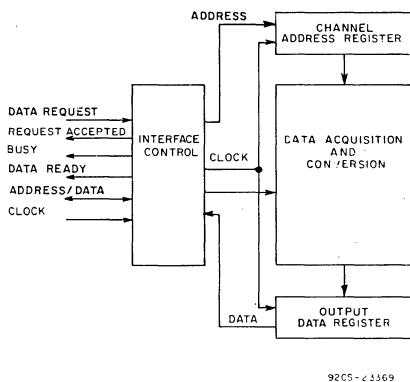


Fig. 13—Diagram of PCM telemetry system of Fig. 4.

The block diagram in Fig. 15 shows the main functional units of the interface scheme of Fig. 14. A request is initiated by



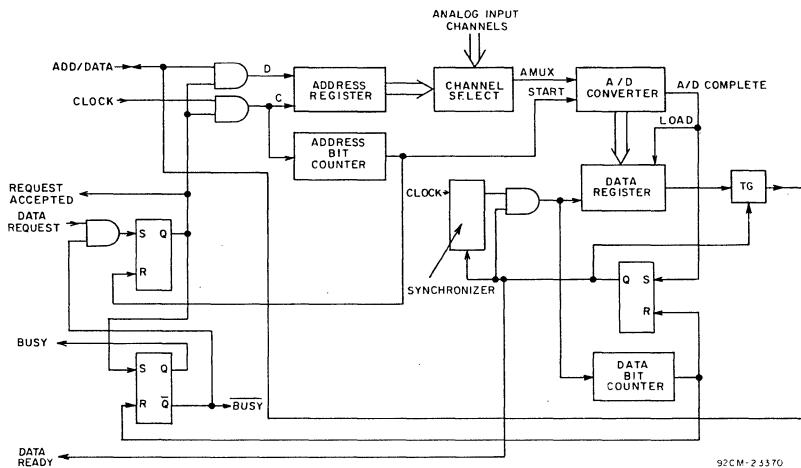
*Fig. 14—Slaved system.*

applying a logic 1 to the DATA REQUEST line. The control logic services requests on a first-in-first-out basis, and ignores any requests initiated while it is in the BUSY state. When a request is initiated at a valid time, a REQUEST ACCEPTED pulse is generated, the BUSY line is set to 1, and the input to the channel-address register is enabled for loading. After the channel-address

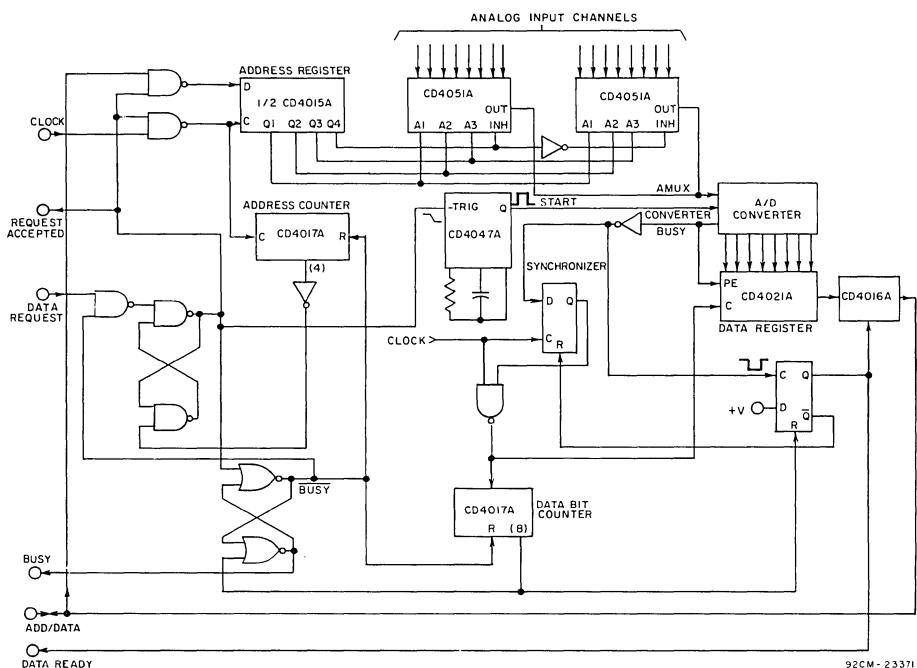
information is received, the requested data is digitized, the DATA READY line is set to 1 and the output data register is clocked onto the ADDRESS/DATA line. The control logic then resets itself, and the system is ready to acquire a new data word.

The implementation of a 16-channel analog system using COS/MOS standard parts is shown in Fig. 16; the associated timing diagram is shown in Fig. 17. A DATA REQUEST sets the data-request flip-flop (REQUEST ACCEPTED) and enables the Clock and Address lines to the CD4015A channel-address register. When the CD4017A address bit-counter indicates that the address has been received, the DATA REQUEST flip-flop is reset, all inputs to the channel-address register are disabled, and one of the 16 input channels is switched to the converter through a CD4051A. The BUSY flip-flop, which was set by the REQUEST ACCEPTED signal, disables any further inputs until the cycle is completed.

A/D conversion can be performed as described above or in reference 2. At the end of the A/D conversion period, the results of the conversion are loaded into a CD4021A shift register, and the DATA READY flip-flop is set. A CD4016A transmission gate is turned on by this signal, and the shift-register output to the ADDRESS/DATA line is enabled. A separate flip-flop is used to synchronize the output with the master clock, assuring that a full clock period is available for each bit. Output data is clocked onto the ADDRESS/DATA line and the clock pulses counted in a CD4017A counter to determine the end of the transfer time. At the end of this time period, the BUSY and DATA READY signals are cleared, and the control flip-flops and counters are reset for the next request.

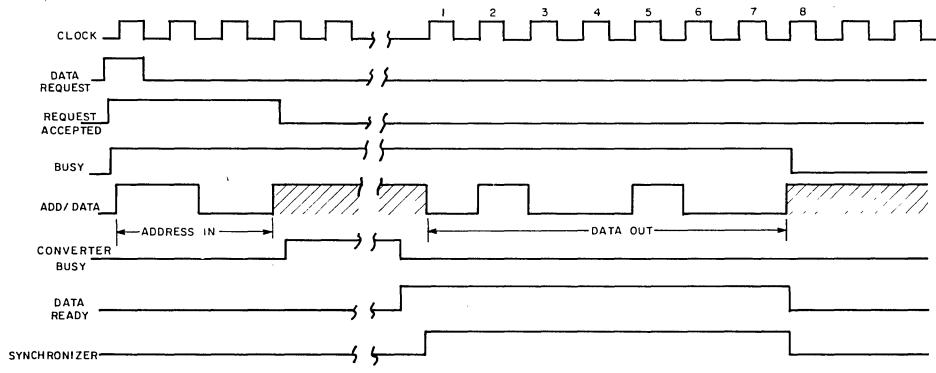


*Fig. 15—Slaved programmer.*



92CM-23371

Fig. 16—Channel-slaved programmer using COS/MOS standard parts.



92CM-23372

Fig. 17—Slaved programmer timing diagram.

### Conclusions

The options available to the designers of data acquisition systems to meet operational requirements are as numerous as the applications for such designs. Features such as extended accuracy, sample-and-hold, selectable input levels, high data-input impedance, control outputs, limit checking, serial data acquisition, calibration-signal output, and digital data processing can be added to the basic system described here. The COS/MOS CD4000 integrated-circuit family provides features particularly suited to telemetry or related data-systems design, and the large number of standard parts available gives the designer consider-

able flexibility to achieve the goals of his application.

### References

1. "Design of Fixed and Programmable Counters Using the RCA CD4018A Presettable Divide-By-'N' Counter," J. Litus, Jr. RCA Application Note ICAN-6498.
2. A technique for generating and subsequently decoding biphasic FSK is described in: "A Typical Data-Gathering and Processing System Using CD4000A-Series COS/MOS Parts"; D. Block, RCA Application Note ICAN-6210.

## Power Supplies for COS/MOS

D. Blandford  
A. Bishop

Two of the major advantages of COS/MOS logic systems are their low power dissipation and ability to operate over a wide range of supply voltages. These features permit the use of simple, small, low-cost power supplies. Examples of various COS/MOS power-supply circuits and their relative costs are given in the following Note along with the factors important in their design. These examples are intended as a guide rather than the optimum design for a particular system.

### DESIGN EXAMPLES

Ten examples of power-supply circuits for use in COS/MOS logic systems are described below. The systems are employed in applications ranging from general-purpose, low-frequency types to those operating at high noise immunity and high frequency. The component values for each power-supply circuit are given for three system sizes, 20, 50, and 100 COS/MOS devices. It is assumed that each system is composed 60 per cent of gate circuits and 40 per cent of MSI circuits, although, as explained below in the section concerning design considerations, these proportions are, in general, not important.

### Low-Frequency Systems

The main requirement in a low-frequency (50-kHz) system is low cost. A  $V_{DD}$  of 5 volts yields a low supply current of 60 microamperes per device and a reasonable noise immunity of 1.5 volts in each logic state. This type of power supply, Fig. 1,

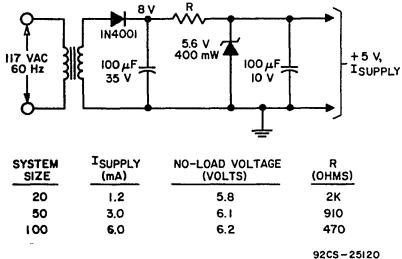
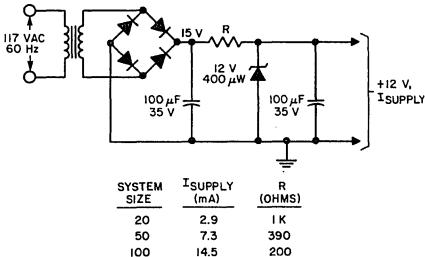


Fig. 1 – Power supply for a low-frequency system.

is used in general-purpose applications, such as digital instruments, remote monitoring equipment, and computer peripherals.

If higher noise immunity is required, for example, in an industrial-control application, a higher value of  $V_{DD}$  would be needed. At 12 volts, the noise immunity is 3.6 volts in each logic state. Fig. 2 shows the circuit used in this type of application.



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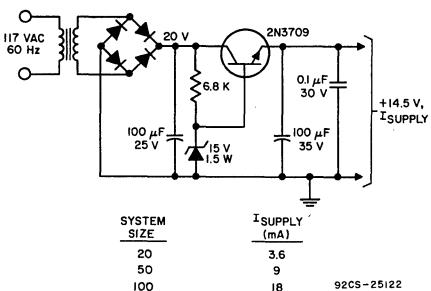
Fig. 2 – Power supply yielding higher noise immunity than the circuit of Fig. 1.

If an application calls for the highest obtainable noise immunity, a  $V_{DD}$  of 14.5 volts could be used. The minimum noise immunity in this case is 4.35 volts in each logic state. Operation at 14.5 volts causes an increase in power consumption and requires that the supply be regulated to ensure that the supply rail does not exceed the maximum rating of 15 volts. Fig. 3 shows the circuit for applications of this type.

### Mixed Systems of 2-MHz and 50-kHz Circuits

10 per cent at 2 MHz, 90 per cent at 50 kHz. A nominal  $V_{DD}$  of 10 volts is selected to enable most COS/MOS circuits to operate at toggle rates greater than 2 MHz, Fig. 4.

50 per cent at 2 MHz, 50 per cent at 50 kHz. The simple zener-diode circuit shown in Fig. 5 is all that is required to provide the nominal 10-volt supply, the power rating of the zener diode depends on the number of devices in the system.



### COS/MOS System Powered by 5-Volt TTL Supply

COS/MOS circuits can be added to or mixed with TTL circuits in a system. The COS/MOS circuits can operate directly from the 5-volt TTL power supply. At 50 kHz the supply current required by the COS/MOS circuit is only 60 microamperes per device, so that for 100 COS/MOS devices, the supply current required is only 6 milliamperes. This current is less than that required by a single TTL quad-gate device, so that the 100 device COS/MOS system can be added to an existing TTL power supply without the need to modify the supply.

### Battery-Powered Systems

COS/MOS circuits, with their low power consumption, are ideally suited for application in portable systems. The wide supply-voltage range permits operation from inexpensive, light-weight dry batteries, which may undergo a large change in voltage capacity from start to end of life. For example, a system containing twenty COS/MOS circuits operating at 10 kHz from three 1.5-volt zinc-carbon dry cells consumes only 220 microamperes. The logic system would operate for more than a year before requiring a battery change.

Retention of data in a semiconductor memory when the main power supply is interrupted or turned off can easily be accomplished by using COS/MOS memory circuits and a standby battery. The battery used could be either a rechargeable nickel-cadmium type, as shown in the memory standby system of Fig. 6, or a dry battery. The memory system shown

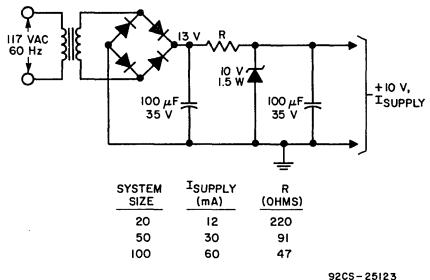


Fig. 4 - Power supply for mixed system consisting of 10 per cent 2-MHz and 90 per cent 50-kHz COS/MOS circuits.

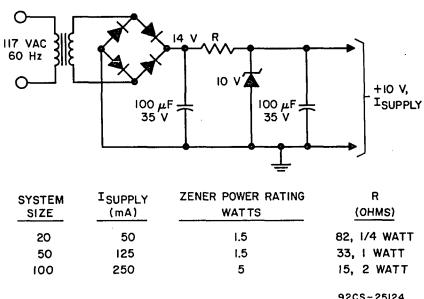


Fig. 5 - Power supply for mixed system consisting of 50 per cent 2-MHz and 50 per cent 50-kHz COS/MOS circuits.

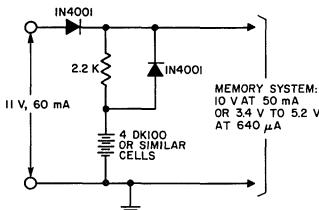


Fig. 6 - Memory standby system.

is a 4K by 8 bit system that uses the CD4061AD, 256-bit RAM. The operating supply voltage is 10 volts, and at a 1-microsecond cycle time, the supply current required is 50 milliamperes. The system power supply trickle-charges the standby battery during normal operation; for the system shown, recharge time is 35 hours. When the main power supply is turned off, the memory is powered by the standby battery. In the system shown, the 32k-bit memory would be powered for approximately one week.

In portable applications requiring operation from a single battery cell, a dc-to-dc converter, Fig. 7, can be used to generate a higher voltage to power the COS/MOS circuits and, possibly, a liquid-crystal display.

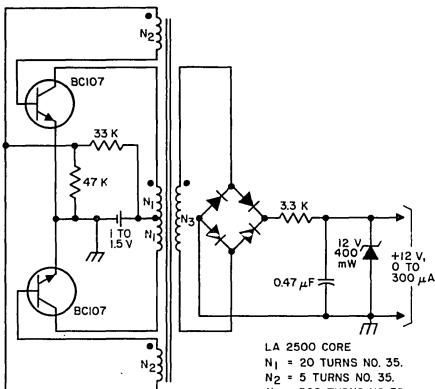


Fig. 7 - DC-to-dc converter.

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### DESIGN CONSIDERATIONS

The primary technical considerations in designing a power supply for a COS/MOS system are the required operating frequency, noise immunity, and power dissipation of the circuits in the system.

#### Operating Frequency

Toggle frequency and propagation delay improve as the supply voltage of a COS/MOS circuit is increased, as shown in Figs. 8 and 9. This improvement occurs because the output resistance of the MOS transistors used in the COS/MOS circuits decreases with increased  $V_{DD}$  while the output mode capacitance remains virtually unchanged, thus reducing the output time constant. The designer should ensure that the worst-case supply voltage is sufficiently high to yield the required switching speed.<sup>1</sup>

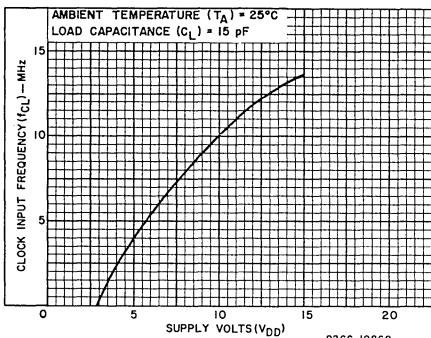


Fig. 8 - Typical clock frequency versus supply voltage for the CD4013A.

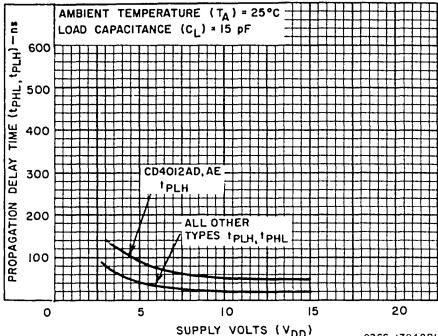


Fig. 9 - Minimum propagation delay time versus supply voltage.

#### Noise Immunity

The switching point of a COS/MOS circuit is typically half the supply voltage,  $V_{DD}$ , so that the noise immunity is typically 45 per cent of  $V_{DD}$  in each logic state. Thus, an increase in  $V_{DD}$  will cause a proportionate increase in noise immunity.<sup>2</sup> The worst-case noise immunity is 30 per cent of  $V_{DD}$ , as shown in Fig. 10. For example, if the required noise

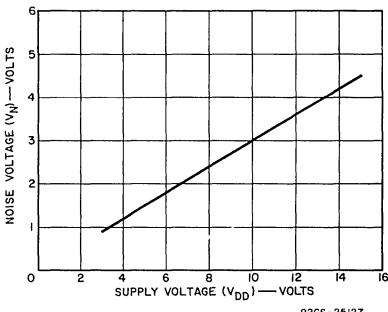


Fig. 10 - Worst-case noise immunity versus supply voltage.

immunity is 1.5 volt in each logic state, then  $V_{DD}$  should be 5 volts or more. Maximum noise immunity is obtained by operating with a 15-volt supply, and is dependent upon maintaining good power-supply rail regulation during peak switching-current conditions. For example, a COS/MOS gate draws 10 milliamperes peak for approximately 50 nanoseconds during a switching mode for a 15-volt supply.

It is good practice to keep the power-bus dynamic impedance low throughout the COS/MOS system. In addition to good ground and supply-bus distribution, 0.01-to 0.1-microfarad ceramic capacitors should be distributed throughout the system and connected from  $V_{DD}$  to  $V_{SS}$ . As a general rule, a 0.01-microfarad capacitor should be used for every four-gate package, and a 0.1 microfarad capacitor for every four MSI packages.

### Power Dissipation

The two previous sections explain the advantages of operating a COS/MOS system at high values of  $V_{DD}$ . However, use of high supply voltages is accompanied by high power consumption. The total power consumed has two components, quiescent or dc power consumption, which increases approximately linearly with  $V_{DD}$ , and switching or ac power consumption, which increases as  $V_{DD}^2$ . Fig. 11 illustrates the typical dissipation of a COS/MOS device.

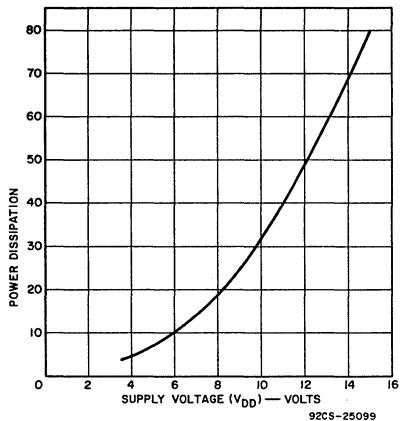


Fig. 11 – Typical dissipation of a CD4011A with a 15-picofarad load at 10 kHz versus supply voltage.

The expected power consumption of a given COS/MOS logic system can be calculated by summing the combinations of dc and ac power consumption of individual devices for expected values of supply voltage, operating frequency, and load capacitance. Generally, for a system larger than about ten devices, it should be sufficient to consider the typical values of power consumption.

A useful guide for calculating system power consumption is shown in Fig. 12. This graph shows the average power

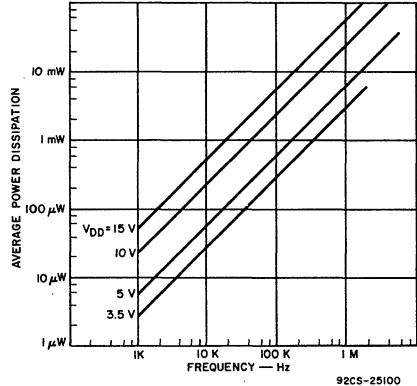


Fig. 12 – Average power dissipation of a CD4000A-series device versus frequency.

consumption per device (e.g., quad NAND, counter, shift-register) versus frequency for various supply voltages at a practical loading of 50 picofarads. For example, assume that the power consumption for a mixture of 100 CD4000A circuits at a  $V_{DD}$  of 5 volts and an operating frequency of 50 kHz is desired. From Fig. 12, the dissipation per device is 300 microwatts, so that the total system dissipation is 30 milliwatts for a supply current of 6 millampères (see practical circuit, Fig. 1). In this example, the dc power is not significant and would typically total less than 1 milliwatt.

If a more accurate value of the system power consumption is required, the contributions from each device may be calculated and summed to give the total. To do this, the value of quiescent dissipation given in the data sheet for the device is used together with the value of ac dissipation. The latter value is taken from the data-sheet graph of dissipation versus frequency at 15-picofarads load. The value obtained is valid for three loads or less; for more than three loads, Fig. 13 is

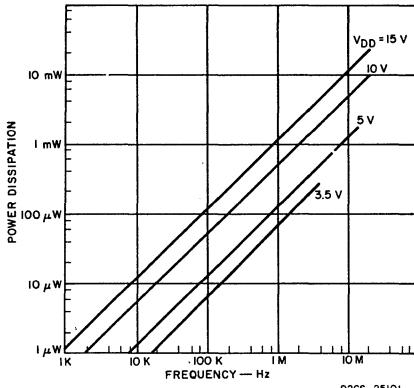


Fig. 13 – Power dissipation per load of 5 picofarads as a function of frequency.

used to determine the power dissipation contributed by the extra loads. For example, assume that the power consumption of a CD4011AE NAND gate at a  $V_{DD}$  of 5 volts and a frequency of 1 kHz with seven loads is desired. From the data sheet, the quiescent power dissipation  $P_Q$  is 25 nanowatts. The dynamic dissipation  $P_D$  for a 15-picofarad load is given in the data sheet as 700 nanowatts. From Fig. 13 the power dissipation  $P_{XL}$  for the four extra loads is 500 nanowatts, so that the total power dissipation  $P_T$ , where  $P_T = P_Q + P_D + P_{XL}$ , is 1225 nanowatts or approximately 1.2 microwatts.

Certain circuits require additional consideration because of their higher than normal power consumption. Such cases include gate circuits having slow input rise and fall times, as shown in Fig. 14. Examples of this type of circuit are RC monostable or astable circuits, and gate circuits with inputs at the end of long transmission lines. Circuits driving large capacitive loads, such as long transmission lines or the clock inputs of non-complementary MOS shift registers, are also representative of circuits with above-normal power consumption. Higher power consumption can also occur at the interface between COS/MOS circuits and transistor drivers, other logic families, and digital displays.

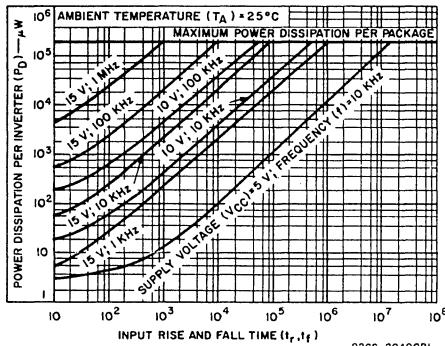


Fig. 14 – Power dissipation as a function of transition time for a CD4049A.

### Regulation

The regulation of a COS/MOS power supply should be designed to maintain  $V_{DD}$  at a value equal to or greater than the value needed to obtain the required switching speed and noise immunity and less than either the maximum  $V_{DD}$  rating of 15 volts or the maximum  $V_{DD}$  required to yield a specific, expected, over-all power-dissipation rating, whichever is lower. The regulator circuit must also suppress any voltage transients that might cause the supply to exceed 15 volts.

### REFERENCES

1. For more information on switching speed see the CD4000A-family data sheets, which contain graphs of switching speed as a function of  $V_{DD}$ .
2. A precise definition of noise immunity is given in the RCA Solid-State DATABOOK Series SSD-203, "COS/MOS Digital Integrated Circuits".

# **Design of Fixed and Programmable Counters Using the RCA CD4018A COS/MOS Presettable Divide - by- "N" Counter**

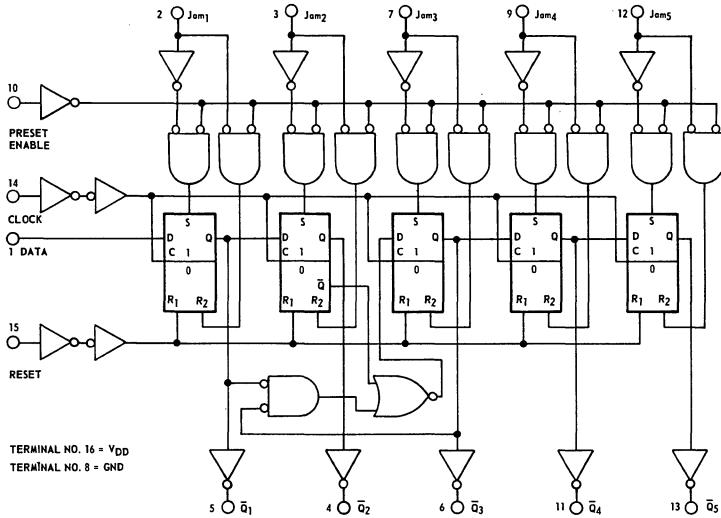
by J. Litus Jr.

The RCA CD4018\* COS/MOS (Complementary-Symmetry Metal-Oxide-Semiconductor) presettable divide-by-“N” counter is designed for use in digital equipment where low power dissipation, low package count, and high noise immunity are primary design requirements. The counter is particularly useful in such systems applications as channel-preset counters in digital frequency synthesizers and

*\*Supplied in plastic dual-in-line package as the CD4018AE, in ceramic dual-in-line package as the CD4018AD and in ceramic flat-pack as the CD4018AK.*

program-counter control. The CD4018A can also be used as a 5-stage parallel input/output holding register. In this application the parallel entry can be controlled by the preset-enable line to perform a 5-stage "latch" operation. This Note describes the use of the CD4018A in single-decade and multi-decade fixed and programmable divide-by-“N” counters. System considerations such as switch simplifications, components minimization, and speed are also discussed.

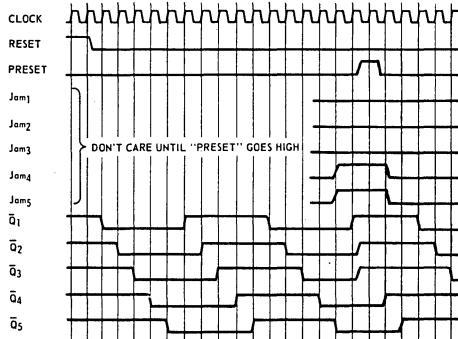
The logic diagram for the CD4018A is shown in Fig. 1. Fig. 2 shows the counting sequence and timing diagram for this device connected as a decade counter.



*Fig. 1 - Logic diagram for CD4018A.*

Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
0	1	1	1	1	1
1	0	1	1	1	1
2	0	0	1	1	1
3	0	0	0	1	1
4	0	0	0	0	1
5	0	0	0	0	0
6	1	0	0	0	0
7	1	1	0	0	0
8	1	1	1	0	0
9	1	1	1	1	0

(a)

("DATA" INPUT TIED TO  $\bar{Q}_5$  FOR DECADE COUNTER CONFIGURATION)

(b)

Fig. 2 - (a) counting sequence for decade-counter operation; (b) timing diagram for decade-counter operation.

The CD4018A consists of five flip-flops that can be connected as a five-, four-, three-, or two-stage Johnson Counter with buffered Q outputs from each stage. Gating is included for presetting the counter. "Clock", "Reset", "Data", "Preset-Enable", and five "Jam" inputs are also provided. The counter is advanced one count at the positive-going transition of the clock. A "high" Reset signal clears the counter to an "all-zero" ( $\bar{Q}$  outputs are all "ones") condition, and a "high" Preset Enable signal allows information on the Jam inputs to preset the counter.

### FIXED SINGLE-STAGE DIVIDE-BY-“N” COUNTERS

Divide-by-10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the  $\bar{Q}_5$ ,  $\bar{Q}_4$ ,  $\bar{Q}_3$ ,  $\bar{Q}_2$ , or  $\bar{Q}_1$  signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of NOR- or NAND-gate packages to gate the proper feedback connection to the Data input line. Fig. 3 shows the feedback connections for divide-by-9, 7, 5, and 3 functions using the CD4011A NAND gate as the feedback circuit.

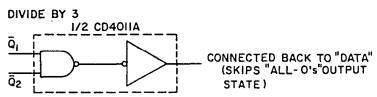
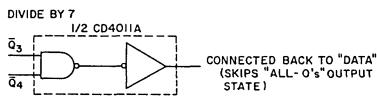
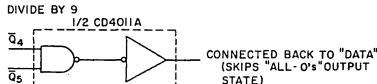
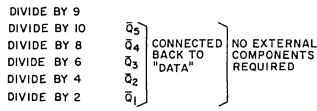
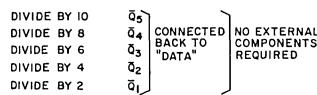
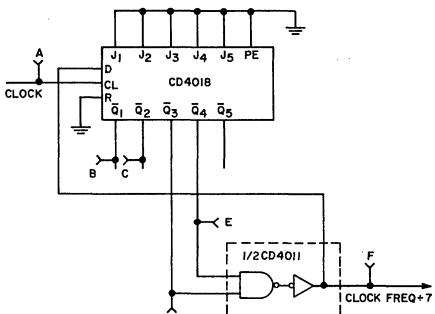
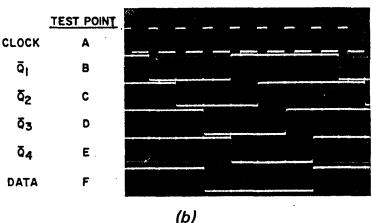


Fig. 3 - External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, and 2 operation.

Fig. 4 shows the divide-by-seven configuration in detail. The logic diagram and pertinent waveforms are shown in Figs. 4a and b. Fig. 4c shows the counting sequences for a divide-by-eight and a divide-by-seven configuration. Division



(a)



Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
0	1	1	1	1
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	0	0	0	0
5	1	0	0	0
6	1	1	0	0
7	1	1	1	0

(b)

Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
0	1	1	1	1
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	1	0	0	0
5	1	1	0	0
6	1	1	1	0

(c)

Fig. 4 - CD4018A in a fixed divide-by-7 counter configuration:  
 (a) logic diagram; (b) timing waveforms; (c) counting sequences for a  $\div 8$  and a  $\div 7$  Johnson Counter.

of the clock frequency by seven is accomplished by altering the counting sequence so as to skip the "all zeros" state of a divide-by-eight counter. The divide-by-seven counting sequence proceeds as in a normal 4-stage Johnson counter until count 3 (0001) at which point  $\bar{Q}3=0$  and  $\bar{Q}4=1$ . At this point the CD4011 Agates  $\bar{Q}3$  and  $\bar{Q}4$  to put a 0 on the Data input to the first stage. Thus, count 4 will be 1000 instead of 0000 as in the unaltered divide-by-eight sequence. The remainder of the counting sequence proceeds in the normal 4-stage manner.

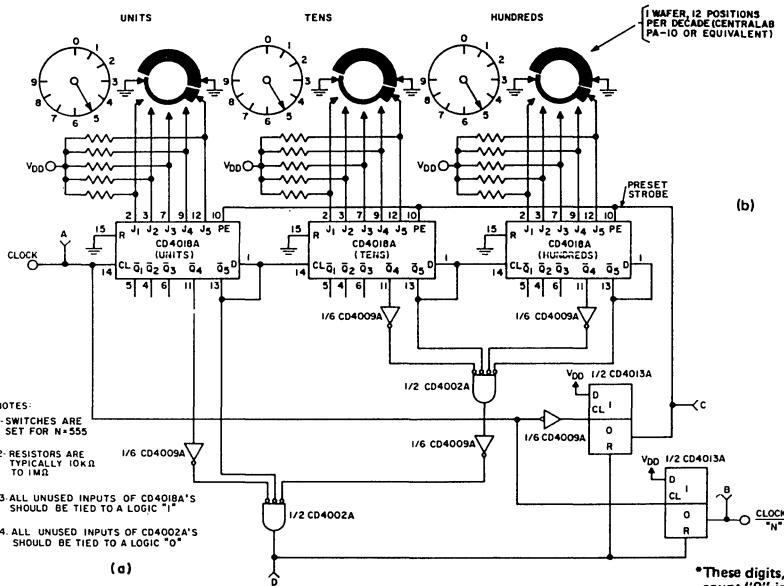
### PROGRAMMABLE MULTI-DECADE DIVIDE-BY-"N" COUNTERS

The CD4018A is especially useful in applications requiring low-power, programmable, divide-by-"N" counting. Two such applications are channel preset counters in digital frequency synthesizers and program counter control.

Fig. 5 illustrates the use of three CD4018 units in a programmable divide by "N" counter, where "N" may be any number from 2 to 999 (counter output is equal to clock frequency divided by N). Extension to higher "N" ranges is readily accomplished by the use of additional CD4018 units. The counter is preset to the value of "N" via the three selector switches. The switches are arranged so that switch position 9 is equivalent to a "0" count in the counter, position 8 is equivalent to a "1" count, position 7 to a "2" count, etc. The counter counts up from the preset value (the N value) to its maximum count (999) and recycles, starting again from the preset value. Fig. 5b shows the counting sequence; oscilloscope photographs of the waveform at various points in the circuit (of Fig. 5a) are shown in Fig. 5c. Fig. 5d shows the N-counter output for various values of N.

The Johnson-Counter configuration utilized in the CD4018A design permits significantly simpler "program-switch" ("N"-Select) implementation than is required in systems that use a BCD decade counter arrangement. The program switch is composed of three standard single-wafer switches, one for each CD4018A (one per decade). This compares with a four-wafer (4-pole) switch per decade for a BCD decade-counter arrangement. Also, the count decoding is much simpler in that only two outputs per CD4018A must be decoded as compared to four for a BCD arrangement. The Johnson-type counter can also operate at higher speeds and provides spike-free decoded outputs.

The configuration shown in Fig. 5 permits frequency division by 2 as a result of performing the Preset function during half a clock cycle. In this mode the maximum allowable frequency of operation is reduced, however. If this reduction in frequency is not acceptable, the logic diagram shown in Fig. 6 can be employed. In this circuit the Preset function is allowed a full clock cycle but the range of frequency division is reduced to 3 to 999. The counting sequence and pertinent timing waveforms for this circuit are shown in Figs. 6b, c, and d, respectively. Typical maximum operating frequency is 4 megahertz, for the counter in Fig. 5 and 6 megahertz for the counter in Fig. 6.

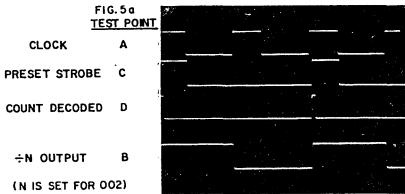


\*These digits, representative of count "9" in each decade, are decoded to give the preset strobe.

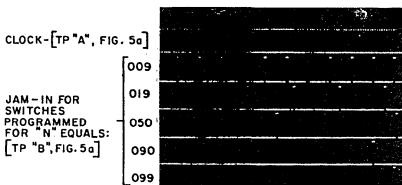
FIRST DECADE (UNITS)						SECOND DECADE (TENS)						THIRD DECADE (HUNDREDS)								
SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1	9	0	1	1	1	1	1	9	0	1	1	1	1	1
8	1	0	1	1	1	1	8	1	0	1	1	1	1	8	1	0	1	1	1	1
7	2	0	0	1	1	1	7	2	0	0	1	1	1	7	2	0	0	1	1	1
6	3	0	0	0	1	1	6	3	0	0	0	1	1	6	3	0	0	0	1	1
5	4	0	0	0	0	1	5	4	0	0	0	0	1	5	4	0	0	0	0	1
4	5	0	0	0	0	0	4	5	0	0	0	0	0	4	5	0	0	0	0	0
3	6	1	0	0	0	0	3	6	1	0	0	0	0	3	6	1	0	0	0	0
2	7	1	1	0	0	0	2	7	1	1	0	0	0	2	7	1	1	0	0	0
1	8	1	1	1	0	0	1	8	1	1	1	0	0	1	8	1	1	1	0	0
0	9	1	1	1	1	0	0	9	1	1	1	1	0	0	9	1	1	1	1	0

(b)

\*These digits, representative of count "9" in each decade, are decoded to give the preset strobe

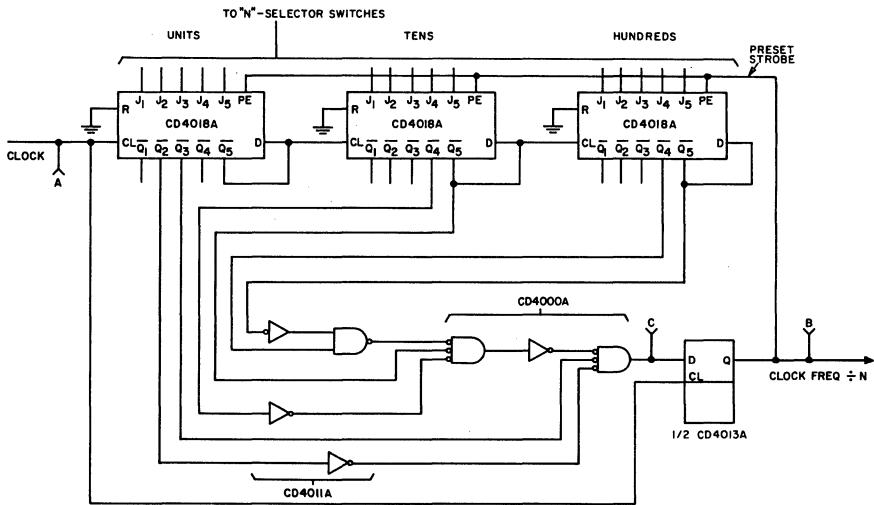


(c)



(d)

Fig. 5 - Three-decade, programmable, divide-by-“N” counter with frequency division from 2 to 999: (a) logic diagram; (b) counting sequence; (c) timing waveforms at various points in the circuit (d)  $\div N$  output for various values of N.



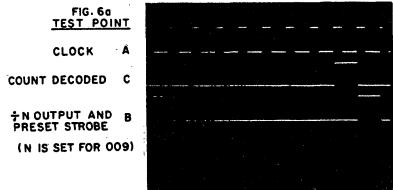
(a) LOGIC DIAGRAM

FIRST DECADE  
(UNITS)SECOND DECADE  
(TENS)THIRD DECADE  
(HUNDREDS)

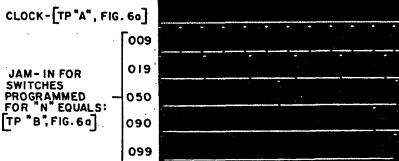
SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1	9	0	1	1	1	1	1	9	0	1	1	1	1	1
8	1	0	1	1	1	1	8	1	0	1	1	1	1	8	1	0	1	1	1	1
7	2	0	0	1	1	1	7	2	0	0	1	1	1	7	2	0	0	1	1	1
6	3	0	0	0	1	1	6	3	0	0	0	1	1	6	3	0	0	0	1	1
5	4	0	0	0	0	1	5	4	0	0	0	0	1	5	4	0	0	0	0	1
4	5	0	0	0	0	0	4	5	0	0	0	0	0	4	5	0	0	0	0	0
3	6	1	0	0	0	0	3	6	1	0	0	0	0	3	6	1	0	0	0	0
2	7	1	1	0	0	0	2	7	1	1	0	0	0	2	7	1	1	0	0	0
1	8	1	1	1	0	0	1	8	1	1	1	1	0	1	8	1	1	1	0	0
0	9	1	1	1	1	0	0	9	1	1	1	1	0	0	9	1	1	1	1	0

NOTE: "N" IS SELECTED BY DIALING IN THE DESIRED PRESET COUNT INDICATED BY THE SWITCH SETTINGS: THE "9" COUNTS FROM THE SECOND AND THIRD DECADE (SHOWN AS **[1 0]**) ARE GATED WITH THE "7" COUNT (SHOWN AS **[1 0]**) FROM THE FIRST DECADE TO ACTIVATE THE "PRESET ENABLE", ONCE PER COUNTER CYCLE.

(b)



(c)



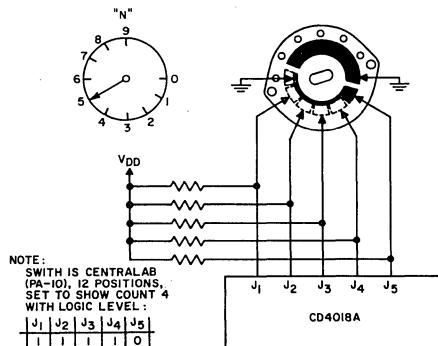
(d)

Fig. 6 – Three-decade, programmable, divide-by-“N” counter with frequency division from 3 to 999: (a) logic diagram; (b) counting sequence; (c) timing waveforms at various points in the circuit; (d) divide-by-N output for various values of N.

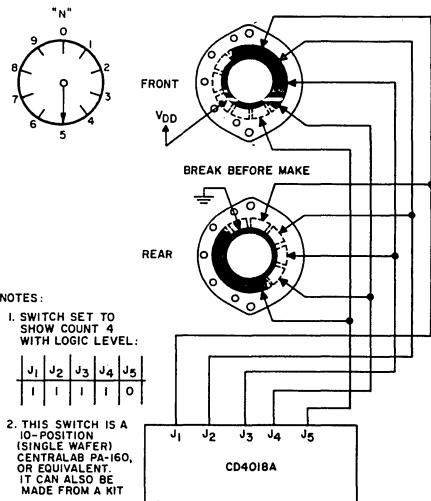
### PROGRAM-SWITCH ("N"-SELECT) OPTIONS

Fig. 7a is a detailed drawing of a standard Centralab 12-position wafer switch and the associated resistor network as used in Fig. 5a. The resistors connected to V<sub>DD</sub> are required to prevent floating inputs on the "JAM" lines. In applications that require lower power dissipations or where component count or space considerations become important, the resistor network can be eliminated by the redesign of the switch. Two such options are shown in Figs. 7b and 7c.

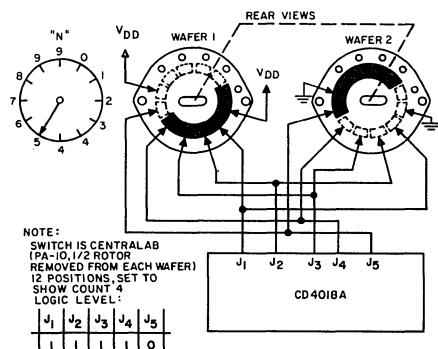
As previously mentioned in the discussion of Fig. 5, the range of N can be extended by adding more CD4018A units. In addition to this type of expansion each stage in the programmable divide-by-N counter can be designed to count to any base or radix. For example, the single stage divide-by-seven counter of Fig. 4 may be used as each stage in a multi-stage programmable counter.



(a)



(c)



(b)

Fig. 7 - Switch configurations; (a) single wafer (standard) per decade; (b) two wafers (modified standard) per decade; (c) single wafer (nonstandard) per decade.

### SUMMARY

The RCA-CD4018A is a versatile counter. Because of the Johnson-Counter design employed, This device permits the design of simple decoding and preset switching circuits. The system can also operate at higher speeds and with much less power dissipation than a comparable BCD decade counter arrangement. Also the CD4018A, a COS/MOS device, possesses all the inherent advantages of this technology.

This versatile device can be used in fixed or programmable divide-by-"N" counters where "N" can vary from two to ten for a single CD4018A and greater than ten for multiple CD4018A stages. From an economical viewpoint, its versatility and low power requirement at high speeds make the RCA-CD4018A the logical choice for counter applications in control and frequency synthesization equipments.

## **Power-Supply Considerations for COS/MOS Devices**

by H.L. Pujol

RCA COS/MOS Digital Integrated Circuits operate at extremely low power dissipation levels. They function reliably with high noise immunity over a wide operating-voltage range. The RCA-CD4000A COS/MOS product line is designed to operate from 3 to 15 volts, which enables system designers to operate RCA COS/MOS devices from unregulated, poorly-filtered supplies, or from a wide variety of single- or multiple-cell battery sources.

This Note describes the salient features of COS/MOS devices which permit operation from such a wide range of power sources and provides the system designer with the necessary information to permit him to design the most economical power source for his COS/MOS system. This Note is applicable to both COS/MOS product lines mentioned above.

### **CHARACTERISTICS OF A BASIC COS/MOS LOGIC INVERTER**

#### **Quiescent Device Dissipation.**

The basic logic inverter (or gate) formed by use of only a p- and an n-type device in series is shown schematically in Fig. 2. When the input lead is grounded or otherwise connected to 0 volts (logical "0"), the n-device is cut-off, and the p-device is biased on. As a result, there is a low-impedance path from the output to  $V_{DD}$ , and an open circuit to ground. The resultant output voltage is essentially  $V_{DD}$ , or a logic "1".

Similarly, when the input voltage is a logic "1", or  $V_{DD}$ , then the n-channel device becomes a low impedance, while the p-channel device becomes an open circuit. The resultant output becomes essentially zero volts (logic "0").

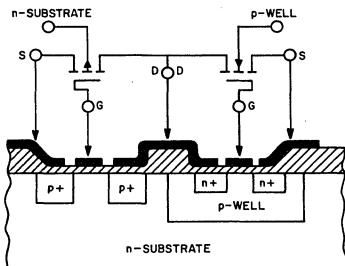


Fig. 1— Cross-section of COS/MOS transistor.

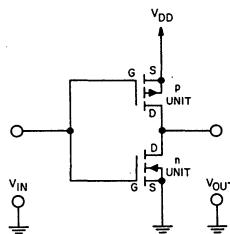
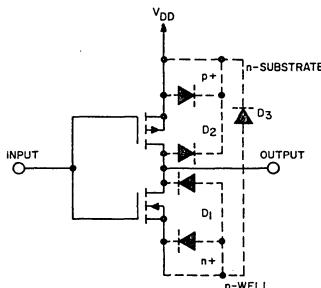


Fig. 2— Basic COS/MOS inverter (schematic).

Note that one of the devices is always cut-off at either logic extreme, and that no current flows into the insulating gates. As a result, the inverter quiescent power dissipation is negligible (equal to the product of  $V_{DD}$  times the leakage current).

A cross section of the COS/MOS inverter as it is formed in an integrated circuit on an n-type substrate is illustrated in Fig. 1. The source-drain diffusions and the p-well diffusion form parasitic diodes (in addition to the desired transistors) at the basic inverter nodes, as shown in Fig. 3. These parasitic elements are back-biased (across the power supply) and contribute, in part, to the device leakage current and thus to the quiescent power dissipation.



*Fig. 3– Basic inverter showing parasitic diodes.*

RCA's product line of COS/MOS devices consists of circuits of varying complexity (i.e., from the dual 4-input logic gate that contain 16 MOS devices, to the more complex 64-bit static shift registers that contain over 1000 devices). These devices occupy different amounts of silicon area and are composed of varying numbers of circuits formed from inverters. Consequently, each device in the family exhibits a particular magnitude of leakage current, depending upon the total effect of device count and parasitic diode area. For example, some logic gates are specified to operate with a typical power dissipation of 5 nW ( $V_{DD} = 10V$ ), but 7-stage counters or registers are specified to operate with a typical power dissipation of 5  $\mu W$  ( $V_{DD} = 10V$ ). Published data includes both typical device quiescent-current levels and maximum levels ( $V_{DD} = 5V$  and  $V_{DD} = 10V$ ). The maximum values are rarely encountered in RCA devices.

#### **Device – Switching Characteristics.**

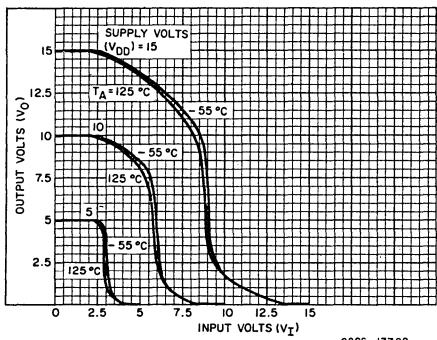
The input/output characteristics for the COS/MOS inverter are shown in Fig. 4. As mentioned earlier the signal extremes at the input and output are approximately zero volts (logic "0") and  $V_{DD}$  (logic "1"). The switching point is shown to be typically 45 to 55% of the magnitude of the power-supply voltage (regardless of the magnitude of the power-supply voltage) over the entire range from 3 to 15 volts. Note the negligible change in operating point from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

These excellent switching characteristics permit COS/MOS devices to be operated reliably over a wide range of voltages, a property not found in other logic forms.

### AC Dissipation Characteristics.

During the transition from a logic "0" to a logic "1", both devices are momentarily on. This condition results in a pulse of instantaneous current being drawn from the power supply. The magnitude and duration of this current depends upon the following factors:

- (a) the impedance of the particular devices being used in the inverter circuit
  - (b) the magnitude of the power-supply voltage
  - (c) the magnitude of the individual device threshold voltages
  - (d) the input driver rise and fall times



*Fig. 4— Typical COS/MOS transfer characteristics as a function of temperature.*

An additional component of current must also be drawn from the power supply to charge and discharge the internal parasitic node capacitances and the load capacitances seen at the output.

The device power dissipation which results from the above current components is a frequency-dependent parameter. The more often the circuit switches, the greater is the resultant power dissipation. The heavier the capacitive loading, the greater is the resultant power dissipation. The power dissipation is not duty-cycle dependent. For all intents and purposes it may be considered frequency (repetition-rate) dependent.

Because the RCA COS/MOS product line ranges widely in circuit complexity from device to device, the ac device dissipations vary widely from device to device. The effect of capacitive loading on the individual devices also varies. Figs. 5 and 6 show a family of curves for a typical gate device and a typical MSI device. These curves, from the published data for the individual devices, illustrate how device power dissipation varies as a function of frequency, supply voltage and capacitive loading.

#### AC Performance Characteristics.

During switching, the node capacitances, within a given circuit, and the load capacitances external to the circuit, are charged and discharged through the p- or n-type device conducting channel. As the magnitude of V<sub>DD</sub> increases, the impedance of the conducting channel decreases accordingly. This lower impedance results in a shorter RC time constant (this non-linear property of MOS devices is due to current saturation at large values of drain-to-source voltage). The result is that the maximum switching frequency of a COS/MOS device increases with increasing supply voltage. (See Fig. 7a).

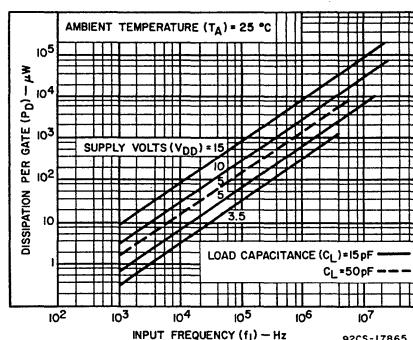


Fig. 5—Basic gate power dissipation characteristics.

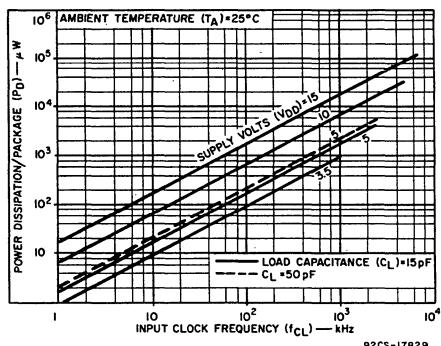


Fig. 6—MSI device power dissipation characteristics.

Fig. 7b shows curves of propagation delay as a function of supply voltage for a typical gate device. However, the trade-off for low supply voltage (i.e., lower output current to drive a load) is lower speed of operation.

The power dissipated during switching (if the load is assumed to be capacitive) is equal to:

$C_0 V_{DD}^2 f$  [power is equal to energy per unit time]  
where  $C_0$  is the output and load capacitance,  $V_{DD}$  is the supply voltage, and  $f$  is the operating frequency in hertz. A measure of this power dissipation as function of frequency can be obtained from the model shown in Figs. 8a and 8b which assumes step inputs and zero mode capacitance.

The average power for the square-wave input voltage shown (repetition rate  $f_0 = 1/t_0$ ) is calculated as follows:

$$P = \frac{1}{t_0} \int_0^{t_0} I_N(t) V_O dt + \frac{1}{t_0} \int_{\frac{t_0}{2}}^{t_0} I_P(t) (V_{DD} - V_O) dt$$

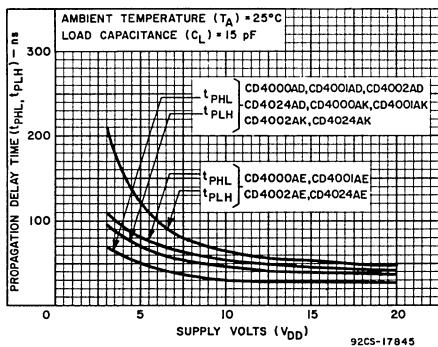
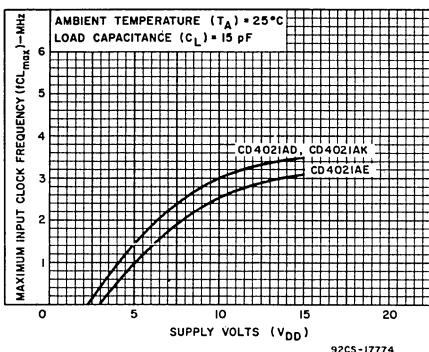


Fig. 7— Operating frequency and propagation delay as a function of power-supply voltage (a) Maximum guaranteed operating frequency as a function of power-supply voltage (b) Propagation delay as a function of power-supply voltage for the basic gate.

For P with  $I_N(t) = I_P(t) = C_o \frac{dV_o}{dt}$  (step inputs only),

$$P = \frac{C_o}{t_o} \int_0^{V_{DD}} V_o dV_o + \frac{C_o}{t_o} \int_{V_{DD}}^0 (V_{DD} - V_o) d(V_{DD} - V_o)$$

$$\therefore P = \frac{C_o V_{DD}^2}{t_o} = C_o V_{DD}^2 f$$

Thus, for a step input, the average power dissipated is directly related to the energy required to charge and discharge the circuit capacitance to the supply voltage,  $V_{DD}$ . It should be noted that this power is independent of the device parameters. Although this equation was derived using an input voltage with a rise time of zero, it has also been shown to be a good approximation for circuits where the input voltage rise and fall times are small with respect to the repetition rate.

#### Calculating System Power

The foregoing material presented fundamental reasons why COS/MOS devices exhibit extremely low quiescent power. Also presented were reasons why ac power dissipation increases with operating frequency and why it varies from device to device.

For these reasons certain guidelines have been developed to assist the designer in estimating system power. Total system power is equal to the sum of quiescent power and dynamic power. Therefore, the two-step approach outlined below can be used:

1. Add up all typical package quiescent power dissipations (as shown in the RCA COS/MOS published data). Because quiescent power dissipation is equal to the product of quiescent device current times supply voltage, this parameter may also be obtained by adding all typical quiescent device currents, and multiplying the sum by the supply voltage,  $V_{DD}$ . Quiescent device current is shown in the published data for supply voltages of 5 volts and 10 volts only.

In cases where the supply voltage is other than that shown in the published data, the quiescent device current can be interpolated because this current varies approximately linearly with voltage.

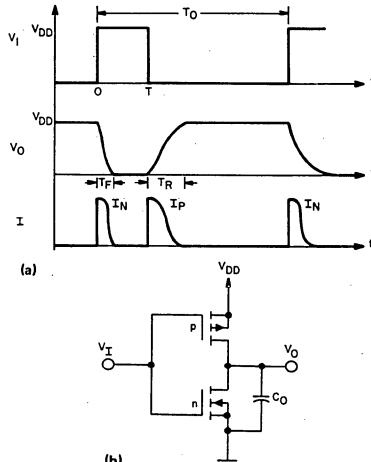


Fig. 8— Model for the evaluation of power dissipation (a) Waveforms (b) Circuit.

2. Add up all dynamic power dissipations using typical curves of dissipation per package as a function of frequency shown in the published data. In a fast-switching system, most of the power dissipation is dynamic, therefore, quiescent power dissipation may be neglected.

The example below illustrates how these rules are used to calculate total system power dissipation. The system illustrated consists of ten 2-input NOR gates, eleven inverters, one D-type flip-flop, and one 7-stage binary counter. The system operates with a supply voltage of 10V at a frequency of 100 kHz, and has a load capacitance of 15 pF. (See Table I)

Table I

Types	P <sub>Quiescent</sub> μW	P <sub>Dynamic</sub> mW
Gates	0.03	2
Inverters	0.01	2
D-type F/F	0.05	0.2
Counter	5	0.6
$P_T = P_Q + P_D = 4.8\text{mW}$ (neglecting $P_Q$ )		

This example assumes that all devices are switching at the clock-rate (100 kHz). Not all of the logic circuits will be switching states at this rate, thus, the total power dissipation will be significantly lower than that stated in the example.

#### Power-Supply Regulation Requirements.

The preceding discussion demonstrated that COS/MOS devices exhibit reliable switching properties over a wide range of power-supply voltages. This fact implies that an unregulated supply may be used with the provision that

- (1) maximum voltage limits are not exceeded or
- (2) system speed is no greater than the speed which can be supported by the COS/MOS devices operating at the lowest value of the  $V_{DD}$  expected from the unregulated supply.

To establish the extent of the regulation required, the system designer must first determine the maximum operating frequency required. Usually, the maximum frequency of the system is limited by the slowest responding devices in a logic chain. By reference to the curve of frequency as a function of  $V_{DD}$  and  $C_L$  given in the published data for that device, a minimum  $V_{DD}$  voltage (required for proper operation) can be determined. Any value above this  $V_{DD}$  (minimum) will provide acceptable performance in the system. By selection of a nominal  $V_{DD}$  half way between  $V_{DD}$  (mini-

mum) and the 15-volt maximum rating for COS/MOS devices, the designer can estimate the percentage regulation required for his system to perform adequately.

For example, the published data of the RCA CD4024A 7-stage binary counter shows a curve (shown in Fig. 9) of frequency as a function of operating voltage for that device. For operation of this counter at 5 MHz, with a loading capacitance of 15 pF, the minimum operating  $V_{DD}$  permitted for reliable operation is 10 volts, as shown on the curve.

Because the maximum  $V_{DD}$  is 15 volts, a half-way voltage of 12.5 volts should be the nominal value used. In this case, the maximum percentage regulation is 20%. If the designer desires a nominal  $V_{DD}$  closer to  $V_{DD}$  minimum, then better regulation is required, (for example in battery-operated equipment where a standard cell is available).

#### Filtering Requirements

Power-supply filtering requirements for COS/MOS systems are minimal. Two factors account for this situation: (1) the low quiescent power dissipations involved, and (2) the fact that the peak value of the ripple does not go below a minimum  $V_{DD}$  (which supports the required switching frequency), so that the COS/MOS logic performs satisfactorily.

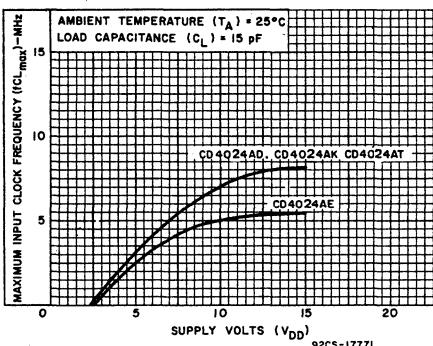


Fig. 9—Maximum frequency as a function of power-supply voltage for the CD4024A types.

This performance has been demonstrated in the laboratory (see Fig. 10). The amount of ripple on the power supply is quite high, yet the device functions properly.

#### Typical Supplies

The following circuits indicate some examples of adequate supplies for COS/MOS systems.

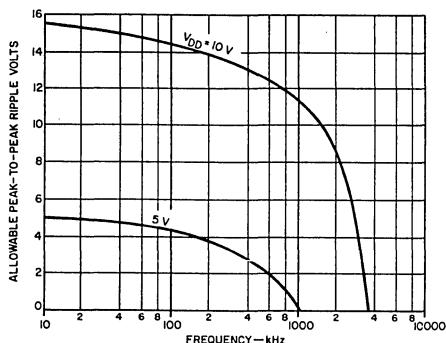


Fig. 10—Peak-to-peak ripple voltage as a function of frequency.

#### Battery Standby System

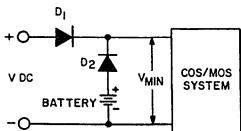


Fig. 11—Battery standby for COS/MOS systems.

This system is advantageous in cases where the dc supply becomes open or short-circuited.

With a low battery voltage the COS/MOS system will continue to function without interruption. In order to drive this system the battery voltage and dc supply voltage should relate as follows:

$$V_{\text{battery}} = V_{\text{min.}} + 0.7V, (0.7V \approx \text{one diode drop})$$

$$V_{\text{max.}} > V_{\text{DC supply}} > V_{\text{min.}} + 1.4V$$

In the event the supply drops below  $V_{\text{min.}}$ , the battery will forward bias diode D2 to form a closed-circuit and the COS/MOS system will continue to function properly through the battery.

#### High DC Source

For applications (especially in aircraft equipment) where the supply voltage exceeds the RCA COS/MOS maximum rating of  $V_{\text{DD}}$ , the circuit of Fig. 12 can be used to reduce the high supply voltage to the normal COS/MOS voltage range. This configuration uses a Zener diode, a resistor R and a capacitor C.

The low current demand of the COS/MOS system permits an inexpensive but effective Zener diode regulator.

Some of the design considerations are as follows:

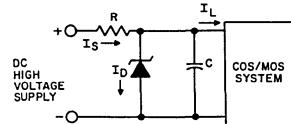


Fig. 12—Circuit for interface of COS/MOS systems to high-voltage supply.

#### 1. Selection of Zener Diode and Resistor R

The amount of current that must be maintained through the diode ( $I_D$ ) is a function of the difference between the worst-case average current required by the COS/MOS systems and the current required by the Zener diode for regulation based on its particular breakdown characteristics.

The diode current ( $I_D$ ) and the worst-case average system current ( $I_{\text{avg}}$ ) determine the value of the resistor (R) for a particular Zener regulating voltage.

#### 2. Selection of Capacitance C

Before the proper capacitance can be selected the following system requirements must be decided upon:

a. Peak charge requirement. This requirement is a function of the peak current and its pulse width. It must be measured for the particular system speed and load capacitance.

b. Permissible  $V_{\text{DD}}$  minimum: As mentioned in previous sections, this minimum voltage will determine the maximum operating speed of the COS/MOS system.

The size of the capacitor (C) may then be determined from the following formula:

$$Q = I_p t \quad (\text{charge} = \text{peak current} \times \text{pulse width})$$

#### SUMMARY

This Note shows that RCA COS/MOS devices offer many advantages in the area of simplified power-supply requirements. The wide operating voltage range (3 to 15 volts) from a single supply, low power dissipation, and high noise immunity permit system designers to use less expensive, unregulated, power supplies. This wide voltage range makes COS/MOS logic circuits ideal for battery-operated equipment because a better selection of cells is feasible. Another advantage is the direct compatibility of COS/MOS devices with bipolar devices which eliminates expensive and power-consuming interface circuits. (See Ref. 1.)

COS/MOS transistors show great potential for use in large arrays because of the low power dissipation and effective use of chip area. The relatively small area consumed by COS/MOS circuits, as well as the elimination of area and power-consuming resistors, results in high circuit-density per unit-silicon-area.

The performance features mentioned in this Note, as well as the reduced costs inherent in IC technology make COS/MOS circuits extremely attractive in many digital systems.

1. "Interfacing COS/MOS WITH OTHER LOGIC Families", ICAN6602 by A. Havasy and M. Kutzin.

## **Arithmetic Arrays using Standard COS/MOS Building Blocks**

By A. Havasy

This Note describes the design of a COS/MOS arithmetic unit. The RCA COS/MOS product line includes a standard line of devices designed to operate from voltage supplies of 5 to 15V and a low voltage "A" series designed to operate from voltage supplies of 3 to 15V. These devices are available in any of the package types or temperature ranges shown in Table I.

TABLE I

Package		Operating Temperature Range (°C)	
Type	Suffix		
Dual-in-line ceramic	5-15V 3-15V ("A")	D	D
Plastic	E	E	-55 to + 125
Flat Pack	—	K	-40 to + 85

When ordering COS/MOS devices, the appropriate suffix should be affixed to the number of the device required, (i.e., if a low voltage, plastic package, four bit full adder is desired, order CD4008AE). This Note is applicable to both COS/MOS product lines, and all package types mentioned above.

### **Arithmetic Unit**

This arithmetic unit is capable of adding, subtracting, multiplying, and dividing. It is also able to perform the logical functions of "OR", "AND" and the "Exclusive OR" of two 4-bit words. Three 4-bit registers are provided that permit either of two words to perform a desired operation with a third word. The system is configured with standard, commercially available, COS/MOS devices which include registers, AND-OR select gates, a full adder, as well as NOR and NAND gates. A block diagram of the 4-bit arithmetic

unit is shown in Fig. 1. The required package count and the function performed by each package are shown in Table II.

A brief description of each COS/MOS device used in the arithmetic system follows:

### **Four-Bit Full Adder — CD4008 or CD4008A**

The CD4008 or CD4008A consists of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuits are included to provide a fast parallel-carry-out bit, which permit high-speed operation in arithmetic sections that use several CD4008's or CD4008A's.

The CD4008 or CD4008A inputs include the four sets of bits to be added ( $A_1$  to  $A_4$  and  $B_1$  to  $B$ ), and the carry-in bit from a previous section. CD4008 or CD4008A outputs include the four sum bits,  $S_1$  to  $S_4$ , and the high-speed parallel-carry-out, which may be used as the input to a succeeding CD4008 or CD4008A section.

The logic diagram for this device is shown in Fig. 2. The electrical characteristics and more detailed information (for the CD4008 or CD4008A) are given in the RCA Data Bulletin File No. 405 or 479, respectively.

### **Quad AND-OR Select Gate — CD4019 or CD4019A**

The CD4019 or CD4019A consists of four AND-OR select gate configurations, each of which have two 2-input AND gates driving a single 2-input OR gate. Selection is performed by control bits  $K_a$  and  $K_b$ . In addition to the selection of either channel A or channel B information, the control bits can be applied in combination to accomplish a third selection of data. The logic diagram for the CD4019 or CD4019A is shown in Fig. 3. The electrical characteristics and additional application diagrams for the CD4019A are given in the RCA Data Bulletin, File No. 439 or 479, respectively. Applications of this device to shifting and logic selection operations are discussed later in this Note.

### **Dual D-Type Flip-Flop — CD4013 or CD4013A**

The RCA CD4013 or CD4013A consists of two identical, independent data-type flip-flops on a single monolithic silicon chip. Each flip-flop has independent data, reset, set, and clock inputs and complementary buffered outputs.

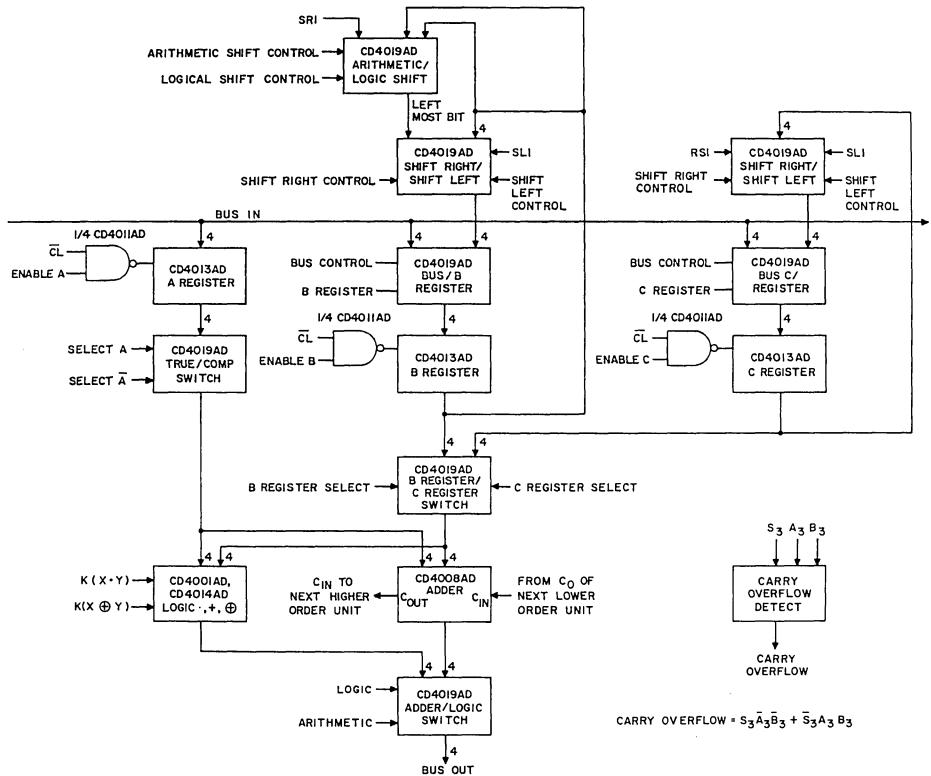


Fig. 1— Four-bit arithmetic unit, block diagram

These devices can be used in shift register applications, and in counter and toggle type flip-flop applications, by connection of the Q output back to the data input. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Resetting or setting is accomplished by the application of a high logic level to the reset line or set line, respectively. Fig. 4 shows the logic diagram for one flip-flop section of the CD4013 or CD4013A. The electrical characteristics and additional information for this flip-flop are given in the RCA Data Bulletin, File No. 411 or 479, respectively.

#### Quad 2 — Input NOR Gates — CD4001 or CD4001A

The RCA CD4001 or CD4001A consists of four, identical, independent 2-input positive-logic NOR gates. Fig. 5 shows the logic diagram and Boolean equations for this device. The electrical characteristics and additional information for these logic gates are given in the RCA Data Bulletin, File No. 420 or 479, respectively.

#### Quad 2 — Input NAND Gates — CD4011 or CD4011A

The RCA CD4011 or CD4011A consists of four, identical, independent 2-input positive-logic NAND gates. Fig. 6 shows the logic diagram and Boolean equations for this device. The electrical characteristics and additional information for these logic gates are given in the RCA Data Bulletin, File No. 345 or 479, respectively.

#### Arithmetic Unit Operation

The A register uses a CD4019 or CD4019A quad AND-OR select gate to present either the true or the complemented data to the logic circuits and the adder. Thus, the data in the A register can be either added or subtracted from the B or C registers.

The CD4019 or CD4019A at the input of the B register has two control lines which permit data to be shifted right or left, or which permit new data to be accepted from the bus lines. Fig. 7 shows the interconnection diagram of two CD4019's or CD4019A's that perform the shift-right shift-left and arithmetic/logic shift functions.

TABLE II PACKAGE COUNT FOR THE ARITHMETIC UNIT

FUNCTION	PACKAGES					
	CD4008 CD4008A	CD4019 CD4019A	CD4013 CD4013A	CD4011 CD4011A	CD4001 CD4001A	
A Register (includes A, $\bar{A}$ select capability and buffered outputs)		1	2			
B Register (includes shift capability and buffered outputs for B and $\bar{B}$ )		3	2			
C Register (includes shift capability and buffered outputs)		2	2			
Select B or C		1				
Add	1					5
Perform logic		1				
Select logic or addition		1				
Overflow detector						1
Clock inhibit (enable)				1		6
TOTALS	1	9	6	1		6

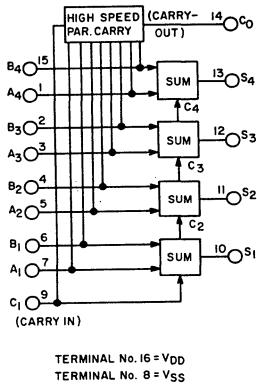


Fig. 2— Four-bit full adder, logic diagram.

The arithmetic shift mode is used only on the highest order bits and insures that the sign bit does not change during the shifting. On the lowest order bits the left shift input for the B register (BSL) is tied to the B<sub>0</sub> output of the next higher set of bits.

The C register is identical to the B register but does not provide for arithmetic mode shifting. Separate shift-right and shift-left controls are provided for the B and C registers. (BSL and BSR is provided for the B register, and CSL and CSR for the C register). Another CD4019 or CD4019A is used to select either the B or the C register information for the logic and arithmetic operations.

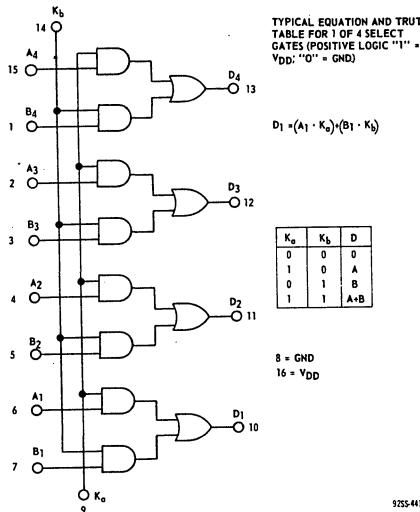


Fig. 3— CD4019 or CD4019A - Logic diagram.

The logic block diagram for the AND/OR/Exclusive-OR logic selector is shown in detail in Fig. 8. One and one-quarter CD4001's or CD4001A's and one-quarter CD4019/CD4019A are used per bit, (or five CD4001 or CD4001A and the CD4019 or CD4019A per four-bit word). The control inputs are labeled K( $\cdot$ ) (K-AND) and K( $\oplus$ ) (K-Exclusive OR). An example of logic selection is as follows:

Assume that B<sub>1</sub> is an output from the B register and A<sub>1</sub> is a true output from the A register via the True/Complement Switch. (Refer to Fig. 1) When K( $\cdot$ ) is "high" and K( $\oplus$ ) is "low", the logic generated is AB. When K( $\cdot$ ) is low and K( $\oplus$ ) is high, the logic generated is A  $\oplus$  B =  $\bar{A}B + \bar{B}A$ . When both K( $\cdot$ ) and K( $\oplus$ ) are "high", the logic is AB + (A  $\oplus$  B) = AB +  $\bar{A}B + \bar{B}A$  = A + B.

The adder is a single CD4008 or CD4008A previously described. The carry input of this adder will be tied to the carry output of the adder on the next-lower-order CD4008 or CD4008A. The carry input of the lowest-order bits will be a logic "0" for addition and a logic "1" for the 2's complement subtraction.

The output buffer is also a CD4019 or CD4019A. In this application the device is used to select either the arithmetic or the logic outputs and to provide more output drive.

The output overflow circuit (shown in Fig. 9) will go "high" if the adder result exceeds the total bit capacity of the arithmetic unit. This overflow occurs only when two numbers that have the same sign bit are added and, the result is a sum which has the opposite sign.

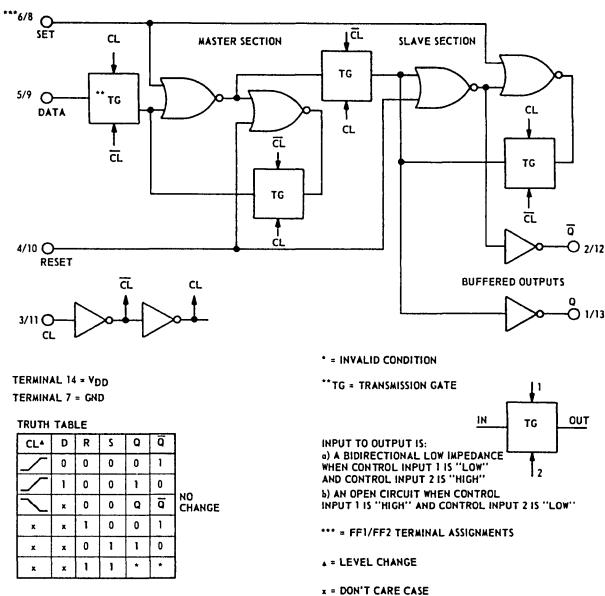


Fig. 4— CD4013 or CD4013A - Logic diagram and truth table (one of two identical flip-flops).

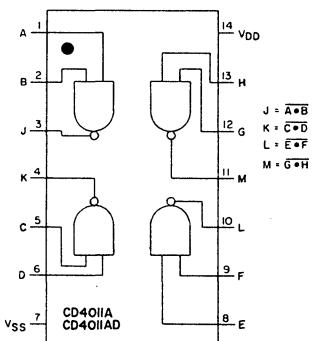


Fig. 5— CD4011 or CD4011A - Logic diagram and equations.

A larger arithmetic unit of any desired word length can be made by cascading additional circuits. The interconnection of eight systems to form a 32-bit arithmetic unit is shown in Fig. 10. The three inhibit signals, common control signals, and

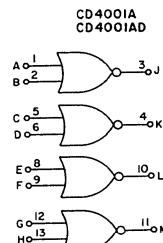


Fig. 6— CD4001 or CD4001A - Logic diagram and equations.

inverted clock signal (which are common to all eight subsystems) are not shown. Table III shows the functions and the symbols.

$$\begin{array}{l} J = \overline{A+B} \\ K = C+D \\ L = \overline{E+F} \\ M = \overline{G+H} \end{array}$$

$$\begin{array}{l} \text{POSITIVE LOGIC} \\ \text{LEVELS} \end{array}$$

"0" = 0V
"1" = $V_{DD}$

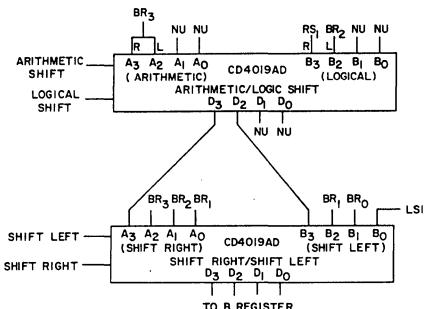


Fig. 7— Shift-Right/Shift-Left - Arithmetic/Logic shift Interconnection diagram.

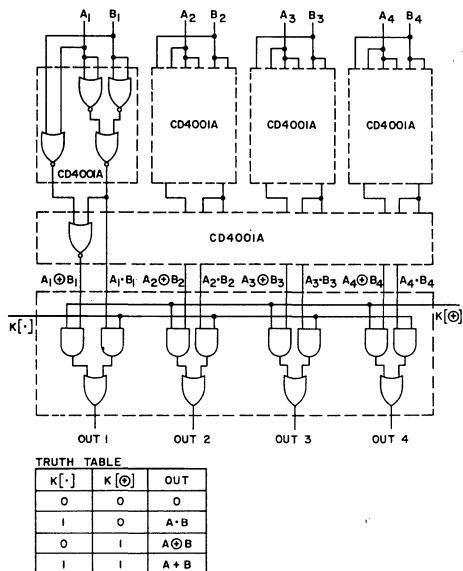


Fig. 8— AND/OR/EXCLUSIVE-OR Selector.

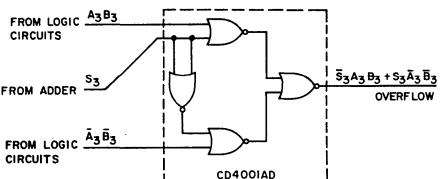


Fig. 9— Overflow logic circuit.

TABLE III FUNCTIONS AND SYMBOLS

SYMBOLS	FUNCTIONS
V <sub>DD</sub>	Input for positive power supply
GND	Ground
CL	Inverted clock
IN <sub>0</sub>	Lowest order bus input
IN <sub>1</sub>	Second lowest order bus input
IN <sub>2</sub>	Third lowest order bus input
IN <sub>3</sub>	Highest order bus input
Enable A	Enables the A register
Enable B	Enables the B register
Enable C	Enables the C register
A	Selects the true of the A register data for half-output function
~A	Selects complement of A register data for half-output function
SEL B	Selects B register data for output function with A register data
SEL C	Selects C register data for output function with A register data
Arithmetic shift	Allows B register to shift in the arithmetic mode
Logic shift	Allow C register to shift in the logical mode
B Bus	Allows B register to accept data from bus inputs
B shift	Allows B register to shift right or left
BSR	Allows B register to shift right
BSL	Allows B register to shift left
BSRI	Input to lowest order bit of the B register when shifting right
BSLI	Input to highest order bit of B register when shifting left
C Bus	Allows C register to accept data from bus inputs
C shift	Allows C register to shift right or left
CSR	Allows C register to shift right
CSL	Allows C register to shift left
CSRI	Input to lowest order bit of C register when shifting right
CSLI	Input to highest order bit of C register when shifting left
Arithmetic	Allows logical sums to appear at S outputs
Logic	Allows logic functions to appear at S outputs
C <sub>IN</sub>	Carry in to lowest order bit of adder
C <sub>OUT</sub>	Carry out from highest order bit of adder

TABLE III (CONTINUED)

## SYMBOLS

## FUNCTIONS

Overflow	Indicates if addition exceeds limit of adder
K(*)	Generates logical AND of logic circuits
K(θ)	Generates logical EXCLUSIVE-OR of logic circuits
S <sub>0</sub>	Lowest order sum output
S <sub>1</sub>	Second lowest order sum output
S <sub>2</sub>	Third lowest order sum output
S <sub>3</sub>	Highest order sum output (sign bit)

## Performance Data

In a 32-bit arithmetic unit constructed in the laboratory the delay time, (under worst-case logic conditions) for the inverted clock to be inverted, for data to be written into the register, and for that data to get to the adder and generate a carry-out from a 4-bit system was found to be 782 nanoseconds. The delay time (under worst-case logic conditions) for a carry-in to generate a carry-out was found to be 87 nanoseconds. The delay time under worst-case logic conditions for a carry-in to generate a sum at the adder and for this sum to appear at the outputs was found to be 623

nanoseconds. These numbers result in an addition time of 1927 [782 + (6 x 87) + 623] nanoseconds for two 32-bit words and 1579 [782 + (2 x 87) + 623] nanoseconds for two 16-bit words.

Since the construction of this adder, improved processing techniques permit faster operation. The delay from the clock to the carry out can be expected to be less than 500 ns; the delay from the carry-in to the carry-out can be expected to be less than 50 ns; and the delay from the carry in to the sum out can be expected to be less than 400 ns. Thus, the maximum addition time for a 32-bit arithmetic unit would be approximately 1200 ns; for a 16-bit unit, 1000 ns (maximum) would be required.

Calculations indicate a typical power dissipation of 100  $\mu$ W and 2350  $\mu$ W for the 4-bit arithmetic unit. These calculations are based on typical and maximum device quiescent power dissipations at a 10-volt supply and +25°C temperature.

## Summary

A complete 32-bit full adder/arithmetic logic system that uses standard COS/MOS devices (commercially available in quantity) is shown. This system offers many advantages to the systems designer: low power dissipation, high noise immunity and reliability.

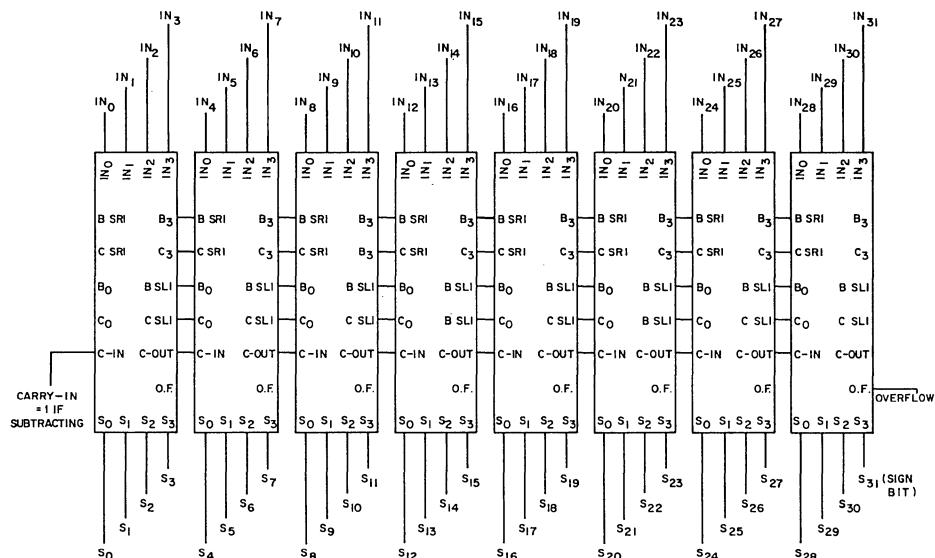


Fig. 10—Major interconnections to form 32-bit arithmetic unit from 4-bit subsystems.

## **Transmission and Multiplexing of Analog or Digital Signals Utilizing the CD4016A Quad Bilateral Switch**

by J. Litus, Jr., S. Niemiec, and J. Paradise

RCA type CD4016A Quad Bilateral Switch is an extremely flexible device. It has many advantages unique to a COS/MOS\* switch configuration and can be used for the transmission of analog or digital signals with low distortion. The CD4016A is the ideal semiconductor switch for use in a multitude of switching applications. This note describes some of the features and several applications of COS/MOS transistor bilateral signal switches (transmission gates).

### **FEATURES OF THE CD4016A**

The functional diagram of the CD4016A is shown in Fig. 1. The CD4016A consists of four independent bilateral signal switches on a single silicon monolithic chip. Each switch consists of an n-channel and a p-channel device. The source of the p-channel device is connected to the drain of the n-channel device and vice-versa. Only one control signal  $V_C$  is required per switch.  $V_C$  directly controls the n-channel unit; the p-channel unit is controlled by  $\bar{V}_C$  (an inverter is included on the chip). Both channels are biased "ON" or "OFF" simultaneously by the control signal  $V_C$ . Fig. 2 shows the schematic diagram of the CD4016A.

Unlike the bipolar switch, the COS/MOS switch has no voltage offset. It is a bi-directional switch. The COS/MOS switch does not require an excessively large control voltage (compared with the incoming signal level), as does the single channel MOS switch. The control voltage required by the COS/MOS switch is of approximately the same amplitude as the input signal. The incoming signal can be a maximum of  $|V_{DD} - V_{SS}| = 15$  V., or a minimum of  $|V_{DD} - V_{SS}| = 3$  V.

Figs. 3 and 4 show the typical "ON" transfer characteristics of the COS/MOS switches. Figs. 5 and 6 show the output voltage as a function of time for an input sine wave and square wave voltage respectively.

### **OPERATION OF THE COS/MOS SWITCH**

Fig. 7 shows the transfer characteristics of a single p-channel MOSFET switch (with a high value of load resistance  $R_L$ ) in the "ON" condition. If it is assumed that this application calls for an input signal voltage ( $V_I$ ) in the range of -5 to +5 V., and that the output signal voltage  $V_O$  follows the input signal voltage linearly within this voltage range, the switch will be "ON" for the following conditions:

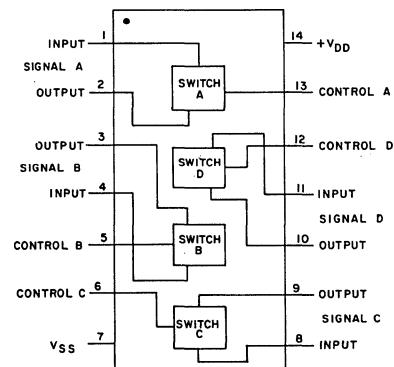
Threshold voltage ( $V_{TH}$ ) = +5 V.

Gate voltage ( $V_G$ ) = -10 V.

Substrate voltage ( $V_{sub}$ ) = +5 V

Input signal voltage ( $V_I$ ) > -5 V.

When the switch is "ON", the input signal voltage is transmitted to the output terminal (subject to the above conditions). However, if the input signal voltage falls below



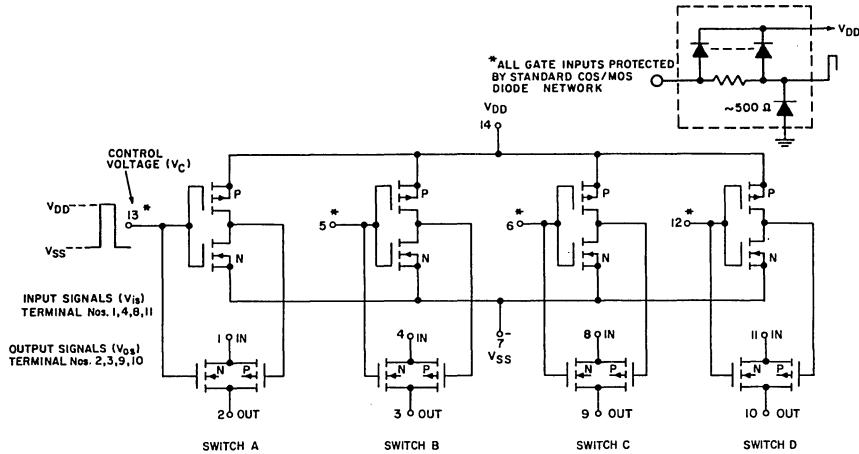
*Fig. 1— Functional diagram (top view).*

\*Complementary-Symmetry Metal-Oxide-Semiconductor

-5 V., (i.e.,  $V_{TH}$ ), the switch operates as a source follower. To avoid this condition, the magnitude of the p-channel gate voltage must be increased by the sum of the threshold voltage and the peak input voltage,  $|V_I(\max) + V_{TH}|$ .

The problems encountered in the single channel

MOSFET switch can be eliminated by the use of a parallel complementary MOSFET arrangement, shown in Fig. 8a. The voltage transfer characteristics ( $V_O$  as a function of  $V_I$ ) are shown in Figs. 8b (single p-channel device), 8c (single n-channel device), and 8d (composite for both devices in



NOTE: All switch P-channel substrates are internally connected to terminal No. 14.  
All switch N-channel substrates are internally connected to terminal No. 7.

#### NORMAL OPERATION:

##### Control Line Biasing

Switch "ON":  $V_C$  "1" =  $V_{DD}$   
Switch "OFF":  $V_C$  "0" =  $V_{SS}$

SIGNAL-LEVEL RANGE:  
 $V_{SS} \leq V_{IS} \leq V_{DD}$

Fig. 2— Schematic diagram.

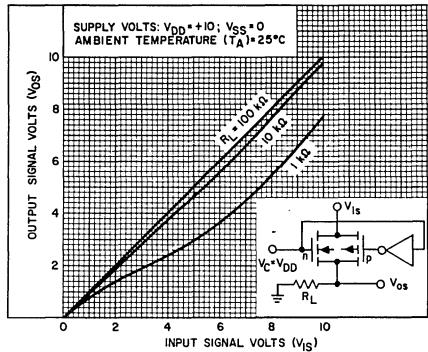


Fig. 3— Typ. "ON" characteristics for 1 of 4 switches with  $V_{DD} = +10V$ ,  $V_{SS} = OV$  (CD4016A).

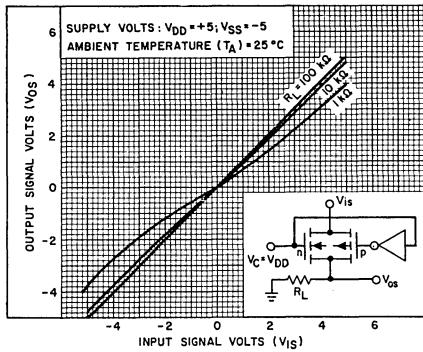


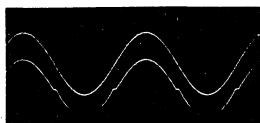
Fig. 4— Typ. "ON" characteristics for 1 of 4 switches with  $V_{DD} = +5V$ ,  $V_{SS} = -5V$  (CD4016A).

parallel). The load resistance,  $R_L$  is assumed to be large compared with the MOSFET "ON" resistance ( $R_{ON}$ ). The composite characteristics are obtained by the graphic addition of the individual characteristics. The "ON" characteristics show that at least one device is "ON" at any given instant, because one gate is controlled by  $V_C$  and the other by the complement,  $\bar{V}_C$ .



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV  
 $V_{DD} = V_C = +7.5V$ ,  $V_{SS} = -7.5V$ ,  $R_L = 10\text{ k}\Omega$   
 $C_L = 15\text{ pF}$   
 $f_{IS} = 1\text{ kHz}$ ,  $V_{IS} = 5\text{ V p-p}$   
DISTORTION = 0.2%

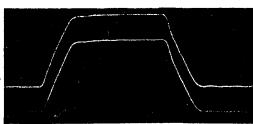
(a)



SCALE: X = 0.2 ms/DIV Y = 2.0 V/DIV  
 $V_{DD} = V_C = +2.5V$ ,  $V_{SS} = -2.5V$ ,  $R_L = 10\text{ k}\Omega$   
 $C_L = 15\text{ pF}$   
 $f_{IS} = 1\text{ kHz}$ ,  $V_{IS} = 5\text{ V p-p}$   
DISTORTION = 3%

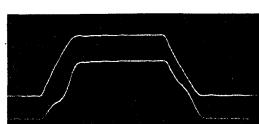
(b)

Fig. 5— a) Typ. Sine wave response of  $V_{DD} = +7.5V$ ,  $V_{SS} = -7.5V$ ; b) Typ. sine wave response of  $V_{DD} = +2.5V$ ,  $V_{SS} = 2.5V$ .



SCALE: X = 100 ns/DIV Y = 5.0 V/DIV

(a)



SCALE: X = 100 ns/DIV Y = 2.0 V/DIV

(b)

Fig. 6— a) Typ. square wave response at  $V_{DD} = V_C = +15V$ ,  $V_{SS} = G_{nd}$ ; b) Typ. Square wave response at  $V_{DD} = +5V$ ,  $V_{SS} = V_C$ .

The gate control voltage required ( $\pm 5\text{ V}$  in this case) need only be equal to the absolute value of the peak input signal voltage. The maximum input signal voltage range is limited by  $V_{DD}$  (+5 V) and  $V_{SS}$  (-5 V). The gate control voltages would then be +5 V and -5 V respectively. There is a minimum threshold voltage ( $V_{TH}$ ) required to turn "ON" the switch. This condition must always be met for proper operation — see published data, Ref. 1.

## LEGEND:

$V_{IS}$  = INPUT SIGNAL VOLTS  
 $V_{OS}$  = OUTPUT SIGNAL VOLTS  
 $V_G$  = GATE CONTROL VOLTS  
 $V_{SUB}$  = SUBSTRATE VOLTS

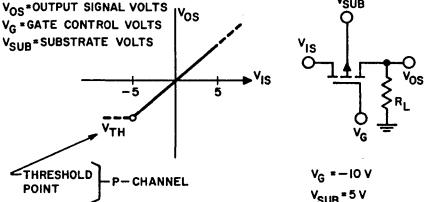
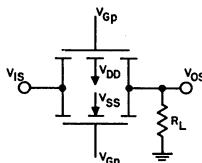
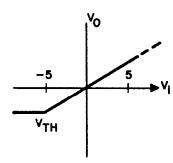


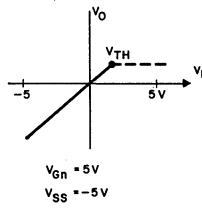
Fig. 7— Single p-channel MOS/FET switch characteristics



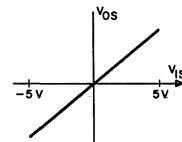
(a)



(b)



(c)



(d)

Fig. 8— a) COS/MOS FET switch (transmission gate); b) p-channel characteristics; c) n-channel characteristics; d) composite characteristics.

## SWITCH AND LOGIC APPLICATIONS

### Switch Functions

The CD4016A Quad Bilateral Switch can be used to perform the four common switch functions shown in Fig. 9 (i.e., SPST, SPDT, DPST, and DPDT).

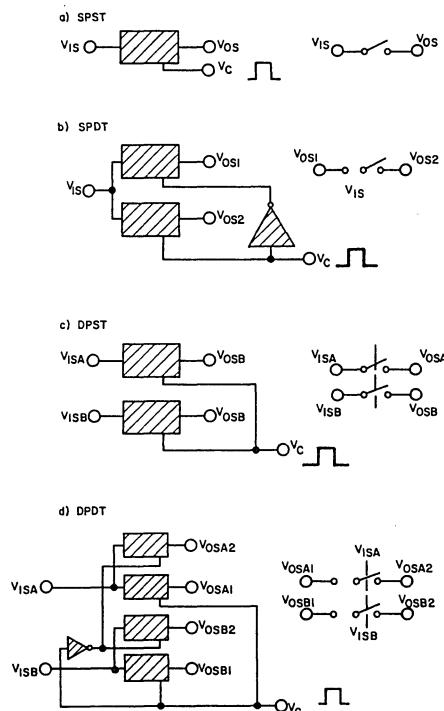


Fig. 9—Basic switch functions using the CD4016A.

### Logic Functions

Fig. 10a illustrates the use of the CD4016A to gate digital (or analog) signals. When the CD4016A is used as a digital "OR" gate, a logic "1" should be present at points a and b. Two control voltages A and B are required as shown. When a logic "1" is not being transmitted ( $A = B = "0"$ ), a logic "0" appears at the output. There are two methods to achieve this result: (1) a resistor tied from the output terminal to a logic "0", or (2) the remaining two transmission gates of the CD4016A can be connected (as shown in Fig. 10a) to a logic "0" and be gated by the complement of the control functions A and B (i.e.,  $\bar{A}$  and  $\bar{B}$ ). Use of the resistor tied to a logic "0" will provide the designer with two "OR" gates from a single CD4016A. Use of the two transmission gates (in place of the resistor) provides lower power dissipation.

Analog signals may be used in place of the logic "1" signals at the signal input terminals ( $V_{IS}$ ) to the transmission gates and these analog signals may be passed to the output if a particular logic function is satisfied. A general logic function may be implemented by the use of transmission gates as shown in Fig. 10d. The function illustrated is  $F = \bar{AB} + CD$ . The implementation of some logic functions may be simpler and the propagation delay time may be shorter when transmission gates are used. The input signals (a, b and c in Fig. 10d) may be analog signals or digital signals. The transmission gates may be used in a wired "OR" configuration, which simplifies many logic designs.

Transmission gates may also be used in flip-flop or memory cell circuits. Fig. 11 shows transmission gates being used in conjunction with NOR gates and inverters to

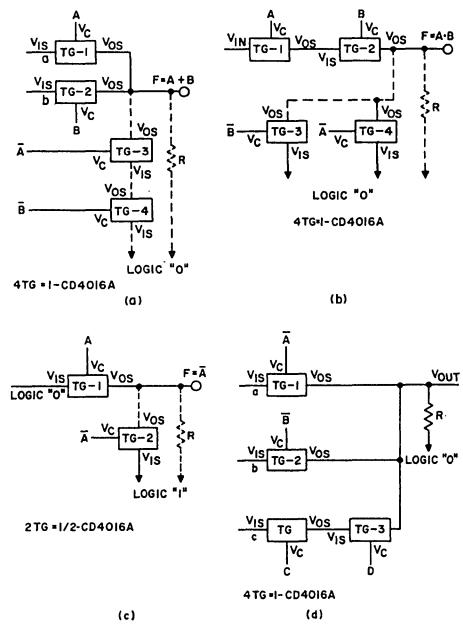


Fig. 10—Logic functions using the CD4016A: a) "OR" gate; b) "AND" gate; c) "NOT" (inverter) gate; d) implementation of  $F = \bar{AB} + CD$  using the CD4016A.

implement a master-slave type D flip-flop. These flip-flops are available commercially. (See Ref. 2.) All COS/MOS logic elements (gates, flip-flops, complex MSI and LSI functions) are comprised of the basic COS/MOS Transmission gate (parallel connection of p- and n-channel units) plus the basic COS/MOS inverter (series connection of p- and n-channel units). (See Ref. 2.)

## Multiplexing/Demultiplexing

A four channel PAM (Pulse Amplitude Modulation) Multiplex/Demultiplex system utilizing the CD4016A is shown in Fig. 12a. Commutator, MUX, and DMUX are the building blocks used to implement the system. Each input signal is sampled sequentially and applied to a single transmission line, but in a different time slot. The signals are detected and reconstructed at the outputs. These outputs will be proportional to the inputs, with no loss of information, as long as the conditions of Nyquist's sampling theorem are met: Sampling rate must be greater than twice the maximum frequency component of the input signal.

An RCA type CD4018A - "Divide-by-N" counter and associated decoding circuitry are used to provide the sequential signals to the control inputs of the CD4016A switches. The analog information is present at the outputs of the CD4016A only during the "ON" time of each switch. The clock frequency required for the counter is as follows:

$$f_{cl} > 2f_m N_c$$

where  $f_m$  is the bandwidth of the input signal and  $N_c$  is the number of channels being sampled. For example, the circuit shown in Fig. 12a has a maximum input signal bandwidth of 10 kHz. Therefore,

$$f_{cl} > 2(10\text{kHz})(4) = 80\text{kHz}.$$

The clock pulse is also applied to the transmission line to provide synchronization pulses for output decoding. A narrow clock pulse is used to prevent significant interaction between the clock and the sampled information. These clock pulses are removed from the output waveforms by taking advantage of the threshold voltage of a second counter (CD4018A). The magnitude of the analog signals is kept at a lower level than the switching voltage [ $V_{IL}(\text{max})$ ] of the CD4018A or the CD4009A (Inverter A). [ $V_{IL}(\text{max}) = 30\%$  of  $V_{DD}$ .] Therefore, only the clock pulses trigger the second counter. Inverter A opens the transmission line during the clock interval. Signals can be transmitted at all other times. In this example, the clock is transmitted on the same line as the analog information, although this procedure need not be followed. Separate transmission of the clock signal removes any restrictions on the signal amplitude provided the signal swing is maintained within the range of the  $V_{DD}$  and  $V_{SS}$  supply levels.

The output decoding is identical to the input decoding. The low-pass filters have a bandwidth equal to the bandwidth of the system and are used to filter the high frequency components generated by the sampling process, and to reconstruct the signals. Figs. 12b, c, and d show the waveforms of the signals at various points in the circuit.

Measurements and observations of a laboratory prototype of the PAM system discussed above, are presented below. Note: In the "all COS/MOS system", the switch

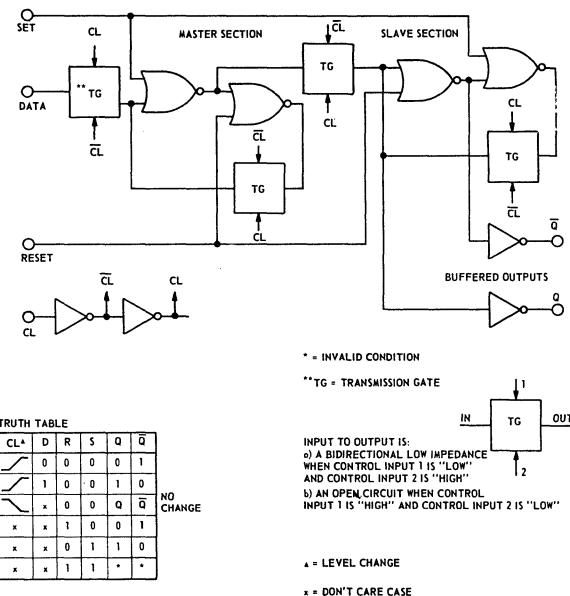


Fig. 11—Type "D" flip-flop logic diagram and truth table.

control signals are compatible with commonly used control system logic levels. Analog input signals whose magnitude is equal in amplitude to these control signals, can be used. The analog signals may be of either polarity, positive or negative.

#### Conditions:

$$\begin{aligned} \text{Signal Input voltage frequency: } & 100 \text{ Hz to } 10 \text{ kHz} \\ \text{Peak to Peak input: } & 400 \text{ mV} \\ \text{RC Low pass filter cut-off frequency: } & \frac{1}{2\pi RC} = 1.33 \text{ kHz} \\ & (R = 12 \text{ k}\Omega, C = 0.01 \mu\text{F}) \end{aligned}$$

#### Results:

- “ON” channel attenuation: 13dB
- Adjacent “OFF” channel signal: -50dB below input
- Adjacent “ON” channel signal: -50dB below input
- Distortion: 3% (1 kHz signal at LPF output, input signal 200mV peak-to-peak; clock frequency 400kHz)

In the example of Figs. 12a, 12b, 12c, and 12d, only one supply is used. The negative signal swing is limited to less than one diode drop ( $V_{BE} \approx 0.5$  V) below ground potential. This one-supply system can be modified to permit higher input signal amplitudes: the ac input voltage is offset by the addition of a resistor tied from  $V_{DD}$  to  $V_{IS}$  terminals of the input CD4016A. The positive signal swing should not exceed the switching voltage of the CD4018A. (See Ref. 3 for detailed applications of the CD4018A.) Fig. 12e shows an oscilloscope trace of the input and output voltage waveforms for this modification using a 2-k $\Omega$  offset resistor with a 600- $\Omega$  source impedance. The input signal amplitude is approximately 3 V and is offset from ground by 1-1/2 V.

A method that permits the transmission of the clock signal on the same line as the multiplexed information is the use of a level detector to separate the clock signal from the information. The circuit modification is shown in Fig. 13. Such a level detector is described in the section that discusses the squelch control circuit. Two supplies are utilized in this application. The level detector permits the use of an input signal amplitude that approaches  $V_{DD}-V_{SS}$ .

In general, PAM provides a simple method to transmit and receive data through a common transmission medium. The above system can be extended to more complex transmission systems such as PDM, PPM, and PCM. In telemetry applications, where transmission of multi-channel analog or digital data from airborne instrumentation is necessary, COS/MOS devices offer the advantage of low power dissipation. Intercom and public address systems can also benefit from the advantages of multi-channel-single transmission line communications.

#### DIGITAL CONTROL OF SIGNAL GAIN, FREQUENCY AND IMPEDANCE

##### Resistor Network

Fig. 14 shows a digitally controlled resistor network. Each resistor is shunted by 1/4 CD4016A COS/MOS switch. When the switch is “ON” the resistor is shorted; when the switch is “OFF” the resistor is in the circuit. The “ON” impedance of the CD4016A is approximately 300  $\Omega$  (10 V

bias); the “OFF” impedance is approximately  $10^{12} \Omega$  (10 V bias). Sixteen (2<sup>4</sup>) resistor value combinations can be obtained from this 4-stage network. Such a network can be controlled from any logic system to select any value at the proper time. The control inputs could, for example, be connected to a binary counter (RCA type CD4004A)\*, to generate a staircase of binary resistor values.

##### Variable Gain Control

Fig. 15a shows the resistor network inserted into the feedback loop of an operational amplifier. This network provides the circuit with a 16 to 1 variation in gain. The gain of an op-amp in the configuration is given by

$$A = \frac{Z_F}{Z_I}$$

$Z_F$  is the digitally controlled resistor network. The control inputs to the CD4016A are connected to a binary counter as shown. The signal inputs can be either ac or dc. Waveforms for the voltage at various points in the circuit are shown in Figs. 15b and 15c.

##### Capacitor Network

A digitally controlled capacitance is shown in Fig. 16. This network has the capability of 128 capacitance values. There will be some resistance in series with each capacitor (i.e.,  $R_{ON}$  of the CD4016A). This resistance can be neglected if  $1/\omega C \gg R_{ON}$ .  $R_{ON}$  is negligible in most frequency control applications discussed in this Note.

##### Variable Frequency Control

Fig. 17a shows an astable multivibrator that uses a digitally controlled capacitance as the frequency-adjustment element. (See Ref. 4.) The control inputs to the CD4016A are obtained from a binary counter (CD4004A). The multivibrator is thus “swept” through a frequency range that depends upon the value of the capacitor network. For the values of resistance and capacitance shown in Figs. 17a and 16, a frequency range of 1 kHz to 70 kHz can be obtained in 128 discrete steps. The sweep-rate is determined by the clock-rate to the binary counter. Fig. 17b shows the waveforms for the circuit.

Combinations of R, L, and C networks can be digitally controlled to provide a variable impedance, gain, frequency, phase-shift or bandpass.

##### Digital-To-Analog (D/A) Conversion

A D/A converter is a decoding device that has two inputs and one output. The inputs are a digital signal (D) and an analog reference (VR); the output (VO) is an analog signal related to the inputs as follows:

$$V_O = (D)(V_R),$$

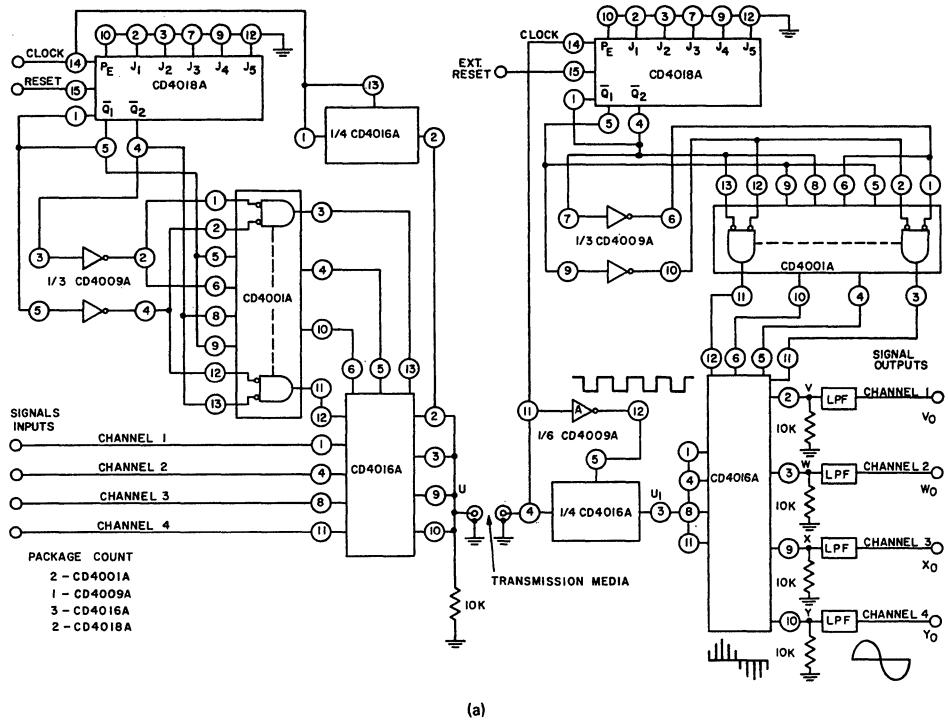
where:  $D = [a_1 2^{-1} + a_2 2^{-2} + \dots + a_n 2^{-n}] < 1$ .

Hence  $V_O = VR [a_1 2^{-1} + a_2 2^{-2} + \dots + a_n 2^{-n}]$ .

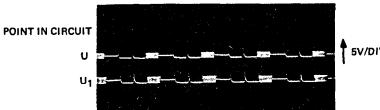
##### Weighted Resistor Network for D/A Converter

Fig. 18a shows a 4-bit D/A converter that uses a binary weighted resistor network and two CD4016A's. The value of each resistor is inversely proportional to the weighted value

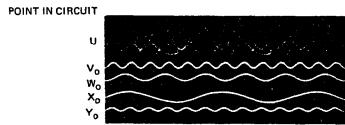
\* CD4004A has been superseded by CD4024A.



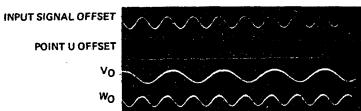
(b)



{d}



(c)



{ey}

**Fig. 12- a) 4-channel PAM multiplex system diagram; b)** waveforms of transmitted multiplexed signal ( $U$ ), and 3 of 4 received demultiplexed channels ( $V$ ,  $W$  and  $X$ ); c) waveforms of transmitted multiplexed signal shown at a long time scale to illustrate

*separate signals ( $U$ ) and 4 demultiplexed reconstructed output signals ( $V_O, W_O, X_O$ , and  $Y_O$ ); d) waveforms showing separation of clock signal from the information (1 channel only); e) waveforms for single supply circuit for input signal dc offset.*

of the particular digit being decoded. There are sixteen possible steps and each step is equal to  $1/15 V_R$ .

When the control inputs of the CD4016A are connected to a binary counter (CD4004A) a staircase output voltage is generated (shown in Fig. 18b). The reference voltage  $V_R$ , can be an analog signal as shown in Fig. 18c.

Although simpler circuitry is an advantage of the weighted resistor network this approach demands widely varying values of resistance and stringent switching requirements. The accuracy of the output voltage depends upon the accuracy of the resistance values and how well the resistance values track with temperature variations. As the number of bits increases, the values of the resistances become physically impractical.

#### R-2R Resistor Ladder D/A Converter

Two types of R-2R ladder networks are used for D/A conversion: (1) voltage-fed and (2) current-fed.

Fig. 19a shows a circuit diagram of a voltage-fed D/A converter that uses 2 CD4016A's and an R-2R network. The circuit provides  $2^n$  equal voltage steps, where  $n$  is the number

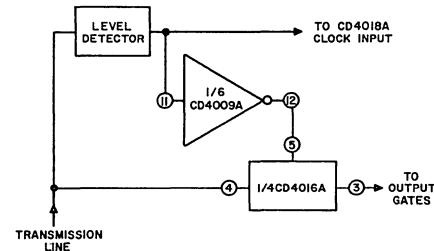


Fig. 13—Modification of the circuit of Fig. 12 to permit increased input signal amplitude.

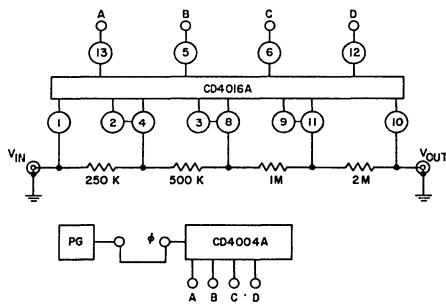
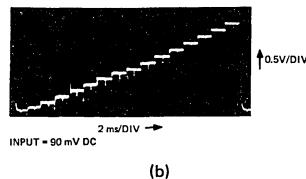
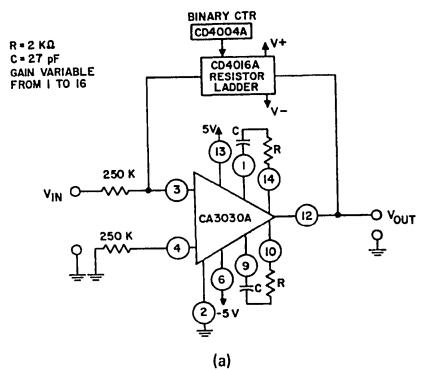
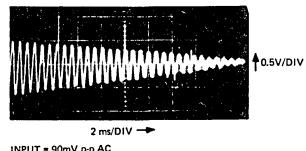


Fig. 14—Digitally controlled resistor network. (See RCA Data Bulletin No. 479 for details of terminal connections).



(b)



(c)

Fig. 15—*a*) Variable gain control circuit; *b*) waveform of output voltage for dc input voltage; *c*) waveform of output voltage for ac input voltage.

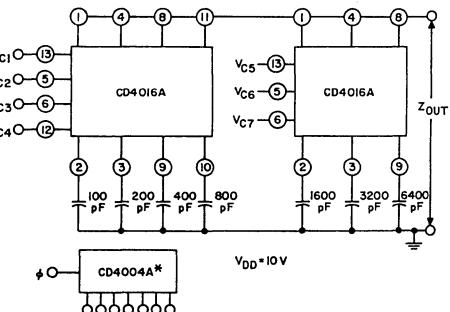


Fig. 16—Capacitor network. (See Data Bulletin File No. 479 for details of terminal connections).

of "legs" used.  $V_R$  is the dc reference input. The R-2R ladder network functions as a successive voltage divider. Each CD4016A connects or disconnects its "leg" to the reference voltage or to ground, and the output voltage is proportional to the input reference as discussed in the previous section. Thus, for the 4-bit system shown the least significant bit (LSB) contributes  $V_R/2^4$  or  $V_R/16$  to the total output

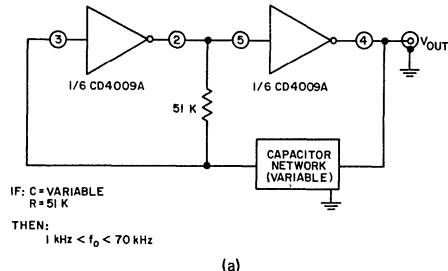
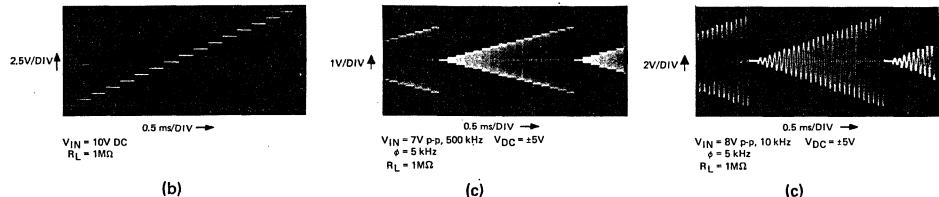
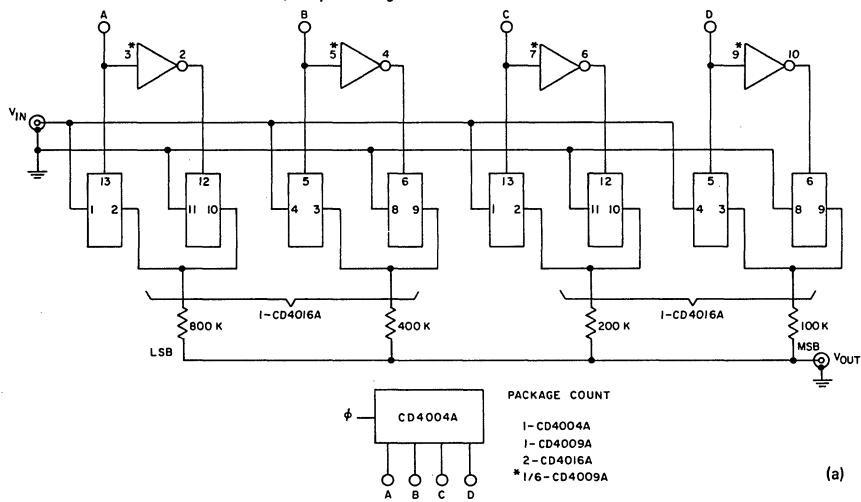
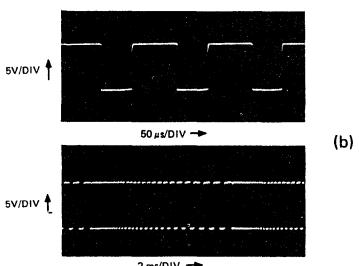


Fig. 17- a) Sweep generator (astable multivibrator) circuit;  
b) output voltage waveforms.

voltage. A CD4004A binary counter is used to provide a staircase output from the D/A converter. (Fig. 19b). An analog reference voltage may be used as the input: Fig. 19c shows the output voltage waveforms. Laboratory data indicate less than a 1% error in accuracy. The overall accuracy is dependent upon the switch "ON" resistance ( $R_{ON}$ ), leakage current and the discrete component accuracy.



output voltage waveforms for ac input voltage. (See Data Bulletin File No. 479 for details of terminal connections).

Fig. 18- a) Weighted resistor network D/A converter; b) output voltage waveforms for dc input voltage; c)

The current-fed D/A converter is shown in Fig. 20a. This circuit is similar in performance to the voltage-fed R-2R, except that the current-fed circuit has a higher accuracy. Higher accuracy is obtained because the same current is supplied from a constant current source over a wide variety of load values (including  $R_{ON}$  of the CD4016A's). The accuracy of the circuit is limited only by the accuracy of the resistors used. In this circuit a constant-current source feeds the R-2R network through the CD4016A. The current is divided by each branch in the same manner as voltage is divided in the voltage-fed circuit:

$$V_{out} = [I_{total}] (R_L),$$

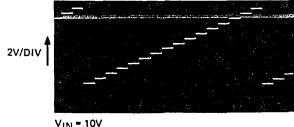
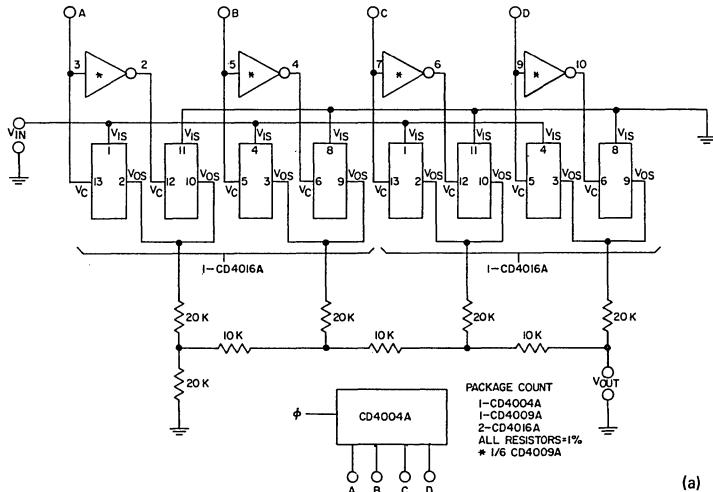
and,

$$V_{out(max)} = (I_C) (R_L) [1 - (1/2^n)],$$

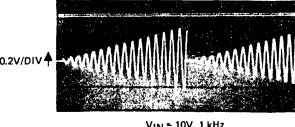
where  $I_C$  is the value of the constant-current. For the example shown in Fig. 20a,  $I_C = 500 \mu A$ ,  $n = 4$ ,  $R_L = 2 k\Omega$  and

$$V_{out(max)} = (500 \mu A) (2 k\Omega) [1 - (1/2^4)] = 0.938 V.$$

Fig. 20b shows the output voltage waveforms for the circuit



(b)



(c)



(c)

Fig. 19-a) R-2R resistive ladder network D/A converter (voltage-fed); b) output voltage waveforms for dc

for both dc and analog inputs. The measured error, including discrete component tolerance, is much less than 1%.

#### SAMPLE-AND-HOLD APPLICATIONS

A basic sample-and-hold circuit consists of a switch and an R-C network as shown in Fig. 21a. The capacitor charges to the peak value of the input signal when the switch is closed. When the switch is opened, the capacitor "holds" the full charge. The  $R_{OFF}$  of the CD4016A is typically  $10^{12} \Omega$ ,  $VDD = 10 V$ , and the leakage is  $10 pA$ , which is excellent for sample-and-hold circuits.

Fig. 21b shows a complete sample-and-hold circuit. The operational amplifiers are used to buffer and to assure stability of operation. When the clock is a logic "1", the CD4016A is "ON" and the input is being sampled. When the clock is a logic "0", the CD4016A is "OFF" and the capacitor holds the value of the sample. The effective sampling-time constant for this circuit is

$$t = \frac{10RC}{1+A},$$

PACKAGE COUNT  
I-CD4004A  
I-CD4009A  
Z-CD4016A  
ALL RESISTORS=1%  
\* 1/6 CD4009A

(a)

input voltage; c) output voltage waveforms for ac input voltage. (See Data Bulletin File No. 479 for details of terminal connections).

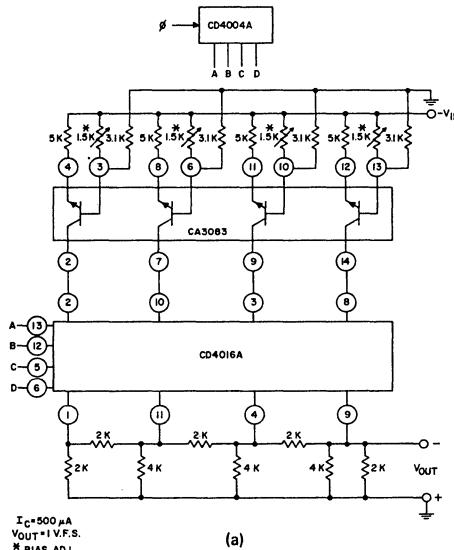
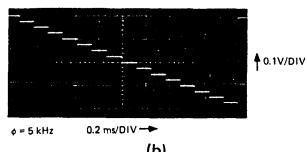


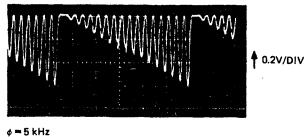
Fig. 20—*a*)  $R$ - $2R$  resistive ladder network D/A converter (current-fed); *b*) output voltage waveforms for dc



(b)

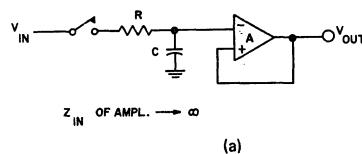


(c)



(d)

*input voltage; c) output voltage waveforms for ac input voltage.*

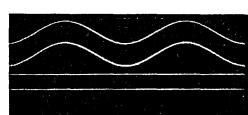


(a)



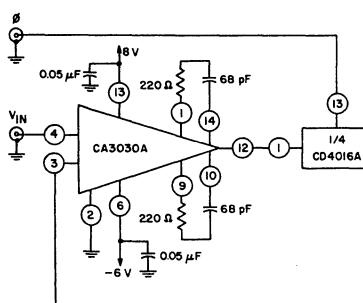
$\phi = 100$  kHz, 50% DUTY CYCLE  
 $R = 500$  kΩ  
 $C = 430$  pF  
 INPUT = 10 kHz, 2V p-p  
 OUTPUT = 0.5V/DIV

(c)



$\phi = 100$  kHz, 50% DUTY CYCLE  
 $R = 500$  kΩ  
 $C = 430$  pF  
 INPUT = 1 kHz, 2V p-p  
 OUTPUT = 2V/DIV

(c)



(b)

$$A_{VOL}(\text{CA3030A}) = 1000 \quad t = \frac{10RC}{1+A} = 5000 \text{ C}$$

Fig. 21—*a*) Basic sample-and-hold circuit; *b*) sample-and-hold circuit using the CD4016A; *c*) input and output voltage waveforms.

where  $A$  is the open-loop voltage gain of the first CA3030A op-amp (typically 60 dB). The second CA3030A op-amp (unity-gain-non-inverting) provides isolation of the output. This output voltage is fed back and compared with  $V_{IN}$  in the first op-amp. Any voltage offsets or variations within the loop do not affect the output. Fig. 21c shows input and output voltage waveforms of the circuit ( $R = 500 \text{ k}\Omega$ ,  $C = 530 \text{ pF}$ ).

Sample-and-hold circuits (without feedback) can be used to implement analog delay lines. A block diagram of an analog delay is shown in Fig. 22. Charge is transferred from one capacitor to the next at each clock pulse. Alternate switches in the delay line open and close simultaneously.

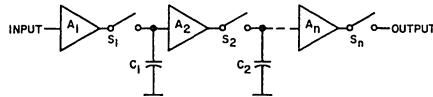


Fig. 22—Analog delay line.

The total delay of the system is given by

$$t_d = \frac{M}{f_s}$$

where  $M$  is the number of stages,

$f_s$  is the sampling frequency ( $f_s > 2f_m$ ), and

$f_m$  is the maximum frequency of the input signal.

#### SQUELCH CONTROL (LEVEL DETECTOR)

Fig. 23a shows a squelch circuit. When the input signal reaches a voltage level (determined by the  $1 \text{ M}\Omega$  resistor), the CD4016A will be gated "ON" and the output signal will be the same as the input. When the input signal is below this value, the CD4016A will be gated "OFF" and there will be no output from the CD4016A.

The control circuitry (CA3030A and CD4007A) functions as follows: The input signal is passed through a diode-capacitor peak detector, whose output will be the envelope of the input waveform. This output is amplified by the CA3030A (whose gain is made variable by adjustment of  $R_1$ ), and applied to the gate input of the CD4007A. The CD4007A is used as a NAND gate and has a very sharp switching voltage characteristic in this configuration. When the input to the CD4007A is equal to or greater than the switching voltage, the CD4007A is "ON" and a logic "1" will appear at the control gate of the CD4016A and turn off the switch. When the input voltage to the CD4007A is less than the switching voltage the CD4007A is off and a logic "1" appears at the control gate of the CD4016A and the desired signal reaches the output. Fig. 23b shows the output voltage waveforms.

The variable resistance which is a front-panel control permits the adjustment of the squelch threshold. This type of circuit is used in communication systems and in systems in which the signal must have a specific voltage level to be transmitted.

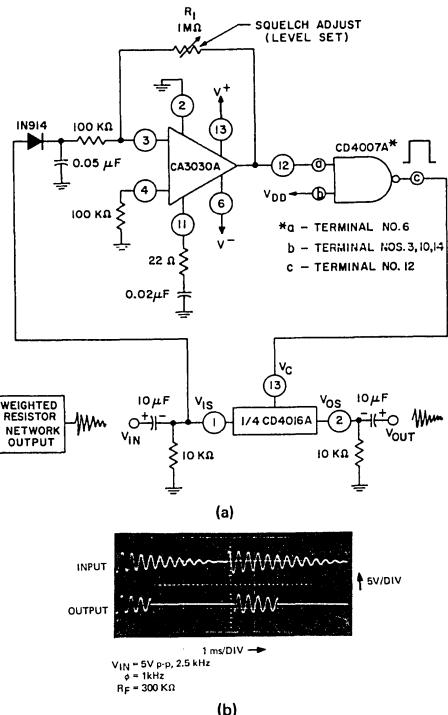


Fig. 23—a) Squelch control (level detector) circuit; b) input and output voltage waveforms.

#### SUMMARY

The CD4016A switch offers the design engineer an electronic switch that can be used in a wide variety of applications, including transmission and multiplexing of analog or digital signals over a large range of voltage levels and signal frequencies. The CD4016A can also perform switching and logic function implementation with low power dissipation. The low "ON" resistance, high "OFF" resistance, wide input signal range, no offset from input to output, and control inputs that are compatible with standard logic voltage levels make the use of the CD4016A highly advantageous to the designer.

#### REFERENCES

1. RCA data bulletin File No. 479, pp. 39-43.
2. RCA data bulletin File No. 479, pp. 30-32.
3. "Design of fixed and programmable counters using the RCA CD4018 COS/MOS presetable divide-by-'N' counter", by J. Litus, Jr., ICAN-6498.
4. "Astable and monostable oscillators using RCA COS/MOS digital integrated circuits", by J. A. Dean and J. P. Rupley, ICAN-6267.

## Interfacing COS/MOS With Other Logic Families

By A. Havasy and M. Kutzin

The interface of different logic families requires that the circuits operate at a common supply voltage and have logic level compatibility. In addition the devices must maintain safe power dissipation levels and good noise immunity over the required operating temperature range.

The RCA CD4000A COS/MOS series circuits operate from power-supplies of 3 to 15 V. Thus they can drive and be driven by a number of logic families (within certain conditions and limitations), including all DTL and TTL families. COS/MOS devices have high noise immunity, low quiescent power dissipation and high packing densities. This Note describes the conditions governing the interface of COS/MOS logic circuits with other logic families.

### COS/MOS-TTL/DTL Interface

Fig. 1 shows the voltage characteristics required at the output and input terminals of saturated logic devices. Fig. 2 shows the COS/MOS input and output characteristics at  $V_{DD} = 5$  V. The COS/MOS devices are designed to switch at a voltage level of 30% of the power supply voltage. However, TTL/DTL devices are designed to switch at 0.8 V for inputs going high and 2 V for inputs going low.

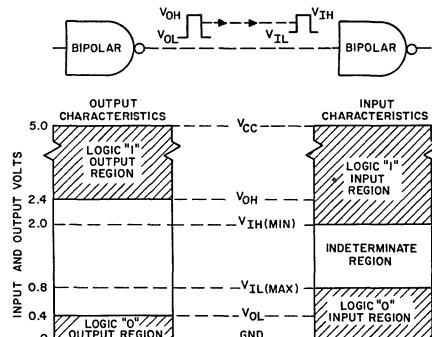


Fig. 1—Interface voltage characteristics required at the output and input terminals of saturated logic devices.

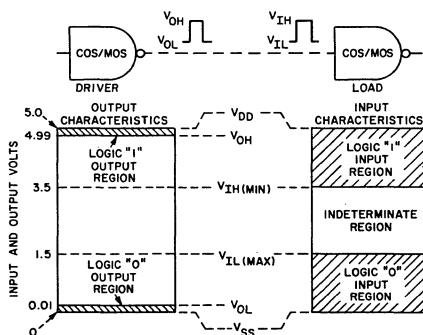


Fig. 2—COS/MOS input and output characteristics at a power-supply voltage of 5 volts.

When interfacing one type of digital integrated circuit with another, attention must be given to the logic swing, output drive capability, dc input current, noise immunity, and speed of each type. Table I shows a comparison of these parameters for COS/MOS, medium power TTL and medium power DTL. The supply voltage column of Table I shows that both saturated bipolar and COS/MOS devices may be operated at a supply voltage of 5 V. Both logic forms are directly compatible at this supply voltage (with certain restrictions).

### Bipolar Driving COS/MOS

When a bipolar device is used to drive a COS/MOS device, the output drive capability of the driving device, the switching levels and input currents of the driven device are important considerations. Table I shows that only 10 picoamperes of dc input current are required by a COS/MOS device in either the "1" or "0" state. The input thresholds, (for the driven COS/MOS device) are 1.5 and 3.5V, hence the output of the TTL/DTL driver must be no more than 1.5V ("0" logic voltage) and no less than 3.5V ("1" logic voltage) in order to obtain some noise immunity.

Table I — Comparison of COS/MOS, TTL, DTL Interfacing Parameters

FAMILY	SUPPLY VOLTAGE (VOLTS)	LOGIC SWING/OUTPUT DRIVE CAPABILITY	DC INPUT CURRENT	NOISE IMMUNITY	PROPAGATION DELAYS
COS/MOS	3.0 to 15	V <sub>SS</sub> to V <sub>DD</sub> (driving COS/MOS) Output drive is type dependent (see text).	10 pA (typical) 1 and 0 State	1.5 at V <sub>DD</sub> = 5V The switching point occurs from 30% to 70% of V <sub>DD</sub> which is 1.5V to 3.5V at V <sub>DD</sub> = 5V	35ns (typical) for inverter C <sub>L</sub> = 15 pF
DTL and TTL	4.5 to 5.5	<u>0 State:</u> 0.4V max. at I <sub>sink</sub> = 16 mA <u>1 State:</u> 2.4V min. at I <sub>load</sub> = -400 μA	<u>0 State:</u> -1.6 mA max. <u>1 State:</u> 40 μA max.	at V <sub>CC</sub> = 5V 0.4V guaranteed. The switching point occurs from 0.8V to 2V	20ns (typical) for inverter C <sub>L</sub> = 15 pF

**Current Sinking**

Fig. 3a shows the low state operation of a loaded bipolar driver stage. When the output drive circuit of the bipolar stage is in the low state, (as shown in Fig. 3b) the collector is essentially at ground potential. The "ON" transistor must go into saturation in order to assure a reliable logic "0" level (0 to 0.4V). To attain this voltage level there should be a high impedance path from the output to the power supply. Current sinking capability is not a problem in this configuration because the COS/MOS devices have extremely high input impedances (typically  $10^{11}\Omega$ ). The voltage level is not a problem either; the COS/MOS devices have high noise immunity (1.5 V).

**Current Sourcing**

Current flows from the V<sub>CC</sub> terminal of a saturated logic output device into the input stages of the load, (i.e., the

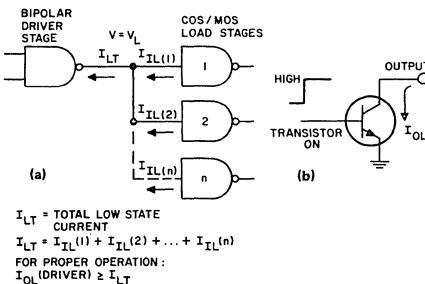


Fig. 3— (a) Low-state operation of a loaded bipolar driver stage. (b) typical bipolar output-drive circuit in the low state.

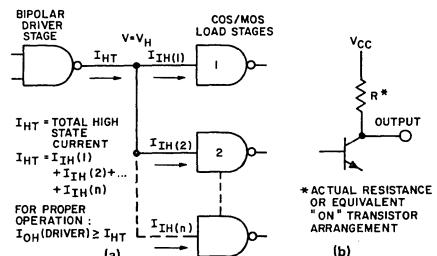
output device acts as the current source for the load). Fig. 4a shows high-state operation of a loaded bipolar driver stage. Whenever a typical bipolar driver circuit is in the high state, a pull up configuration (resistor or transistor) ties V<sub>CC</sub> to the output pin. The total load configuration should not draw sufficient current to reduce the output voltage level below the V<sub>IH</sub> required by the COS/MOS devices.

There are three bipolar output configurations to consider:

- a) Resistor pull-up
- b) Open Collector
- c) Active pull-up

**Resistor Pull-Up**

Devices with resistor pull-ups, (shown in Fig. 4b) present no problem in the interface with COS/MOS devices.



I<sub>OH</sub> = Maximum Permissible output driver current in high state ("1").  
I<sub>OL</sub> = Minimum output driver sinking current in low state ("0").  
I<sub>IL</sub> = Low state input current drawn from the load stage (to the driver).  
I<sub>IH</sub> = High state input current flowing into the load stage from driver.

Fig. 4— (a) High-state operation of a loaded bipolar driver stage. (b) typical bipolar output-drive circuit in the high state.

**Open Collector**

Devices with open collectors require an external pull-up resistor as shown in Fig. 5. The selection of the external pull-up resistor is discussed below. It is recommended that when driving a COS/MOS device from an arrangement such as the one shown in Fig. 5, (with both VDD and VCC supply voltages at 5V) the driver should not fan out to any TTL/DTL gate, but can be fanned out to other COS/MOS devices.

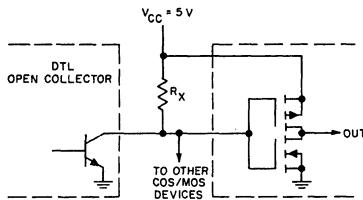


Fig. 5— Example of DTL/TTL circuit with open collectors that require a resistor between the output and VCC.

**Active Pull-Ups**

When an active pull-up is used such as the transistor plus diode arrangement (shown in Fig. 6), there can be a problem in the "1" state because the minimum output level, (2.4V) cannot assure an acceptable "1" state input for the COS/MOS device. The 2.4-volt minimum TTL/DTL output level is often specified at a load current of 400μA. However, negligible current is being drawn by the COS/MOS device, hence the minimum TTL/DTL high-output level would typically be 3.4 to 3.6V under these conditions. There is no noise immunity in such a configuration. Therefore, it is recommended that a pull-up resistor be added from the output terminal of the bipolar device to VCC. The selection of the external pull-up resistor is discussed below. N in the formulae [(2) and (4)] is equal to 1, because it is not recommended that the outputs of devices that use active pull-ups be tied together.

When driving a COS/MOS device from such an output arrangement (as shown in Fig. 7), the driver should not fan out to TTL/DTL circuits; only to other COS/MOS devices.

**PULL-UP RESISTOR SELECTION**

Selection of a pull-up resistor for a circuit requires consideration of fan-out, maximum allowable collector current in the low state ( $I_{OL(max)}$ ), collector-emitter leakage current in the high state ( $I_{CEX}$ ), power consumption, power-supply voltage and propagation delay times. The minimum value of the external pull-up resistor in Fig. 8a is given by:

$$R_X(\min) = \frac{V_{DD} - V_{OL(max)}}{I_{OL} - (M) I_{IL}} \quad (1)$$

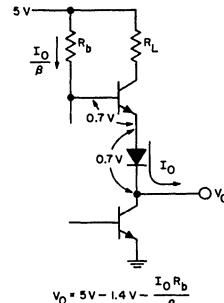


Fig. 6— Transistor-diode pull-up.

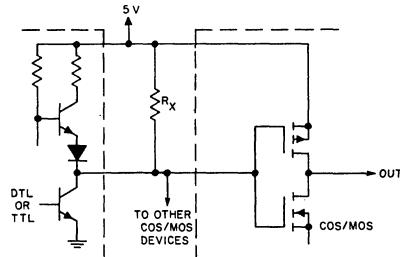


Fig. 7— Modification of the circuit in Fig. 6 to drive COS/MOS devices.

where M is the number of COS/MOS load stages. The maximum value of the external pull-up resistor shown in Fig. 8b is given by:

$$R_X(\max) = \frac{V_{CC} - V_{IH}}{(N) I_{CEX} + (M) I_{IH}} \quad (2)$$

where N is the number of TTL/DTL driver stages.

As previously discussed, the values of  $I_{IH}$  and  $I_{IL}$  for the COS/MOS input currents in both high- and low-level states are approximately 10 pA and are neglected because their value is insignificant when compared with the value of the bipolar currents. Therefore, the equations for bipolar-to-COS/MOS interface using a pull-up resistor can be reduced to:

$$R_X(\min) = \frac{V_{DD} - V_{OL(max)}}{I_{OL}} \quad (3)$$

$$R_X(\max) = \frac{V_{CC(\min)} - V_{IH(\min)}^*}{(N) I_{CEX(max)}} \quad (4)$$

\* $V_{IH}$  in eq. 4 is the value for the COS/MOS Device.

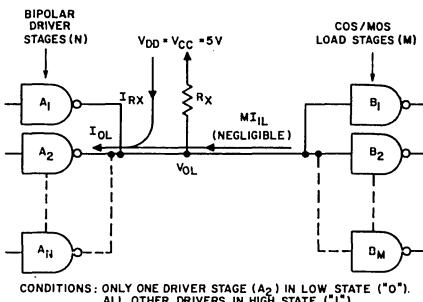


Fig. 8a— Bipolar output (with pull-up resistor) driving COS/MOS in low-state operation.

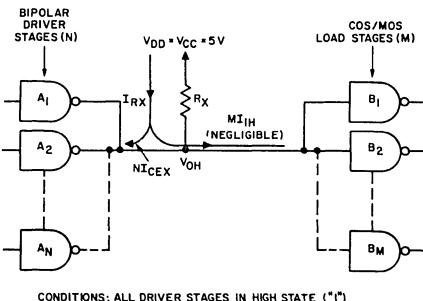


Fig. 8b— Bipolar output (with pull-up resistor) driving COS/MOS in high state operation.

An example in which a typical 9000-series TTL gate is used to drive a CD4000A COS/MOS gate the operating voltage and current specifications might be as follows:

Operating Voltage	Current Specifications
$V_{CC} = 5V \pm 0.5V$	$I_{OL} = 16\text{ mA}$ (TTL Gate)
$V_{DD} = 5V$	$I_{IL} = 10\text{ pA}$ (COS/MOS Gate)
	$I_{IH} = 10\text{ pA}$ (COS/MOS Gate)
	$I_{CEX} = 10\mu\text{A}$ max (TTL Gate)

$V_{OL}$  is obtained from Fig. 1 and is 0.40V;

$V_{IH}$  is obtained from Fig. 2 and is 3.5V.

If N & M are both 1, then:

$$R_{X(\min)} = \frac{(5.5 - 0.4)\text{ V}}{16\text{ mA}} \approx 330\Omega$$

$$R_{X(\max)} = \frac{(5 - 3.5)\text{ V}}{100\mu\text{A}} = 15k\Omega$$

For short propagation delay times, it is best to keep  $R_X$  small. However, power consumption increases rapidly at values below 1000 ohms. Some compromise is necessary. The typical power consumption is 14 mW (with the output of the TTL/DTL gate low) if a 2kΩ resistor is used. Final selection of the pull-up resistor, however, will depend on what is most important for the intended application: high speed or low power.

Figs. 8c and 8d show typical speed/power relationships as a function of  $R_X$  for two popular bipolar open collector drivers. These figures illustrate the trade-off between speed and power; the power figure shown is the power dissipated in both the bipolar driver and the pull-up resistor.

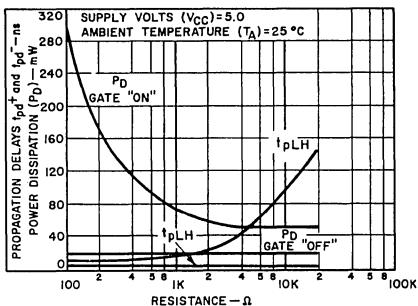


Fig. 8c— Typical speed-power trade-off of open collector TTL buffer and pull-up resistor.

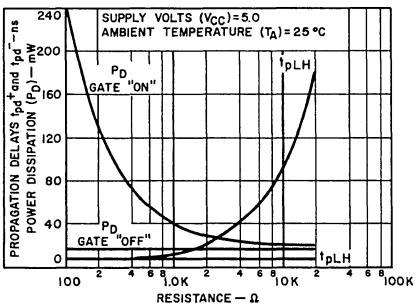


Fig. 8d— Typical speed-power trade-off of open collector TTL gate and pull-up resistor.

#### COS/MOS DRIVING BIPOLAR

Figs. 9a and 10a show COS/MOS devices driving bipolar devices. The current sinking capability of the COS/MOS device must be considered when the device is driving a medium power DTL and TTL circuit. Table I shows that the TTL/DTL device requires no more than  $-1.6\text{ mA}$  in the "0" input state and a maximum of  $40\mu\text{A}$  in the "1" input state.

The COS/MOS device must be capable of sinking and sourcing these currents, while maintaining voltage output levels required by the TTL/DTL gate. Any given TTL/DTL gate will switch state at a voltage that ranges from 0.8 to 2V. Hence the output drive capability of the COS/MOS driver must be at least  $-40\mu A$  for a given "1"-state output voltage of 2V, and at least 1.6 mA for a given "0"-state output voltage of 0.8V. In order to provide a noise margin of 400 mV, for the driven bipolar device, the COS/MOS device must sink 1.6 mA at a "0" logic state voltage of 0.4V and  $-40\mu A$  at a logic "1" level at 2.4 V. For low-power TTL devices the required sink current is  $180\mu A$  at 0.4 V output.

#### Current Sourcing

In the high-state operation, (Fig. 9b)  $V_{DD}$  is normally connected to the driver output through one or more "ON" p-channel devices which must be able to source the total leakage current of the bipolar load stages. The published data for the particular COS/MOS and bipolar devices, must be consulted in order to determine the leakage currents (for the logic "1" state) and drive fan out to be used in the equation shown in Fig. 9a. Saturated-logic devices will not achieve their required switching levels unless this equation has been satisfied. All of the presently available COS/MOS devices are able to source  $40\mu A$  at 2.4V, (supply voltage,  $V_{DD} = 5V$ ), hence current sourcing is not a problem.

#### Current Sinking

When the output of a COS/MOS driver is in the low-state an n-channel device is "ON" and the output is approximately at ground potential. The COS/MOS device sinks the current flowing from the bipolar input-load stage. The published data for the COS/MOS device must be consulted to determine the maximum output low-level sinking current, and the published data for the bipolar device must be consulted to determine its input low-level current.

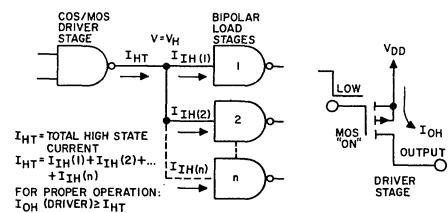


Fig. 9— (a) Logic diagram for a COS/MOS device driving a bipolar device, high-state operation; (b) schematic diagram showing current flow.

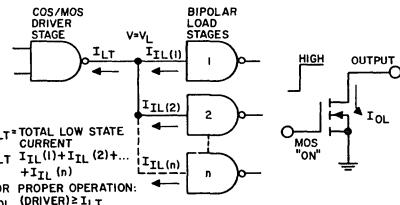


Fig. 9— (a) Logic diagram for a COS/MOS device driving a bipolar device, low-state operation; (b) schematic diagram showing current flow.

Not all COS/MOS devices can sink 1.6 mA required by normal-power TTL devices at only a 0.8 V or 0.4 V "0"-state output level. Table II shows eleven types of COS/MOS circuits and their n-channel current-sinking capabilities at output voltages of both 0.8 and 0.4 V. The hex buffers can each sink 6 mA at 0.8 V and thus can drive 6/(1.6) or, for recommended good noise immunity, three TTL/DTL gates (worst case).

Table II — Current Sinking Limits of COS/MOS Devices

COS/MOS TYPE	DESCRIPTION	SINK CURRENT-mA at +25°C			
		V <sub>O</sub> L = 0.4 VOLTS		V <sub>O</sub> L = 0.8 VOLTS	
		CERAMIC	PLASTIC	CERAMIC	PLASTIC
CD4000A	Dual 3-input NOR Gate Plus Inverter	0.4	0.3	0.8	0.6
CD4001A	Quad 2-input NOR Gate	0.4	0.3	0.8	0.6
CD4002A	Dual 4-input NOR Gate	0.4	0.3	0.8	0.6
CD4007A	Dual Complementary Pair plus Inverter	0.6	0.3	1.2	0.6
CD4009A/ CD4049A	Inverting Hex Buffer	3.0	3.0	6.0	6.0
CD4010A/ CD4050A	Noninverting Hex Buffer	3.0	3.0	6.0	6.0
CD4011A	Quad 2-Input NAND Gate	0.2	0.1	0.4	0.2
CD4012A	Dual 4-Input NAND Gate	0.1	0.05	0.2	0.1
CD4041A	Quad True/Complement Buffer	0.4	0.2	0.8	0.4
CD4031A (Q Output)	64-Stage Static Shift Register	1.3	1.3	2.6	2.6
CD4048A	Expandable 8-Input Gate	1.6	1.6	3.2	3.2

By paralleling inputs of the CD4000A, CD4001A, or CD4002A gates, "N" times the sink current capability listed for each type may be obtained. Thus, all four inputs of one 4-input NOR gate (CD4002A) could be tied together as shown in Fig. 11 for a maximum sink-current capability of 3.2 mA, which allows a fan out of two TTL/DTL gates at 0.8V, or 1 TTL gate at 0.4V.

Most COS/MOS MSI devices (such as counters and shift registers) have limited drive capability, hence their outputs may require buffering if they are to drive TTL/DTL gates. This buffering (use of added driver stages) can be provided by the hex buffers or any device with the same current sinking capability. The logic and circuit diagrams for the CD4009A and the CD4010A are shown in Figs. 12 and 13, respectively.

The CD4009A and CD4010 have the added advantage of shifting voltage levels and may be used to interface TTL with COS/MOS devices operating at supply voltages up to 15 V as shown in Fig. 14. With this driving arrangement, designers who use higher voltages for COS/MOS circuits can achieve the maximum COS/MOS speed capability, as well as to be able to fan out to the bipolar devices. Fan out capability versus supply voltage for a bipolar supply level of 5V and COS/MOS levels of 5 and 10V is given in Table III. The drive capability of most COS/MOS devices enables them to drive some low power bipolar circuits (such as the 54L and 74L series) directly, as shown in Fig. 15. Table IV gives dc fan out capability of COS/MOS devices driving low-power TTL devices in unit loads (as defined by the manufacturer) of 0.18 mA.,

#### COS/MOS-BIPOLAR HTL INTERFACE

Bipolar HTL (high-threshold-logic) circuits operate at voltage levels between 14 and 16V. COS/MOS logic circuits

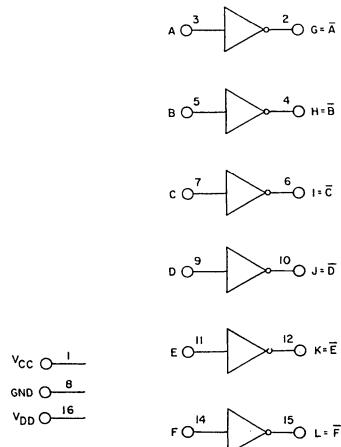
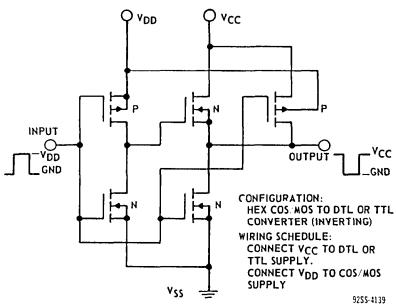


Fig. 12—Logic and circuit diagram for the CD4009A.

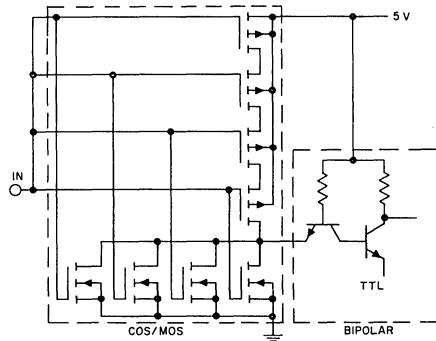


Fig. 11—Method of interconnection of inputs of CD4002A to obtain maximum sink-current capability of 3.2 mA.

can operate at these voltages as well, but generally are limited to voltages no higher than 15V. HTL circuits are, in general, identical in construction to the DTL circuits with some resistance value changes necessary, as a result of the higher voltage levels used and the extremely important distinction of an added base/emitter junction in the reverse direction on the emitter side of the input transistor. This added junction is a zener diode which gives a higher threshold switching voltage. Conduction does not occur until the junction breaks down at a voltage of approximately 6.7V. This provides the HTL with its high noise immunity.

Bipolar high-threshold-logic circuits have a more limited temperature range and dissipate much more power than do COS/MOS circuits. Therefore, care should be exercised when using the combination in extreme temperature environments, as the HTL resistance values vary by about 20 percent from

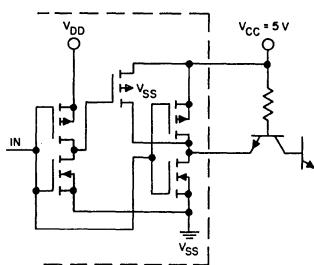
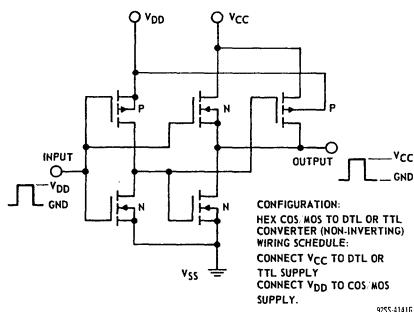


Fig. 14—COS/MOS devices operating at 15 volts interfacing with TTL devices.

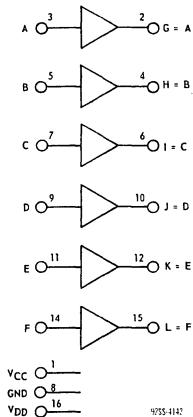


Fig. 13—Logic and circuit diagram for the CD4010A.

one end of their temperature range to the other. In addition, the bipolar transistor's sensitivity to temperature, increases the thermal runaway problems. The VOL level, propagation delay, and noise immunity of HTL circuits vary widely across the temperature range. COS/MOS circuits, however, show almost negligible variation for these same parameters over a temperature range that is approximately 75-percent wider than that of HTL.

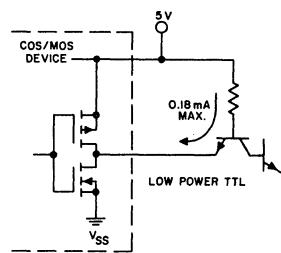


Fig. 15—COS/MOS devices driving low-power bipolar circuits.

The same general rules of interfacing described in the section that discusses COS/MOS-TTL/DTL interface also apply to the interface of HTL with COS/MOS circuits. Fig. 16 shows the voltage characteristics required at the output and input of an HTL device for a  $V_{CC} = 15V$ . Fig. 17 shows the same characteristics for COS/MOS devices at  $V_{DD} = 15V$ . The HTL types either have a built in pull-up resistor (typically  $15k\Omega$ ) or an active pull-up. An external pull-up resistor is unnecessary when COS/MOS devices are being driven by these HTL circuits. There is a difference in the noise immunity for these circuits. The dc noise immunity in the high state (logic "1") will be  $3.5V$  for an active pull-up circuit and  $5V$  (typically) for a resistor pull-up circuit.

Table III — Fanout Capability and Supply Voltage for the CD4009A/CD4049A and CD4010A/CD4050A

$V_{CC} = 0.4V$	$V_{CC} = 0.8V$	$V_{DD}^*$
All Package Types	All Package Types	
2	4	5V
4	7	10V

\* $V_{CC} = 5V$ .

Table IV – DC Fanout Capability of COS/MOS Devices Into Low Power TTL Devices

TYPE	DESCRIPTION	FANOUT (UNIT LOAD = 0.18 mA)			
		PLASTIC		CERAMIC	
		V <sub>OL</sub> = 0.4V	V <sub>OL</sub> = 0.8V	V <sub>OL</sub> = 0.4V	V <sub>OL</sub> = 0.8V
CD4000A	Dual 3-Input NOR gates plus Inverter	1	3	2	4
CD4001A	Quad 2-Input NOR gates	1	3	2	4
CD4002A	Dual 4-Input NOR gates	1	3	2	4
CD4006A	18-Stage Static Shift register	0	0	0	0
CD4007A	Dual Complementary Pair-plus Inverter	1	3	3	6
CD4008A	4-Bit full adder	0	0	0	0
CD4009A	Hex Buffer Inverter	16	33	16	33
CD4010A	Hex Buffer Non-Inverting	16	33	16	33
CD4011A	Quad 2-Input NAND gates	0	1	1	2
CD4012A	Dual 4-Input NAND gates	0	0	0	1
CD4013A	Dual type D Flip-Flops	1	2	2	4
CD4014A	8-Stage static shift register Synchronous parallel-in/serial-out	0	0	0	1
CD4015A	Dual 4-stage static shift register Serial-in/parallel-out	0	0	0	1
CD4017A	Decade counter/divider plus 10 decoded decimal outputs	0	0	0	0
CD4018A	Presettable divide-by-N Counter	0	0	0	0
CD4019A	Quad AND-OR select gate	1	3	2	4
CD4020A	14-Stage binary counter	0	0	0	1
CD4021A	8-Stage static shift register Asynchronous parallel-in/ serial-out	0	0	0	1

The published data should be consulted to be sure that the rise, fall times and pulse widths of the HTL output are compatible with the required pulse width and input rise and fall time of the COS/MOS circuits. The procedure for the selection of a pull-up resistor for open-collector-output HTL circuits is the same as that of the open collector DTL/TTL. (See section that discusses pull-up resistors.) The procedure and equation for COS/MOS devices driving HTL are the same as those for COS/MOS devices driving DTL/TTL. The input current requirements for the HTL devices are obtained from the published data and substituted in the formulae. (See the section that discusses COS/MOS driving bipolar.) For example, the values, taken from the published data, for a COS/MOS CD4009A driving a particular HTL circuit are as

follows:

Particular HTL Input Data: V<sub>CC</sub> = 15V

V<sub>IH</sub> = 8.5V min. I<sub>IH</sub> max. = 2.0 $\mu$ A (leakage)  
 V<sub>IL</sub> = 6.5V max. I<sub>IL</sub>(max.) = 1.2mA

CD4009A COS/MOS output Data: V<sub>DD</sub> = 15V, V<sub>SS</sub> = gnd

V<sub>OH</sub> = 14.99V V<sub>DD</sub> = 15V, V<sub>SS</sub> = gnd  
 V<sub>OL</sub> = 0.01V I<sub>OH</sub> = 10 pA (leakage)  
 I<sub>OL</sub>max. = 6 mA (sinking)

The COS/MOS CD4009A easily provides the necessary voltage levels and sinking currents required to satisfactorily drive 5 of the HTL types in question.

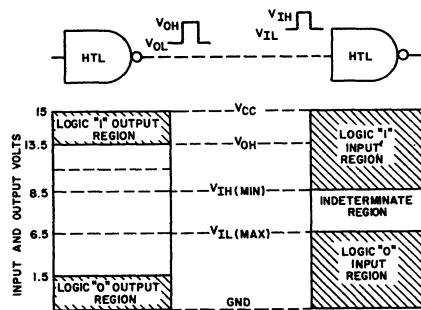


Fig. 16—HTL output and input voltage characteristics at a  $V_{CC}$  of 15 volts.

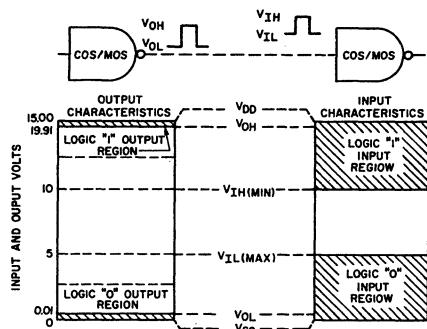


Fig. 17—COS/MOS output and input voltage characteristics at a  $V_{CC}$  of 15 volts.

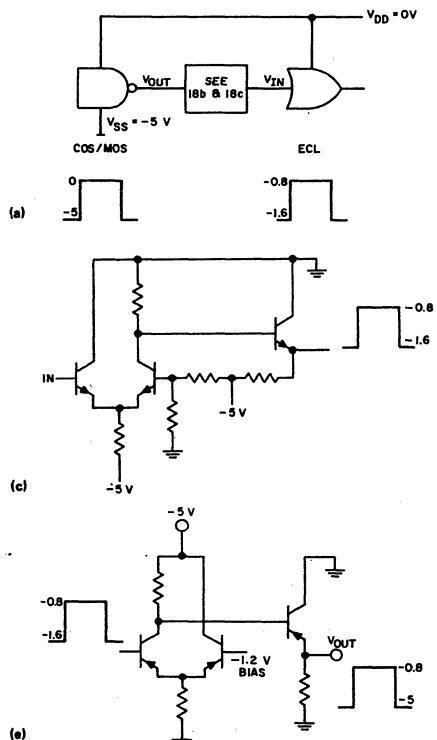


Fig. 18—Interface circuits used with high-speed ECL circuit.

### COS/MOS – ECL/ECCSL INTERFACE

Fig. 18 shows the interface of COS/MOS devices with ECL devices. High-speed ECL (emitter-coupled logic) and ECCSL (emitter-coupled current-steering logic) are non-saturating bipolar logic families. The V<sub>CC</sub> to V<sub>EE</sub> voltage range is fixed from a ground level to -5 or -5.2V; logic "1" to logic "0" values are separated by only 300 to 500 mV depending upon the particular type of ECL family used. Because each manufacturer shows different logic levels for a number of ECL families, care should be taken to use only the applicable values taken directly from the published data which describe the units chosen.

A logic "1" is the most positive frame of reference and a logic "0" the most negative. For example, for positive logic an RCA type CD2150 OR/NOR gate is at a logic "1" level when its voltage is -0.8V and at a logic "0" when its voltage is -1.6V (more negative value).

The COS/MOS device requires a greater voltage swing than that of the ECL, hence an amplifier circuit must be connected between the two when ECL drives COS/MOS. Several RCA linear amplifier circuits have been successfully used to provide higher switching level outputs from the high-speed ECL circuits. Among these are the differential amplifier arrays, (CA3026, CA3028, CA3049, CA3050, CA3051, CA3054) and wideband amplifiers. Use of a separate transistor circuit such as the one shown in Fig. 18e is suggested. Here the transistor must provide a voltage swing at the output of between V<sub>DD</sub> and V<sub>SS</sub> in order to drive the COS/MOS device from an input swing of only 0.8V. Proper biasing of the transistor is essential. It is suggested that the V<sub>SS</sub> level for the COS/MOS circuit be the same as the V<sub>EE</sub> level of the ECL circuit, in order to minimize the number of power supplies as well as to provide better interface conditions.

The interfacing of COS/MOS devices that are driving ECL devices is a simpler matter. A number of methods are available to reduce the output voltage swing to 0.3 to 0.9V. A precise resistor-divider network arrangement, an emitter follower, or numerous combinations of resistor, diode, and transistor configurations can successfully reduce the COS/MOS output swing (V<sub>DD</sub> to V<sub>SS</sub>) to the ECL logic "1" and logic "0" levels. However, care must be taken to meet the necessary current sinking requirements of the ECL device in its logic "0" state. External circuitry is required when the COS/MOS circuit selected does not have the capacity to sink the current from the ECL load. Rise times, fall times, and pulse widths must be restricted to those specified in the published data.

### LEVEL SHIFTERS

The speed consideration is most important when a separate interfacing circuit is used. It is desirable, (unless high ac noise immunity is a prime design consideration) for the speed of the interfacing circuit to be maximized or at least made no slower than either type of logic. No interfacing device other than a pull-up resistor is required, however, between the COS/MOS and TTL logic at a supply voltage of 5 V. Speeds from the COS/MOS to TTL logic (which can be

found in the published data for COS/MOS devices) are comparable to the COS/MOS propagation delays. Speeds from TTL to COS/MOS, even with a large external resistor, are no slower than delay times for COS/MOS logic circuits. Speed, therefore, is not a problem in COS/MOS-TTL logic interfacing, if the clock rates are within the COS/MOS range.

When interfacing DTL or TTL devices with COS/MOS devices which are operated at a higher voltage supply, the same resistor-interface shown in Fig. 5 can be used. The resistor is tied to the higher level (V<sub>DD</sub>). The maximum supply voltage for the DTL and TTL gates, however, is specified at 8V. Thus, not all units of this type may be used for interface applications that require higher supply voltages (V<sub>DD</sub>). Guaranteed operation at these higher supply voltages can be accomplished by selection of DTL and TTL units that have breakdown voltages [V(BR)CER] which exceed the COS/MOS operating voltage, or by using a level shifting circuit such as the level translator shown in Fig. 19. This circuit converts DTL, TTL, and RTL input logic levels to voltages compatible with COS/MOS circuitry. In interface applications, the supply voltage for the translator should be equal to the supply voltage required for the COS/MOS circuitry. The entire COS/MOS supply-voltage range, that exceeds that of the bipolar device, (up to 15V) may be used.

The COS/MOS CD4009A and CD4010A Inverting Hex Buffer and Non-Inverting Hex Buffer types, respectively, were designed to shift voltage levels from a driven high-voltage supply (V<sub>DD</sub>) level. This feature enables designers to operate COS/MOS circuits at 15-volt (V<sub>DD</sub>) levels so that these circuits can achieve their maximum-speed capability, as well as fan out to lower voltage DTL or TTL circuits; or to any other logic forms which operate below the 15-volt level. Further use of these circuits (CD4009A and CD4010A) is described in the COS/MOS-TTL/DTL interface and the COS/MOS-ECL interface sections. The statements in the former section concerning fan out and current sinking are applicable to all other compatible current-sinking logic families as well.

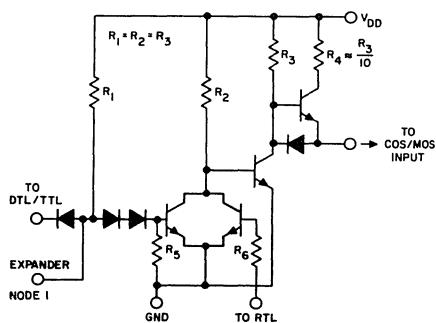


Fig. 19—Level translator used to convert DTL, TTL, and RTL input logic levels and voltages compatible with COS/MOS circuitry.

**COS/MOS TO P-MOS INTERFACE**

A large number of p-MOS devices operate at supply voltages of  $V_{DD}=0$  and  $V_{SS} = -6$  to  $-15$  volts; voltages compatible to those required by COS/MOS devices. However, if the p-MOS system is using a negative logic convention, a conversion of COS/MOS positive logic functions must be made so that the two systems maintain a single logic criterion. Care must be taken when interfacing COS/MOS with p-MOS to assure that the same logic criterion is being used to describe each device type. An explanation of the

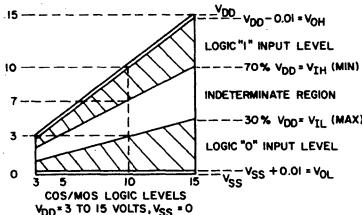
simple transposition from positive-logic NAND to negative-logic NOR and similar transpositions of other functions is given in the RCA COS/MOS Manual section "Logic Design" considerations.

**COS/MOS TO N-MOS INTERFACE**

A number of n-MOS devices are available which function at the same  $V_{DD}$  and  $V_{SS}$  ranges of (COS/MOS devices) and with the same positive voltage logic levels. There is relatively no problem in directly interfacing these devices, when operated at the same  $V_{DD}$  and  $V_{SS}$ .

**Appendix Table I – Common Logic Voltages, Supply Voltage and Temperature Range for COS/MOS Devices**

LOGIC VOLTAGE SYMBOL	DESCRIPTION	
$V_{OH}$	Minimum guaranteed noise free output level of device in high-level output state	
$V_{IH}$	Minimum acceptable input level for device in high-level input state	
$V_{IL}$	Maximum acceptable input level for device in low-level input state	
$V_{OL}$	Maximum guaranteed noise free output level of device in low-level output state	
$V_{NL}$	Maximum (positive) noise level tolerated at low level state	
$V_{NH}$	Maximum (negative) noise level tolerated at high level state	
$V_{OL} + V_{NL} \geq V_{IL}$		
$V_{OH} + V_{NH} \leq V_{IH}$	Operating Temperature Range	
$V_{DD}$	Positive Supply Voltage	-55°C to + 125°C (Full Temperature Prod.)
$V_{SS}$	Negative Supply Voltage	-400°C to + 85°C (Limited Temperature Prod.)



**Appendix Table II – Common Logic Voltages, Supply Voltage, and Operating Temperature Range Required to Interface with DTL/TTL Circuits**

LOGIC VOLTAGE	DESCRIPTION	VOLTAGE (VOLTS)
V <sub>OL</sub>	Maximum output level in low-level output state	0.4
V <sub>OH</sub>	Minimum output level in high-level output state	2.4
V <sub>IL</sub>	Maximum input level in low-level input state	0.8
V <sub>IH</sub>	Minimum input level in high-level input state	2.0
V <sub>CC</sub>	Positive supply voltage	5.0 ± 0.5

Operating Temperature Range: -55° to + 125°C—Full temperature range product.  
0° to + 85°C—Limited temperature range product.

**Appendix Table III – HTL Common Logic Voltages, Supply Voltage and Operating Temperature Ranges**

LOGIC VOLTAGE SYMBOL	DESCRIPTION	VOLTAGE
V <sub>OL</sub>	Maximum output level in low-level output state	1.5V
V <sub>OH</sub>	Minimum output level in high-level output state	13.5V
V <sub>IL</sub>	Maximum input level in low-level input state	6.5V
V <sub>IH</sub>	Minimum input level in high-level input state	8.5V
V <sub>NL</sub>	Worst case positive noise level tolerated at low level state	5.0V
V <sub>NH</sub>	Worst case negative noise level tolerated at high level state	5.0V
V <sub>CC</sub>	Positive supply voltage	15.0 ± 1V

Operating Temperature Range -30°C to +75°C

**Appendix Table IV – ECL Common Logic Voltages, Supply Voltages and Operating Temperature Range**

LOGIC VOLTAGE SYMBOL	DESCRIPTION	VOLTAGE RANGE** FROM	VOLTAGE RANGE** TO
V <sub>OL</sub>	Maximum output level low-level state	-1.6	-1.45*
V <sub>OH</sub>	Minimum output level high-level state	-.8	-.795*
V <sub>IL</sub>	Minimum input level low-level state	-1.4	-1.7*
V <sub>IH</sub>	Maximum input level high-level state	-.75	-1.1
V <sub>NL</sub>	Worst case positive noise level tolerated at low-level state	.20*	.35*
V <sub>NH</sub>	Worst case negative noise level tolerated at high-level state	-.235	-.305*
V <sub>CC</sub>	Positive supply voltage	0	0
V <sub>EE</sub>	Negative supply voltage	-5.5	-5.0

Temperature Range +10 to +60°C

\*At T = +25°C  
\*\*These values are representative of the range for several ECL families.

## **Low-Power Digital Frequency Synthesizers Utilizing COS/MOS IC's**

by R. E. Funk

Low-power low-cost digital frequency synthesizers are now achievable with Complementary Symmetry Metal-Oxide-Semiconductor (COS/MOS) integrated circuits. These devices dissipate nanowatt standby power and milliwatt operational power. The cost effectiveness of MOS/LSI now permits the designer to use digital frequency synthesis.

Digital Frequency synthesizers using integrated circuits offer the communications equipment designer several advantages as compared to the use of tuned circuits and banks of quartz crystals. These are:

1. Employment of digital MSI functions, which reduces the cost and increases reliability;
2. Only one crystal reference is used for all synthesized frequencies;
3. Spurious signals and unwanted harmonics are reduced (yielding a cleaner waveform) by the elimination of tuned circuits (resulting in lower manufacturing-test costs and lower maintenance on equipment);
4. A simplified manual control by replacement of complex, and often unreliable, mechanical turning mechanisms with simple digitally coded switches.

Battery-powered digital frequency synthesizers have not been feasible because bipolar circuits require too much power. Additionally, the cost of this type of equipment could not be justified using bipolar IC's.

This Note describes digital phase-locked loops and the use of COS/MOS integrated circuits in the design and implementation of digital frequency synthesizers.

### **REVIEW OF DIGITAL PHASE-LOCKED LOOP FUNDAMENTALS**

The digital frequency synthesizer uses a phase-locked loop to produce desired output frequencies dependent upon the setting of a programmable counter. The counter is controlled by dialing up frequencies with front-panel control switches. The frequency setting of the switches is always proportional to a given programmable divider ratio.

Fig. 1 shows the phase-lock loop arrangement commonly employed. The output frequency of the programmable divide-by-“N” counter locks onto and tracks the phase of the reference frequency. A phase difference between the divide-by-“N” counter output and the reference frequency produces a correction voltage at the output of the phase comparator. The polarity of this correction voltage is such that it will pull the voltage-controlled oscillator (VCO) frequency in such a direction that the divide-by-“N” output frequency will phase-track the reference frequency. Thus, for each setting of the frequency control switches, a digital code presets the divide-by-“N” count to an integral number representing a desired output frequency. For each desired

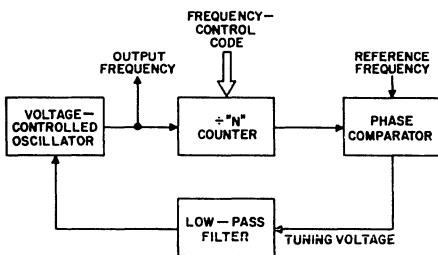


Fig. 1. Basic digital phase-locked loop

output frequency, there is a corresponding unique phase difference and tuning voltage. At each "tuned condition", it is to be noted that the divide-by-'N'-counter output frequency is phase-locked to the reference frequency and that the two frequencies are equal.

A low-pass filter is employed in phase-locked loops to remove time-variant components from the VCO control voltage. Otherwise, for example, the reference frequency and its harmonic output from the phase detector may be of sufficient magnitude to cause an audio-rate phase jitter at the VCO output, which can result in a most unpleasant distortion of the audio output.

### PRACTICAL DIGITAL PHASE-LOCKED LOOPS

In practical digital phase-locked loops for communications systems, VCO-output frequencies are often in the VHF and UHF bands, that is, from 30 to 400 MHz, and it is usually impractical or impossible to design IC divide-by-'N' counters that will operate within this range. For example, even high-power ECL circuits will not permit use of the complex divide-by-'N' function above 100 MHz. Required are low-cost techniques of lowering the VCO output frequency so that cost-effective low power MSI and LSI arrays can be employed as the logical divide-by-'N' counter. For low-power portable communications sets, efficient

COS/MOS arrays are employed using either of two basic techniques for lowering VCO output frequencies. These two techniques are prescaling and heterodyne down-conversion; they are described below.

#### Prescaling

In the phase-locked loop diagram of Fig. 2 a fixed counter prescales the VCO output frequency down by a division factor of "K" to the greatest value ( $f_k$  max) that can be handled by the I-C divide-by-'N' counter. The reference frequency ( $f_r$ ) is nominally equal to the channel spacing frequency ( $f_c$ ). However, where a prescaling counter is employed, the value of  $f_r$  must be reduced by a division by "K". Hence:

$$f_r = \frac{f_c}{K} \quad (1)$$

Phase-comparator reference frequencies are normally in the 1-to-10-kHz range, while the highly stable crystal-controlled oscillators usually operate ( $f_x$ ) in the 2-to-5-MHz range. For this reason, divide-by-'R' counters are employed where  $f_r = \frac{f_x}{R}$ .

At phase-lock, the divide-by-'N' output frequency ( $f_n$ ) tracks the reference frequency  $f_r$ , and so  $f_n = f_r$ . Furthermore, the modulo of the divide-by-'N' counter ( $N$ ) uniquely determines the output frequency ( $f_o$ ) that will satisfy the equation:

$$f_o = f_n K N. \quad (2)$$

K operates in a fixed-integer counter, and N operates in a programmable modulo-N counter where the modulo is programmed by an external frequency-control code. The range of N is given by:

$$N_{\max} = \frac{f_o \max}{f_c}, \quad (3)$$

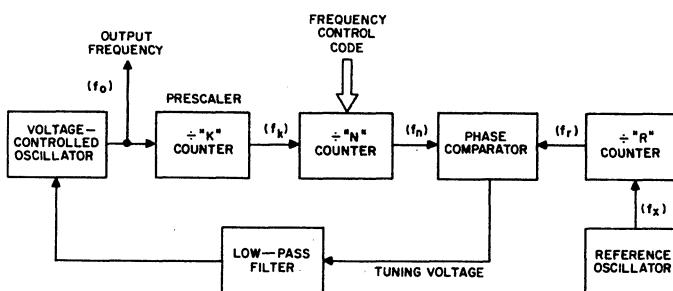


Fig. 2. Digital phase-locked loop with prescaler

and

$$N \min = \frac{f_0 \text{ min}}{f_c} \quad (4)$$

Having specified values of  $K$ ,  $N$ ,  $R$ ,  $f_X$ ,  $f_0$ , and  $f_c$ , it is simple arithmetic to completely specify all digital functions including the phase comparator, which, in most cases, also functions digitally. Further, the divide-by-“ $N$ ” counter can be broken into decade or binary segments. This leads directly to specification of programmable-switch design. The low-pass filter can now be specified for optimum rejection of reference-frequency components.

However, since the frequencies of signals within the loop of Fig. 2 vary over a range of  $N$ , optimum stabilization of the negative part of the loop is compromised by the variation of gain with frequency. In addition to loop stabilization, the designer must also consider several other aspects of phase-locked loops. These matters are well covered in literature on the subject and include:

1. Loop settling time, loop switching time,
2. Resolution: related to reference-oscillator accuracy,
3. Spectral purity: A. spurious outputs,  
B. Signal-to-phase-noise ratio,
4. Loop modulation: Practical mode for transceivers,
5. Sweep mode: Applicable to test equipment usage,
6. System interface: A. Remote code programming,  
B. Preset channel memory.

#### Heterodyne Down-Conversion

Fig. 3 illustrates a digital phase-locked loop employing heterodyne down-conversion. Here the input frequency to the divide-by-“ $N$ ” counter ( $f_k$ ) is described as follows:

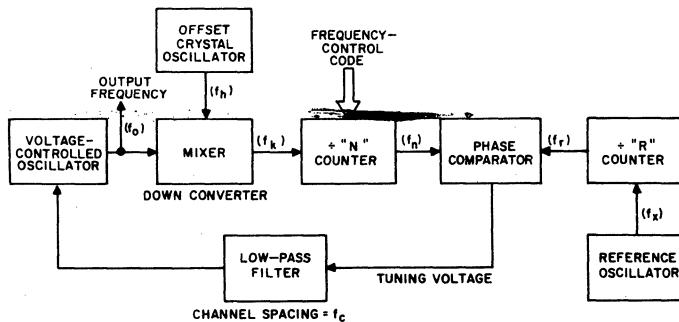


Fig. 3. Digital phase-locked loop with heterodyne down-converter

$$f_k = f_0 - f_h \quad (5)$$

An offset crystal oscillator is employed to “mix down” the VCO output frequency ( $f_0$ ), and the desired output frequency range of  $f_k$  is enclosed by suitable band-pass filtering. In the scheme shown in Fig. 3, the output frequency is expressed as:

$$f_0 = f_n N. \quad (6)$$

The input frequency to the “ $N$ ” counter is given by:

$$f_k = f_0 - f_h. \quad (7)$$

The range of the “ $N$ ” counter is defined by these two equations:

$$N \max = \frac{f_k \text{ max.}}{f_c}, \quad (8)$$

$$N \min = \frac{f_k \text{ min.}}{f_c}. \quad (9)$$

In many synthesizer systems employing heterodyne down-conversion, more than one value of offset frequency ( $f_h$ ) is switched in. For example, if the desired VCO output frequency band is broken into two equal ranges, and if values of  $f_h$  are switched in for the two respective bands, the range of  $N$  will be exactly half that used in a prescaling system. The range of  $N$  will be traversed twice in tuning across the entire band. Practical application of this method is illustrated two paragraphs below in the description of an FM-broadcast-band synthesizer.

Advantages of heterodyne down-conversion are:

1. The reference frequency ( $f_r$ ) equals the channel spacing ( $f_c$ ); hence, the loop band-pass is wider,
2. Lowest power consumption; therefore, the offset oscillator and mixer can be extremely efficient.

The disadvantage of the heterodyne technique is that, because a second reference crystal and a mixer are needed, the designer may be afforded an unsought opportunity to demonstrate his prowess in eliminating spurious beat and sum frequencies.

### COS/MOS IN FM RECEIVER SYNTHESIZERS

#### SYSTEM REQUIREMENTS

FM-broadcast-receiver synthesizers can be designed to use efficient COS/MOS IC's as principal counter elements. Both heterodyne and prescaling system techniques will be examined.

One-hundred FM channels are spaced 200 kHz apart in the 88-to-108-MHz band. The channel-1 carrier frequency is 88.1 MHz; channel 100 is 107.9 MHz. Since the standard FM if frequency is centered at 10.7 MHz, the synthesizer must provide high-side LO-injection output frequencies of 98.8 to 118.6 MHz.

#### PRESCALER SYSTEM DESIGN

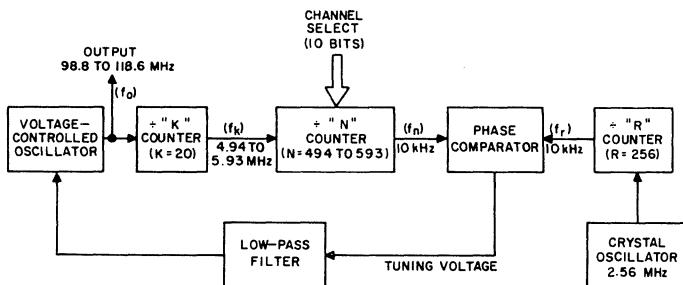
FM synthesizer design parameters can be calculated and plugged into the block diagram of Fig. 4. The resulting synthesizer block diagram and parameter calculations are illustrated in Fig. 4. Each block is described below.

#### Divide-by-“N” Counter

The divide-by-“N” counter is parallel loaded to have a unique count (modulus) for each required synthesizer output-channel frequency. It has been demonstrated that each counter step represents a 200-kHz channel. For example, to tune the system to 118.6 MHz, a count of 593 (See Fig. 4) is loaded into the counter and, hence, “divide-by-593” results. The “N” counter should be considered as counting down repeatedly from 593 to zero. Fig. 5 illustrates this counter's organization. Note that for each frequency integer, there is a one-to-one relation between each switch (one frequency integer) and the corresponding counter block.

For example, a divide-by-5 counter programs the 200-kHz integer. Five counts of this counter step the 1-MHz counter by a “1” count, etc.

While the span of the “N” counter must be 494 to 593, as illustrated in Fig. 4, the actual range of a practical “N”-counter for an FM-band digital synthesizer can be offset as indicated in Table I. Here 6 counts (equivalent to a 1.2-MHz offset) are added to both the top and bottom of the counter range to make the actual count span from 500 to 599; two simplifications in the synthesizer design result from this refinement: (1) the 100-MHz binary count shown in Fig. 5 always starts in the 100-MHz state, and, therefore, it does



$$f_c (\text{CHANNEL SPACING}) = 200 \text{ kHz}$$

$$k = 20$$

$$f_k = \frac{f_0}{20}; f_k \text{ MAX.} = \frac{118.6 \text{ MHz}}{20} = 5.93 \text{ MHz}, f_k \text{ MIN.} = \frac{98.8 \text{ MHz}}{20} = 4.94 \text{ MHz}$$

$$f_r = \frac{200 \text{ kHz}}{20} = 10 \text{ kHz}$$

$$N \text{ MAX.} = \frac{118.6 \text{ MHz}}{200 \text{ kHz}} = 593$$

$$N \text{ MIN.} = \frac{98.8 \text{ MHz}}{200 \text{ kHz}} = 494$$

$$R = \frac{2.56 \text{ MHz}}{10 \text{ kHz}} = 256$$

Fig. 4. FM-band synthesizer using prescaler

Table I. Divide-by-“N”-Count/Frequency Relationships

CHANNEL NO.	FM RECEIVER FREQUENCY (fm) MHz	LO INJECTION FREQUENCY ( $f_o$ ) (fm + 10.7) MHz	REQUIRED “N” COUNT	OFFSET FREQUENCY ( $f_o + 1.2$ MHz) MHz	OFFSET N-COUNT (N + 6)
1	88.1	98.8	494	100.0	500
2	88.3	99.0	495	100.2	501
3	88.5	99.2	496	100.4	502
4	88.7	99.4	497	100.6	503
5	88.9	99.6	498	100.8	504
6	89.1	99.8	499	101.0	505
⋮	⋮	⋮	⋮	⋮	⋮
98	107.5	118.2	591	119.4	597
99	107.7	118.4	592	119.6	598
100	107.9	118.6	593	119.8	599

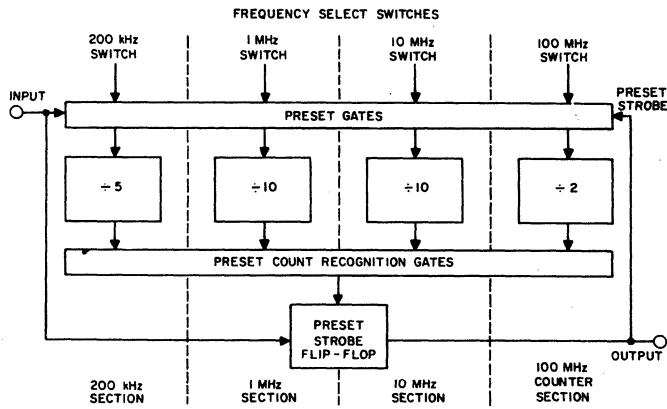


Fig. 5. Divide-by-“N” counter organization

not have to be under switch control, and (2) the necessary one-to-one correspondence between switch position and “N”-count preset state is achievable. The latter statement means that when switching from channel 5 to channel 6, as shown in Table I, the system is in fact switching from the 88.9-MHz channel to the 89.1-MHz channel. Note that the two least significant integers switch over. Note further that as the actual LO-injection frequency goes from 99.6 MHz to 99.8 MHz only one integer switches over. However, the 1.2-MHz-offset frequencies of 100.8 and 101.0 MHz do switch

over in the two least significant integers. Therefore, the 1.2-MHz offset makes it possible to use the needed switch-compatible “N” counter.

Fig. 6 is a logic diagram showing the four counting elements of the “N” counter illustrated in Fig. 4. Table II contains the counter truth tables, and Fig. 7 is a detailed logic diagram of the divide-by-5 counter. Table III illustrates that the 9-bit frequency-select code permits presetting the “N” counter to counts ranging from 500 to 599. The counter

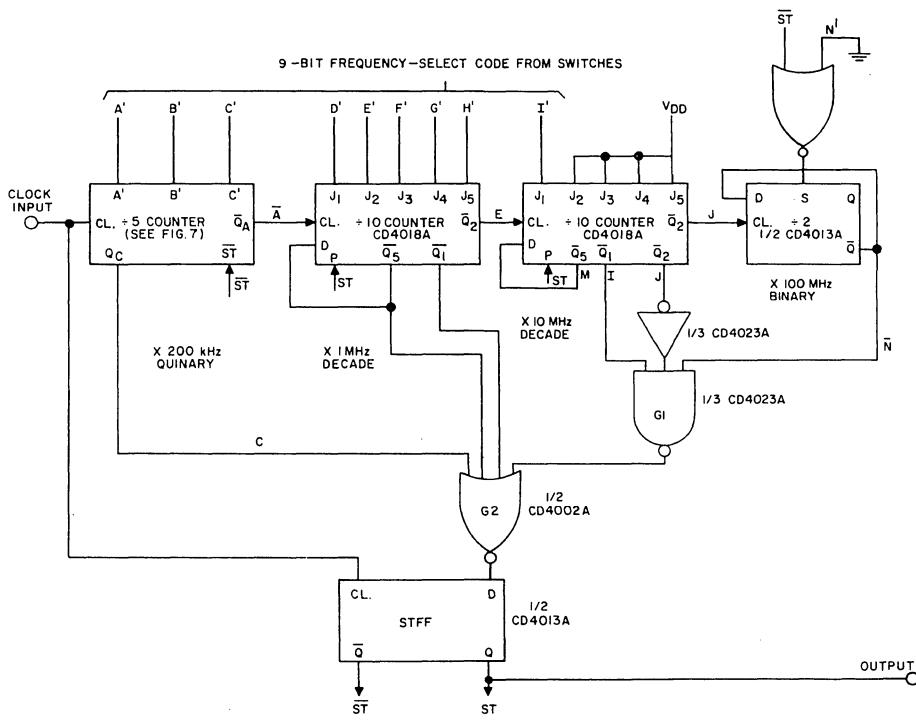


Fig. 6. Divide-by-'N' counter logic

"down-counts" to the "8" state, at which time a preset strobe count-recognition signal goes "high" (Output of G2 of Fig. 6). Fig. 8 shows the critical preset strobe-generation timing sequence. Following the "high" that appears on D of STFF (Fig. 6), the strobe goes "high" on the next positive clock transition as shown in Fig. 8. The strobe presets the entire "N" counter to the dialed frequency. Note that the immediately succeeding positive clock transition is lost due to its being overlapped by the preset strobe. The second following clock transition, however, trips the counter to state N-1. Table IV is a wiring truth table for two frequency-select switches, S<sub>1</sub> and S<sub>2</sub>. The nine wires, A' through N', follow the patterns indicated and interface directly with the divide-by-'N' counter of Fig. 6.

#### Divide-by-'N'-Counter Implementation

The divide-by-'N' counter is the frequency-control element of the digital phase-lock loop. It is logically complex and must operate at the highest possible frequency consistent with minimum power for battery operation. The COS/MOS low-voltage technology exhibits several characteristics that allow outstanding divide-by-'N'-counter performance. The

COS/MOS implementation and performance will be examined in depth.

Figs. 6 and 7 show COS/MOS counter logic containing the following complement of eight low-voltage devices.

- 1 CD4023A Triple 3-Input NAND Gate
- 1 CD4001A Quad 2-input NOR Gate
- 1/2 CD4002A Dual 4-input NOR Gate
- 3 CD4013A Dual "D" Flip-Flop
- 2 CD4018A Presettable Decade Counter

Characteristics of the above devices are contained in data sheets in RCA bulletin 479. This family of low-voltage devices (3 volts to 15 volts) exhibits a typical flip-flop toggle rate of 10 MHz at 10 volts and a typical gate delay of 25 nanoseconds at 10 volts. In both cases a fan-out of 3 (15 picofarads) is used.

Before examining the performance of the "N" counter, some additional operating details are of interest. The four counter sections shown in Fig. 6 are rippled; that is, they are not synchronously clocked. Because of that, speed and, hence, COS/MOS power, is substantially less in each succeeding counter section from left to right; the divide-by-2

Table II. Divide-By-“N” Counter Truth Tables

(a) Divide-by-5 Counter

X200 kHz	A	B	C
4	0	1	1
3	0	0	0
2	1	0	0
1	1	1	0
0	1	1	1

(b) Divide-by-10 Counter

X1 MHz	D	E	F	G	H
X10 MHz	I	J	K	L	M
9	0	0	1	1	1
8	0	0	0	1	1
7	0	0	0	0	1
6	0	0	0	0	0
5	1	0	0	0	0
4	1	1	0	0	0
3	1	1	1	0	0
2	1	1	1	1	0
1	1	1	1	1	1
0	0	1	1	1	1

(c) Divide-by-2 Counter

X100 MHz	N
1	1
0	0

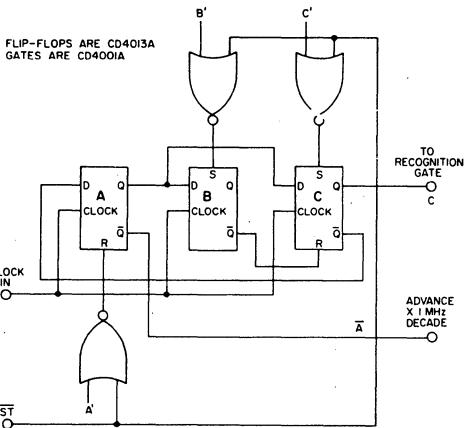


Fig. 7. Divide-by-5 counter logic

counter, for example, operates at one five-hundredth of the input-clock rate.

Briefly, counter operation is as follows:

(1) The synchronous divide-by-5 counter (Fig. 7) advances the 1-MHz decade counter once every five counts; that is, when A goes from 1 to 0 as shown in Table II(a).

(2) The synchronous 1-MHz decade counter advances the 10-MHz decade once every 50 counts; that is, when E goes from 1 to 0 as shown in Table II (b).

(3) The 10-MHz decade advances the 100-MHz binary counter once every 500 counts, that is, when J goes from 1 to 0.

(4) Preset count-logic state-recognition occurs at count 8 as shown in Table III.

(5) Preset strobe generation occurs at count 7 as shown in Fig. 8.

The CD4018A decade counter, which is a 5-stage Johnson-counter configuration, has two outstanding characteristics.

1. Each flip-flop changes state at one-tenth of the input rate; hence, the power/speed ratio is minimized.

2. Frequency-control switching is accomplished using a single-wafer Johnson-code switch. A simple miniaturized 2-pole 10-position switch is available from Grayhill (See Fig. 9).

#### Divide-by-“N”-Counter Performance

Fig. 10 shows the divide-by-“N” counter's power consumption as a function of operating frequency with a  $V_{DD}$

of 15 volts. The curves show that a frequency of 8.7 MHz is possible. Maximum operating frequencies for 10 volts and 5 volts are 6.2 MHz and 2.7 MHz respectively. The maximum operating frequency required by the circuit in Fig. 4 is 5.93 MHz, which can be obtained with a supply potential of 9.6 volts and with a power consumption of 47 milliwatts.

Operation of the divide-by-“N” counter using only a 3-volt power supply is possible; in such a case, the maximum operating speed is 55 kHz and the power consumption is only 40 microwatts.

Fig. 11 illustrates the decrease in maximum operating frequency as the temperature is increased. This curve shows that up to 50°C the 5.93-MHz operation can be achieved at a supply potential of 10 volts. The dynamic signal power remains fairly constant from -25°C to more than +100°C, variations being well within 10 percent of the power dissipated at 50°C, as shown in Fig. 12.

For 6-MHz operation at 10 volts, the critical timing waveforms for generation of the preset strobe are shown in Fig. 13. Delay from the positive edge of the clock pulse of count 9 (Fig. 8) to the output of gate 2 (Fig. 6) is 250 nanoseconds. Maximum allowable delay is 320 nanoseconds or nearly two clock periods at 6 MHz. Thus, 60 nanoseconds of margin exist for safe operation.

The complementary nature of the COS/MOS devices permits a wide range of operating voltages to be used and yields high noise immunity. For example, the p and n thresholds are typically 1.5 volts for RCA CD4000A-series devices, permitting operation from 3 to 15 volts. Fig. 14 illustrates that 6-MHz operation can be achieved using a 12-volt supply having 2.3 volts peak-to-peak ripple.

Table III. Divide-By-'N' Counter Recognition-State Truth Table

COUNT	TRUTH TABLE CODE													
	A	B	C	D	E	F	G	H	I	J	K	L	M	N
599	0	1	1	0	0	1	1	1	1	1	1	1	1	1
598	0	0	0	0	0	1	1	1	1	1	1	1	1	1
597	1	0	0	0	0	1	1	1	1	1	1	1	1	1
														$N_{\max.} \equiv 599 - 6 = 593$
501	1	1	0	0	1	1	1	1	0	1	1	1	1	1
500	1	1	1	0	1	1	1	1	0	1	1	1	1	1
499	0	1	1	0	0	1	1	1	0	0	1	1	1	0
														$N_{\min} \equiv 500 - 6 = 494$
10	1	1	1	1	1	1	1	0	0	1	1	1	1	0
9	0	1	1	1	1	1	1							
8	0	0	0	1	1	1	1	1						Recognition State
7	1	0	0	1	1	1	1	1						Generate Preset Strobe
6	1	1	0	1	1	1	1	1						Effective "O" State
5	1	1	1	1	1	1	1	1						
4	0	1	1	0	1	1	1	1						
3	0	0	0	0	1	1	1	1						
2	1	0	0	0	1	1	1	1						
1	1	1	0	0	1	1	1	1						
0	1	1	1	0	1	1	1	1						

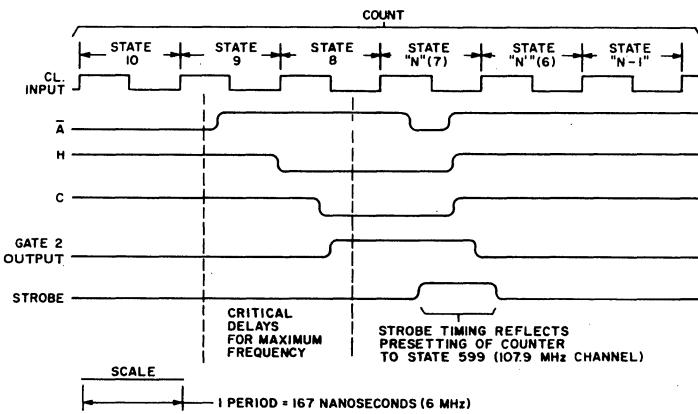


Fig. 8. Divide-by-'N' preset state timing

Quiescent power dissipated by any COS/MOS logic system is extremely low, and the quiescent power dissipated at +25°C by the "N" counter of Fig. 6 is 2 microwatts at a V<sub>DD</sub> of 10 volts. Fig. 15 shows the increase in quiescent power with increasing temperature. For the system described, however, the "N" counter runs continuously, so the quiescent power figure is academic, although some ultra-

low-power digital frequency-synthesizer systems do place the "N" counter and other loop elements on standby power periodically.

The complete divide-by-'N' logic system shown in Fig. 6 can be integrated on one practical-sized LSI COS/MOS chip. For example, the logic of Fig. 6 uses approximately

Table IV. Frequency-Select Switch Table

S1 (kHz)					
RECEIVER FREQUENCY kHz	POS.	WIRES			
		A'	B'	C'	
900	5	0	0	0	
700	4	0	1	1	
500	3	1	1	1	
300	2	1	0	1	
100	1	1	1	0	

NOTE

"0" ≡ GROUND  
 "1" ≡ V<sub>DD</sub>

1000 active transistors, definitely a state-of-the-art number of devices. Also, less than 16 I/O leads are necessary, making it feasible to package such a customized counter in a low-cost 16-lead plastic package. A more universal COS/MOS 4-decade counter, the CD4059A (Preliminary) can be adapted for use as the ÷ N counter.\*

It is fair to compare the COS/MOS power consumption to the power consumption of a bipolar "N" counter performing the identical function. The popular 54N TTL logic, or the equivalent, is used for high-speed counting, as shown in Fig. 16, and 54L logic, or the equivalent, is used for lower-speed functions.

Approximately 265 milliwatts at +5 volts is required by the bipolar design of Fig. 16, compared with only 50 milliwatts for the COS/MOS design at a V<sub>DD</sub> of 10 volts.

## Divide-by-“R” Counter

The FM receiver synthesizer system shown in Fig. 4 requires a fixed reference counter to divide by 256. To accomplish this, a 2.56-MHz reference crystal oscillator is counted down to the 10-kHz phase-comparison frequency.

\* If the CD4059A (Preliminary) is employed, K must be increased from 20 to 40 and other loop parameters adjusted accordingly. Also, the CD4059A (Preliminary) is controlled using BCD-coded switches.

		S2 (MHz)					
RECEIVER FREQUENCY MHz	POS.	WIRES					
		D'	E'	F'	G'	H'	I'
107	20	0	0	1	1	1	1
106	19	0	0	0	1	1	1
105	18	0	0	0	0	1	1
104	17	0	0	0	0	0	1
103	16	1	0	0	0	0	1
102	15	1	1	0	0	0	1
101	14	1	1	1	0	0	1
100	13	1	1	1	1	0	1
99	12	1	1	1	1	1	1
98	11	0	1	1	1	1	1
97	10	0	0	1	1	1	0
96	9	0	0	0	1	1	0
95	8	0	0	0	0	1	0
94	7	0	0	0	0	0	0
93	6	1	0	0	0	0	0
92	5	1	1	0	0	0	0
91	4	1	1	1	0	0	0
90	3	1	1	1	1	0	0
89	2	1	1	1	1	1	0
88	1	0	1	1	1	1	0

Here, one CD4020A 14-stage ripple-carry counter may be used. Fig. 17 shows power consumption as a function of supply voltage for this counter. For a V<sub>DD</sub> of 5 volts, power is below 3 milliwatts for the 2.56-MHz input. If an even lower-threshold-voltage COS/MOS device is used for the reference counter, such as the RCA TA5938, operating voltage and, hence, power consumption can be even lower. The TA5938 is a 14-stage counter (CD4020A) manufactured with an ultra-low-threshold process, but still using the basic COS/MOS metal-gate technology. The thresholds of the TA5938 are less than 1 volt. Fig. 17 shows that only 0.4 milliwatts are consumed for 2.56-MHz operation using the TA5938 at a supply potential of 2.3 volts.

## Phase Comparator

A simple type "D" flip-flop (COS/MOS CD4013A) will suffice for a phase comparator in the digital phase-lock loop system of Fig. 4. Fig. 18 shows the simple flip-flop phase comparator and low-pass filter; Fig. 19 demonstrates the operation of this phase comparator. Note that a positive charge is impressed on the low-pass filter when f<sub>n</sub> > f<sub>r</sub> in the case shown. Also, phase-lock can occur only during 180° of

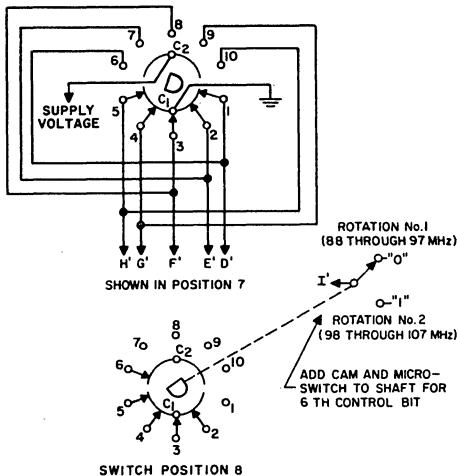


Fig. 9. Frequency control switch S2(Ref. Table IV)

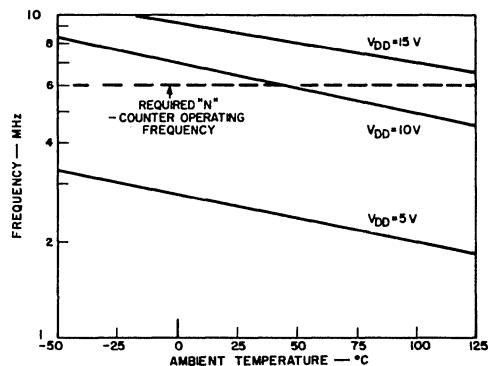


Fig. 11. Divide-by-'N'-counter temperature-frequency characteristics

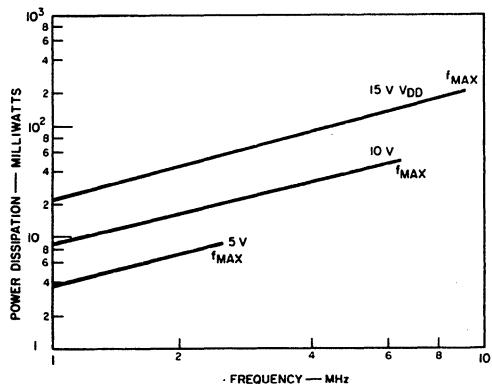


Fig. 10. Divide-by-'N'-counter power consumption

the period. In the case shown in Fig. 19, negative feedback in the loop exists during the  $180^\circ$  when  $f_r$  is positive. When  $f_n$  coincides with the negative-half phase of  $f_r$ , positive feedback exists in the loop and lock-up cannot occur. The waveforms of Fig. 19 show that when:

$$f_n = f_r,$$

lock-up exists, and that when  $f_n > f_r$ , or  $f_n < f_r$  either an out-of-lock condition exists or an error-correction voltage is being produced during lock-up.

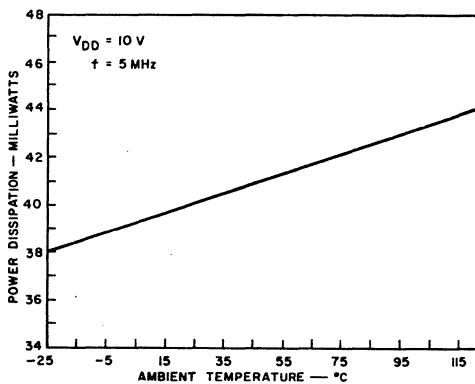


Fig. 12. Divide-by-'N'-counter dynamic power dissipation

The simple COS/MOS flip-flop phase comparator of Fig. 18 consumes only 0.1 milliwatts at a  $V_{DD}$  of 10 volts. Although only one I-C flip-flop is required, a bulky LC filter must be provided to smooth and store the output error voltage. Also, such a phase comparator is non-centering; when loss of an input signal occurs, a maximum error voltage is created.

Another example of a COS/MOS low-power phase comparator is the familiar Exclusive-OR gate (CD4030A).

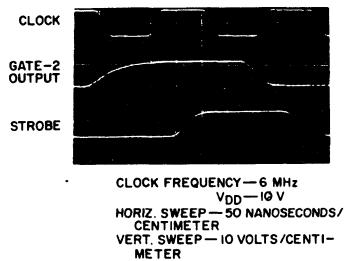


Fig. 13. Strobe generation timing

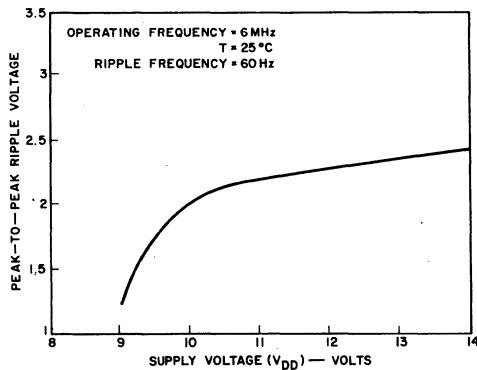


Fig. 14. Divide-by-'N'-counter ripple-frequency characteristics

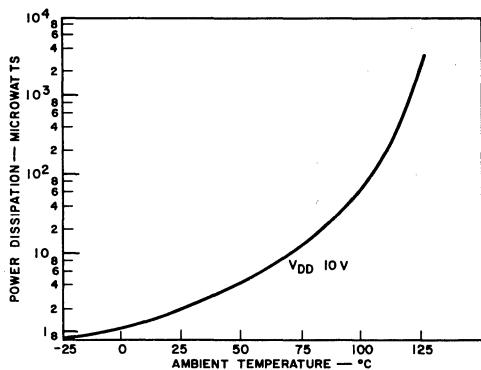


Fig. 15. Divide-by-'N'-counter quiescent power dissipation

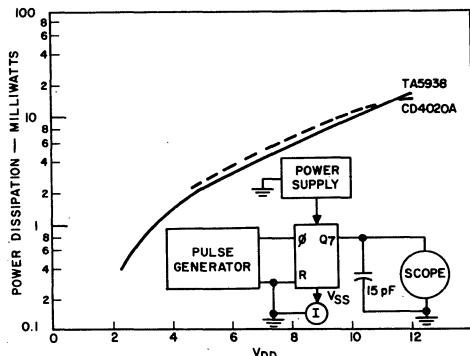


Fig. 17. Divide-by-'R'-counter power consumption

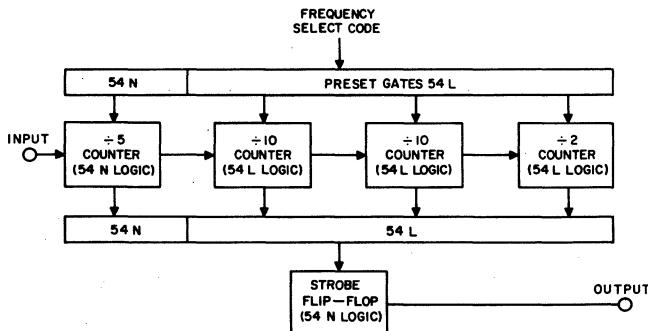


Fig. 16. Bipolar-logic divide-by-'N' counter

The primary advantage in the use of this unit is that it will produce an error voltage for frequency centering when one of the inputs is lost. Either the Type I or Type II phase comparator of the CD4046A (low-frequency phase-locked-loop device) may also be used.

Another high-performance phase comparator is a sample-and-hold circuit employing COS/MOS as shown in Fig. 20. The sample-and-hold phase comparator will substantially reduce the 10-kHz carrier frequencies, thus reducing filter requirements for the loop and increasing the loop's gain-bandwidth product. COS/MOS IC's are used as the ramp generator and the sampling switch as illustrated in Fig. 21. Total power consumption at 10-kHz operation is less than 15 milliwatts.

#### Crystal Oscillator

The required 2.56-MHz crystal oscillator can be implemented with a COS/MOS inverter-amplifier and feed-back network as shown in Fig. 21.

The inverter is one-third of a CD4007A IC. Power consumption is approximately 2 milliwatts at a V<sub>DD</sub> of 5 volts.

#### SUMMARY OF DIVIDE-BY-“N” COS/MOS SUBSYSTEM

It has been demonstrated that COS/MOS can be effectively utilized in the synthesizer's divide-by-“N” and divide-by-“R” functions, in phase comparators, and in crystal oscillators.

Ten currently available CD4000A low-voltage COS/MOS parts can be utilized in the design of the COS/MOS portion of the FM synthesizer phase-locked loop. Soon, with the availability of a universal divide-by-“N” subsystem, only three IC's will be needed to do the job. On a custom basis, the entire divide-by-“N”, divide-by-“R”, and phase-comparator functions can be integrated on one COS/MOS chip; this will be exceptionally cost effective and will also result in lower over-all power consumption.

For the complete synthesizer employing digital pre-scaling as shown in Fig. 4, the power consumption of the VCO and prescaler must be added to obtain the total synthesizer power of 204.4 milliwatts as shown in Table V. It is estimated that if the prescaler were designed to use high performance discrete devices it would consume less than 125 milliwatts and the VCO's could be designed to consume less than 25 milliwatts.

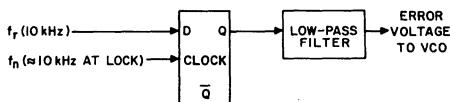


Fig. 18. Flip-flop phase comparator

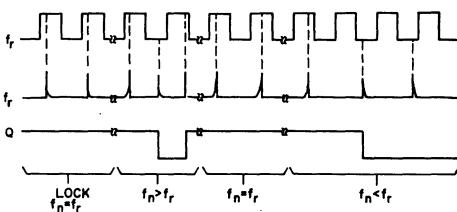


Fig. 19. Flip-flop phase comparator operation

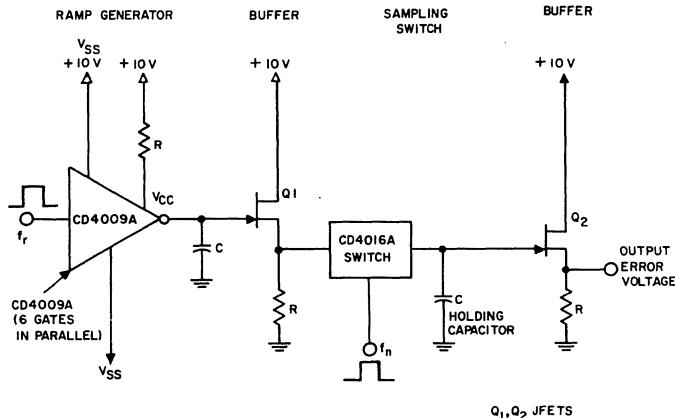


Fig. 20. Sample-and-hold phase comparator

## FM SYNTHESIZER SYSTEM USING HETERODYNE DOWN-CONVERSION

From the previous discussion of the prescaling FM receiver synthesizer, it is apparent that system consumes relatively large amounts of power. The system described in Fig. 3, however, illustrates a heterodyne down-conversion technique that avoids high-frequency digital prescaling. Fig. 22 shows a detailed block diagram of a down-conversion system where a divide-by-2 prescaler is also employed to simplify the design.

Table VI shows how the heterodyne down-conversion operates. For frequencies selected between 88.1 MHz and 97.9 MHz, the respective LO-injection frequencies of 98.8 MHz and 108.6 MHz are down-converted by 98 MHz to 0.8 MHz and 10.8 MHz respectively. The range between those two frequencies is then prescaled by 2 down to 0.4 MHz and 5.4 MHz, which is the range of operating frequencies for the divide-by-“N” counter. For the divide-by-“N” counter of Fig. 22 the range is given by:

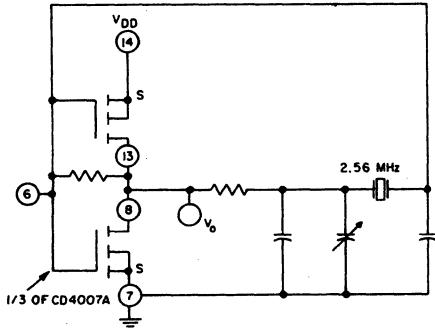


Fig. 21 Crystal oscillator

$$N_{\max} = \frac{10.8 \text{ MHz}}{0.2 \text{ MHz}} = 54, \quad (10)$$

$$N_{\min} = \frac{0.8 \text{ MHz}}{0.2 \text{ MHz}} = 4. \quad (11)$$

In order to simplify the correspondence between switch settings and counter-preset states, a 1.2-MHz, or “6-count”, positive offset is introduced into the divide-by-“N” counter design so that the range of N is actually 10 to 60, as shown in Table VI. For receiver frequencies between 98.1 MHz and 107.9 MHz, 108 MHz is mixed with the VCO output frequencies to down-convert to the 0.8-to-10.8 MHz range. Thus, the divide-by-“N” counter is “folded” and actually runs through the same count sequence for both of the two ranges of the band as illustrated in Table VI.

Table V. COS/MOS Divide-by-“N” Synthesizer Power Consumption

FUNCTION	OPERATING FREQUENCY	POWER CONSUMPTION – (MILLIWATTS)
÷ N COUNTER	5.93 MHz	49
÷ R COUNTER	1.28 MHz	3
φ COMPARATOR	10 kHz	0.4
CRYSTAL OSCILLATOR	1.28 MHz	2
VCO's AND BUFFER (ESTIMATED)	98 to 108 MHz	25
PRESCALER (ESTIMATED)	98 to 108 MHz	125
		204.4 Total

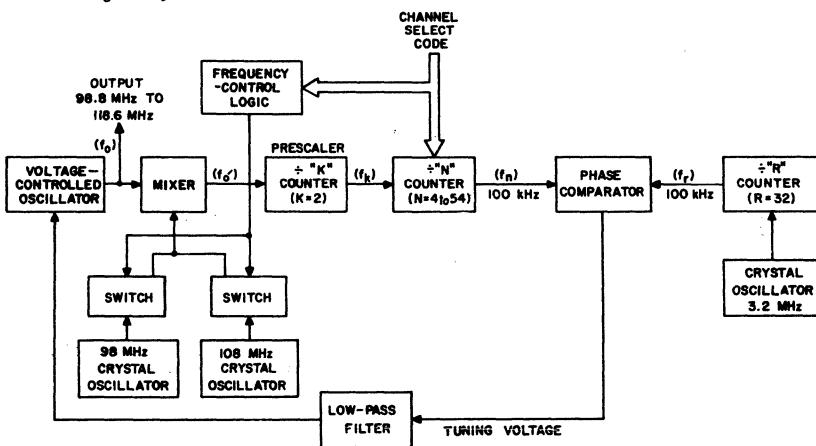


Fig. 22. Heterodyne down-conversion synthesizer

Table VI. Heterodyne Down-Conversion Operation

CHANNEL NO.	RECEIVER FREQUENCY (fm) MHz	LO INJECT FREQUENCY ( $f_o$ ) (fm + 10.7 MHz) MHz	DOWN-CONVERSION FREQUENCY MHz	$f_o'$ (as in Fig. 22) MHz	N COUNT	PRESET FREQUENCY OFFSET ( $f_o' + 1.2$ MHz) MHz	N-COUNT ACTUAL PRESET (N + 6)
1	88.1	98.8	98	.8	4	2	10
50	97.9	108.6	98	10.8	54	12	60
51	98.1	108.8	108	.8	4	2	10
100	107.9	118.6	108	10.8	54	12	60

As Fig. 22 shows, the heterodyne system requires a "2" prescaler. Thus, the phase comparison reference frequency is now given by:

$$f_k = \frac{200 \text{ kHz}}{2} = 100 \text{ kHz}, \quad (12)$$

and, compared to the presealing synthesizer, a 10-to-1 improvement in loop bandwidth becomes apparent.

Since the divide-by-"N" counter now is required to span a count range of 10 to 60, one less decade is required in the logic of the divide-by-"N" counter. Such a divide-by-"N" counter will operate in a fashion similar to the one described earlier in Fig. 6. Power consumption for this counter will be approximately 40 milliwatts at the 5.4-MHz input rate for a V<sub>DD</sub> of 10 volts.

Even though the divide-by-"R" counter consists of only five stages, instead of eight stages as needed for the prescaling system, power consumption again, as in that prescaling system, is concentrated in the first few flip-flops. The divide-by-"R"-counter power dissipation is approximately 9 milliwatts at 3.2 MHz with a V<sub>DD</sub> of 10 volts.

The phase comparator required by the heterodyne system of Fig. 22 operates at 100 kHz as distinguished from the 10 kHz used in the prescaling system. Power consumption is now approximately 30 milliwatts for a sample-and-hold circuit design.

As has been noted, the heterodyne system (Fig. 22) requires a prescaler of "2" operating at up to 10.8 MHz. While a COS/MOS flip-flop can be used at this frequency, lowest power may be achieved by using a discrete flip-flop. Power could be less than 5 milliwatts.

Power consumption for the heterodyne type of FM synthesizer is summarized in Table VII, where total power

consumption is shown to be approximately 146 milliwatts. This is 58 milliwatts less than the 204 milliwatts consumed by the prescaling system.

#### PRESET CHANNEL MEMORY

One of the many advantages of digitally tuning communications sets is the added versatility of control that emerges. For example, the digital channel-select word can be used to drive a digital display showing channel number and frequency. Another scheme often employed is to control the set remotely through a hard-wired serial bit-stream of data or through transmission and reception of a digital word.

An outstanding advantage of using low-voltage COS/MOS to implement digital tuning is the cost effectiveness that permits adding a small preset channel memory to the system using the COS/MOS ultra-low-power memory capability. For example, a 4-word-by-9-bit memory will enable an individual to set up, by push button or rotary switch, four favorite FM stations within a given reception area.

A suitable preset memory scheme is depicted in Fig. 23. When S<sub>1</sub> is closed, the memory is powered from the primary system power source. However, when S<sub>1</sub> is opened and the set turned off, the small 3-volt battery supplies the few microamperes required to hold the memory in a non-volatile condition. Preset channels are written into the memory by setting up the selected channel on the frequency-select switches and switching the R/W switch to Write. The channel-select word is written into one of four words selected by the preset-select switch. By setting the R/W switch to Read and the P/M switch to Preset, the "N" counter is thereby preset to retrieve any one of four selected words. When the P/M switch is in Manual, the frequency-select switches control the divide-by-"N" counter directly.

Table VII. Power Consumption of Heterodyne Synthesizer

FUNCTION	FREQUENCY RANGE MHz	POWER CONSUMPTION - (MILLIWATTS)
÷ "N" COUNTER	0.4 to 5.4	40
÷ "R" COUNTER	1.6	9
CRYSTAL OSCILLATOR	1.6	2
φ COMPARATOR	0.1	30
÷ "K" COUNTER	0.8 to 10.8	5
VCO (ESTIMATED)	98.8 to 118.6	25
MIXER AND OFFSET OSCILLATOR (ESTIMATED)	98 to 118.6	35
		146 Total

Fig. 24 illustrates mechanization of a 4-word-by-9-bit preset channel memory using two COS/MOS CD4039A scratch-pad memories. This memory chip is a 4-word-by-8-bit unit with all of the requisite control inputs as shown in Fig. 23 and described in the paragraph above. The circuit is easily expandable in both word-length and bit-length by direct connections, needing no additional interfacing gates.

In system cost, size and performance, the preset channel memory using the CD4039A is unparalleled. For example, the preset channel memory shown in Fig. 24 will cost under \$10 per chip and will dissipate approximately 0.5 microwatts at a 3-volt holding potential.

Either ordinary flash-light batteries or trickle-charge batteries can be used to provide long periods of maintenance-free operation.

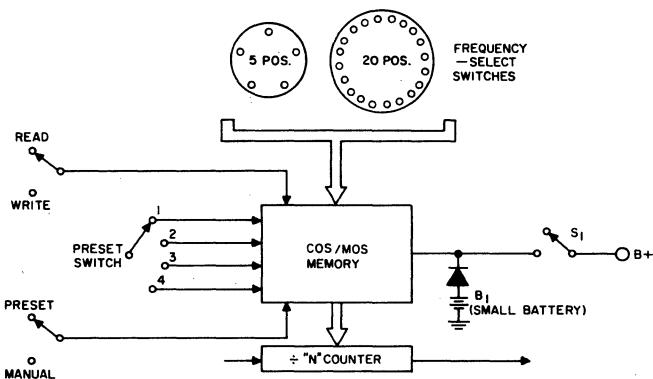


Fig. 23. Digital preset channel-memory concept

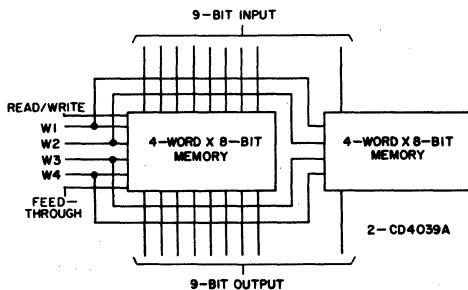


Fig. 24. Preset channel-memory circuit

## **Battery-Powered Digital-Display Clock/Timer and Metering Applications Utilizing the RCA CD4026A and CD4033A Decade Counters-7 Segment Output Types**

by R. Heuner, R. Knapp, J. Litus, Jr. and S. Niemiec

RCA CD4026A and CD4033A consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output to drive each stage of a numerical display. The CD4033A has Ripple Blanking Input and Output (RBI and RBO) and lamp-test capability. The CD4026A has Display Enable capability. Both types are derived from the same basic layout but use different metallization patterns. Both types are particularly advantageous for display applications in which low power dissipation and/or low package count are important.

This Note describes the CD4033A and CD4026A and their use with various 7-segment display units presently available. Interface packages and methods are discussed to help the designer select the best system to meet his needs. Also included are battery-operated systems for digital clocks and watches.

### **CIRCUIT OPERATION AND PERFORMANCE CHARACTERISTICS**

The inputs to the CD4033A IC are "Clock", "Reset", "Clock Enable", "Ripple Blanking Input" (RBI), and "Lamp Test" as shown in Fig. 1. The outputs are "Carry Out", "Ripple Blanking Output" (RBO), and the seven decoded outputs (a,b,c,d,e,f,g). A "high" reset signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the Clock Enable signal is "low". Counter advancement by way of the clock line is inhibited when the Clock Enable signal is "high". A timing diagram for the CD4033A is shown in Fig. 2. Antilock gating is provided on the Johnson counter to assure proper counting sequence.

The Carry-Out (Cout) signal completes one cycle every ten clock input cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven

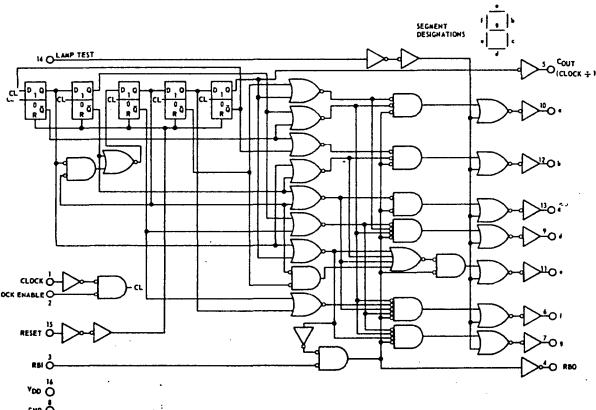


Fig. 1— Logic diagram of CD4033A — decade counter/divider with decoded 7-segment display outputs.

decoded outputs (a,b,c,d,e,f,g) illuminate the proper segments in a 7-segment display device used to present the decimal number 0 to 9. The 7-segment outputs go "high" on selection.

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number. This feature results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight-digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by the connection of the RBI terminal of the CD4033A associated with the most significant digit in the display to a "low-level" voltage and the connection of the RBO terminal of the same stage to the RBI terminal of the CD4033A in the next-lower-significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

On the fraction side of the display, the RBI of the CD4033A associated with the least significant bit is connected to a "low-level" voltage and the RBO of the same CD4033A is connected to the RBI terminal of the CD4033A in the next more significant-bit position. This procedure is continued for all CD4033A on the fraction side of the display.

In a purely fractional number (e.g. 0.7346) the zero immediately preceding the decimal point can be displayed by the connection of the RBI of that stage to a "high-level" voltage (instead of to the RBO of the next more significant stage). Similarly, the zero in a number such as 763.0 can be displayed by the connection of the RBI of the CD4033A associated with it to a "high-level" voltage. Ripple blanking of non-significant zeros provides an appreciable savings of display power.

The CD4033A has a "Lamp Test" input which, when connected to a "high-level" voltage, overrides normal

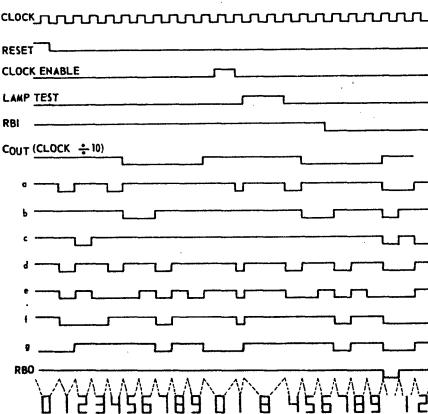


Fig. 2— CD4033A — timing diagram.

decoder operation and enables a check to be made of possible display malfunctions by putting the 7 outputs in the "high" state.

Figs. 3a, 3b, and 3c define the current capability of the 7-segment outputs when selected for supply voltages of 3.5V, 5V, 10V and 15V. Table I shows the maximum ratings and some features of the CD4033A. (Additional information is given in the RCA data bulletin for the CD4033A, File No. 503.)

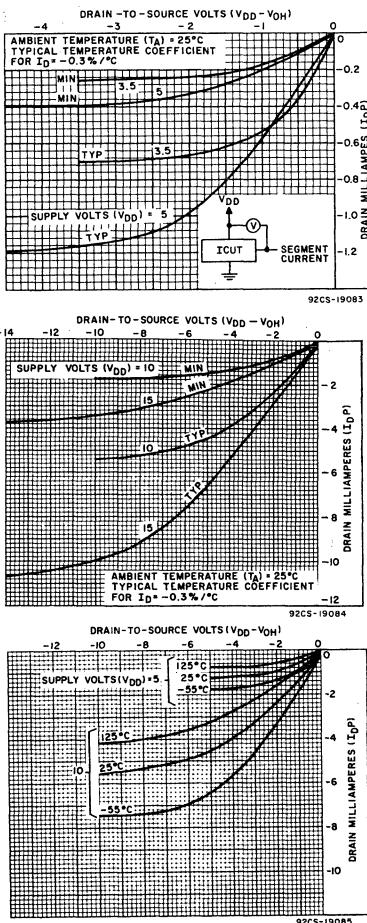


Fig. 3— a) Output current capability of CD4033A,  $V_{DD} = 3.5$  and 5V; b) Output current capability of CD4033A,  $V_{DD} = 10, 15V$ ; c) Output current capability,  $V_{DD} = 5, 10$  V,  $T = -55^\circ C, +25^\circ C, +125^\circ C$ .

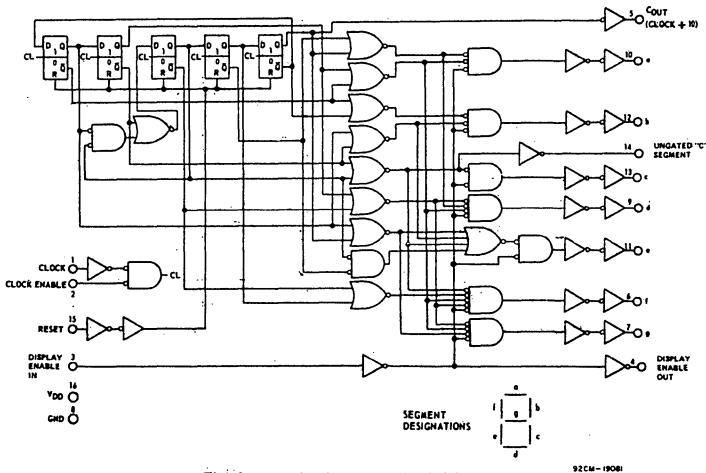


Fig. 4— Logic diagram of CD4026A

Fig. 4 shows the logic diagram of the RCA CD4026A. The CD4026A is identical to the CD4033A except that the Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) and lamp test capabilities have been replaced by a "Display Enable" control. An extra "C" segment output (not gated with the Display Enable) is available to retain the ability to implement the divide-by-12 function. The power dissipation and output characteristics of the CD4026A and CD4033A are identical.

#### DISPLAY-DRIVER CIRCUIT TYPES FOR USE WITH THE CD4033A AND CD4026A

##### CD4009A/CD4010A — COS/MOS Hex Buffer/Logic Level Converters Inverting/Non-inverting

Figs. 5 and 6 show the circuit diagrams for the CD4009A (Inverting Hex Buffer) and CD4010A (Non-Inverting Hex Buffer), respectively. Six buffers are provided per package. Figs. 7 and 8 show  $V_O$  "0" output characteristics (n-channel) and  $V_O$  "1" output characteristics (combined p-and-n-channel devices) for both types.

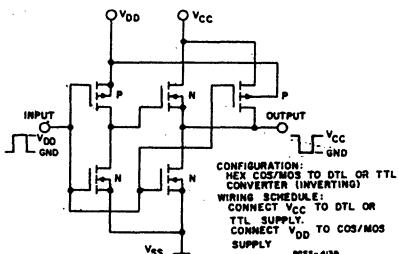


Fig. 5— a) Schematic diagram (1 of 6 identical stages) of CD4009A.

Table I — Maximum Ratings and Features

#### MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES

DC Supply Voltage ( $V_{DD} - V_{SS}$ )	3 to 15 V
Operating Temperature Range (Ceramic & TO-5) (Plastic)	-55°C to +125°C -40°C to +85°C
Storage Temperature Range	-65°C to +150°C
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$
Features:	
Noise Immunity	45% of $V_{DD}$ (Typical Value)
Clock Pulse Frequency	5 MHz @ $V_{DD} = 10$ V (Typical Value)

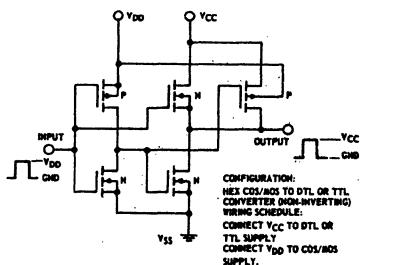


Fig. 6— a) Schematic diagram (1 of 6 identical stages) of CD4010A.

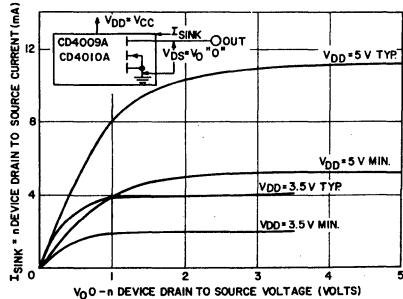
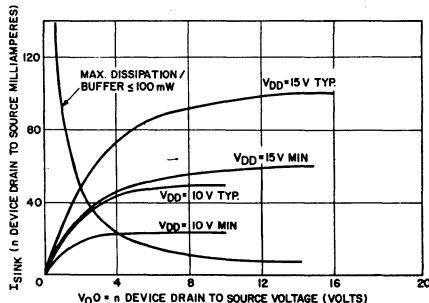


Fig. 7— a) CD4009A and CD4010A  $V_O$  "O" output drive capability,  $V_{DD} = V_{CC} = 3.5, 5$ ; b) CD4009A and



CD4010A  $V_O$  "O" output drive capability,  $V_{DD} = V_{CC} = 10, 15$ .

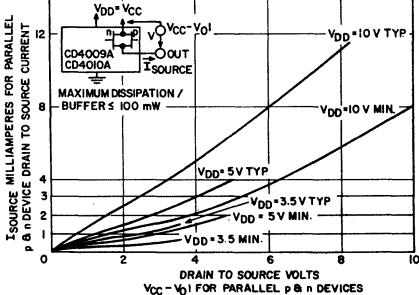
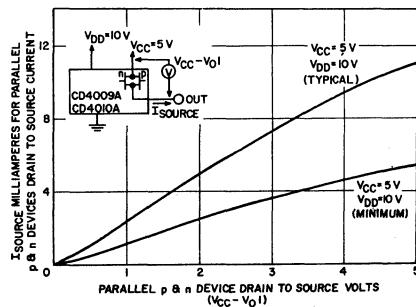


Fig. 8— a) CD4009A & CD4010A  $V_{CC} - V_O$  "1" output drive capability,  $V_{DD} = V_{CC} = 10, 5$ , and  $3.5$  V; b)



CD4009A & CD4010A  $V_{CC} - V_O$  "1" output drive capability,  $V_{DD} = 10$  V and  $V_{CC} = 5$  V.

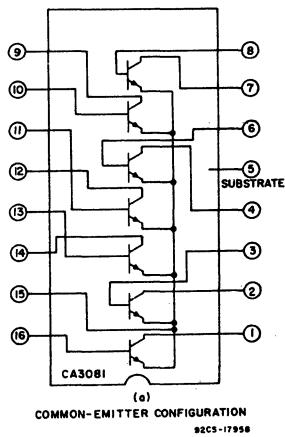
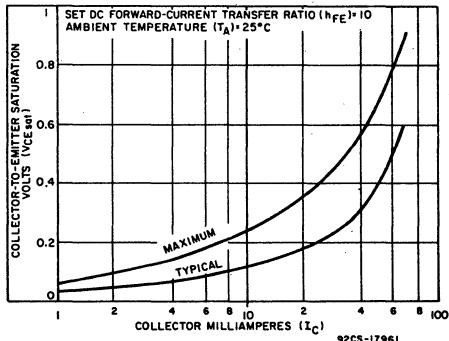


Fig. 9— a) Functional diagram of CA3081; b)  $V_{CE(sat)}$  as a function of  $I_C$  at  $T_A = 25^\circ C$ .



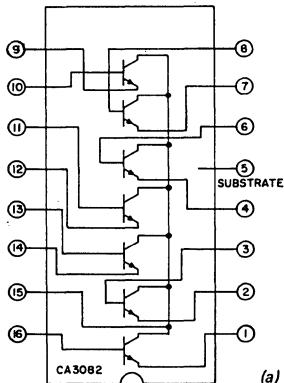
**CA3081 and CA3082 – General-Purpose High-Current n-p-n Transistor Arrays.**

Fig. 9a shows the schematic diagram of the CA3081 (common emitter array). Fig. 9b shows  $V_{CE(sat)}$  as a function of  $I_C$  for one of 7 identical transistors (See Ref. 1 for additional information.)

Fig. 10a shows the schematic diagram of CA3082 (common collector array). Fig. 10b shows  $h_{FE}$  as a function of  $I_C$  at  $V_{CE} = 3$  V.

**INTERFACING THE CD4033A AND CD4026A WITH POPULAR 7-SEGMENT DISPLAY TYPES**
**Light Emitting Diodes**

The MAN 3 (Monsanto or equivalent) is a low power monolithic, 7-segment diffused planar GaAsP "Light Emitting Diode" display. Figs. 11a and 11b show the equivalent schematic and physical dimensions of the MAN 3. Fig. 11c shows brightness as a function of forward current. A fairly bright display (200 foot lamberts) is achieved at a



COMMON-COLLECTOR CONFIGURATION  
92CS-17957

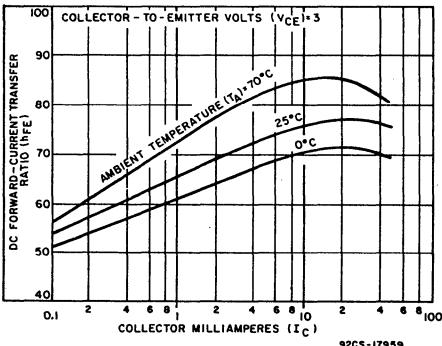
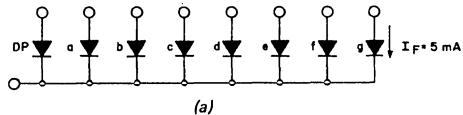


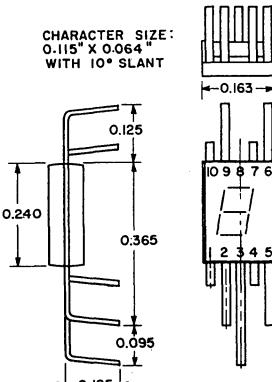
Fig. 10-b) Functional diagram of CA3082; b)  $h_{FE}$  as a function of  $I_C$ .

typical power dissipation of 8.5 milliwatts (1.7 V x 5 mA) per segment for a 100%-duty-cycle drive mode. Greater display intensities can be realized by the utilization of

$V_F = 1.7 \text{ V (TYP)} \text{ TO } 2.0 \text{ V (MAX)}$ ;  $T_A = 25^\circ\text{C}$ ;  $I_F = 5 \text{ mA}$   
 $\Delta V_F = 2 \text{ mV/}^\circ\text{C}$ ;  $I_F \text{ MAX / SEGMENT} = 10 \text{ mA CONTINUOUS}$ ,  
TEMPERATURE RANGE:  $-55^\circ\text{C} < T < 85^\circ\text{C}$



CHARACTER SIZE:  
0.115" X 0.064"  
WITH 10° SLANT



NOTE: FOR ADDITIONAL INFORMATION  
SEE MONSANTO'S PUBLISHED  
DATA ESP 35 DATED 2/70

(b)

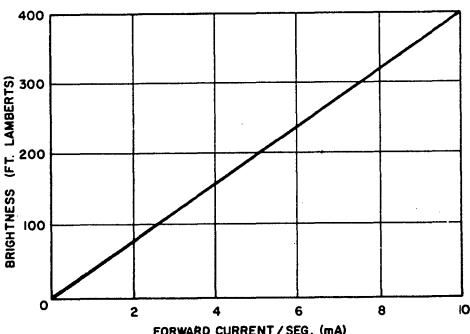


Fig. 11-c) MAN-3 schematic diagram; b) Package physical dimensions; c) brightness as a function of forward current.

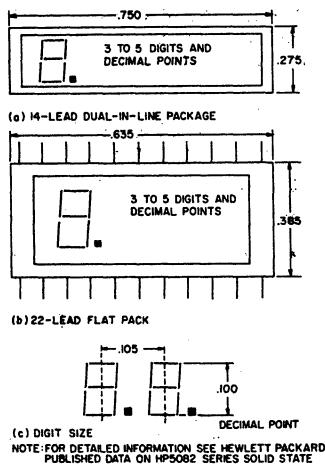


Fig. 12—Package physical dimensions for HP5082.

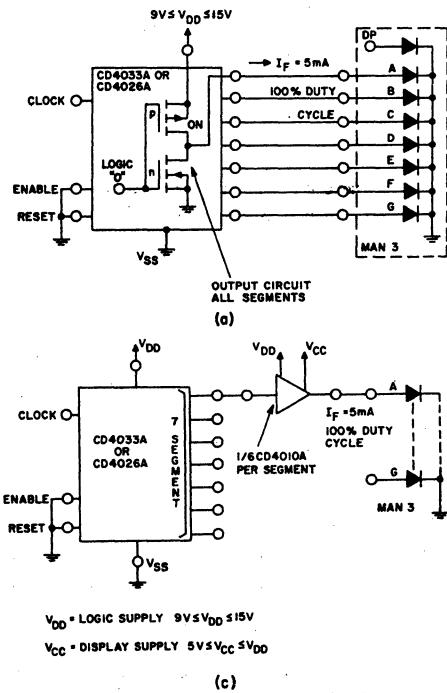
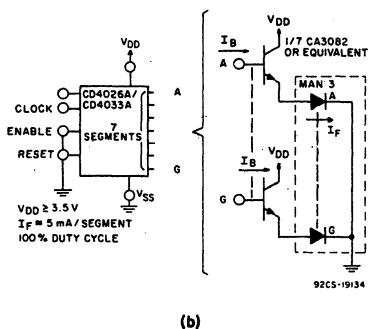


Fig. 13—CD4033A (or CD4026A) being interfaced with MAN-3 at various supply voltages as shown.

higher-forward-current drives for less than 100% duty cycle (i.e., Light Enhancement Factor equals dc current divided by pulsed current  $I_F(AV)$ ) and is greater than unity, where both dc and pulsed current result in similar light intensity as seen by the human eye).

The requirement of lowest power at greatest light intensity makes it desirable to multiplex the display current between characters of a display, as well as between segments of a character. Display wiring may also be simplified by such multiplexing methods. Displays similar to MAN 3 characteristics, but containing multiple 7-segment display elements are available from Hewlett Packard and others. For example, Fig. 12 shows the approximate physical dimensions for the HP 5082 Series of LED's. The characteristics are similar to those of the MAN 3.

Fig. 13 shows techniques for the interface of the CD4033A or CD4026A to the MAN 3 display at various supply voltage conditions. Fig. 13a shows a direct drive condition at 100% duty cycle for  $V_{DD}$  between 9 and 15 V. A typical CD4033A can supply a forward current of 5 mA per segment with a supply voltage as low as 9 V and yields a fairly bright display. The power supply dissipation is approximately 45 mW per segment (9 V x 5 mA).



For lower system power dissipation and separate logic and display supply sources, the RCA CD4010A COS/MOS Hex Buffer package can be utilized, as shown in Fig. 13b. In this case, the power supply dissipation per segment is less than 25 mW ( $5\text{ V} \times 5\text{ mA}$ ).

For supply voltages as low as 3.5 V, an n-p-n transistor array interface circuit is required as shown in Fig. 13c. External base or emitter resistors may be used to obtain finer control of forward current, depending on the n-p-n array selected. For supply voltages less than 3.5 V, both the CD4009A and a p-n-p transistor array interface-circuit are required as shown in Fig. 13d.

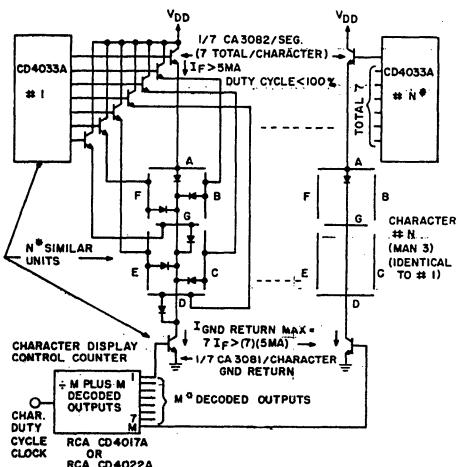
Fig. 14a illustrates a method for character-drive-multiplexing using the CD4033A. Character multiplexing and the use of higher forward-segment currents at less than 100% duty cycle permit light enhancement factors greater than 1 to be realized. This mode of operation (compared with the 100% duty cycle mode, for the same display brightness) permits savings in display power dissipation. Fig. 14b shows a similar character multiplexing arrangement using the CD4026A. The multiplexing is accomplished at the logic level, as opposed to switching the Display character ground currents. A Character Display Driver Multiplexing circuit to interface the CD4026A with the HPSQ82 series Multiple Character Display is shown in Fig. 14c. A remetalization (not shown), of the CD4033A could be used to eliminate the

"N" channel device of all segment outputs. This permits direct connection of respective segments of all characters to the base of one common set of CA3082 segment drivers. A common set of segment ground return resistors would be required at the base of each CA3082.

The MAN 1 is a 7-segment diffused planar GaAsP "Light Emitting Diode" display. Figs. 15a and 15b show the equivalent schematic and physical dimension-diagrams of the MAN 1. Fig. 15c shows the brightness as a function of forward current characteristics. Good brightness (275 foot Lamberts) is obtained at a forward current of 16 mA, for a 100% duty cycle drive mode.

Figs. 16a and 16b show the CD4033A or CD4026A being interfaced with the MAN 1 display at various supply voltages. The CD4009A (shown in Fig. 16a) is able to sink 16 mA or more at "0" output voltage up to 2 V, with a supply voltage ( $V_{DD}$ ) as low as 7 V. This feature permits a drop of 4 V or more across the MAN 1 diodes. When the CD4009A is used in this application care should be taken not to exceed its maximum power ratings (100 mW/per buffer stage; 200 mW per package).

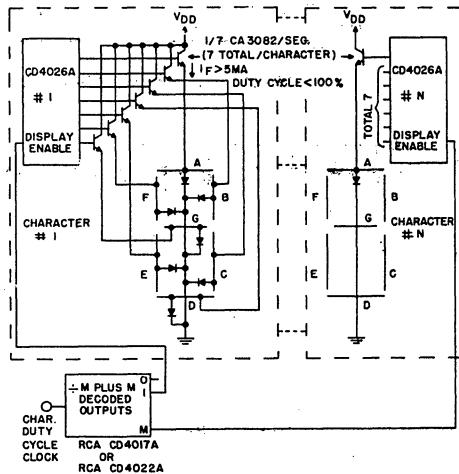
The CD4033A (shown in Fig. 16b) provides a minimum base current of 0.4 mA into the CA3081 at a supply voltage of  $V_{DD} = 5.0\text{ V}$ , for a forward current in excess of 12 mA. The forward voltage of the MAN 1 (4.0 V) limits the minimum  $V_{DD}$  to approximately 5.0 V.



\* N IS THE NUMBER OF CHARACTERS IN THE DISPLAY.

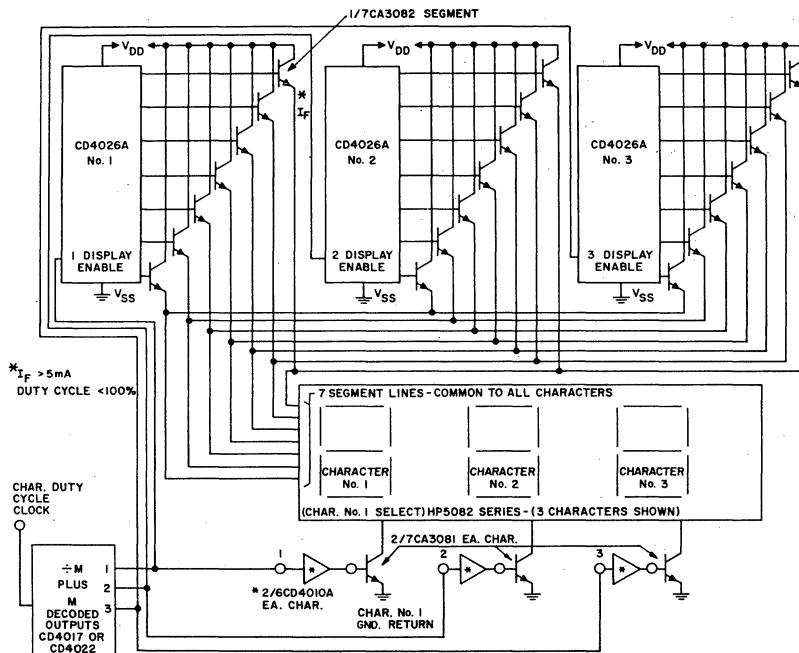
M IS THE NUMBER OF CHARACTER DISPLAY CONTROL COUNTER DECODED OUTPUTS. THE DISPLAY CONTROL COUNTER CLOCK AND THE VALUE OF M DETERMINES THE DISPLAY DUTY CYCLE OF THE CHARACTERS.

(a)

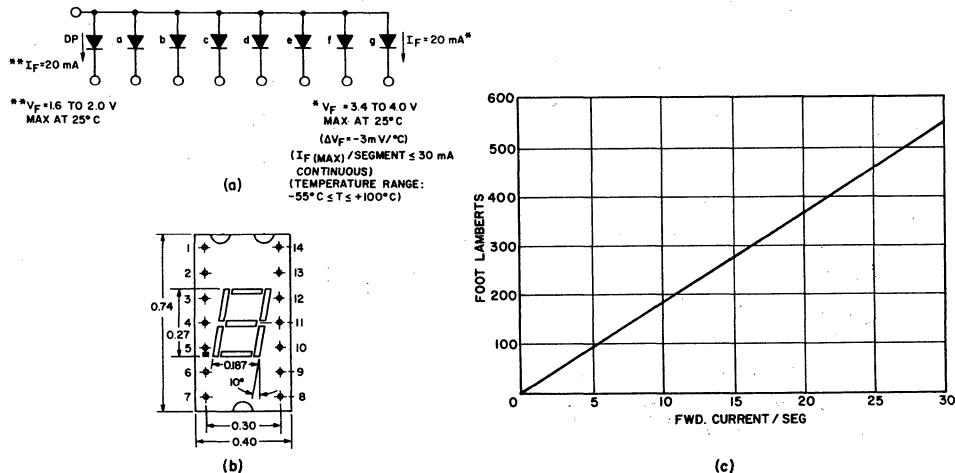


(b)

Fig. 14— a) Character display drive multiplexing using the CD4033A and the MAN-3; b) character display drive multiplexing using the CD4026A and the MAN-3.



*Fig. 14—c) Character display drive multiplexing using the CD4026A and the HP5082 Series.*



**Fig. 15—** a) MAN-1 schematic diagram; b) package dimensions; c) brightness as a function of forward current.

### INCANDESCENT READOUTS

The Pinlite\* Series "O" and "R" devices are low-power, miniaturized, incandescent readouts. Fig. 17 summarizes the voltage-current requirements, brightness (foot-lamberts), and physical dimensions of these display devices. Figs. 18a & 18b show the CD4033A being interfaced with Pinlite devices.

Fig. 19a shows the physical dimensions of the RCA's NUMITRON Devices, DR2000 and DR2100 series. Brightness and segment current as a function of segment voltage are plotted in Figs. 19b and 19c. Typical brightness is 7000 ft. lamberts, at a segment voltage of 4.5 V and a current of 24 mA.

Fig. 20a and 20b show the CD4033A or CD4026A being interfaced with RCA NUMITRON Devices DR2000 Series

\*Trademark of Pinlite, Inc.

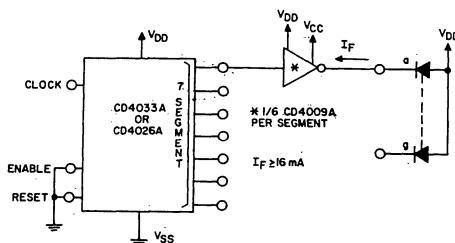


Fig. 16-a) CD4033A (or CD4026A) driving the MAN-1 at  $7V \leq V_{DD} \leq 15V$ ,  $V_{DD} = V_{CC}$ ; b) CD4033A (or CD4026A) driving MAN-1 at  $V_{DD} \geq 5V$ .

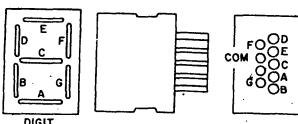
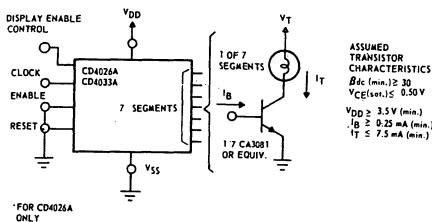


Fig. 17—Pinlite, Inc. series "O" and "R" 7-segment display

CURRENT, BRIGHTNESS, AND PHYSICAL DIMENSIONS								
"O" SERIES	Model	Character Height	Dimensional			Volt	mA per Segment	Brightness Ft.-1 mbt.
			H Height	W Width	D Depth			
	03-15	3/16"	0.305	0.225	0.312	1.5	8	120
	04-30	1/4"	0.375	0.275	0.312	3.0	8	300
	06-30	5/16"	0.455	0.305	0.312	3.0	8	250
	R3-20	3/16"	0.305	0.225	0.312	2.0	4.3	100
	4R-30	1/4"	0.375	0.275	0.312	3.0	4.3	100

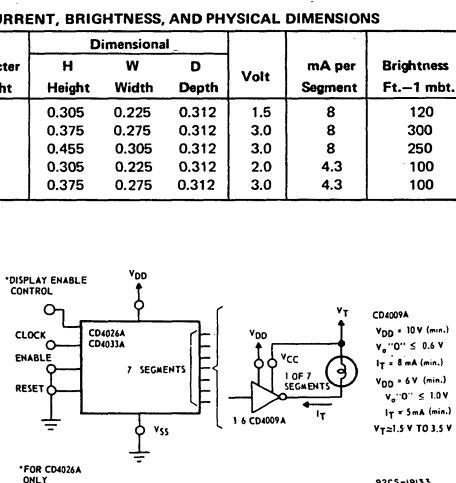
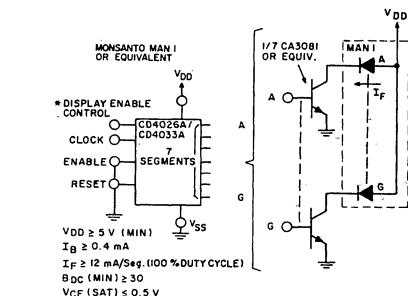


displays. In Fig. 20a, if  $V_{DD}$  is less than 8.0 v, a CD4010A buffer must be used between the CD4033A or CD4026A segments and the CA3081. For Fig. 20b, care should be taken not to exceed the maximum power dissipation of the CD4009A (100 mW per buffer unit, 200 mW per package).

### LOW VOLTAGE VACUUM FLUORESCENT READOUTS

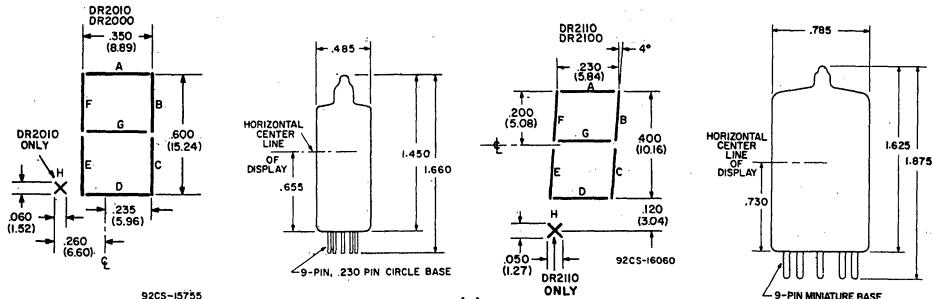
The TungSol Digivac S/G\*\* Type DT1704B or DT1705D, Nippon Electric (NEC)-Type DG12E/LD915 and Sylvania Type 8894 are low voltage and low power Vacuum Fluorescent 7-Segment Readouts. Figs. 21a and 21b show the physical dimensions and brightness characteristics of the

\*\*Trademark of Tung-Sol Division Wagner Electric Corp.

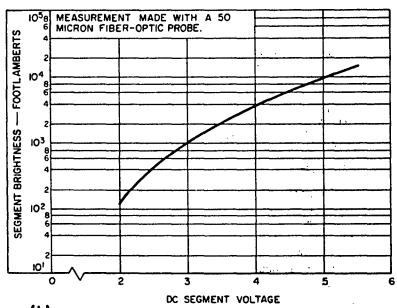


92CS-19133

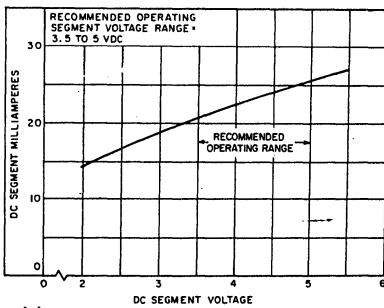
Fig. 18—Interfacing CD4033A (or CD4026A) with Pinlite series "O" and "R" 7-segment displays.



(a)



(b)



(c)

Fig. 19—a) Package physical dimensions for RCA's NUMITRON devices, series DR2000 and DR2100; b) brightness as a function of segment voltage; c) segment current as a function of segment voltage.

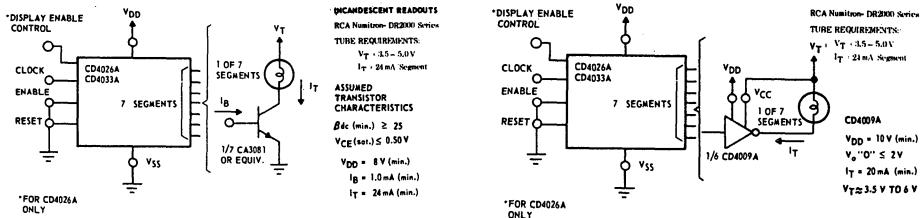
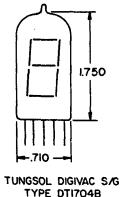


Fig. 20—CD4033A (or CD4026A) driving RCA's NUMITRON DR2000 Series.



(a)

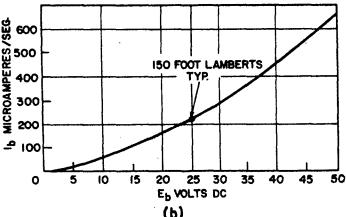


Fig. 21—a) Tung-Sol S/G type DT1704B & DT1705D physical dimensions; b) plate current as a function of plate voltage.

TungSol Digivac DT1704B & DT1705D. A brightness level of 150 foot lamberts (typical) is indicated at a plate voltage of 25 V. Fig. 22 illustrates a method of driving these devices with the CD4033A. The requirements are 100 to 300 $\mu$ A per segment at tube voltages of 12 to 25 V depending on the required brightness level. The filaments require 45 mA at 1.6 V, (ac or dc). With a  $V_{ON} = 18$  V, medium brightness in low ambient light background, will result. The point of no noticeable glow is  $V_{OFF} = 4.5$  V.

#### DIGITAL TIMER/CLOCK/WATCH APPLICATIONS

The decoded 7-segment outputs of the CD4033A can be utilized to control its counting function. Table II shows the truth table for the CD4033A segment and carry out signals. Figs. 23a to 23h show the logic configurations for counting from 2 through 9 using the CD4033A signal for count control. The CD4026A can be utilized in a similar manner.

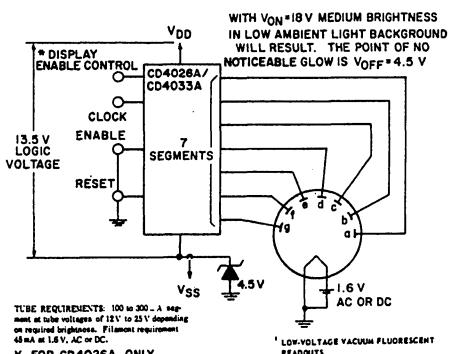


Fig. 22—Interfacing CD4033A (or CD4026A) with Tung-Sol S/G type DT1704B or DT1705D.

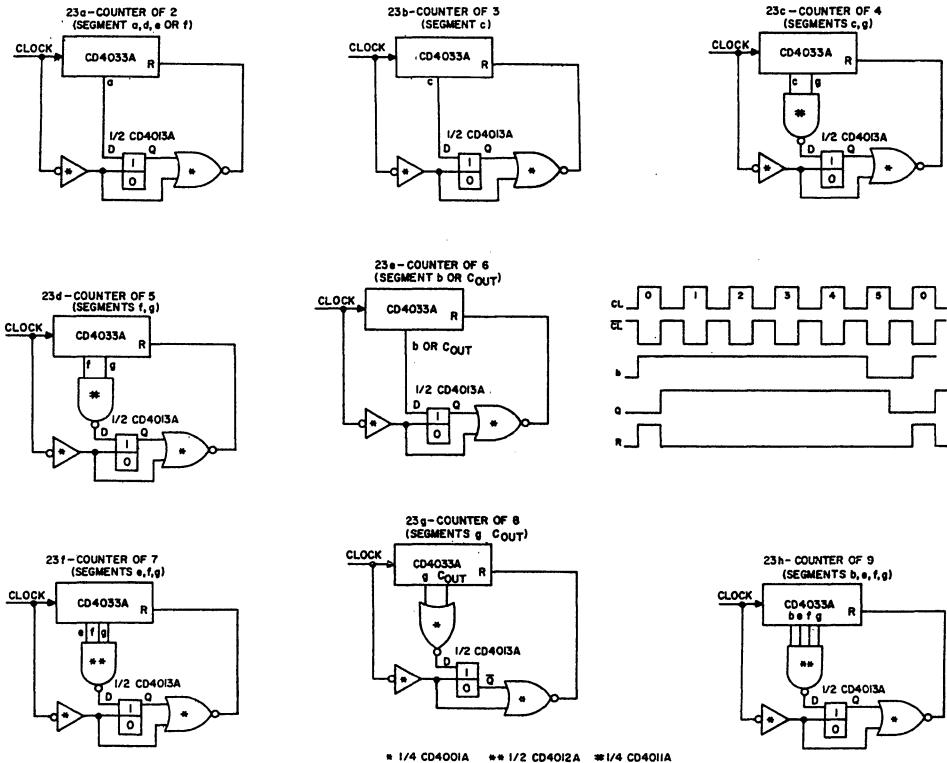


Fig. 23—Logic configurations to control counting functions of CD4033A.

### Digital Display Clock/Watch Configuration (Divide-by-60, Divide-by-60, Divide-by-12)

Fig. 24 shows the logic diagram of a divide-by-60, divide-by-60, divide-by-12 digital-display counting circuit. The input clock-signal rate is 1 Hz. The two 60 counters cycle synchronously from 0 to 59, while the 12 counter cycles from 1 to 12.

Figs. 25a and 25b show pertinent waveforms of the divide-by-60 and divide-by-12 sections, respectively. Minutes and hours updating switches (second rate) as well as the seconds, minutes and hours reset switches are provided. A 24-hour counter can be easily substituted for the 12 hour counter.

With reference to Figs. 24 and 25a, the CD4033A-II "b" segment goes low at the 59th clock pulse input. At the 60th clock pulse input, the CD4033A-I goes from a "0" to a "0" and the CD4013A-I is clocked to a "0" state, which in turn resets CD4033A-II from a "5" to a "0". A reset condition has been realized after 60 clock input pulses. The CD4013A-I is then set at the 5th clock input pulse in preparation for the next cycle.

With reference to Figs. 24 and 25b, the "c" segment goes low at the 12th clock input pulse. The CD4013A-III's Q output is low from the 10th clock input pulse. At the 13th clock input pulse CD4013A-IV is clocked to the "1" state

Table II – Truth Table – 7 Segment and Carry Out Signals

COUNTER OF:	1	2	3	4	5	6	7	8	9	10
COUNT	0	1	2	3	4	5	6	7	8	9
DECODED OUTPUT										
a	1	0	1	1	0	1	1	1	1	1
b	1	1	1	1	1	0	0	1	1	1
c	1	1	0	1	1	1	1	1	1	1
d	1	0	1	1	0	1	1	0	1	1
e	1	0	1	0	0	0	1	0	1	0
f	1	0	1	0	1	1	1	0	1	1
g	0	0	0	1	1	1	1	0	1	1
C <sub>OUT</sub>	1	1	1	1	1	0	0	0	0	0

which in turn resets CD4013A-V and VI. The CD4013A-V and VI combination then generates a one second wide reset pulse to the CD4033A-V and CD4013A-III reset inputs, as well as a two second wide pulse to the clock enable input of the CD4033A-V to advance it to the "1" count. The reset and advance to one operation may be clocked at a rate much faster than the seconds clock.

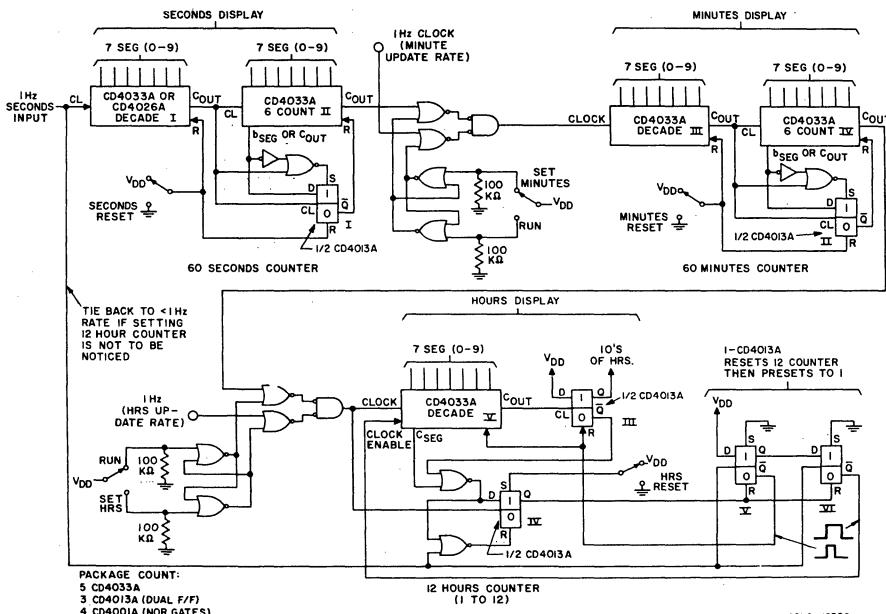


Fig. 24 – Divide-by-60, divide-by-60, divide-by-12 digital display counting circuit.

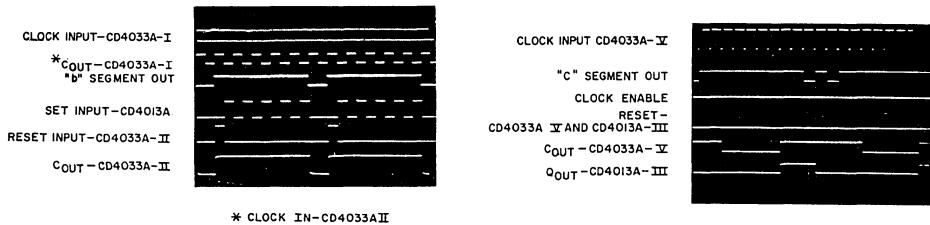


Fig. 25—*a)* Divide-by-60 voltage waveforms; *b)* divide-by-12 voltage waveforms.

The CD4026A may be utilized in place of the CD4033A, if "Display Blanking" is desirable to effect power savings. For this case the divide-by-12 function utilizes the ungated "C" output for counter gating.

#### Battery Powered Digital Clock Prototype

##### Using the MAN 3-LED Displays

Fig. 26 shows the photographs and logic diagram of a complete battery powered digital clock prototype, utilizing MAN 3-LED display devices. A 9-V battery is utilized to drive all of the logic circuitry. Power drain on the 9-V battery is approximately 7 mA continuous, (over 90% of which is consumed in the 262 kHz crystal oscillator configuration). Other oscillator configurations and lower crystal frequencies enable very significant reductions of this current drain. To conserve power, the MAN 3 display devices are powered by two series 1.5 volt batteries. The CD4010A's permit translation from the 9-V logic level to the lower voltage, higher current 3-V display drive levels. While the display is activated, a maximum of approximately 120 mA of display current is required.

Although not utilized in the prototype shown, the character display multiplexing methods of Figs. 14a, b or c may be utilized for greater light enhancement and/or lower power dissipation.

#### Battery Powered Digital Clock Prototype Utilizing TungSol Digivac S/G DT1704B's Displays

Fig. 27 shows the logic diagram and a photograph of a complete battery powered digital clock prototype utilizing TungSol Digivac display devices. As noted in the discussion of low-voltage vacuum fluorescent readouts, medium brightness levels are obtained under low to medium ambient light conditions. A larger display is achieved by use of the Digivac units than with the MAN 3 units. The logic is powered by two series 9-V cells at  $V_{DD}$  with a 4.5-V zener offset of  $V_{SS}$  (the logic sees 18 V - 4.5 V = 13.5V.) The logic circuit drives the 150- $\mu$ A segment plate currents of the Digivacs directly. The filament power for the Digivacs is supplied by two parallel 1.5-V batteries. Filament power is off until a display is required.

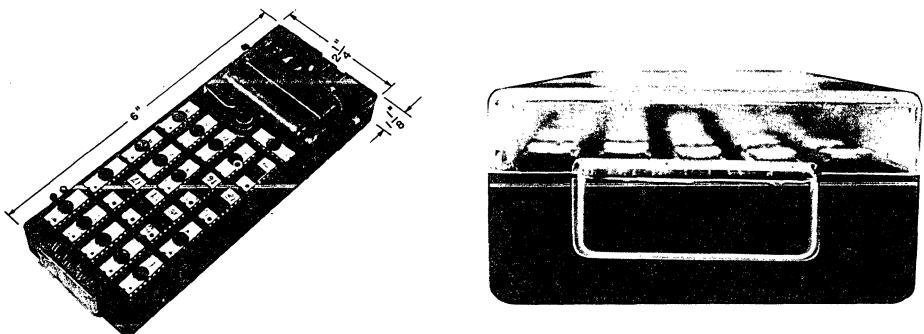


Fig. 26—*a)* Photograph of battery-powered L.E.D. digital clock.

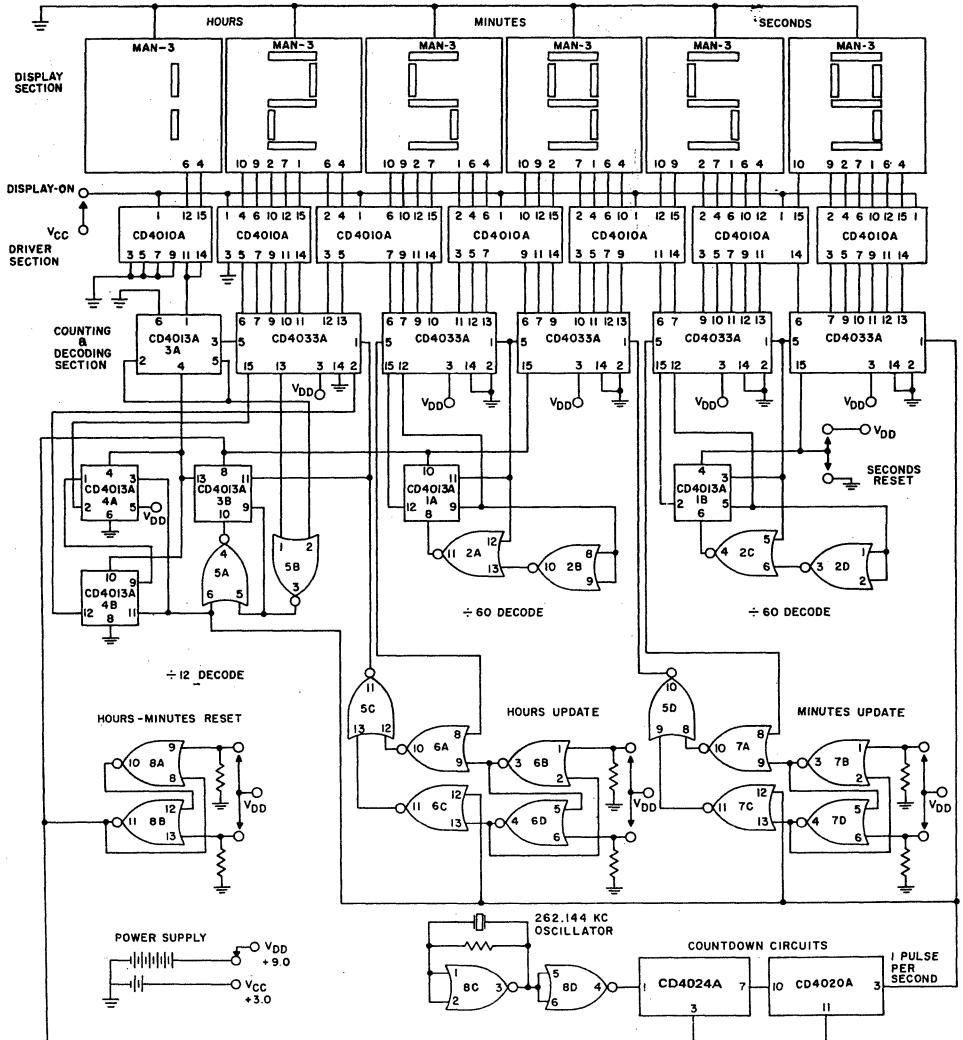


Fig. 26-b) Logic/Wiring Diagram

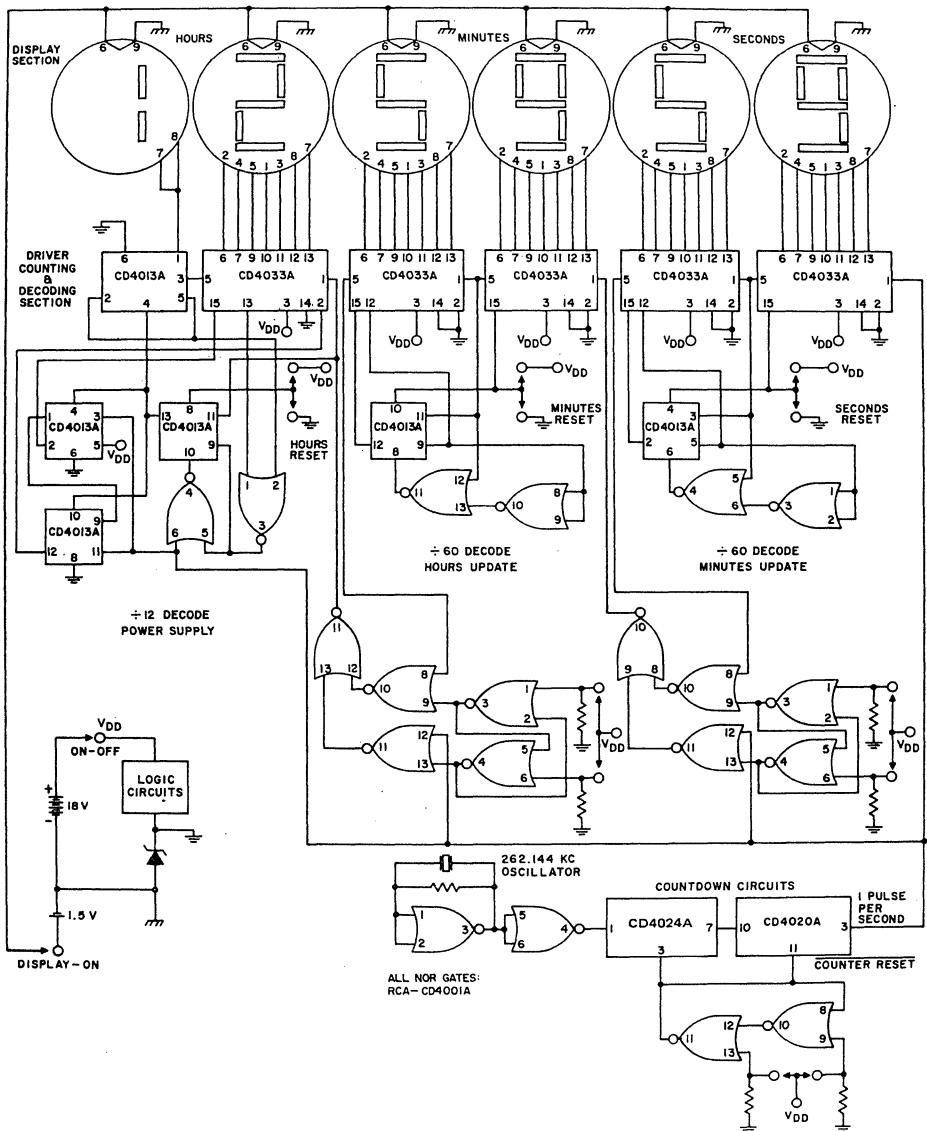


Fig. 27- a) Logic/Wiring Diagram.

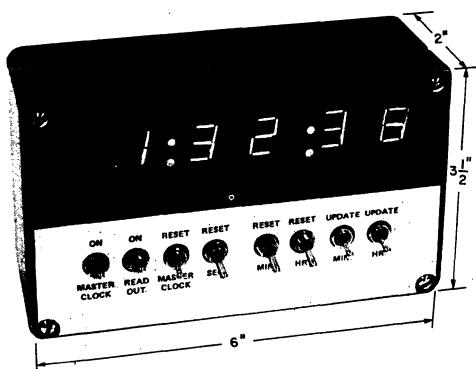


Fig. 27-b) Photograph of Clock.

#### OTHER DIGITAL CLOCK APPLICATIONS

Plug In Industrial Digital Wall Clocks — 100 V Powered Clock. If primary 110-V power fails a rechargeable battery maintains current to the counters and the clock continues to operate. The displays go off until the 110-V power is restored. When the 110-V power is restored the display comes on; the clock continues to keep correct time; and no resetting is required. A "display on demand" feature with loss of the 110-V power can also be included.

Commercial Digital Clock (110-V Powered Clock). The regulation requirements are from 3.5 V to 15 V.

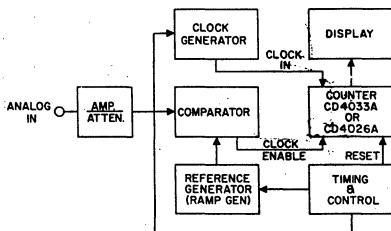


Fig. 28—Block diagram dc metering using CD4033A or CD4026A.

Portable Elapsed Time Meter a digital watch, and a down-time clock are other applications which can be achieved through the use of the CD4033A or CD4026A.

#### DIGITAL METER APPLICATIONS

The CD4033A and CD4026A are unique in that they have both counting and decoding on a single chip. The block diagram of Fig. 28 demonstrates the use of the CD4033A and CD4026A in digital meter applications where time multiplexing or sampling-and-display functions are utilized (to eliminate the need for holding circuits). An analog input is converted to a sequence of pulses where the pulse count is proportional to the analog input level. Sampling rates may be fast enough to result in an apparent fixed display, or they may be slower and cause noticeable changes in display during sampling. Longer display times or display blanking during sampling may be used to prevent flicker.

#### Timers/Frequency-Delay-Phase Meters

Fig. 29 shows a general block diagram using the CD4033A or CD4026A in Digital Counter/Timers. As in the dc meter applications, time multiplexing of sampling and display functions is utilized.

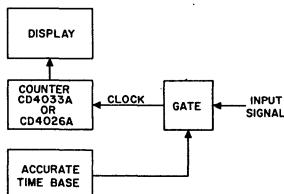


Fig. 29—Block diagram using CD4033A or CD4026A in Digital-Counter/Timers.

#### REFERENCES

1. RCA data bulletin for CA3081, CA3082 File No. 480
2. RCA data bulletin for CD4033A and CD4026A File No. 503

## COS/MOS Rate Multipliers—Versatile Circuits for Synthesizing Digital Functions

by G. J. Summers

The RCA COS/MOS rate multipliers, CD4527B and CD4089B, are versatile MSI circuits that can be used as building blocks to generate a range of digital functions in low-power systems where minimum package count is desirable. Rate multipliers can be used in various applications, such as numerical control, instrumentation, digital filtering, and frequency synthesis. When used with an up/down counter and control logic, they can be used to perform such operations as multiplication, addition, subtraction, generation of algebraic equations and differential equations, integration, and to raise numbers to various powers. This Note discusses each of these applications and symmetric rate multiplication, the problem of eliminating round-off error in a direct frequency-synthesis application in a common-carrier multiplex system.

### Rate-Multiplier Description

The rate multiplier is a circuit that produces an output pulse train whose frequency is proportional to the product of two inputs. One of the inputs is a clock frequency,  $f_c$ , and the other a pre-programmed multiplier number (binary or BCD) whose value is fixed at a given instant. The output of the rate multiplier is a frequency whose average rate is equal to  $f_{cx}$ , where  $0 < x \leq 1$ . Thus the output rate is always less than or equal to  $f_c$ , and, in general, is composed of pulses which are unevenly spaced. It should be noted that even though the output rate is time averaged to the correct fractional rate of the input, there is always a round-off error associated with the output. This error can be reduced by increasing the bit capacity of the multiplier.

The principle of rate multiplication may be illustrated with the aid of the simplified circuit of a binary rate multiplier shown in Fig. 1(a). Four bits of binary information are used to perform multiplication by any factor from 1/16 to 15/16 by programming the  $S_8$ ,  $S_4$ ,  $S_2$ , or  $S_1$  gates for the proper factor. The final output frequency,  $f_x$ , is obtained by ORing the outputs of each AND gate as shown in the figure. The timing diagram in Fig. 1(b) shows how a value for  $f_x = \left(\frac{S_4 + S_2}{16}\right) f_c$  can be obtained by gating the  $S_4$  and  $S_2$  outputs.

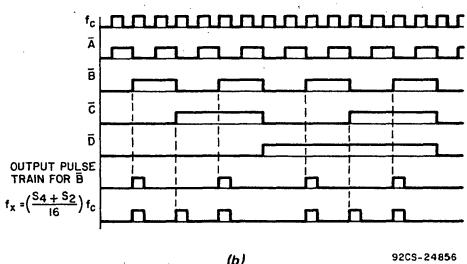
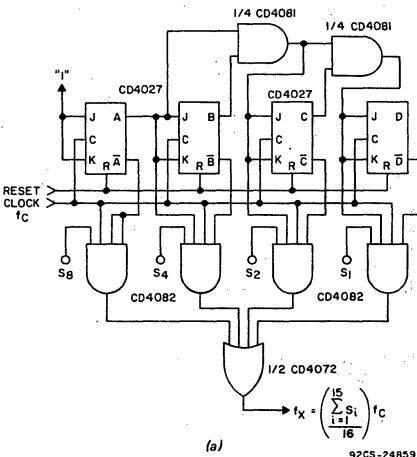


Fig. 1—(a) Simplified circuit of binary rate multiplier; (b) timing diagram for (a).

The functional diagram of the CD4527B (BCD rate multiplier) is shown in Fig. 2. The BCD inputs can be programmed from 1 to 9 to form an output multiplier constant of 1/10 to 9/10. For example, if the BCD input were set to seven (0111), the output rate would be  $f_c(7/10)$ . This multiplication factor can be expanded to a greater number of bits by using the cascade/enable feature of the CD4527B as demonstrated in Fig. 3. The strobe feature

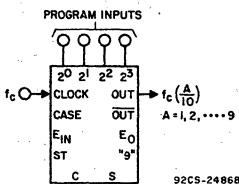


Fig. 2—Functional diagram of the CD4527B, BCD rate multiplier.

programmed from 1 to 9 to form an output multiplier constant of 1/10 to 9/10. For example, if the BCD input were set to seven (0111), the output rate would be  $f_c(7/10)$ . This multiplication factor can be expanded to a greater number of bits by using the cascade/enable feature of the CD4527B as demonstrated in Fig. 3. The strobe feature

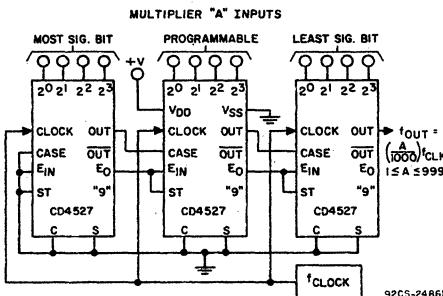


Fig. 3—BCD rate multiplier cascaded for multiplier A/1000,  $1 \leq A \leq 999$ .

allows outputs to be enabled or inhibited.<sup>1</sup>

### RATE-MULTIPLIER APPLICATIONS

#### Cascading

The rate multiplier can be connected in parallel or series as shown in Figs. 3 and 4. When devices are connected in parallel, as in Fig. 3, an n-bit rate multiplier is formed which obeys the input/output relation:

$$f_{out} = \frac{A}{K^n} f_{clk}$$

where  $0 < \frac{A}{K^n} \leq 1$

In the case of the CD4527B (BCD), the  $K^n$  factor is  $(10)^n$ , where  $n$  denotes the number of stages; for the CD4089B (binary),  $K^n$  becomes  $(2)^n$ , where  $n$  denotes the number of bits.

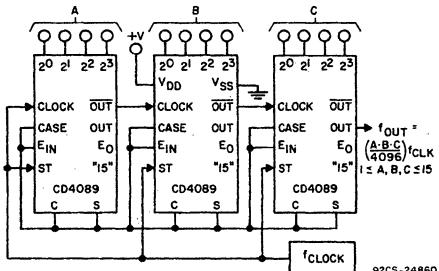


Fig. 4—Multiplication of three variables, A, B, and C.

In the circuit of Fig. 3, three BCD rate multipliers are connected in parallel; they produce an output rate which is proportional to the input clock by any multiple of  $A/1000$ . The A variable can be made to assume any value from 1 to 999 by programming the BCD inputs with a logical 1 or a logical 0. By using the CD4089B, the same circuit could be used to build a binary multiplier. The variable A would then range from 1 to 4095, and  $K^n$  would be  $(2)^n$  or 4096.

When rate multipliers are arranged serially, as shown in Fig. 4, two or more variables can be multiplied. The input/output relationship for the circuit shown in Fig. 4 is:

$$f_{out} = \frac{A \cdot B \cdot C}{4096} f_{clk}$$

where  $1 \leq A, B, \text{ or } C \leq 15$ .

#### Multiplication

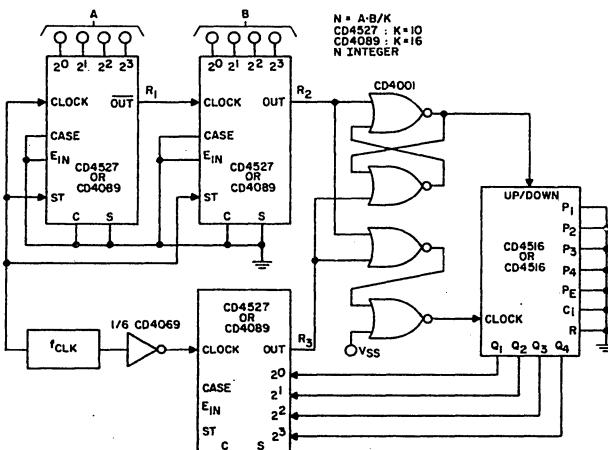
Two or more variables can be multiplied by using three or more rate multipliers and one up/down counter. The output is then a fixed number, either BCD or binary, not a pulse rate or frequency as before. Thus, in this discussion, as well as in the following arithmetic applications, the output is referred to as N ( $N = 1, 2, \dots$ ) and not  $f_{out}$ .

As an example, consider the circuit shown in Fig. 5. The input variables, A and B, are programmed to a BCD or binary number; the resultant output from the counter ( $Q_1, Q_2, Q_3, Q_4$ ) is  $N = (A \cdot B)/K$ . For the CD4527B,  $K = 10$ , and for the CD4089B,  $K = 16$ . Since the output of the up/down counter must be an integer from 1 to 9,  $A \cdot B/K$  must also be an integer. For example, if  $K = 10$ ,  $A = 0101$ , and  $B = 0100$ , then  $N = 5(4/10) = 2 = 0010$  as read on the  $Q_4, Q_3, Q_2$ , and  $Q_1$  lines, respectively. Analysis of the circuit of Fig. 5 shows that:

$$R_1 = f_{clk} \left( \frac{A}{10} \right)$$

$$R_2 = f_{clk} \left( \frac{A}{10} \right) \left( \frac{B}{10} \right) = f_{clk} \left( \frac{A \cdot B}{100} \right)$$

$$R_3 = f_{clk} \left( \frac{N}{10} \right)$$



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Fig. 5—Multiplication of two variables, A and B.

The interface circuit (CD4001A) shown preceding the up/down counter in Fig. 5 is used to convert the counter from a single clock to a dual-clock input device. Since the counter must count both up and down at random intervals it is desirable to have separate inputs for the up and down commands. The counter cannot accept simultaneous inputs to the command terminal, therefore, a multi-phase clock frequency is used at the input.

In Fig. 5 the output rate,  $R_2$ , addresses the "up count", and command,  $R_3$ , addresses the "down count" of the CD4516B. As  $R_2$  and  $R_3$  change, the counter steps up or down until the loop stabilizes. The counter acts as a null detector, equalizing the input rates so that  $R_2 = R_3$  when stability is reached. Thus, at equilibrium:

$$R_2 = R_3$$

or

$$f_{clk} \left( \frac{A \cdot B}{100} \right) = f_{clk} \left( \frac{N}{10} \right)$$

therefore

$$N = \left( \frac{A \cdot B}{10} \right)$$

If the true product  $A \cdot B$  is desired, then another rate multiplier can be used in the feedback loop to eliminate the 1/10 scaler multiplier. When the rate multiplier is programmed for a multiplier of 1,  $R_3 = f_{clk} \left( \frac{N}{100} \right)$ ; thus,  $R_2 = R_3$  yields  $N = A \cdot B$ .

### Addition and Subtraction

Two or more variables can be added or subtracted by using three or more rate multipliers, one up/down counter, and one summing circuit. These circuits are constructed in a loop arrangement, as in Figs. 6 and 7, similar to the one shown for multiplication in Fig. 5.

It should be noted that a simple OR gate cannot be used to sum  $R_1$  and  $R_2$  because, if pulses occur simultaneously on  $R_1$  and  $R_2$  during the same clock period, information can be lost. The circuits shown in Figs. 6, 7, and 8 eliminate the problem provided the synchronization rate is higher than that of  $R_1$  and  $R_2$ .

Fig. 6 is the diagram of a circuit used to sum two variables, A and B. The figure shows that  $R_1$  and  $R_2$  are summed and routed to the "up count" terminal of the counter. In subtraction, the summing circuit is placed in the signal path to the "down count" terminal of the counter, as illustrated in the circuit of Fig. 7. Both addition and subtraction can be performed.

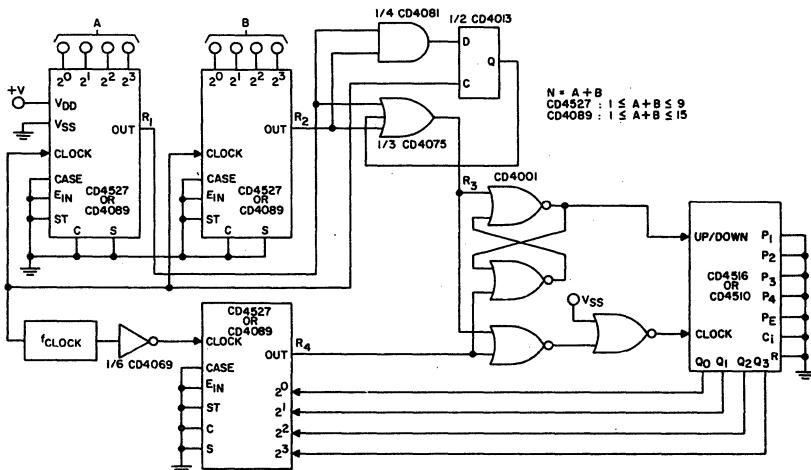
In Fig. 6:

$$R_3 = R_1 + R_2 = f_{clk} \left( \frac{A}{10} \right) + f_{clk} \left( \frac{B}{10} \right)$$

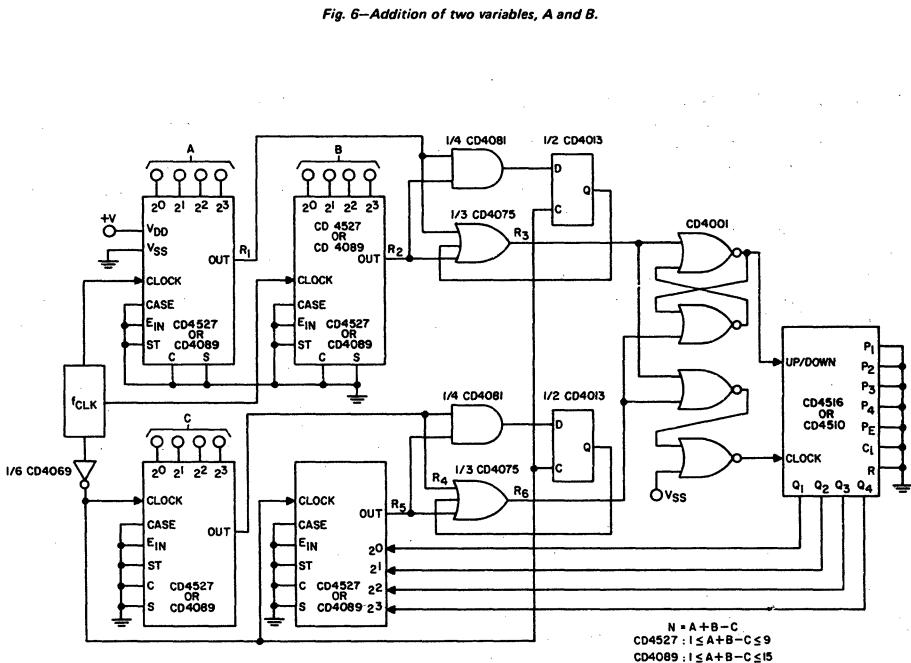
$$R_4 = f_{clk} \left( \frac{N}{10} \right)$$

Then, at equilibrium:

$$R_3 = R_4$$



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Fig. 7—Combined addition and subtraction .

therefore

$$f_{\text{clk}} \left( \frac{A}{10} \right) + f_{\text{clk}} \left( \frac{B}{10} \right) = f_{\text{clk}} \left( \frac{N}{10} \right)$$

or

$$N = A + B$$

As discussed above, the circuit shown in Fig. 7 is used to add and subtract simultaneously. From Fig. 7:

$$R_3 = R_1 + R_2 = f_{\text{clk}} \left( \frac{A}{10} \right) + f_{\text{clk}} \left( \frac{B}{10} \right)$$

$$R_6 = R_4 + R_5 = f_{\text{clk}} \left( \frac{C}{10} \right) + f_{\text{clk}} \left( \frac{N}{10} \right)$$

Then, at equilibrium:

$$R_3 = R_6$$

and

$$N = A + B - C$$

Finally, the average-rate output of the rate multiplier can be modified by the sum of two variables by using the less complex circuit shown in Fig. 8. It should be noted that the output is a time-averaged rate, not a fixed number, N, as before.

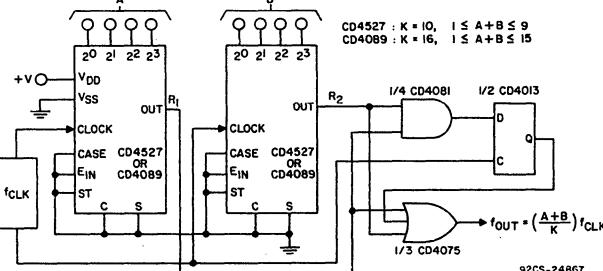


Fig. 8—The sum of two variables, A and B, with a constant multiplier.

#### Division

Two variables, A and B, can be divided by use of the circuit shown in Fig. 9. Two rate multipliers are connected in parallel to form the A variable. The parallel connection ensures that the multiplier constant, 1/10, does not appear in the final result, A/B. From Fig. 9:

$$R_1 = f_{\text{clk}} \left( \frac{A}{100} \right)$$

$$R_2 = f_{\text{clk}} \left( \frac{B}{10} \right)$$

$$R_3 = R_2 \left( \frac{N}{10} \right) = f_{\text{clk}} \left( \frac{N}{10} \right) \left( \frac{B}{10} \right)$$

At equilibrium,  $R_1 = R_3$ ; therefore:

$$\frac{A}{100} = \left( \frac{N}{10} \right) \left( \frac{B}{10} \right)$$

or

$$N = \frac{A}{B}$$

#### Square Roots/Higer-Order Roots/Algebraic Equations

The RCA COS/MOS rate multiplier can be used in circuits such as those shown in Figs. 10 and 11 to generate roots of the form  $A^{x/y}$ , where x and y are integers. The up/down counter is also used in a feedback loop configuration, as in Figs. 5 through 8, above, to perform this operation. The circuit shown in Fig. 11 can also be used to generate  $A^{1/3}$  by programming one of the three rate multipliers with the variable A and the other two with unity.

From Fig. 10:

$$R_1 = f_{\text{clk}} \left( \frac{1}{10} \right) \left( \frac{A}{10} \right) = f_{\text{clk}} \left( \frac{A}{100} \right)$$

$$R_2 = f_{\text{clk}} \left( \frac{N}{10} \right) \left( \frac{N}{10} \right) = f_{\text{clk}} \left( \frac{N^2}{100} \right)$$

Then, at equilibrium:

$$R_1 = R_2$$

therefore

$$N = \sqrt{A}$$

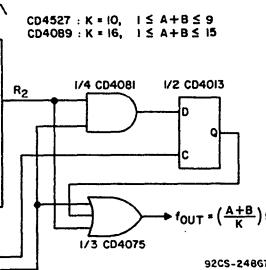


Fig. 10—Square root generator.

From Fig. 11:

$$R_1 = f_{\text{clk}} \left( \frac{A^2}{100} \right) \left( \frac{1}{10} \right) = f_{\text{clk}} \left( \frac{A^2}{1000} \right)$$

$$R_2 = f_{\text{clk}} \left( \frac{N}{10} \right) \left( \frac{N}{10} \right) \left( \frac{N}{10} \right) = f_{\text{clk}} \left( \frac{N^3}{1000} \right)$$

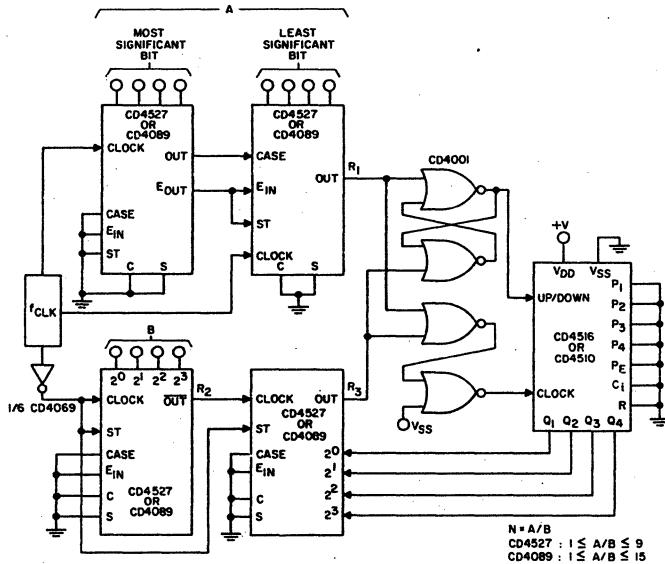
At equilibrium,  $R_1 = R_2$ ; therefore:

$$N^3 = A^2$$

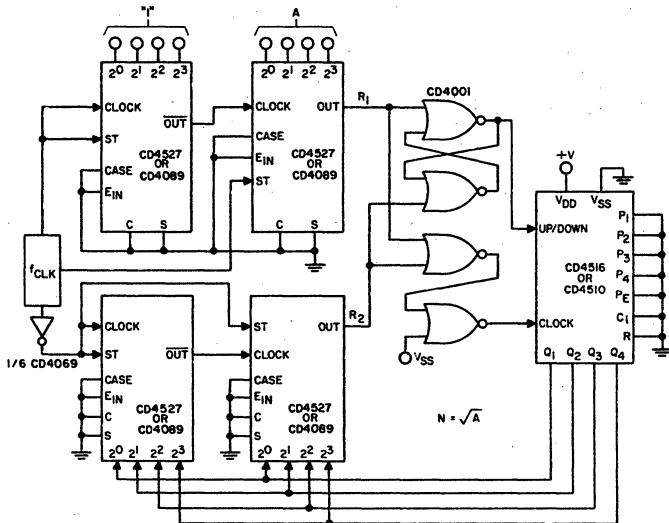
or

$$N = A^{2/3}$$

In addition to generating roots of the form  $A^{x/y}$  various algebraic equations can be generated and solved by combining the root-determining techniques with those used in multiplication, division, addition, and subtraction. Only block diagrams with input/output relationships are shown for these circuits owing to the complexity of the wiring interconnects.



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Fig. 9—Division of the variable  $A$  by the variable  $B$ .

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Fig. 10—Generation of  $A^{1/2}$

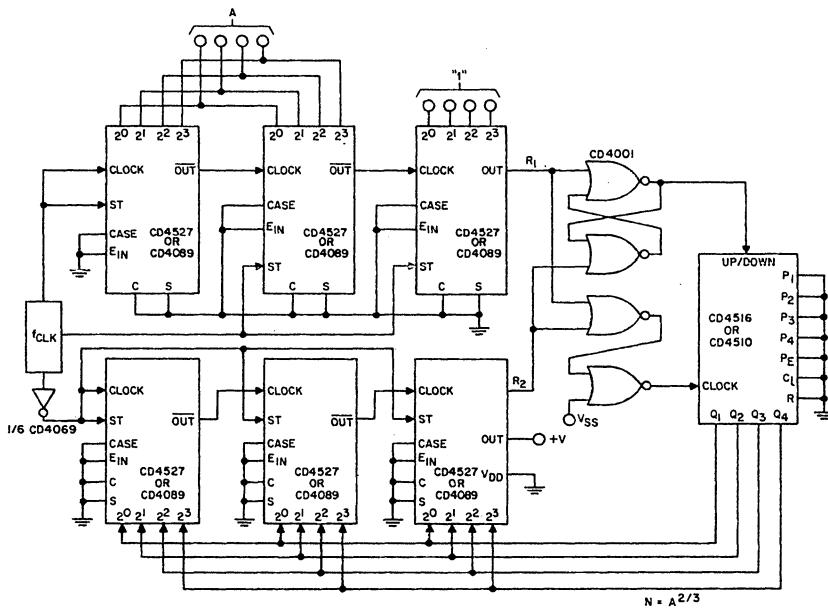


Fig. 11—Generation of  $A^{2/3}$

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From Fig. 12:

Then, at equilibrium:

$$R_1 = A^2 / K^2 n$$

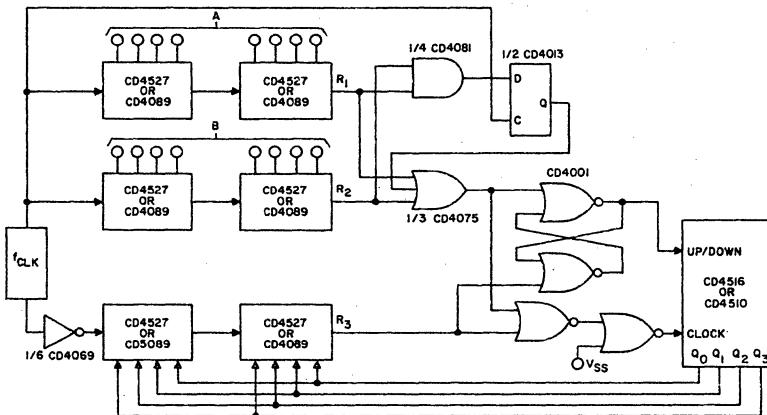
$$R_2 = B^2 / K^2 n$$

$$R_3 = N^2 / K^{2n}$$

$$R_1 + R_2 = R_3$$

therefore,

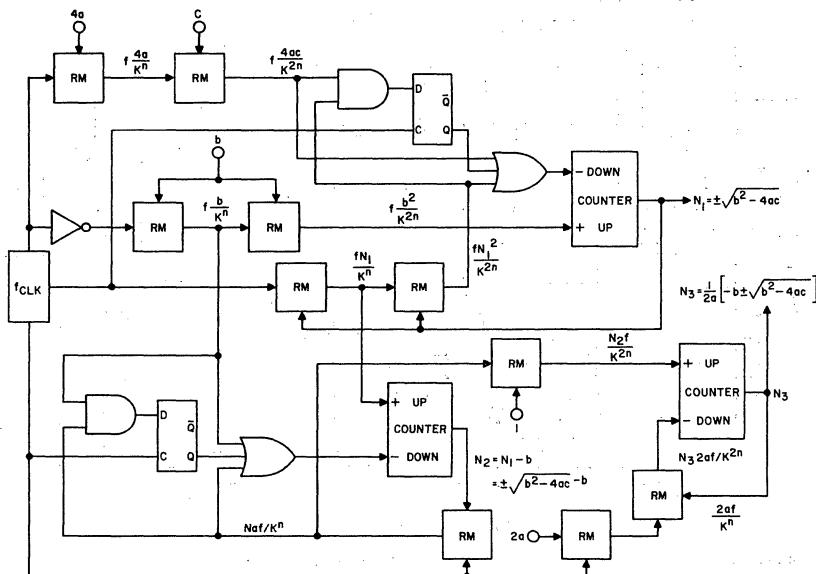
$$N^2 = A^2 + B^2$$



*Fig. 12—Generation of the equation  $N^2 = A^2 + B^2$ .*

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The COS/MOS CD4527B and CD4089B rate multipliers can also be used to solve a known equation. For example, Fig. 13 can be used to solve the well-known quadratic equation,

Fig. 13—Solutions of the quadratic equation,  $ax^2 + bx + c = 0$ .

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$ax^2 + bx + c = 0$ . The solutions,  $x_1$  and  $x_2$ , are assumed to be real, and can be found by monitoring the output of counter  $N_3$ . As discussed above, the  $K^n$ ,  $K^{2n}$  factors are the multiplication factors inherent with the type of rate multiplier (BCD or binary) used.

#### Frequency Ratios

The circuit shown in Fig. 14 can be used to compute the ratio of two frequencies,  $f_1$  and  $f_2$ . Since the frequencies are usually random, care should be taken to condition these inputs to ensure that coincidence does not occur at the counter command input. Fig. 15 shows a circuit that can be used to condition the input frequencies.<sup>4</sup> The input clock frequency should be at least 4 times faster than the highest input frequency ( $f_1$  or  $f_2$ ).

From Fig. 14:

$$R_1 = f_1/K^n$$

and

$$R_2 = f_2/N/K^n$$

Then, at equilibrium,  $R_1 = R_2$ ; therefore:

$$N = f_1/f_2$$

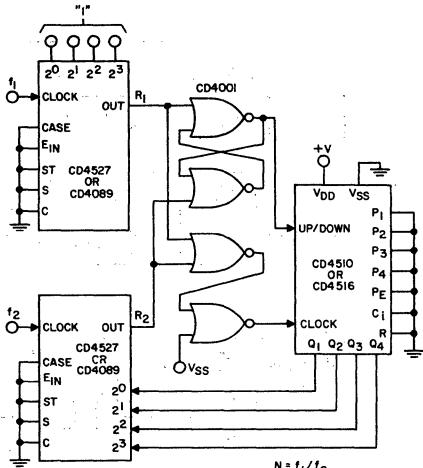


Fig. 14—Frequency ratios.

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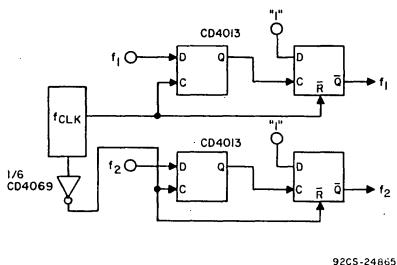
Fig. 15—Retiming circuit for  $f_1$  and  $f_2$ 

Fig. 16 illustrates the principle of integration as described above. If the feedback loop scheme is used in Fig. 16 i.e., if  $N(\mu)$  is the program input A to the multiplier:

$$N(\mu) = \int_0^{\mu} K d\mu = \int_0^{\mu} \frac{A}{n} d\mu = A$$

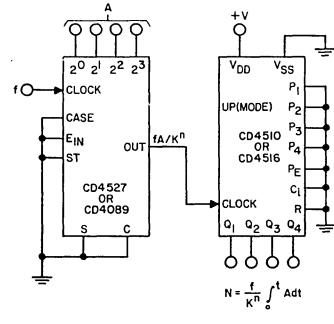


Fig. 16—Integration.

Therefore

$$\frac{dA}{d\mu} = \dot{A} = \frac{1}{K^n} \mu$$

or

$$A = e^{\mu/K^n}$$

Thus, the rate multiplier can also be used to solve differential equations.

#### Symmetric Rate Multiplication

In the previous discussion, the classic rate multiplier was used to produce an output pulse train whose period is not generally symmetrical. In many cases, the multiplication factor  $1/K$  is not of the form  $1/2^n$  (n integer); thus, a "round off" error is associated with the output signal. In fact, if the output waveform is observed on a spectrum analyzer, a Bessel distribution similar to that caused by an FM modulated signal will appear. In many applications where spectral purity is important, such harmonics and spurious outputs are intolerable.

There is a technique, the symmetric rate multiplication technique (SRM), that can be used to eliminate rate outputs with the above mentioned spectral characteristics. The SRM approach yields output rates with symmetrical duty cycles (50 percent) and no "round off" errors. The only limitation to the SRM technique is the clock frequency. However, in applications where limited numbers of frequencies are to be synthesized, the SRM approach works very well, and the clock or master oscillator is not a controlling factor.

#### Integration

The CD4527B and CD4089B rate multipliers can be used as digital integrators by feeding the output of the rate multiplier to the input of an up/down counter in the up-count mode only. The system will operate as an integrator if the input to the counter is in pulse form. Each pulse input to the counter acts as an increment with respect to time, so that the counter accumulates the pulse increments. If the counter is large enough, so that the delta increment represents only a small portion of the total counter contents, then the delta increment approaches a differential and the counter accumulates the integral of this differential over time. For example, assume that the counter output is  $N(\mu)$  where  $\mu$  represents the incremental pulse and is monotonically increasing. If each pulse at the input to the rate multiplier increases  $\mu$  by one unit, and the frequency  $f$  is defined as  $f = d\mu/dt$ , then the output of the rate multiplier is:

$$K \frac{d\mu}{dt} = Kf_{clk}$$

This relation is the same as that described above under the heading "Rate Multiplier Description".

If the output of the rate multiplier is supplied to the up-count input of the counter, then, at a given instant:

$$K \frac{d\mu}{dt} = N(\mu)$$

But the counter output  $N(\mu)$  is changing with time owing to its input  $K \frac{d\mu}{dt}$ , thus:

$$K \frac{d\mu}{dt} = -\frac{dn}{dt}$$

or

$$Kd\mu = dn$$

Therefore

$$N(\mu) = \int_0^{\mu} Kd\mu$$

Consider the circuit shown in Fig. 17, where the input clock frequency  $f_c$  is derived from an oscillator whose period is symmetrical (50-percent duty cycle) and whose frequency is fixed. For simplicity, the multiplication factors programmed in are of the form  $1/K$ , where  $1 \leq K \leq 9$ . The final output frequency is:

$$f_{\text{out}} = f_c \left( \frac{1}{K} \right)$$

where  $f_{\text{out}}$  is a frequency whose period is symmetrical. The multiplication factors  $1/K$  are assumed to be available and stored for use at any given time as they are in the CD4527B.

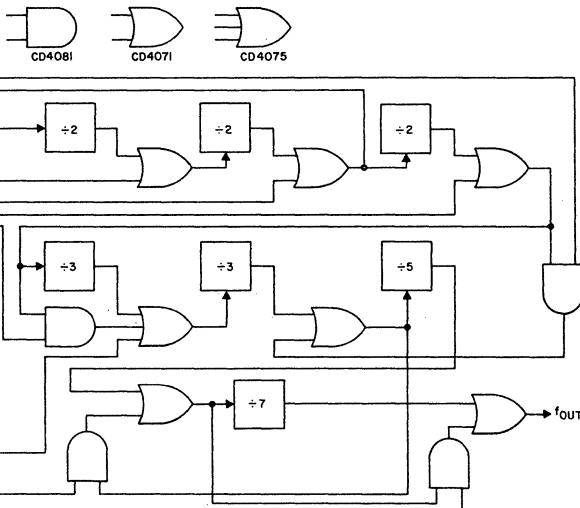


Fig. 17—Symmetric rate multiplier for  $1 < K \leq 9$ .

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In addition, two numbers,  $N$  and  $R$ , are defined:  $N$  is the lowest common multiple of the  $K$  factors and  $R$  is the product of the remaining  $K$  factors when one is chosen for rate multiplication. The output frequency then becomes:

$$f_{\text{out}} = f_c \left( \frac{R}{N} \right)$$

In Fig. 17, the number  $N$  is:

$$N = 5 \cdot 7 \cdot 8 \cdot 9 = 2520$$

Note that the  $\div 2$  and  $\div 3$  stages are included in  $\div 8$  and  $\div 9$ . As an example, to multiply the clock  $f_c$  by  $1/6$ :

$$N = 2520$$

$$R = 2 \cdot 2 \cdot 3 \cdot 5 \cdot 7$$

and

$$f_{\text{out}} = f_c \left( \frac{2 \cdot 2 \cdot 3 \cdot 5 \cdot 7}{2520} \right) = f_c \left( \frac{1}{6} \right)$$

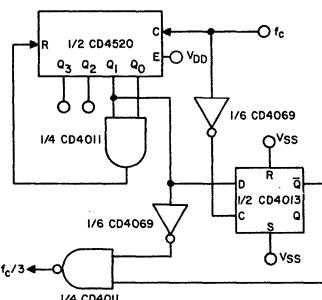
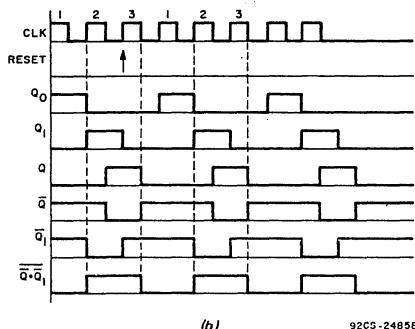
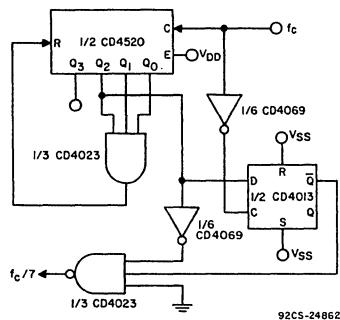
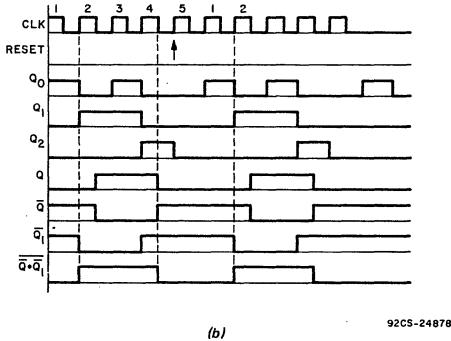
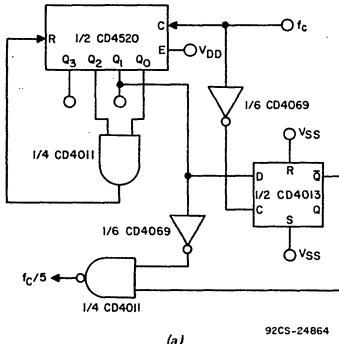
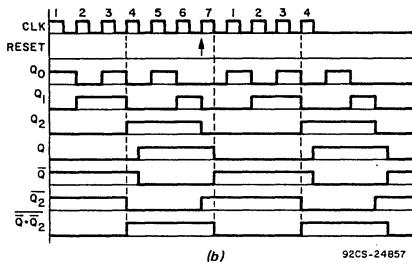


Fig. 18—(a) Symmetrical  $\div 3$  and (b) timing diagram.

Fig. 18—(a) Symmetrical  $\div 3$  and (b) timing diagram.Fig. 18—(a) Symmetrical  $\div 3$  and (b) timing diagram.Fig. 19—(a) Symmetrical  $\div 5$  and (b) timing diagram.Fig. 20—(a) Symmetrical  $\div 7$  and (b) timing diagram.

system up through the first (CCITT) group will demonstrate the SRM techniques. The numbers listed next to each channel frequency are the lowest common factors of that frequency.

In an application of this type, channel carriers must be spectrally pure (spurious emission  $> 70$ -dB down) and the phase jitter must be low (typically  $\leq 1^\circ$ ). From a systems point of view, if these carriers do not meet requirements such as these, then other system (crosstalk) specifications cannot be met. If carriers are synthesized using the classic rate multiplier, then requirements such as those mentioned above will not be met unless measures are taken to remove spurious emission from the waveform after generation has taken place. For example, the voice carrier has a channel separation of 4 kHz, so that the unwanted sideband separation is 8 kHz. To eliminate spurious emission with this type of distribution requires a critical filter with a high Q (usually 4 coils, 9 poles). Suppression of FM jitter or noise is another problem altogether. The SRM approach minimizes that problem because:

1. Output frequencies synthesized by the SRM technique have 50-percent duty cycles; thus, only odd harmonics exist, and these are easy to filter out.
2. The output has been derived from divider chains; thus, FM suppression by factors of  $20 \log N$  will exist. For example, a  $\div 2$  yields  $20 \log 2$  or approximately 6 dB of suppression.

Table I indicates that dividers ranging from 2 to 31 are needed to synthesize the 28 carriers listed. To synthesize these frequencies, a clock whose LCM (lowest common multiple) is that of the desired frequencies is chosen; as described above,

Table I — Channel Frequencies

Channel Freq. (kHz)	Lowest Common Factors (Divider Stages)
28	2, 2, 7
32	2, 2, 2, 2, 2
36	2, 2, 3, 3
40	2, 2, 2, 5
44	2, 2, 11
48	2, 2, 2, 2, 3
52	2, 2, 13
56	2, 2, 2, 7
60	2, 2, 3, 5
64	2, 2, 2, 2, 2, 2
68	2, 2, 17
72	2, 2, 2, 3, 3
76	2, 2, 19
80	2, 2, 2, 2, 5
84	2, 2, 3, 7
88	2, 2, 2, 11
92	2, 2, 23
96	2, 2, 2, 2, 2, 3
100	2, 2, 5, 5
104	2, 2, 2, 13
108	2, 2, 3, 3, 3
112	2, 2, 2, 2, 7
116	2, 2, 29
120	2, 2, 2, 3, 5
124	2, 2, 31
128	2, 2, 2, 2, 2, 2, 2
132	2, 2, 3, 11
136	2, 2, 2, 17

the limiting factor of the SRM approach is the clock frequency. The table shows that the clock frequency increases as the number of frequencies to be synthesized increases. COS/MOS circuitry is used in this example, and since a COS/MOS device normally operates at 10 MHz,  $f_{CLK}$  will not exceed this frequency. Table II lists some of the many combinations that can be used to obtain channel carriers that can be synthesized with clock frequencies not exceeding 10 MHz; those not listed can be obtained by a number of clock frequency choices. Using Table II, circuits similar to those shown in Fig. 17 can be constructed to implement this application.

Many possible LCM combinations can be used to implement the SRM technique, as illustrated; however, the common factors (dividers) must be bypassed in the synthesized frequency, and remainder (R dividers) used to obtain the final result. For example, when 72 kHz is to be synthesized, the  $\div 2$ ,  $\div 2$ ,  $\div 2$ ,  $\div 3$ , and  $\div 3$  factors are bypassed and the  $\div 2$ ,  $\div 2$ ,  $\div 2$ ,  $\div 2$ ,  $\div 3$ , and  $\div 5$  remainder used.

Table II — Channel Carriers Synthesizable with Clock Frequencies Not Exceeding 10 MHz

Channel Frequency (kHz)	Lowest Common Factors (Divider Stages)
32	2, 2, 2, 2, 2
36	2, 2, 2, 3, 3
40	2, 2, 2, 5
48	2, 2, 2, 2, 3
60	2, 2, 3, 5
64	2, 2, 2, 2, 2, 2
72	2, 2, 2, 3, 3
80	2, 2, 2, 2, 5
96	2, 2, 2, 2, 2, 3
120	2, 2, 2, 3, 5
128	2, 2, 2, 2, 2, 2, 2
28	2, 2, 7
44	2, 2, 11
56	2, 2, 7
84	2, 2, 3, 7
88	2, 2, 2, 11
112	2, 2, 2, 2, 7
132	2, 2, 3, 11
52	2, 2, 13
68	2, 2, 17
104	2, 2, 2, 13
136	2, 2, 2, 17

#### SUMMARY

The COS / MOS rate multipliers CD4527B and CD4089B can be used to generate many digital functions. These MSI circuits are very useful as basic building blocks in low-power systems where minimum package count is desirable. Several of these applications, such as frequency synthesis and instrumentation, require low power and low package count to be competitive. Many arithmetic functions can also be performed by the COS/MOS rate multipliers with the aid of an up/down counter and some control logic. This feature is very useful in several areas of numeric control and digital processing systems. All of these features, and the fact that the CD4527B and CD4089B are part of the standard COS/MOS family of digital IC's, make these devices very useful to the design engineer.

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