

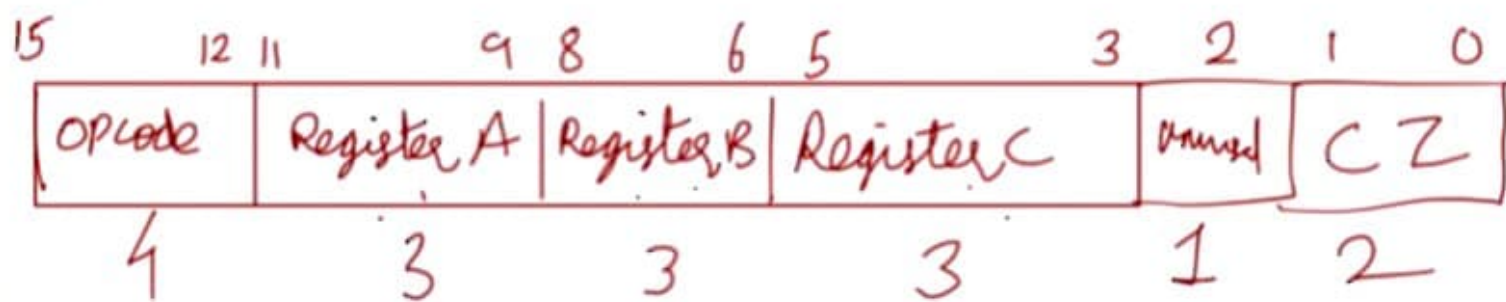
1) ADD - add  $rc, ra, rb$

15	12	11	9	8	6	5	3	2	1	0		
Opcode				Register A			Register B		Register C		unused	CZ
4				3			3		3		1	2

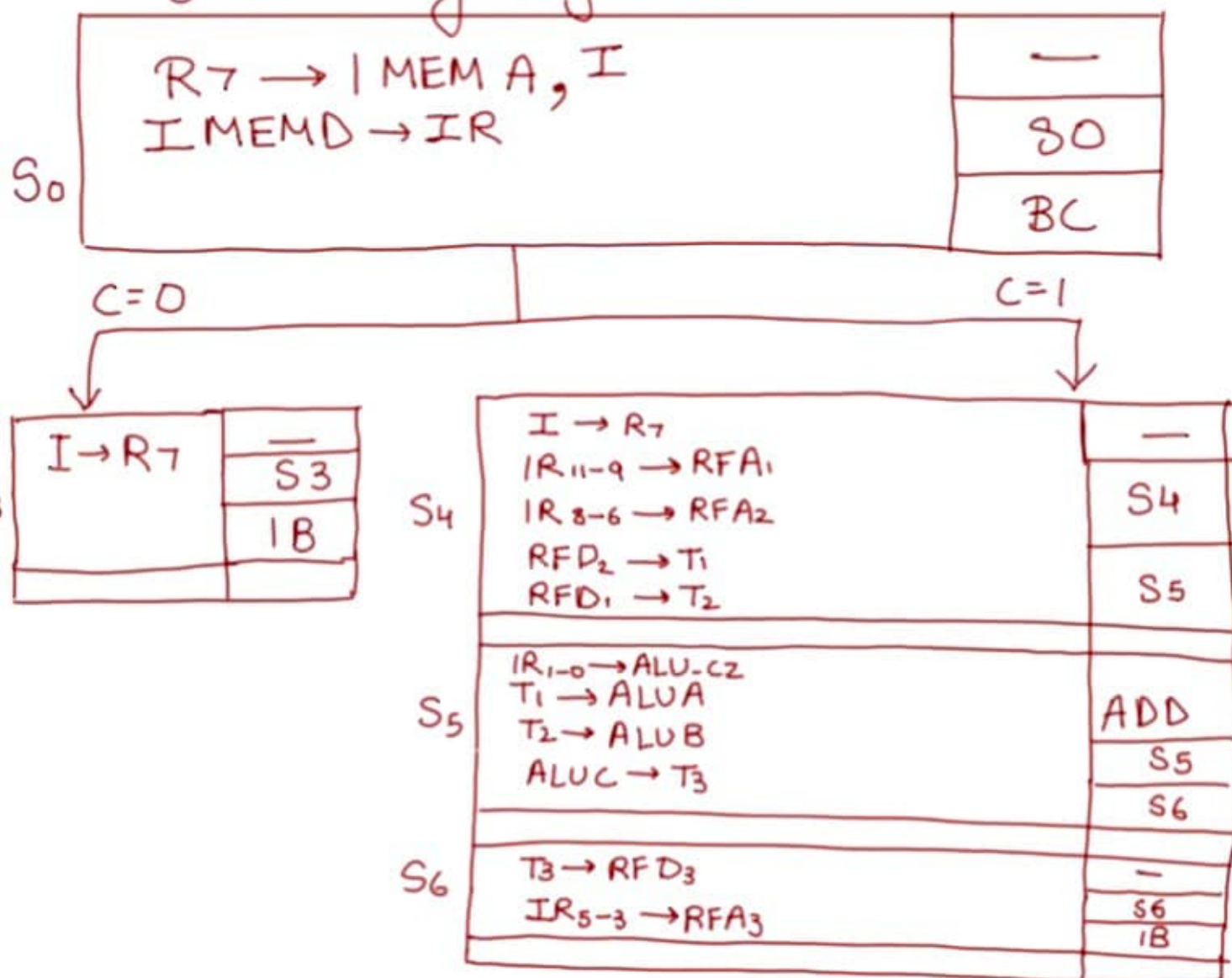
Add content of reg B to reg A and store result in reg C

S <sub>0</sub>	R7 → IMEM A, I IMEMD → IR	—
		80
		S1
S <sub>1</sub>	I → R7 IR <sub>11-9</sub> → RFA <sub>1</sub> IR <sub>8-6</sub> → RFA <sub>2</sub> RFD <sub>2</sub> → T <sub>1</sub> RFD <sub>1</sub> → T <sub>2</sub>	—
		S1
		S2
S <sub>2</sub>	IR <sub>1-0</sub> → ALU-CZ T <sub>1</sub> → ALUA T <sub>2</sub> → ALUB ALUC → T <sub>3</sub>	ADD
		S2
		S3
S <sub>3</sub>	T <sub>3</sub> → RFD <sub>3</sub> IR <sub>5-3</sub> → RFA <sub>3</sub>	—
		S3
		IB

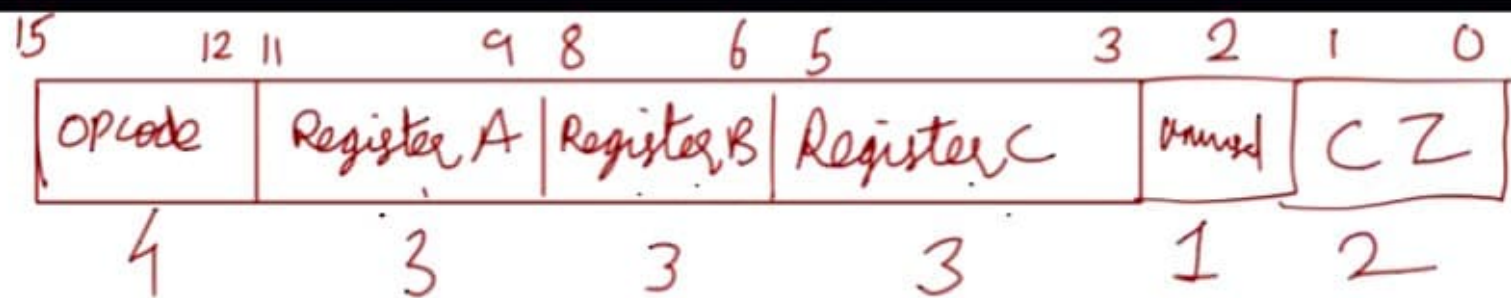
## 2) ADC - adc rc, ra, rb



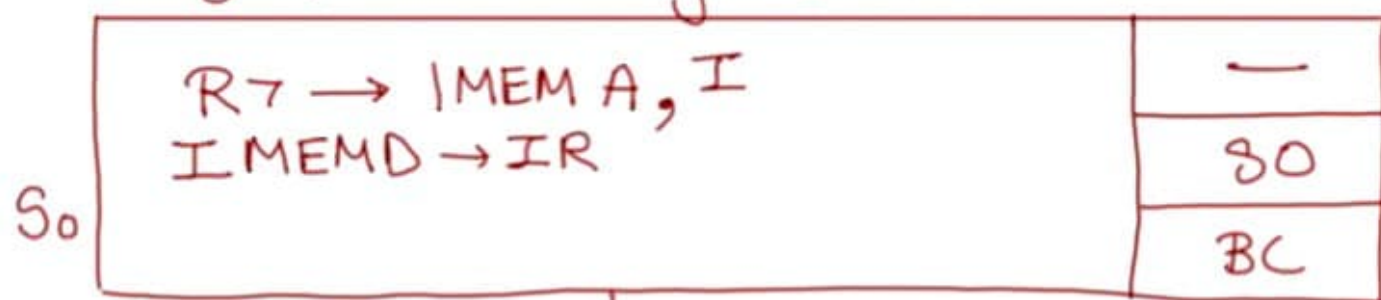
Add content of reg B to reg A and store result in reg C, carry flag is set.



### 3) ADZ - adz rc, ra, rb



Add content of reg B to reg A and store result in reg C, if zero flag is set.



Z = 0

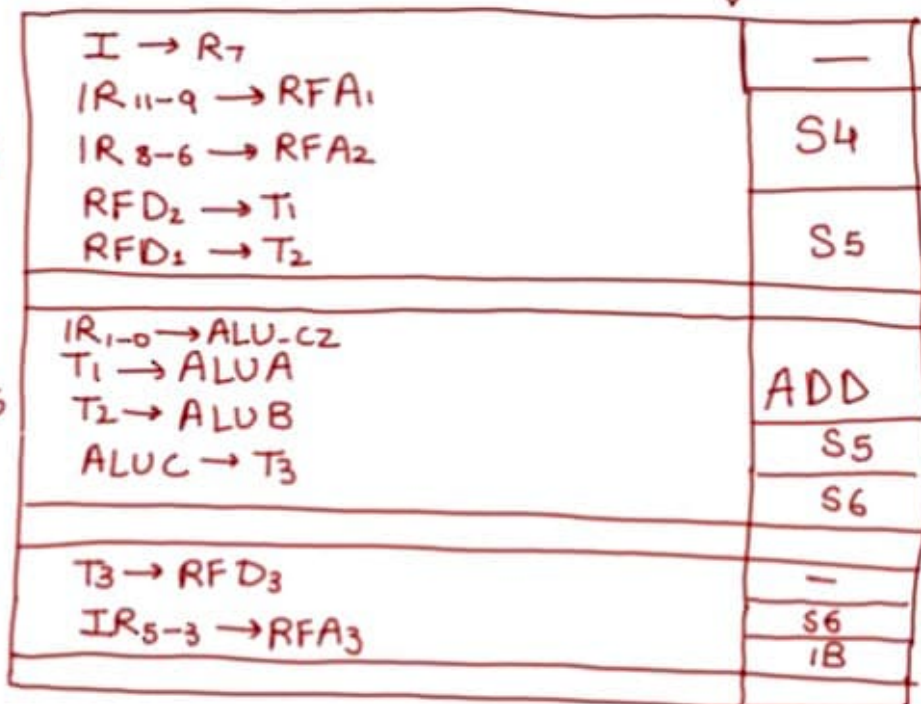
Z = 1



S<sub>4</sub>

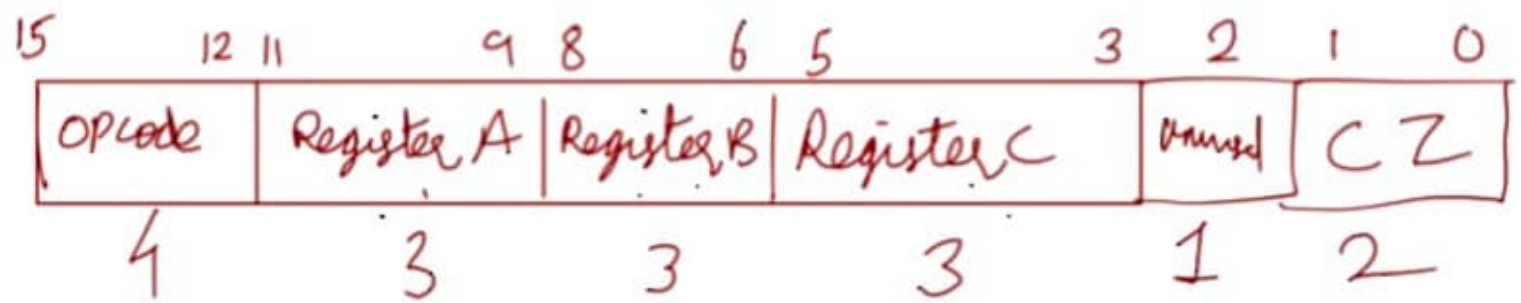
S<sub>5</sub>

S<sub>6</sub>





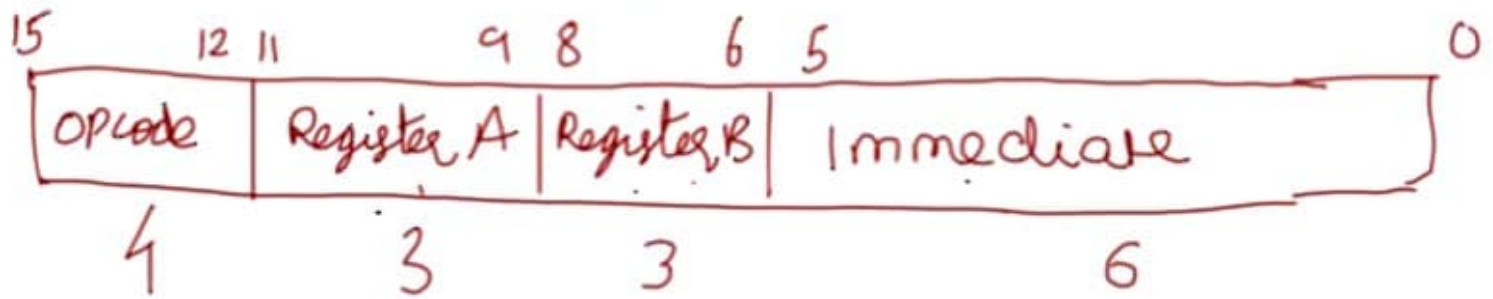
4) ADL - add rc, ra, rb



Add content of reg B (after one bit left shift) to reg A and store result in reg C

S <sub>0</sub>	R7 → IMEM A, I IMEMD → IR	—
		80
		S1
S <sub>1</sub>	I → R7 IR <sub>11-9</sub> → RFA <sub>1</sub> IR <sub>8-6</sub> → RFA <sub>2</sub> RFD <sub>2</sub> → T <sub>1</sub> RFD <sub>1</sub> → LS1 → T <sub>2</sub>	—
		S1
		S2
S <sub>2</sub>	IR <sub>1-0</sub> → ALU-CZ T <sub>1</sub> → ALUA T <sub>2</sub> → ALUB ALUC → T <sub>3</sub>	ADD
		S2
		S3
S <sub>3</sub>	T <sub>3</sub> → RFD <sub>3</sub> IR <sub>5-3</sub> → RFA <sub>3</sub>	—
		S3
		IB

5) ADI - add rB, rA, imm6



S <sub>0</sub>	R7 → IMEMA, I IMEMD → IR	—
		S <sub>0</sub>
		S <sub>1</sub>
S <sub>1</sub>	IR <sub>11-9</sub> → RFA1 RFD <sub>2</sub> → T <sub>1</sub> IR <sub>5-0</sub> → SE_6_16 → T <sub>2</sub> I → R7	—
		S <sub>1</sub>
		S <sub>2</sub>
S <sub>2</sub>	T <sub>1</sub> → ALUA T <sub>2</sub> → ALUB ALUC → T <sub>3</sub>	ADD
		S <sub>2</sub>
		S <sub>3</sub>
S <sub>3</sub>	IR <sub>8-6</sub> → RFA3 T <sub>3</sub> → RFD <sub>3</sub>	—
		S <sub>3</sub>
		IB

6)

NDU

Sunday, April 10, 2022 12:58 PM

16 12 11 9 8 6 5 3

opcode	reg-A	reg-B	reg-C	001
--------	-------	-------	-------	-----

ND2 TA TB TC  $\Rightarrow$  TC  $\leftarrow$  TA NAND TB

S0

R7 $\rightarrow$ IMEM-A, I	-
IMEM-D $\rightarrow$ IR	S0
	S1

S1

IR <sub>5-6</sub> $\rightarrow$ RF-A2	-
RF-D2 $\rightarrow$ T1	S1
IR <sub>11-9</sub> $\rightarrow$ RF-A1	
RF-D1 $\rightarrow$ T2	S2
I $\rightarrow$ R7	

S2

T1 $\rightarrow$ ALU-A	NAND
T2 $\rightarrow$ ALU-B	S2
ALU-C $\rightarrow$ T3	S3

S3

T3 $\rightarrow$ RF-D3	-
IR <sub>5-3</sub> $\rightarrow$ RF-A3	S3
	S8



# NDC

Sunday, April 10, 2022 12:58 PM

16 12 11 9 8 6 5 3  
 opcode reg-A reg-B reg-C 001

NDC TA TB TC  $\Rightarrow$  if C=1, TC  $\leftarrow$  TA NAND TB

S0

R7  $\rightarrow$  IMEM-A, I  
 IMEM-D  $\rightarrow$  IR

-  
S0  
BCc

C=1

C=0

S2

IR<sub>5-6</sub>  $\rightarrow$  RF-A2  
 RF-D2  $\rightarrow$  T1  
 IR<sub>11-9</sub>  $\rightarrow$  RF-A1  
 RF-D1  $\rightarrow$  T2  
 I  $\rightarrow$  R7

-  
S2  
S3

S1

I  $\rightarrow$  R7

-  
S1  
IB

S3

T1  $\rightarrow$  ALU-A  
 T2  $\rightarrow$  ALU-B  
 ALU-C  $\rightarrow$  T3

NAND  
S3  
S4

S4

T3  $\rightarrow$  RF-D3  
 IR<sub>5-3</sub>  $\rightarrow$  RF-A3

-  
S4  
IB

8

NDZ

Sunday, April 10, 2022 12:58 PM

6 12 18 24 30 36 42 48 54 60 66 72 78 84 90 96 102 108 114 120 126 132 138 144 150 156 162 168 174 180 186 192 198 204 210 216 222 228 234 240 246 252 258 264 270 276 282 288 294 300 306 312 318 324 330 336 342 348 354 360 366 372 378 384 390 396 402 408 414 420 426 432 438 444 450 456 462 468 474 480 486 492 498 504 510 516 522 528 534 540 546 552 558 564 570 576 582 588 594 600 606 612 618 624 630 636 642 648 654 660 666 672 678 684 690 696 702 708 714 720 726 732 738 744 750 756 762 768 774 780 786 792 798 804 810 816 822 828 834 840 846 852 858 864 870 876 882 888 894 900 906 912 918 924 930 936 942 948 954 960 966 972 978 984 990 996 1000

NDZ TA TB TC  $\Rightarrow$  if  $Z=1$ ,  $TC \leftarrow TA \text{ NAND } r6$

S0

R7  $\rightarrow$  IMEM-A, I  
IMEM-D  $\rightarrow$  IR

Z=1

Z=0

S2

IR<sub>5-6</sub>  $\rightarrow$  RF-A2  
RF-D2  $\rightarrow$  T1  
IR<sub>11-12</sub>  $\rightarrow$  RF-A1  
RF-D1  $\rightarrow$  T2  
I  $\rightarrow$  R7

S1

I  $\rightarrow$  R7

S3

T1  $\rightarrow$  ALU-A  
T2  $\rightarrow$  ALU-B  
ALU-C  $\rightarrow$  T3

NAND

S3

S4

S4

T3  $\rightarrow$  RF-D3  
IR<sub>5-6</sub>  $\rightarrow$  RF-A3

-

S4

IB





load @ (rb+imm) in ra

lw ra, rb, Imm

87 → I, ImmA			-
ImmD → IR			
IR <sub>8-6</sub> → RF_A1			
RF_D1 → T2			
IR <sub>5-0</sub> → sc_6-16 → T1			
I → r7			
T1 → aluA			ADD-N
T2 → aluB			
aluC → T3			
T3 → DmemA			-
IR <sub>11-9</sub> → RF_A3			

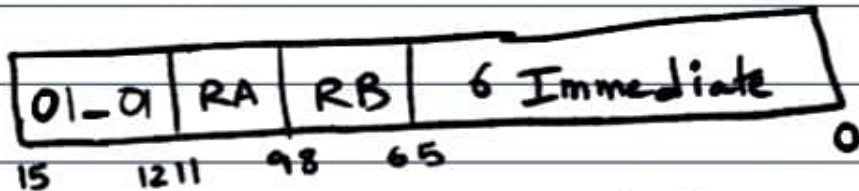
LHI

IR <sub>11-9</sub> → RF_A3			
DmemD → RF_D3			IB

LHI

10)

SW :



(I)

Store value in ra @ (rb+imm) SW ra, rb, Imm

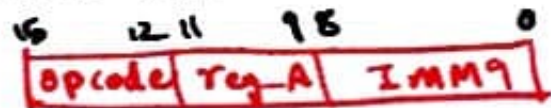
r7 → I, ImmA			-
ImmD → IR			
IR <sub>8-6</sub> → RF_A,			
RF_DI → T2			
IR <sub>5-0</sub> → 8-6-16 → T1			
I → r7			
T1 → aluA			ADD-N
T2 → aluB			
aluC → T3			
T3 → DmemA			-
T2 → RF_A1			

T3 → DmemA			ID
IR <sub>11-9</sub> → RF_A1			
RF_DI → DmemI			

11)

LHI

Sunday, April 10, 2022 12:50 PM



LHI reg-A IMM9.

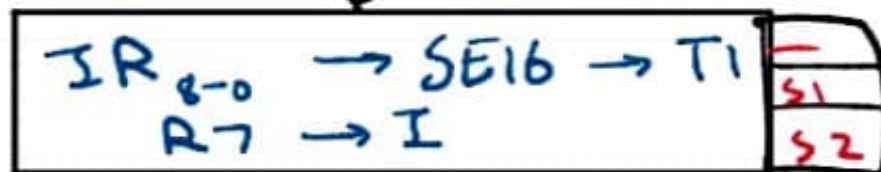
for IMM9 =  $b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0$

then reg-A becomes  $b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0 00000000$

S0



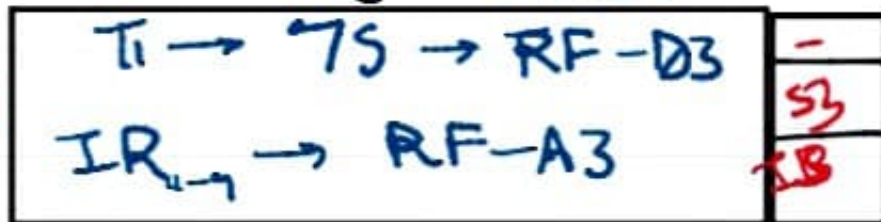
S1



S2



S3





IR 0-4 000000000000  
 Each register is address incrementing  
 starting from 0, if over corresponding  
 bit is set.

S0 IR7 → 3 memA  
 IMEMB → IR

S1 IR4 → RF A1  
 RF-D1 → T1  
 IR7 → S016 → T2

S2 T1 → ALWA  
 T2 → ALUB, DMEM-A  
 ALUC → T3  
 IR20 → BA7 → Dec → RFAI  
 RFD1 → Dmem DD

S3 IR6 → S016 → T1  
 T3 → T2

S4 T1 → ALWA  
 T2 → ALUB, DMEM  
 ALUC → T3  
 IR20 → BA6 → Dec → RFAI  
 RFD1 → Dmem DD

S5 IR5 → S016 → T1  
 T3 → T2

S6 T1 → ALWA  
 T2 → ALUB, DMEM  
 ALUC → T3  
 IR20 → BA5 → Dec → RFAI  
 RFD1 → Dmem DD

S7 IR4 → S016 → T1  
 T3 → T2

S8 T1 → ALWA  
 T2 → ALUB, DMEM  
 ALUC → T3  
 IR20 → BA4 → Dec → RFAI  
 RFD1 → Dmem DD

S9 IR3 → S016 → T1  
 T3 → T2

S10 T1 → ALWA  
 T2 → ALUB, DMEM  
 ALUC → T3  
 IR20 → BA3 → Dec → RFAI  
 RFD1 → Dmem DD

S11 IR2 → S016 → T1  
 T3 → T2

S12 T1 → ALWA  
 T2 → ALUB, DMEM  
 ALUC → T3  
 IR20 → BA2 → Dec → RFAI  
 RFD1 → Dmem DD

S13 IR1 → S016 → T1  
 T3 → T2

S14 T1 → ALWA  
 T2 → ALUB, DMEM  
 ALUC → T3  
 IR20 → BA1 → Dec → RFAI  
 RFD1 → Dmem DD

S15 IR0 → S016 → T1  
 T3 → T2

S16 T1 → ALWA  
 T2 → ALUB, DMEM  
 ALUC → T3  
 IR20 → BA0 → Dec → RFAI  
 RFD1 → Dmem DD

$\frac{1}{2} \times \frac{1}{2} = \frac{1}{4}$

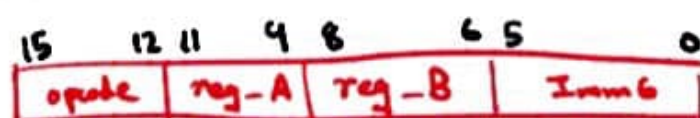
$$\begin{array}{l} IR^4 \rightarrow S^2 \times B \rightarrow T \\ T_3 \rightarrow T_2 \end{array}$$

$T1 \rightarrow ALWA$   
 $T2 \rightarrow ALUB, Dmem$   
 $ALUC \rightarrow T3$   
 $IR \rightarrow BAO \rightarrow DEC \rightarrow RFA$   
 $RF \rightarrow D3 \rightarrow Dmem \rightarrow DI$

14)

BEQ

Sunday, April 10, 2022 11:49 AM



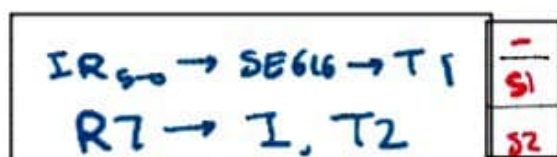
BEQ RA RB IMM6

if RA = RB, PC → PC + IMM6

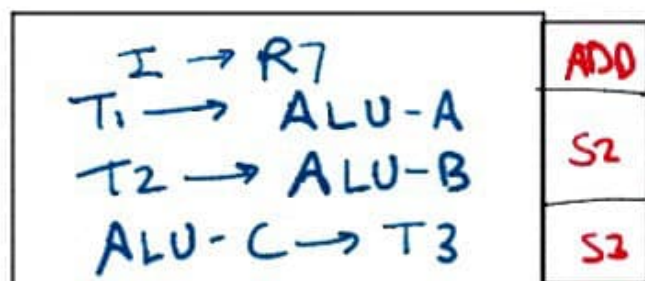
S0



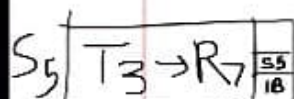
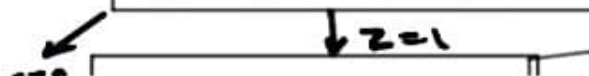
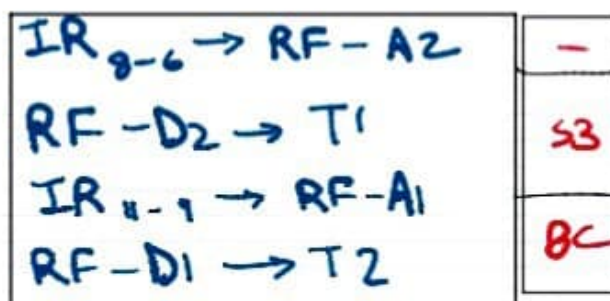
S1



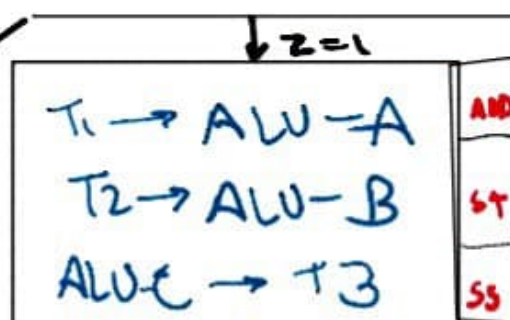
S2



S3



S4



S5





15)

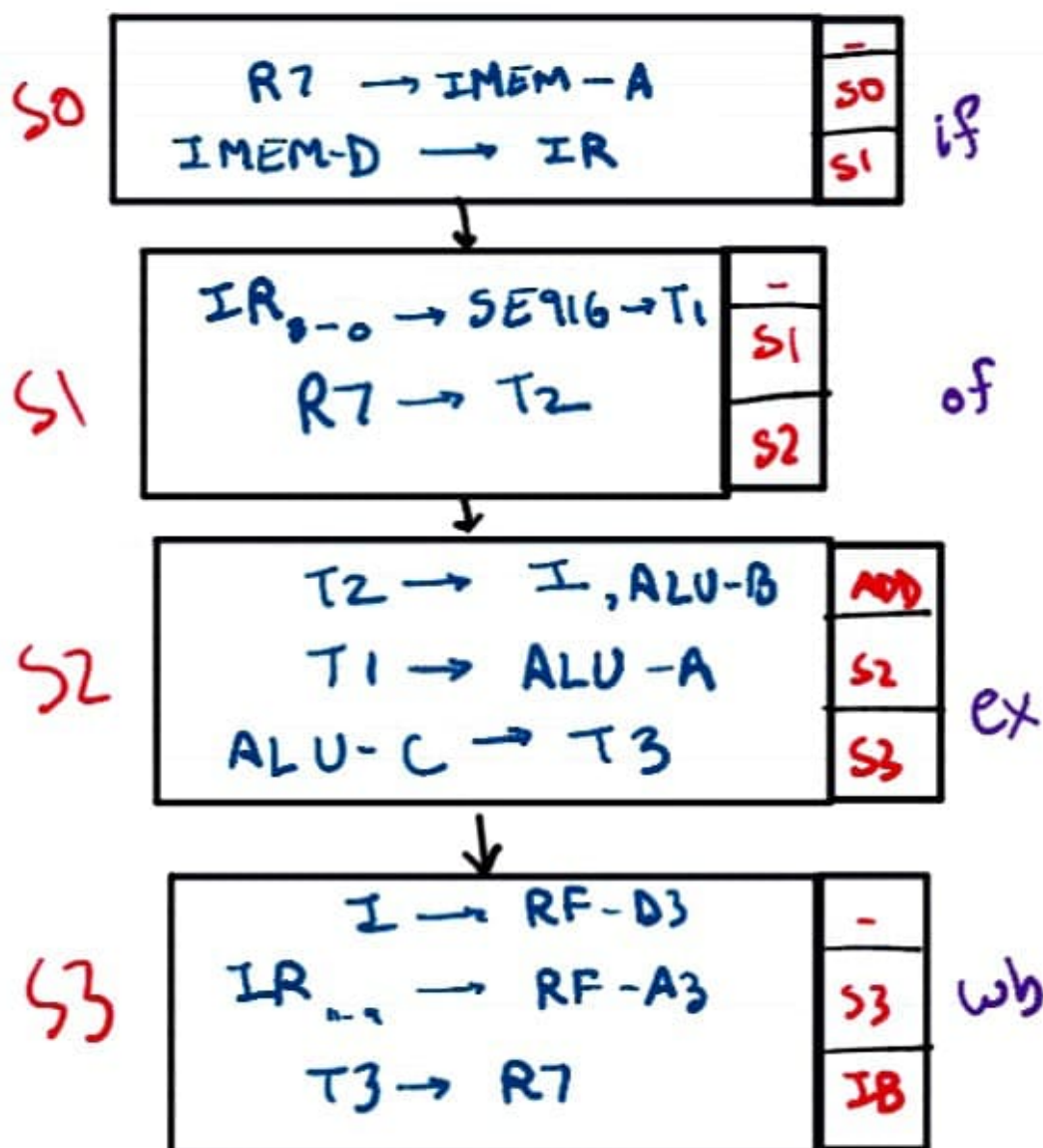
JAL

Sunday, April 10, 2022 11:18 AM



JAL RA Imm9

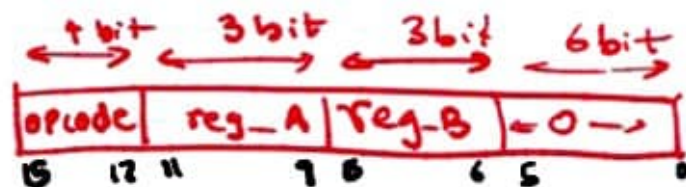
Branch to Imm9+PC &amp; store PC+1 in reg-A.



16)

JLR

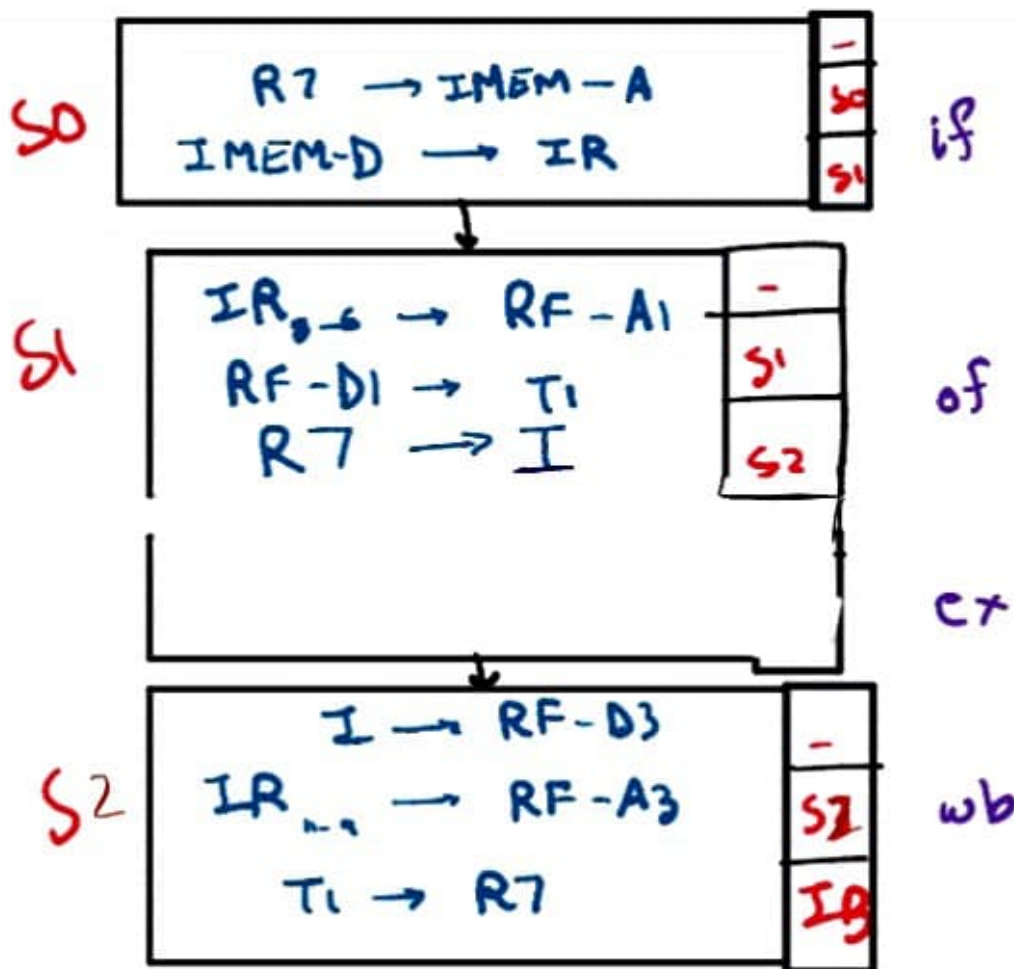
Friday, April 8, 2022 6:35 PM



(J)

JLR RA RB

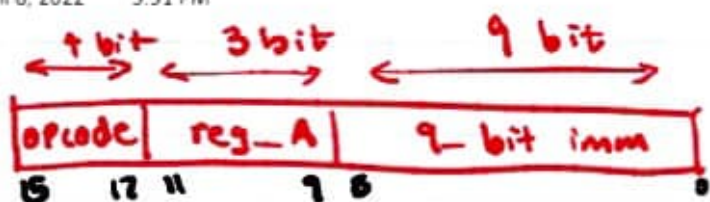
→ Branches to RB, stores PC+1 in RA



17)

JRI

Friday, April 8, 2022 5:51 PM

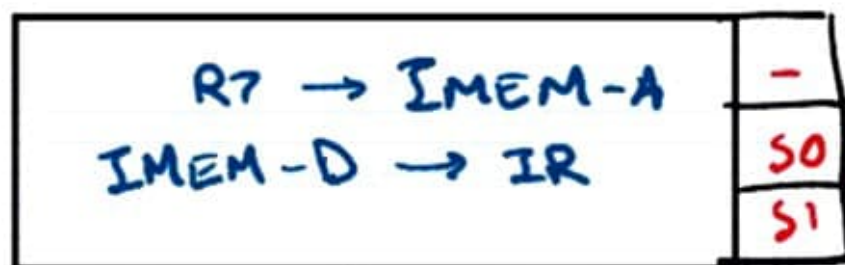


(J)

JRI RA

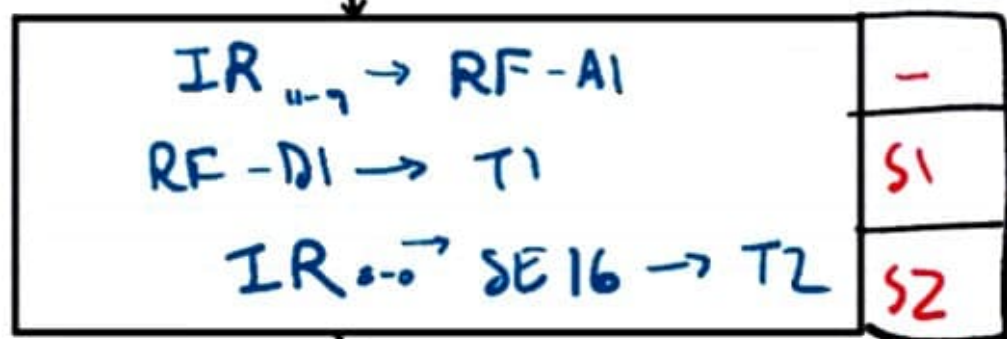
⇒ Branches to memory location pointed by  
RA + Imm 16

S0



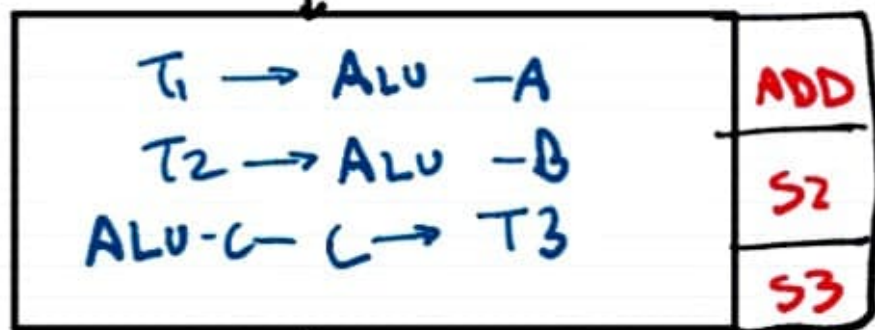
if

S1



of

S2



ex

S3



wb