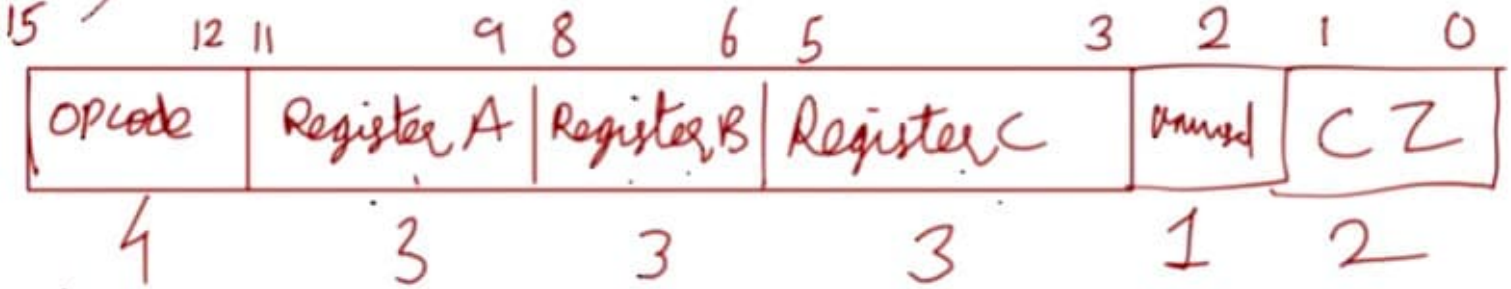
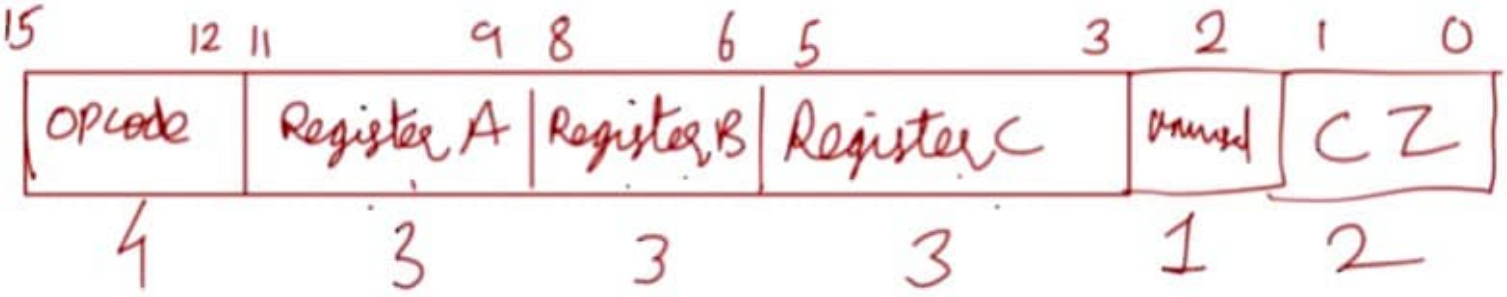
1) ADD - add $c, $a, $b



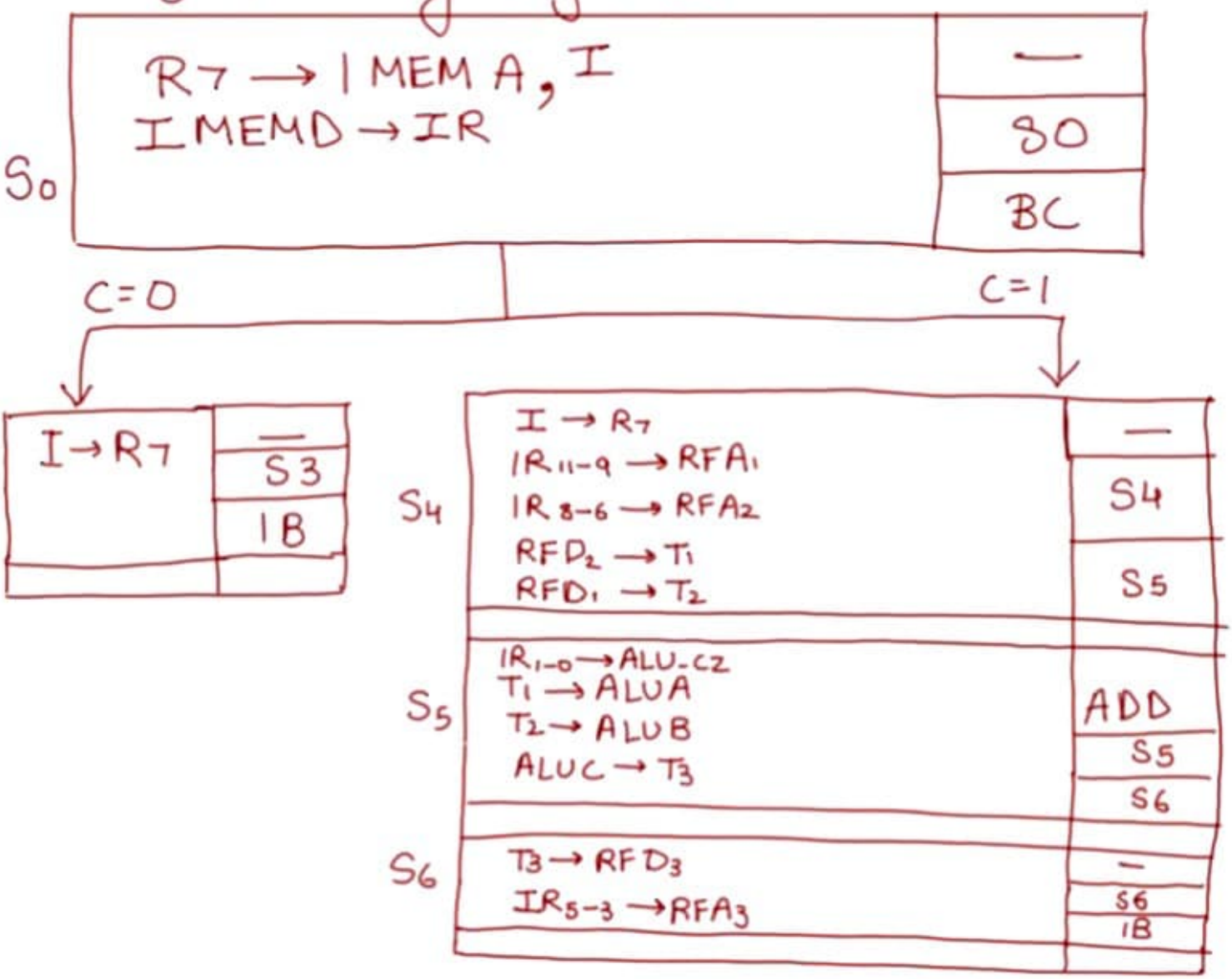
Add content of reg B to reg A and store result in reg C

S_0	$R7 \rightarrow IMEM\ A, I$ $IMEMD \rightarrow IR$	— S_0 S_1
S_1	$I \rightarrow R7$ $IR_{11-9} \rightarrow RFA_1$ $IR_{8-6} \rightarrow RFA_2$ $RFD_2 \rightarrow T_1$ $RFD_1 \rightarrow T_2$	— S_1 S_2
S_2	$IR_{1-0} \rightarrow ALU\_CZ$ $T_1 \rightarrow ALU\ A$ $T_2 \rightarrow ALU\ B$ $ALU\ C \rightarrow T_3$	ADD S_2 S_3
S_3	$T_3 \rightarrow RFD_3$ $IR_{5-3} \rightarrow RFA_3$	— S_3 IB

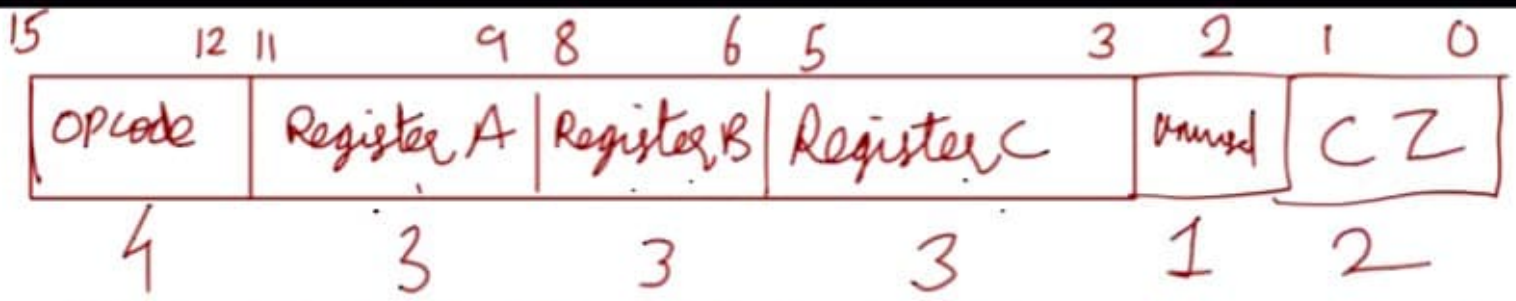
2) ADC - adc rc, ra, rb



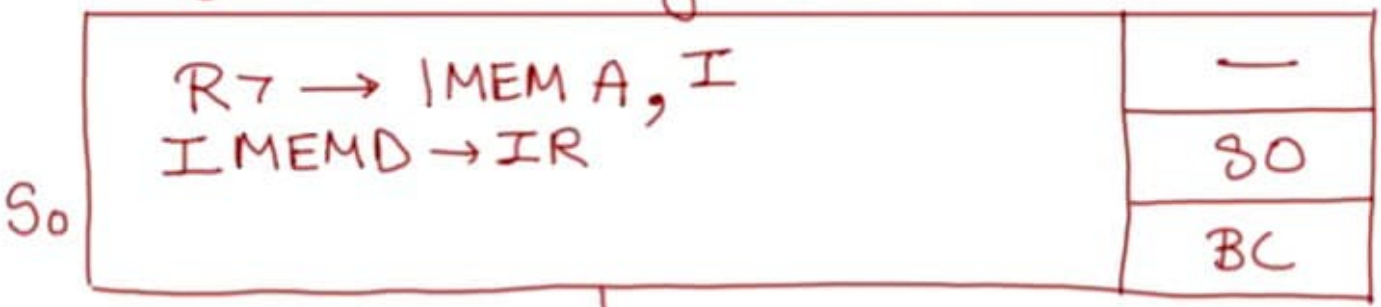
Add content of reg B to reg A and store result in reg C, if carry flag is set



3) ADZ - adz rc, ra, rb

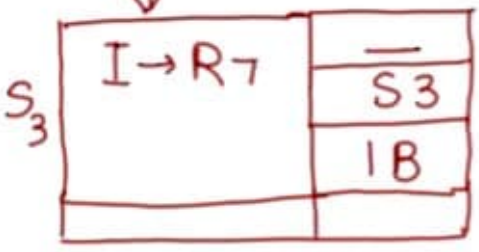


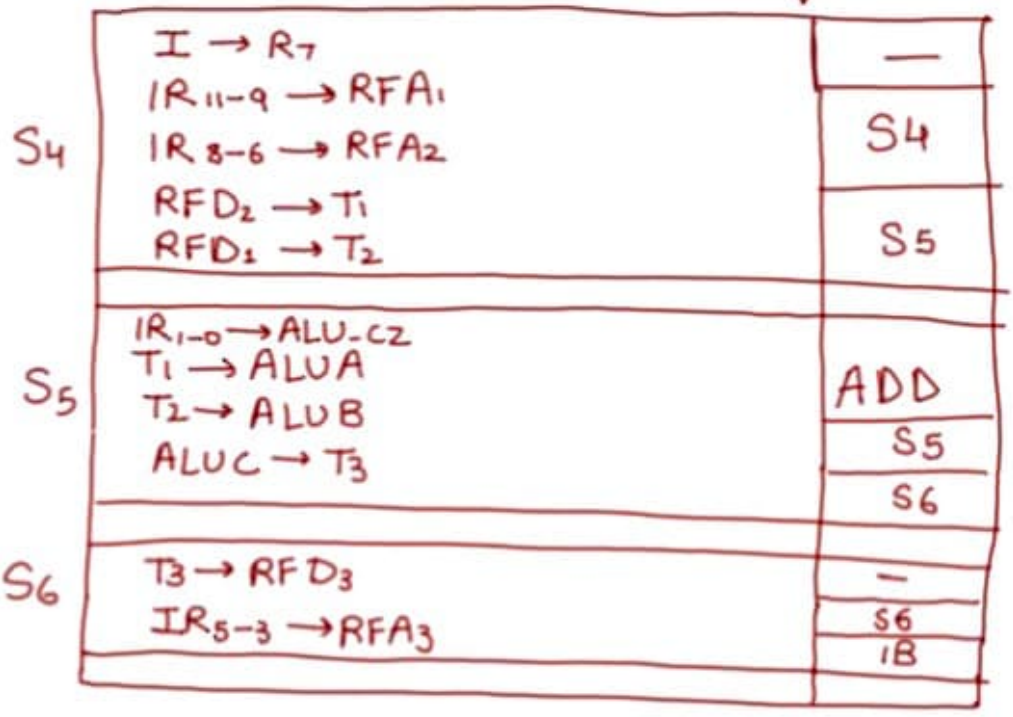
Add content of reg B to reg A and store result in reg C, if zero flag is set.



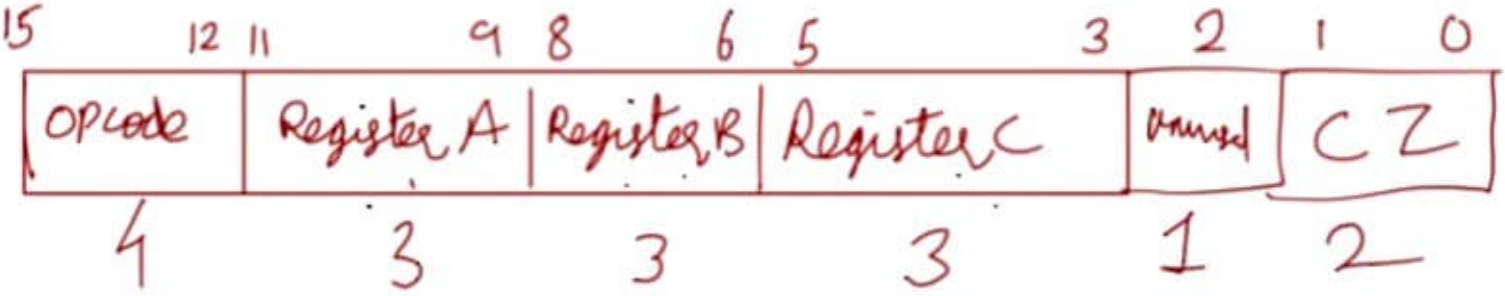
Z = 0

Z = 1





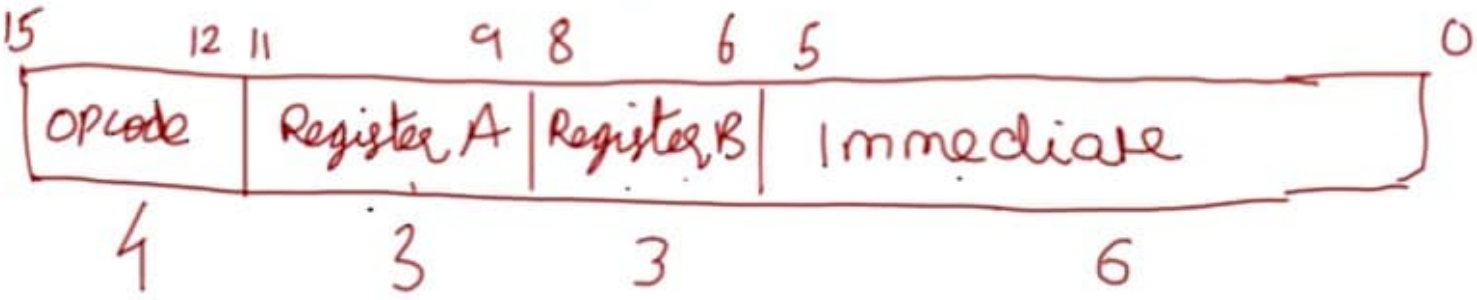
4) ADL - adl rc, ra, rb



Add content of reg B (after one bit left shift) to reg A and store result in reg C

	$R7 \rightarrow IMEM\ A, I$ $IMEMD \rightarrow IR$	— S0 S1
S1	$I \rightarrow R7$ $IR_{11-9} \rightarrow RFA_1$ $IR_{8-6} \rightarrow RFA_2$ $RFD_2 \rightarrow T1$ $RFD_1 \rightarrow LS1 \rightarrow T2$	— S1 S2
S2	$IR_{1-0} \rightarrow ALU\text{-}CZ$ $T1 \rightarrow ALUA$ $T2 \rightarrow ALUB$ $ALUC \rightarrow T3$	ADD S2 S3
S3	$T3 \rightarrow RFD_3$ $IR_{5-3} \rightarrow RFA_3$	— S3 IB

5) ADI - adi rb, ra, imm6

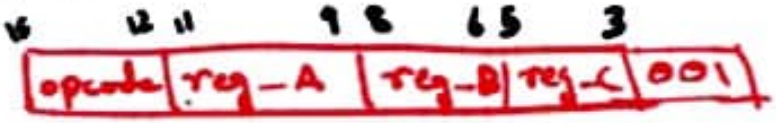


S_0	$R7 \rightarrow IMEMA, I$ $IMEMD \rightarrow IR$	— S0 S1
S_1	$IR_{11-9} \rightarrow RFA1$ $RFD_2 \rightarrow T1$ $IR_{5-0} \rightarrow SE\_6\_16 \rightarrow T2$ $I \rightarrow R7$	— S1 S2
S_2	$T1 \rightarrow ALUA$ $T2 \rightarrow ALUB$ $ALUC \rightarrow T3$	ADD S2 S3
S_3	$IR_{8-6} \rightarrow RFA3$ $T3 \rightarrow RFD3$	— S3 IB

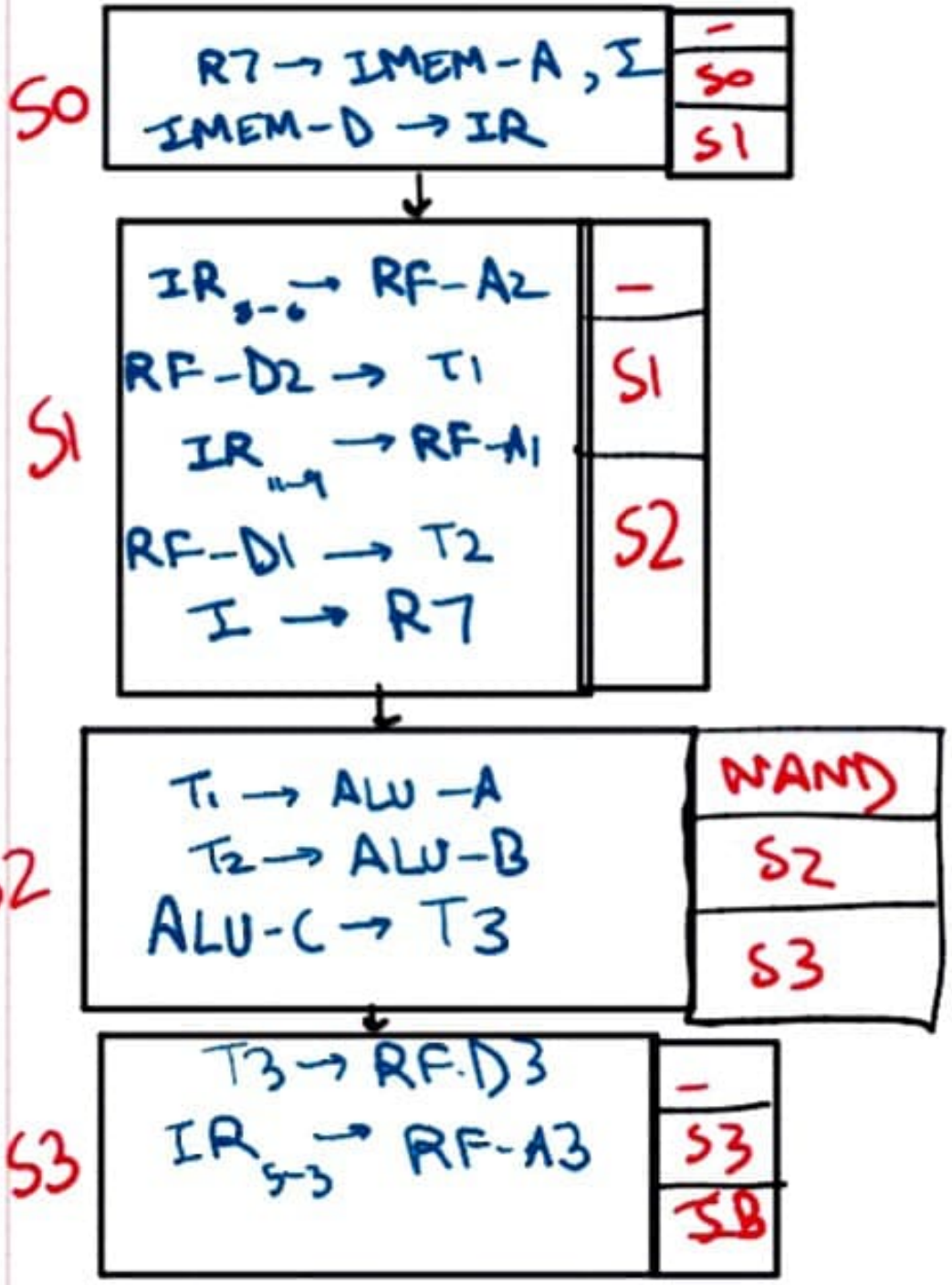
6)

NDU

Sunday, April 10, 2022 12:58 PM



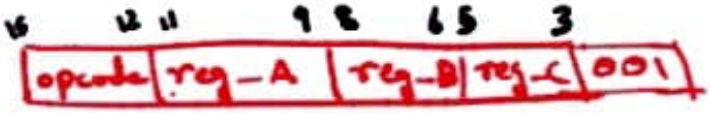
ND2 TA TB TC ⇒ TC ← TA NAND TB



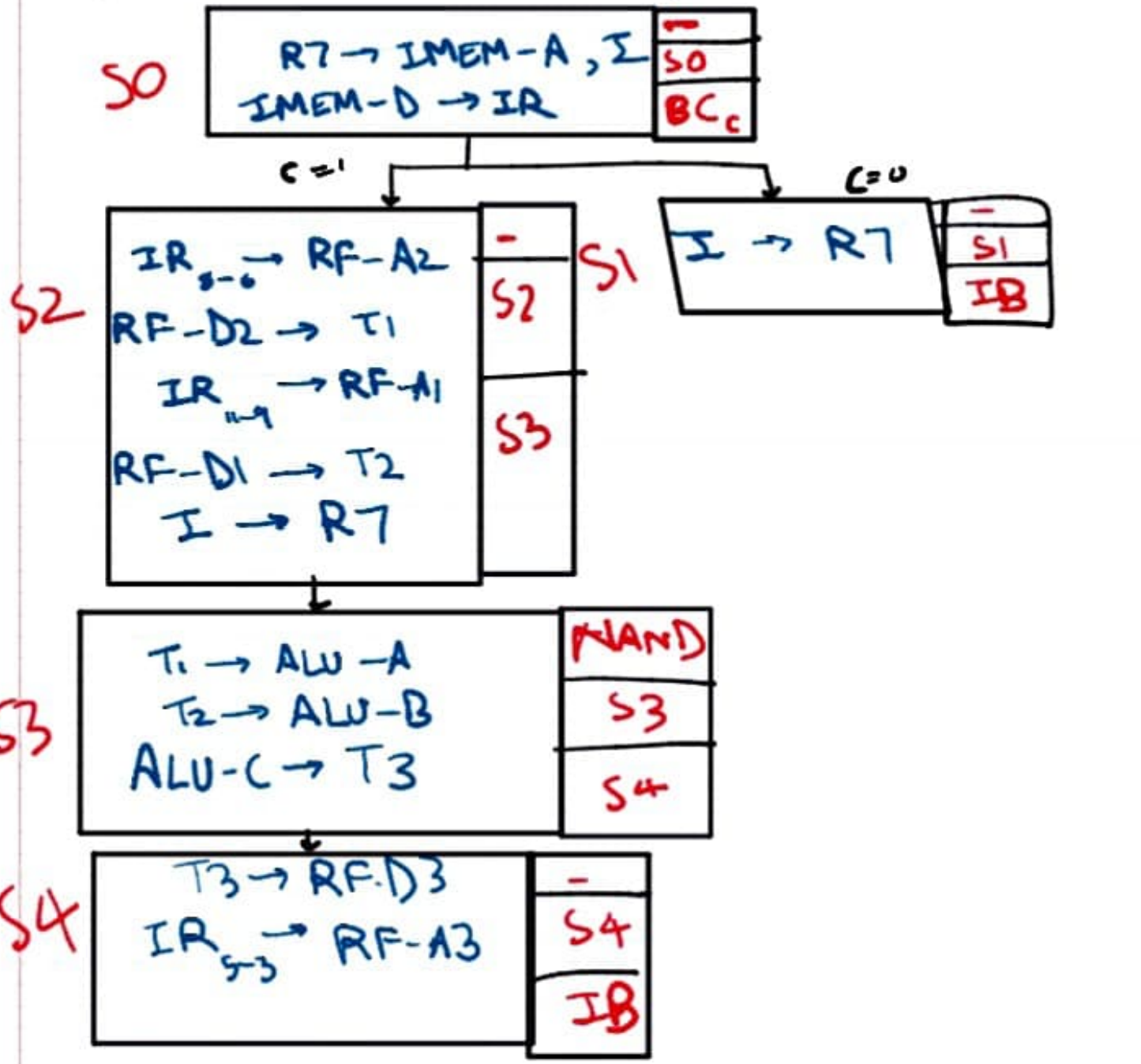
7)

NDC

Sunday, April 10, 2022 12:58 PM

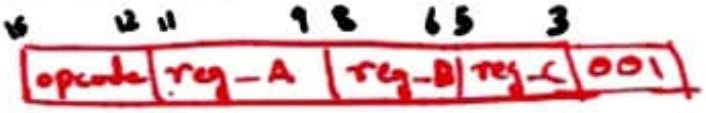


NDC rA rB rC ⇒ if C=1, rC ← rA NAND rB

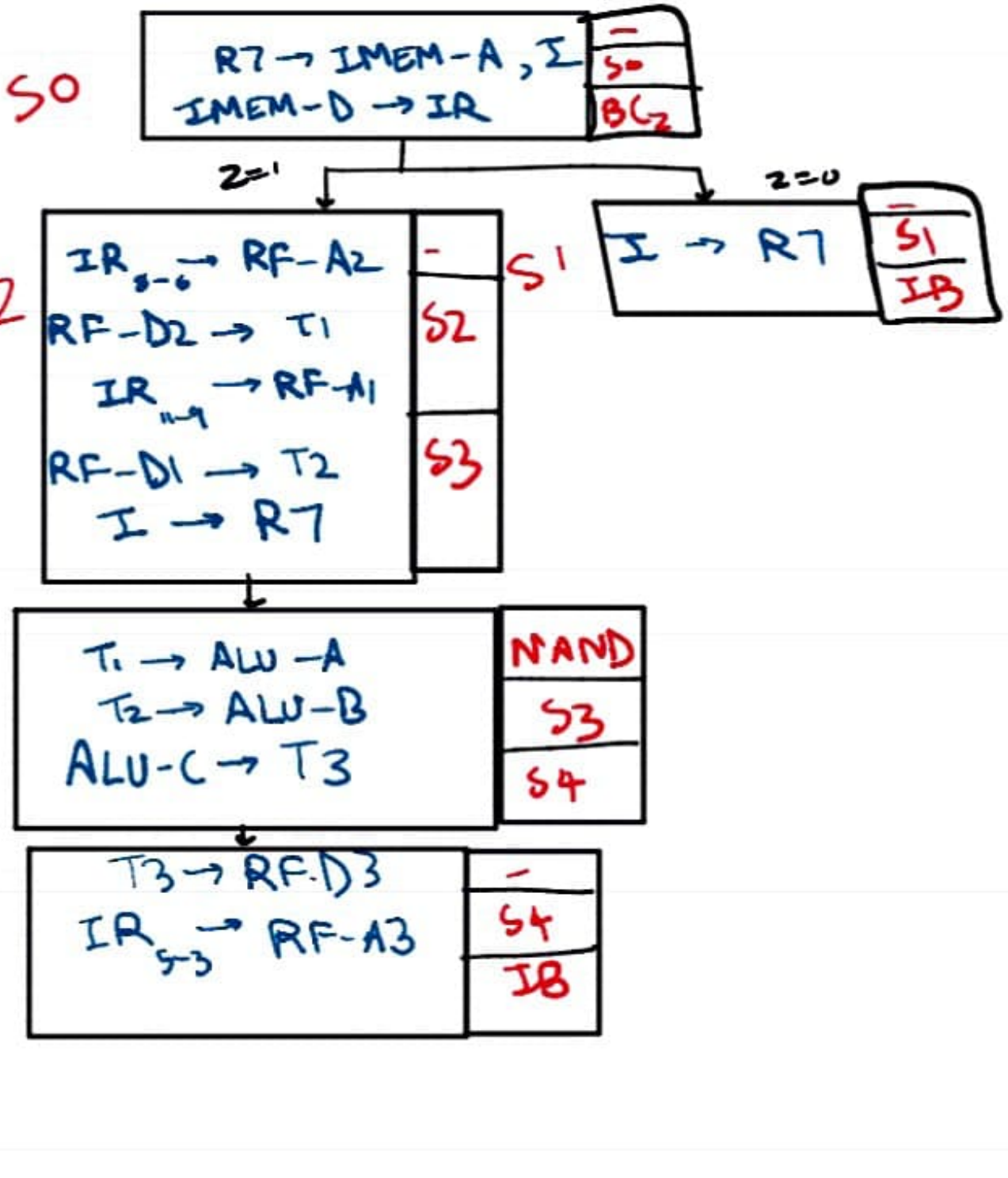


8) NDZ

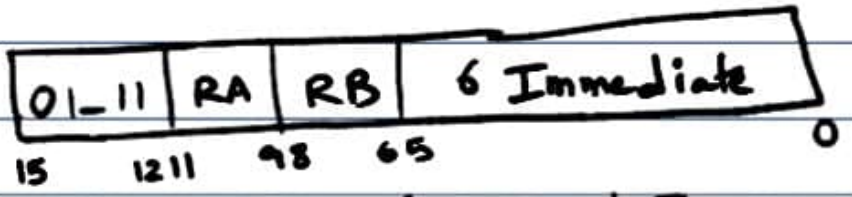
Sunday, April 10, 2022 12:58 PM



NDZ rA rB rC ⇒ if z=1, rC ← rA NAND rB



9) LW:



(I)

load @(rb+imm) in ra

lw ra, rb, Imm

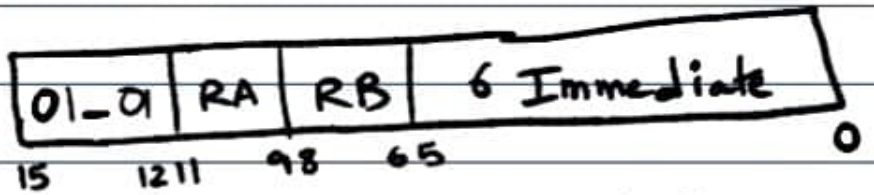
R7 → I, ImemA	–
ImemD → IR	
IR_{8-6} → RF_A1	
RF_D1 → T2	
IR_{5-0} → sx_6_16 → T1	
I → r7	
T1 → aluA	ADD-N
T2 → aluB	
aluC → T3	
T3 → DmemA	–
IR_{11-9} → RF_A3	

LHI

IR_{11-9} → RF_A3	
DmemD → RF_D3	IB

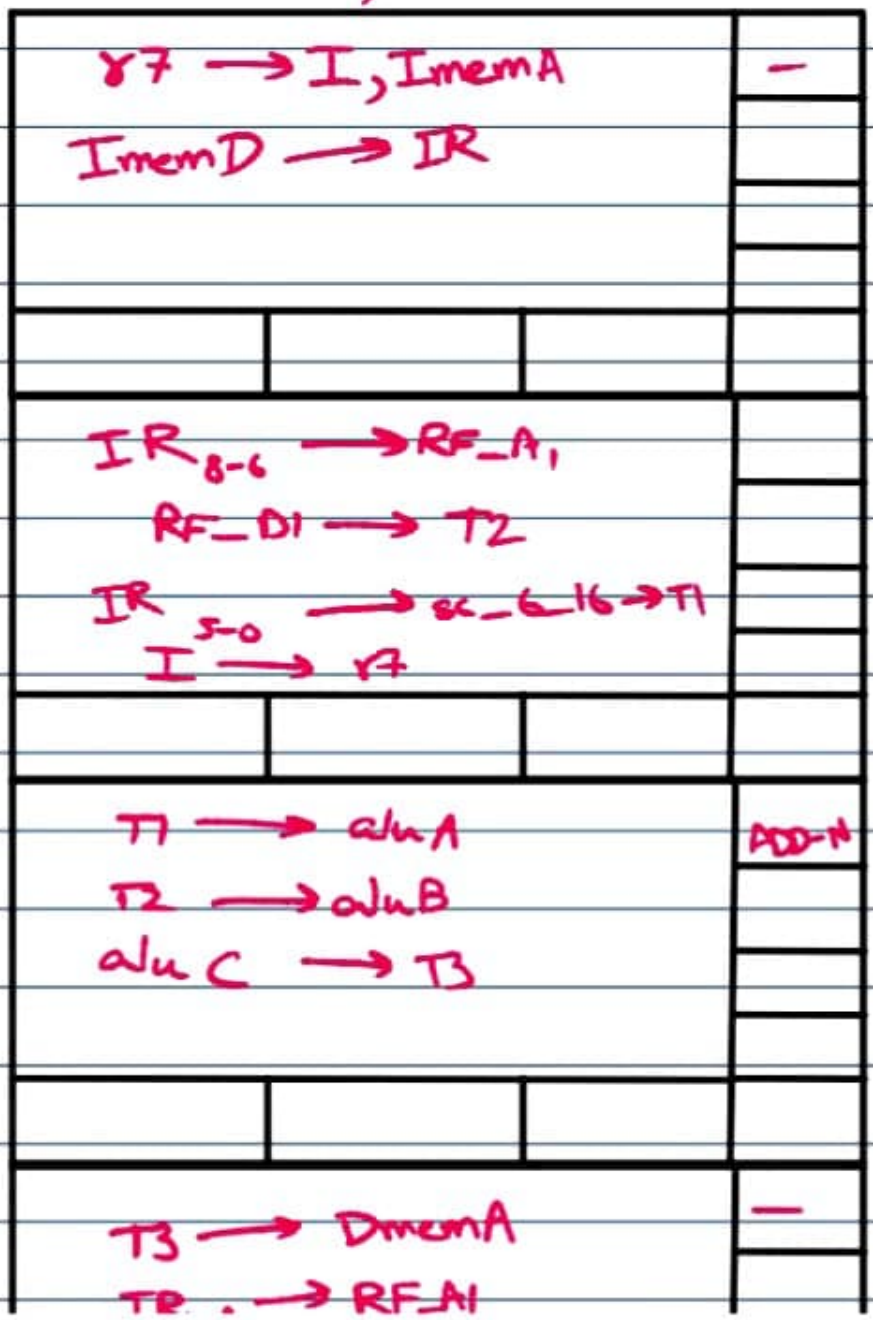
LHI

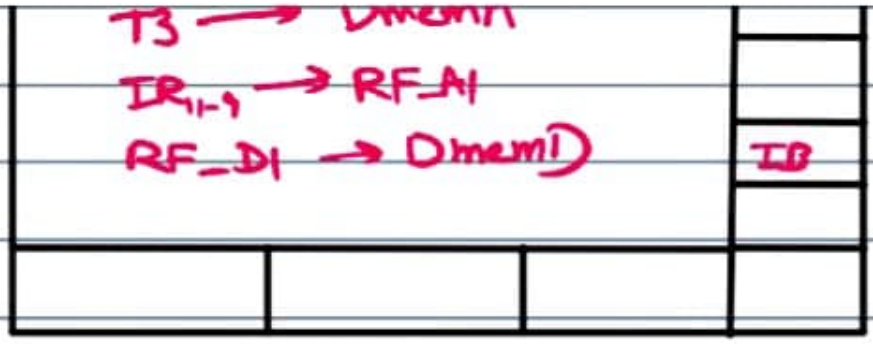
10) SW :



(I)

Store value in ra @ (rb+imm) SW ra, rb, Imm

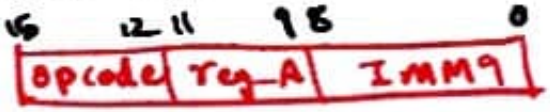




11)

LHI

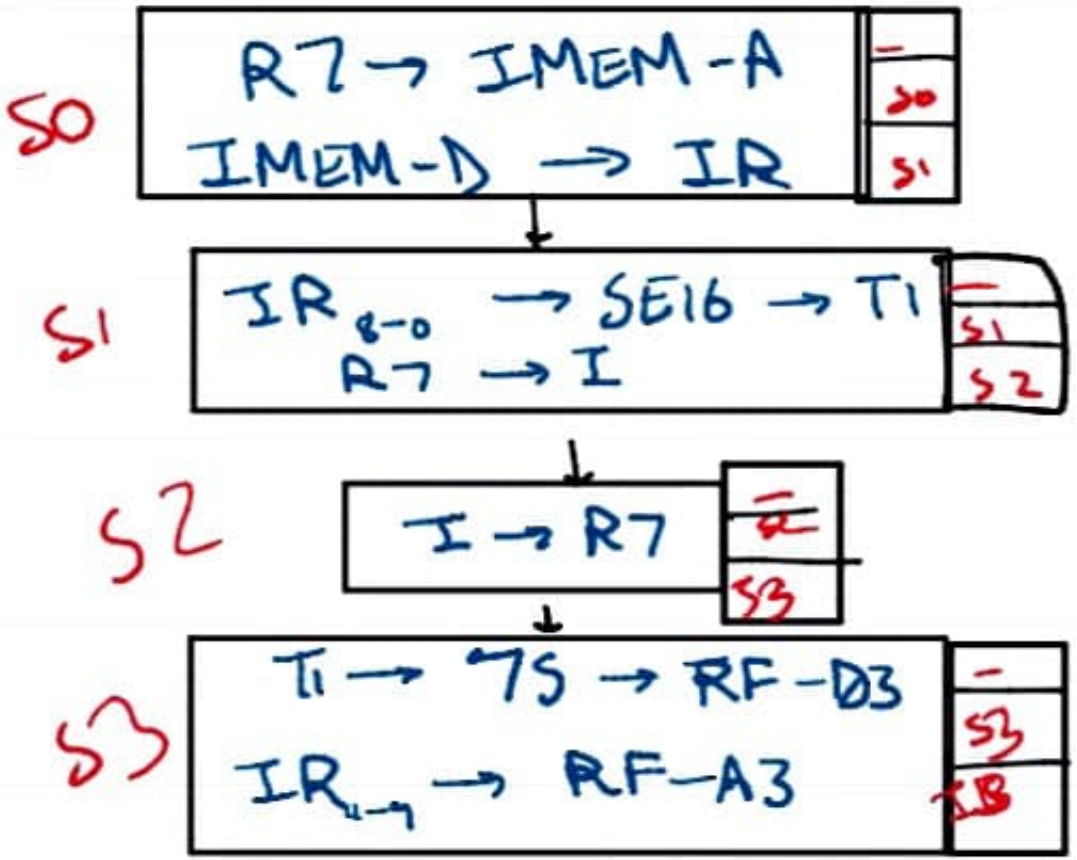
Sunday, April 10, 2022 12:50 PM



LHI reg_A Imm9.

for IMM9 = $b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0$

then reg_A becomes $b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0 0000000$



12)

S0
R7 → IMEM-A
IMEMD → IR

S24
IR_{11-9} → RF-A1
RF-D1 → T1
IR7 → SE16 → T2

S25
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR_{2-0} → BA7 → Dec → RFA1
RF-D1 → Dmem DD

S26
IR_6 → SE16 → T1
T3 → T2

S27
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR_{2-0} → BA6 → Dec → RFA1
RF-D1 → Dmem DD

S28
IR_5 → SE16 → T1
T3 → T2

S29
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR_{2-0} → BA5 → Dec → RFA1
RF-D1 → Dmem DD

S30
IR_4 → SE16 → T1
T3 → T2

S31
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR_{2-0} → BA4 → Dec → RFA1
RF-D1 → Dmem DD

S32
IR3 → SE16 → T1
T3 → T2

S33
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR_{2-0} → BA3 → Dec → RFA1
RF-D1 → Dmem DD

S34
IR2 → SE16 → T1
T3 → T2

S35
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR_{2-0} → BA2 → Dec → RFA1
RF-D1 → Dmem DD

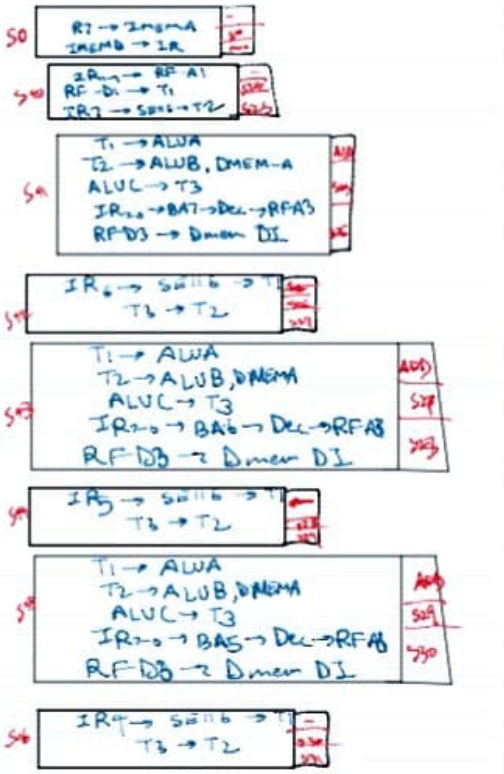
S36
IR1 → SE16 → T1
T3 → T2

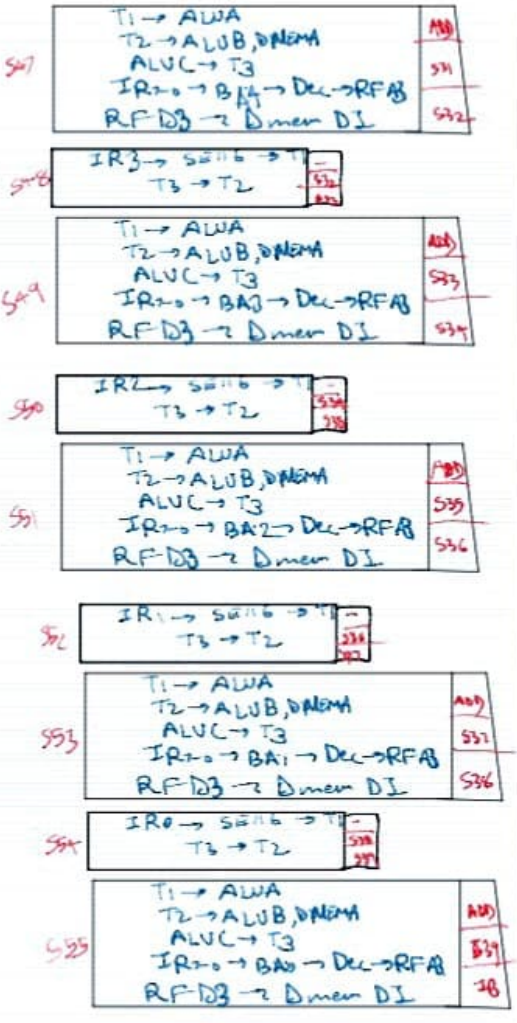
S37
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR_{2-0} → BA1 → Dec → RFA1
RF-D1 → Dmem DD

S38
IR0 → SE16 → T1
T3 → T2

S39
T1 → ALUA
T2 → ALUB, DMEMA
ALUC → T3
IR_{2-0} → BA0 → Dec → RFA1
RF-D1 → Dmem DD

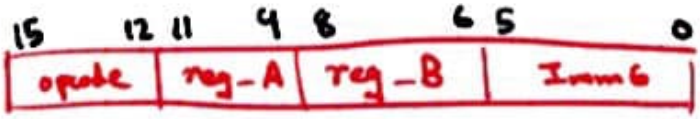
B)


S0
R7 → IMEMA
IMEMB → IR
S1
IR → RF-A1
RF-D1 → T1
IR7 → SE16 → T2
S2
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA7 → Dec → RFA3
RF-D3 → Dmem DI
S3
IR6 → SE16 → T2
T3 → T2
S4
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA6 → Dec → RFA3
RF-D3 → Dmem DI
S5
IR5 → SE16 → T2
T3 → T2
S6
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA5 → Dec → RFA3
RF-D3 → Dmem DI
S7
IR4 → SE16 → T2
T3 → T2


S8
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA4 → Dec → RFA3
RF-D3 → Dmem DI
S9
IR3 → SE16 → T2
T3 → T2
S10
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA3 → Dec → RFA3
RF-D3 → Dmem DI
S11
IR2 → SE16 → T2
T3 → T2
S12
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA2 → Dec → RFA3
RF-D3 → Dmem DI
S13
IR1 → SE16 → T2
T3 → T2
S14
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA1 → Dec → RFA3
RF-D3 → Dmem DI
S15
IR0 → SE16 → T2
T3 → T2
S16
T1 → ALUA
T2 → ALUB, DMEM-A
ALUC → T3
IR10→8 → BA0 → Dec → RFA3
RF-D3 → Dmem DI

14) BEQ

Sunday, April 10, 2022 11:49 AM



BEQ RA RB IMM6

if RA = RB, PC → PC + IMM6

S0

R7 → IMEM-A

IMEM-D → IR

S1

IR_{5-0} → SE6 → T1

R7 → I, T2

S2

I → R7

T1 → ALU-A

T2 → ALU-B

ALU-C → T3

S3

IR_{8-6} → RF-A2

RF-D2 → T1

IR_{11-9} → RF-A1

RF-D1 → T2

Z=1

Z=0

S4

T1 → ALU-A

T2 → ALU-B

ALU-C → T3

S5

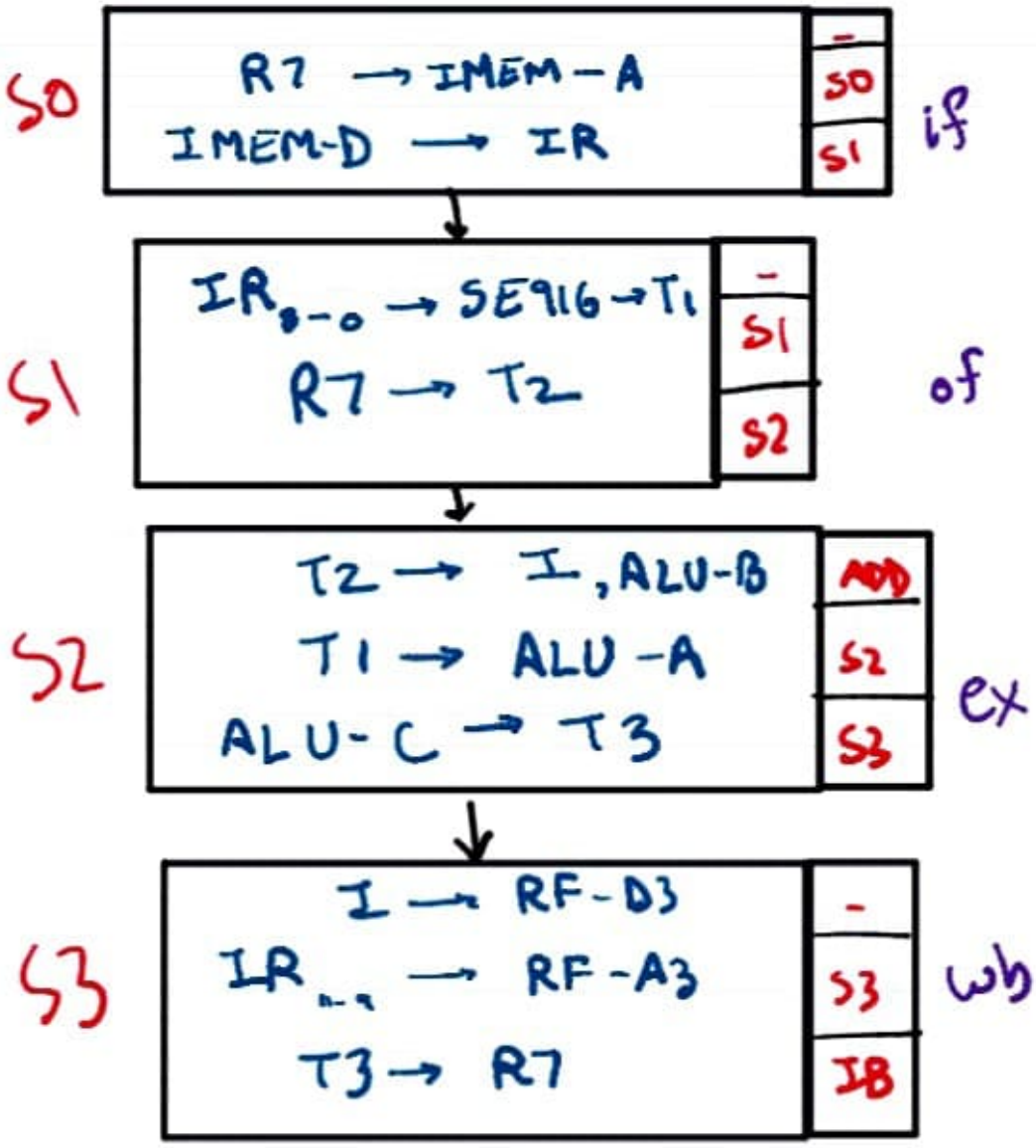
T3 → R7

15) JAL

Sunday, April 10, 2022 11:18 AM

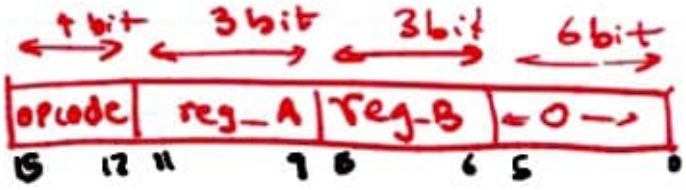
JAL RA Imm9

Branch to Imm9+PC & store PC+1 in reg-A.



16) JLR

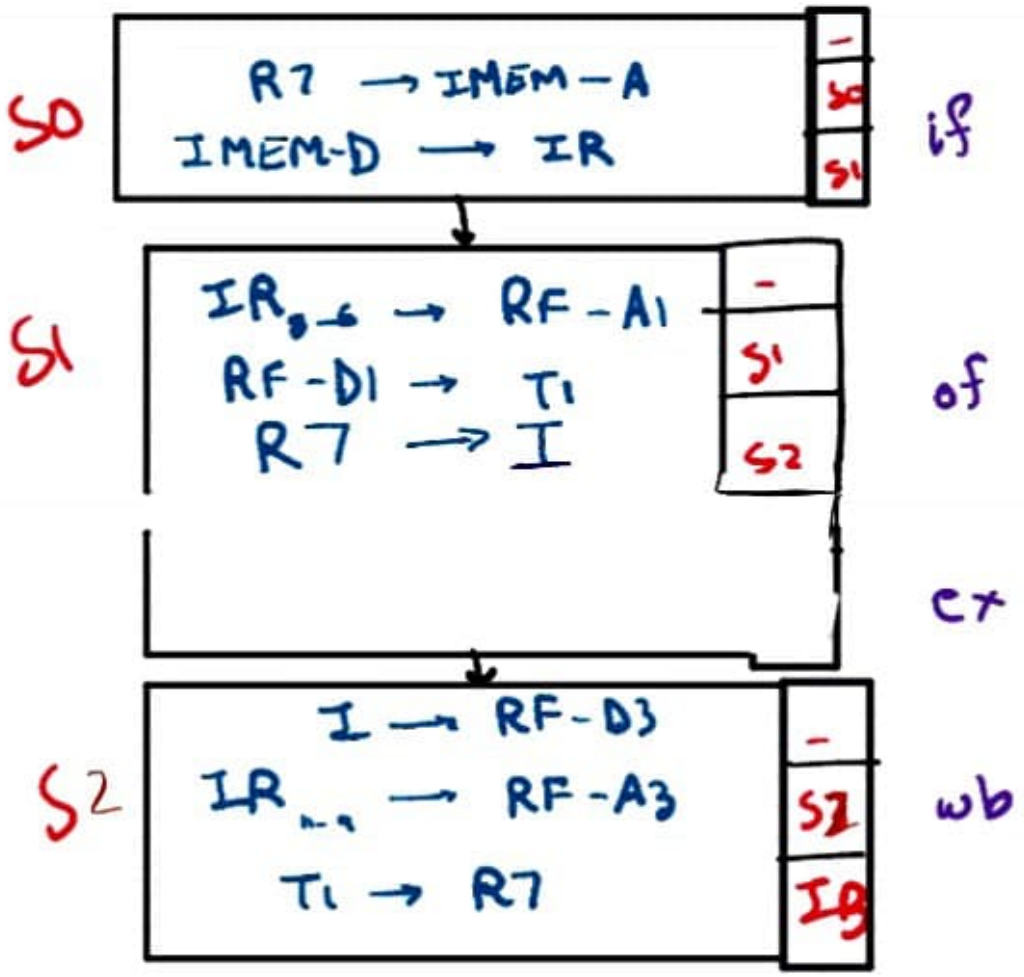
Friday, April 8, 2022 6:35 PM



(J)

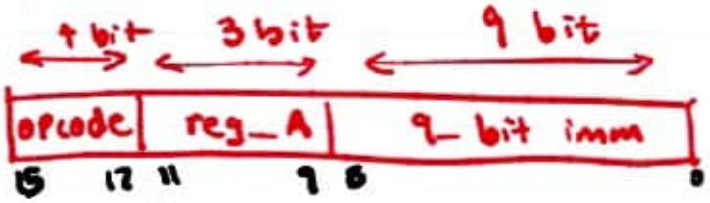
JLR RA RB

⇒ Branches to RB, stores PC+1 in RA



17) JRI

Friday, April 8, 2022 5:51 PM



(J)

JRI RA

⇒ Branches to memory location pointed by RA + Imm16