Project 1

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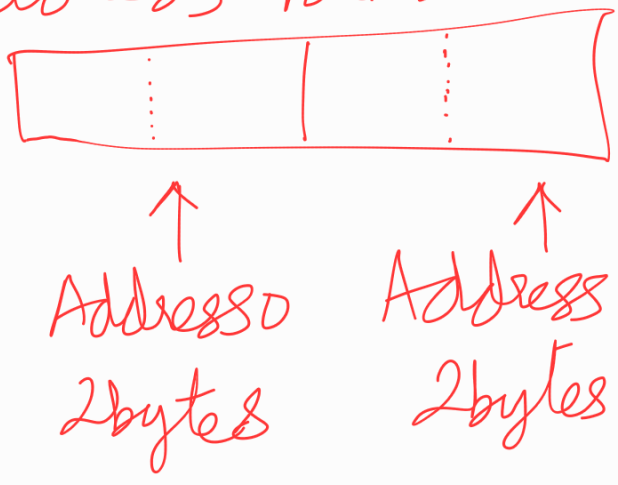
Question Description

Multicycle Processor

8 general purpose registers (R0-R7)

R7 → Always holds PC

Address format

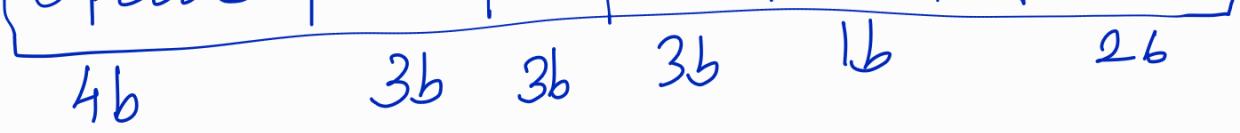


Uses Condition Code Registers [Carry (C) & Zero (Z)]

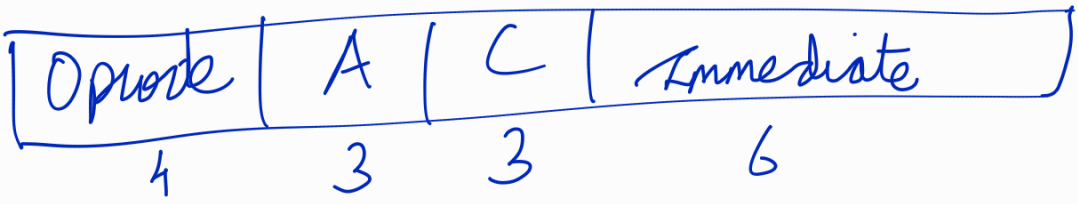
17 Instructions

R Type Instruction format

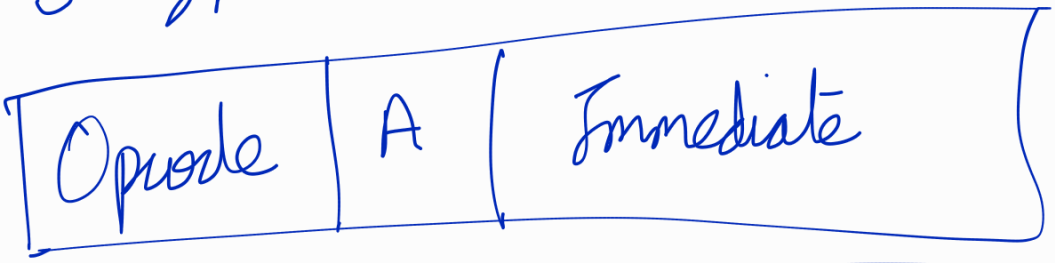
Opcode	A	B	C	Unused	CZ



I Type Instruction format



J type



Things to do:-

(1) Get datapath organization

- component descriptions
- control signals
- State Descriptions

↓

Register
Register file

I'll look into IP core?

ALU

← Memory

Opcode data extraction & memory alignment (Sign extender)

- Draw Final Datapath Org

I want this done in two days.
(Apr 9)

2) VHDL description (Apr 10 -)

- Opcode parser
- Code Storage
- Components individually implemented & tested

- Integration
- Verification

Train split later.