Supported ARMv8 recommended IMPLEMENTATION DEFINED events for the Ampere Computing eMAG core PMU

Event Code	Type	Name	Description
0x00	Software	Increment	Instruction architecturally executed - Software increment
0x01	Cache	Instruction refill	L1 instruction cache refill
0x02	Cache	Inst TLB refill	L1 instruction TLB refill
0x03	Cache	Data refill	L1 data cache refill
0x04	Cache	Data access	L1 data cache access
0x05	Cache	Data TLB refill	L1 data TLB refill
0x08	Instruction	Executed	Instruction architecturally executed
0x09	Exception	Taken	Exception taken
0x0a	Exception	Return	Instruction architecturally executed, condition code check pass, exception return
0x0b	Instruction	CONTEXTIDR	Instruction architecturally executed, condition code check pass, write to CONTEXTIDR
0x10	Branch	Mispredicted	Mispredicted or not predicted branch speculatively executed
0x11	Clock	Clock	Cycles
0x12	Branch	Potential prediction	Predictable branch speculatively executed
0x13	Memory	Memory access	Data memory access
0x14	Cache	L1 inst access	L1 instruction cache access
0x16	Cache	L2 data access	L2 data cache access
0x17	Cache	L2 data refill	L2 data cache refill
0x18	Cache	L2 data write	L2 data cache Write-Back
0x19	Bus	Access	Bus access
0x1a	Memory	Memory Error	Local memory error. This event counts any correctable or uncorrectable memory error (ECC or parity) in the protected core RAMs.
0x1b	Instruction	Speculative	Operation speculatively executed
0x1c	Instruction	Writes to TTBR	Instruction architecturally executed (condition check pass) - Write to TTBR
0x1e	Counter chain	Odd Performance	For odd-numbered counters, increments the count by one for each overflow of the preceding even-numbered counter. For even-numbered counters there is no increment.
0x21	Instruction	Branch Retried	Instruction architecturally executed, branch. This event counts all branches, taken or not. This excludes exception entries, debug entries and CCFAIL branches.
0x22	Instruction	Branch mispredicted retried	Instruction architecturally executed, mispredicted branch. The event counts any branch counted by BR_RETIRED which is not correctly predicted and causes a pipeline flush.
0x25	Cache	Level 1 data TLB access	This event counts any load or store operation which accesses the data L1 TLB.
0x26	Cache	Level 1 instruction TLB access	his event counts any instruction fetch which accesses the instruction L1 TLB.
0x34	Cache	Access data TLB	Access to data TLB that caused a page table walk. This event counts on any data access which causes L2D_TLB_REFILL to count.
0x35	Cache	Access to instruction TLB	Access to instruction TLB that caused a page table walk. This event counts on any instruction access which causes L2D_TLB_REFILL to count.
0x40	Cache	L1 data access read	L1 data cache access, read
0x41	Cache	L1 data access write	L1 data cache access, write
0x42	Cache	L1 data refill read	L1 data cache refill, read.
0x48	Cache	L1 data invalidate	L1 data cache invalidate.
0x4c	Cache	L1 data TLB refill read	L1 data TLB refill, read.
0x4d	Cache	L1 data TLB refill write	L1 data TLB refill, write
0x50	Cache	L2 data access read	L2 data cache access, read
0x51	Cache	L2 data access write	L2 data cache access, write
0x52	Cache	L2 data refill read	L2 data cache refill, read
0x53	Cache	L2 data refill write	L2 data cache refill, write
0x56	Cache	L2 data victim (wb)	L2 data cache write-back, victim
0x57	Cache	L2 data clean	L2 data cache write-back, cleaning and coherency
0x58	Cache	L2 data invalidate	L2 data cache invalidate
0x60	Bus	Bus access read	The event counts for every beat of data transferred over the read data channel between the core and the SCU.
0x61	Bus	Bus access write	The event counts for every beat of data transferred over the write data channel between the core and the SCU.
0x62	Bus	Access shared	Bus access, Normal, Cacheable, Shareable

0x63	Bus	Access not shared	Bus access, not Normal, Cacheable, or Shareable
0x64	Bus	Access normal	Bus access, Normal
0x65	Bus	Peripheral	Bus access, Device
0x66	Memory	Read	Data memory access, read
0x67	Memory	Write	Data memory access, write
0x68	Memory	Read access	Unaligned access, read
0x69	Memory	Write access	Unaligned access, write
0x6a	Memory	Unaligned	Unaligned access
0x6c	Intrinsic	LDREX	Exclusive operation speculatively executed, LDREX, or LDX
0x6d	Intrinsic	STREX pass	Exclusive operation speculatively executed, STREX or STX pass.
0x6e	Intrinsic	STREX fail	Exclusive operation speculatively executed, STREX, or STX fail
0x6f	Intrinsic	STREX	Exclusive operation speculatively executed, STREX or STX.
0x70	Instruction	Load	Operation speculatively executed, load
0x71	Instruction	Store	Operation speculatively executed, store
0x72	Instruction	Load/Store	Operation speculatively executed, load or store
0x73	Instruction	Integer	Operation speculatively executed, integer data processing
0x74	Instruction	Advanced SIMD	Operation speculatively executed, Advanced SIMD instruction
0x75	Instruction	VFP	Operation speculatively executed, floating-point instruction
0x76	Instruction	PC write	Operation speculatively executed, software change of the PC.
0x77	Instruction	Crypto	Operation speculatively executed, Cryptographic instruction
0x78	Branch	Immediate branch	Branch speculatively executed, immediate branch.
0x79	Branch	Procedure return	Branch speculatively executed, procedure return.
0x7a	Branch	Indirect	Branch speculatively executed - Indirect branch
0x7c	Instruction	ISB	Barrier speculatively executed, ISB
0x7d	Instruction	DSB	Barrier speculatively executed, DSB
0x7e	Instruction	DMB	Barrier speculatively executed, DMB
0x81	Exception	Undefined exception count	Counts the number of undefined exceptions taken locally.
0x82	Exception	Supervisor Call	Exception taken locally, Supervisor Call.
0x83	Exception	Instruction Abort	Exception taken locally, Instruction Abort.
0x84	Exception	Data abort	Exception taken locally, Data Abort and SError.
0x86	Exception	IRQ	Exception taken locally, IRQ.
0x87	Exception	FIQ	Exception taken locally, FIQ
0x8a	Exception	Hypervisor call	Exception taken locally, Hypervisor Call.
0x8b	Exception	Instruction Abort not taken locally	Exception taken, Instruction Abort not taken locally.
0x8c	Exception	Data Abort not taken locally	Exception taken, Data Abort or SError not taken locally.
0x8d	Exception	Other traps not taken locally	Exception taken, Other traps not taken locally.
0x8e	Exception	IRQ not taken locally	Exception taken, IRQ not taken locally.
0x8f	Exception	FIQ not taken locally	Exception taken, FIQ not taken locally.
0x90	Instruction	Release operation executed	Release consistency operation speculatively executed, load-acquire
0x91	Instruction	Release operation executed	Release consistency operation speculatively executed, store-release.
0x101	Clock	FSU clocking gated off cycle	FSU clocking gated off cycle
0x102	Branch	BTB misprediction	BTB misprediction
0x103	Cache	ITB miss	ITB miss
0x104	Cache	DTB miss	DTB miss
0x105	Cache	L1 data cache late miss	L1 data cache late miss
0x106	Cache	L1 data cache prefetch request	L1 data cache prefetch request
0x107	Cache	L2 data prefetch request	L2 data prefetch request
0x108	Instruction	Decode starved for instruction cycle	Decode starved for instruction cycle
0x109	Instruction	Op dispatch stalled cycle	Op dispatch stalled cycle
0x10A	Instruction	IXA Op non-issue	IXA Op non-issue
0x10B	Instruction	IXB Op non-issue	IXB Op non-issue
0x10C	Instruction	BX Op non-issue	BX Op non-issue
0x10D	Instruction	LX Op non-issue	LX Op non-issue
0x10E	Instruction	SX Op non-issue	SX Op non-issue
0x10F	Instruction	FX Op non-issue	FX Op non-issue
0x110	Instruction	Wait state cycle	Wait state cycle
0x111	Cache	L1 stage-2 TLB refill	L1 stage-2 TLB refill
0x112	Cache	Page Walk Cache level-0 stage-1 hit	Page Walk Cache level-0 stage-1 hit
0x113	Cache	Page Walk Cache level-1 stage-1 hit	Page Walk Cache level-1 stage-1 hit
0x114	Cache	Page Walk Cache level-2 stage-1 hit	Page Walk Cache level-2 stage-1 hit
0x115	Cache	Page Walk Cache level-1 stage-2 hit	Page Walk Cache level-1 stage-2 hit
0x116	Cache	Page Walk Cache level-2 stage-2 hit	Page Walk Cache level-2 stage-2 hit