Logic Design Final Project：

In search of the maximum value from number sequences

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Key Summary

First, I created a functional unit that performs mathematical or logical operations on two input signal sequences and outputs the results. This functional unit can perform eight different operations, and the schematic diagram and instruction table are shown below.

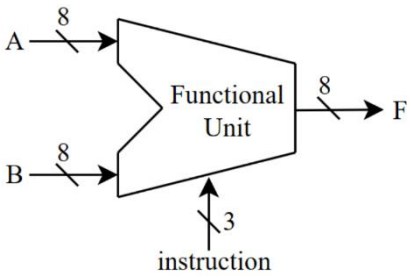

Fig. 1. The Functional

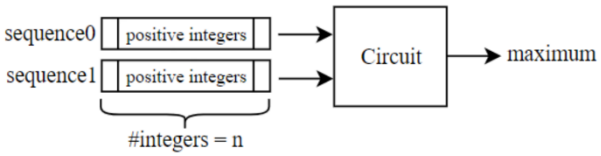

Fig. 2. Problem Formulation

Table 1. Functional Table

Function	Instruction	Operation (unsigned)
Arithmetic	3’b000	F = A + B
Arithmetic	3’b001	F = A + ~B
Logic	3’b010	F = A and B
Logic	3’b011	F = A or B
Logic	3’b100	F = A xor B
Shifter, Arithmetic	3’b101	F = (shift-right A by 1 bit) + B
Rotate, Arithmetic	3’b110	F = (right-rotate A by 1 bit) + B
Rotate, Arithmetic	3’b111	F = (left-rotate A by 1 bit) + B

With the basic functional unit in place, the next step is to design the circuit. The simplified diagram of the problem can be condensed into Fig. 2. The purpose is to find the maximum value in the signal sequence. Therefore, I designed the circuit based on a synchronous circuit with a positive-edge-triggered clock. The sequence that is continuously input, after being output from the function unit, is compared to the value stored in the output FF. If the newly generated value is larger, the value of the output FF is updated. Otherwise, it remains unchanged. The circuit schematic is shown in Fig. 3. The state diagram of the FSM that controls the overall operation of the circuit is shown in Fig. 4.

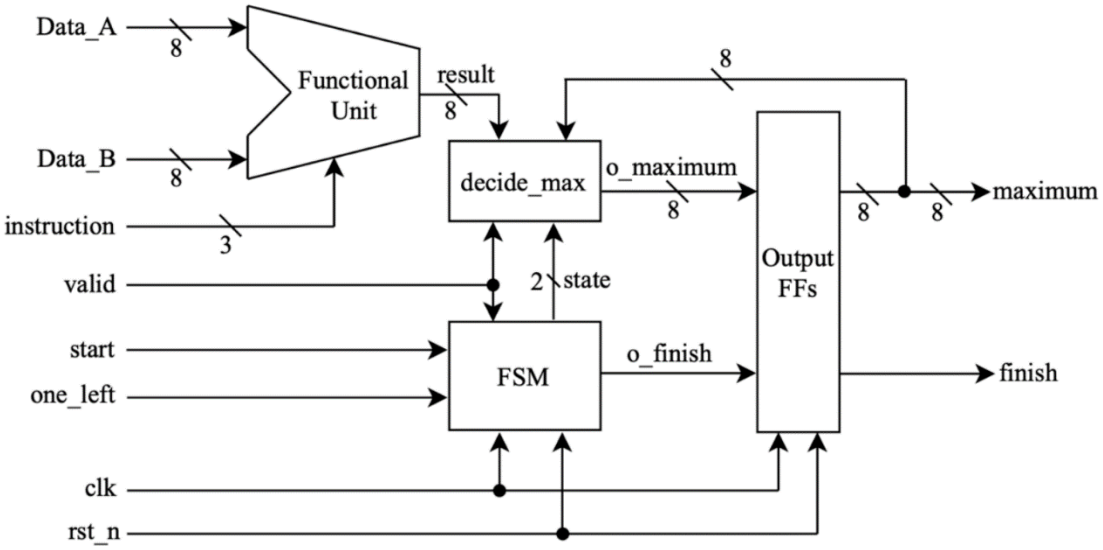

Fig. 3. The circuit structure

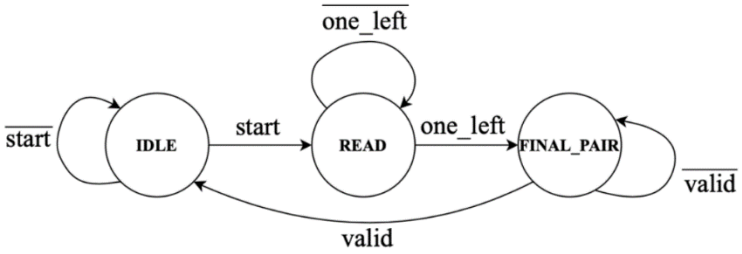

Fig. 4. State diagram of FSM

FSM State description:

IDLE: The circuit does not do anything and stay still.

READ: Read the pairs of the integers until there remains one pair of the integers to be read/computed.

FINAL_PAIR: Read the final pair of the integers.

The relevant I/O signals are presented in Table 2. This project is designed in Verilog.

Table 2. I/O description

Signal Name	Width	I/O	Description
clk	1	I	Clock (positive-edge-triggered clock)
rst_n	1	I	Active-low reset (synchronous reset)
start	1	I	Single-cycle active-high pulse. After this signal becomes 1, it means the circuit can start reading the integers and doing the computation.
valid	1	I	Only when this signal is 1, the input data are valid to be computed; otherwise, it is invalid input data, which you cannot use.
Data_A	8	I	A positive integer read from sequence0.
Data_B	8	I	A positive integer read from sequence1.
one_left	1	I	Single-cycle active-high pulse. This signal indicates one pair of integers is left to be read/computed.
instruction	3	I	3-bit instruction. The functional table is shown as Table 1.
maximum	8	O	The maximum among the results of the operations on several pairs of integers.
finish	1	O	Single-cycle active-high pulse. This signal is used to inform the testbench to examine your output results. It should be pulled high in the same cycle when the maximum is ready.