Faculty Of Engineering and Technology

Electrical and Computer Engineering Department

ENCS3330, Digital Integrated Circuits

Assignment #2

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Section: 2

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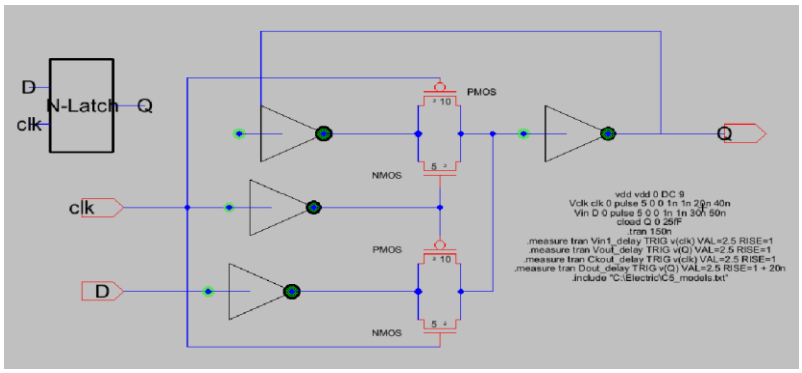
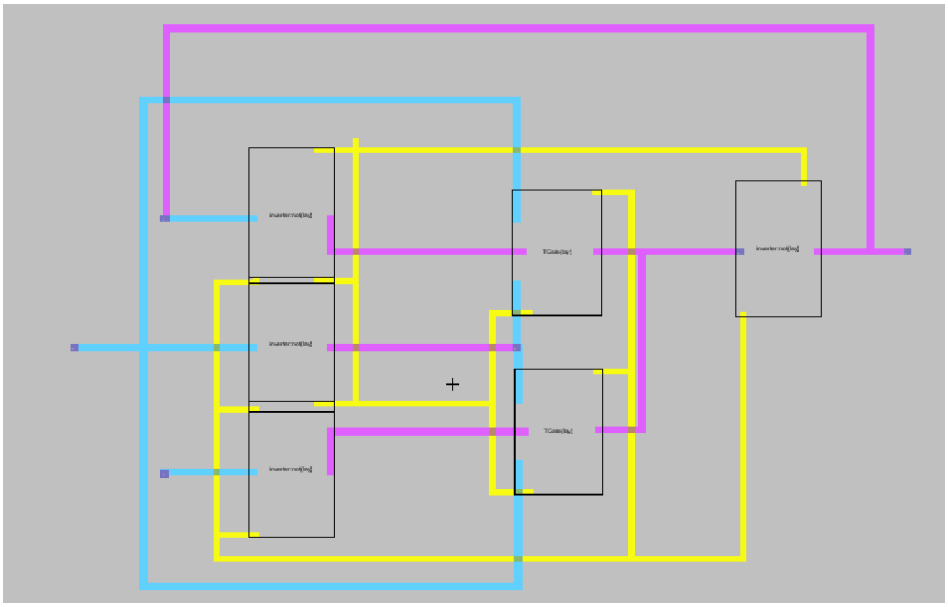


Figure 1: N-Latch Schematic.



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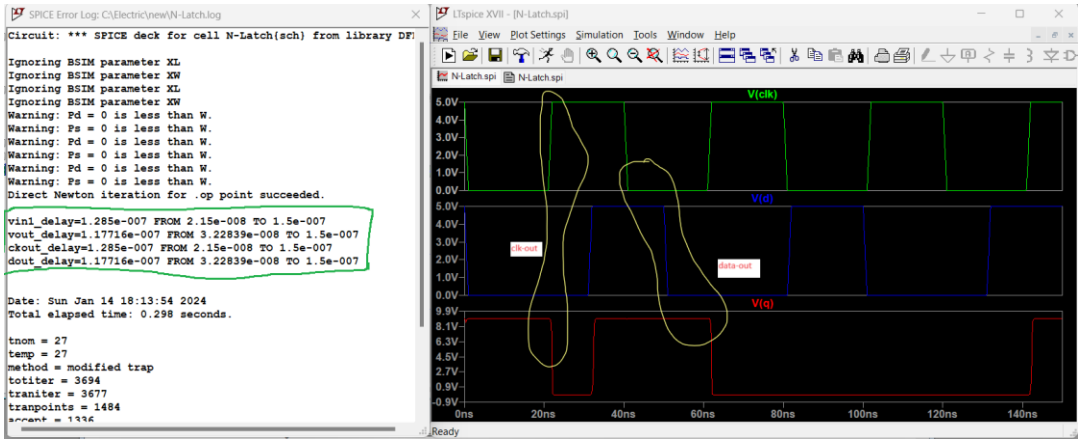

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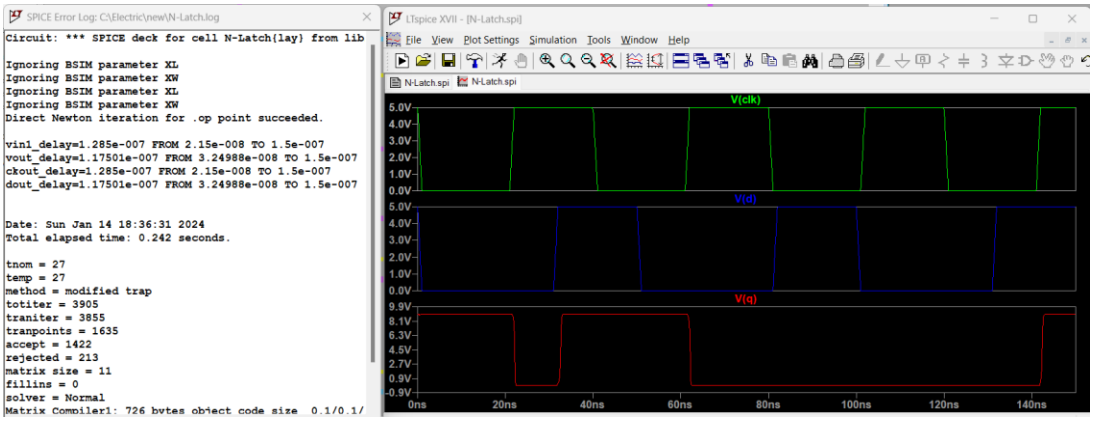
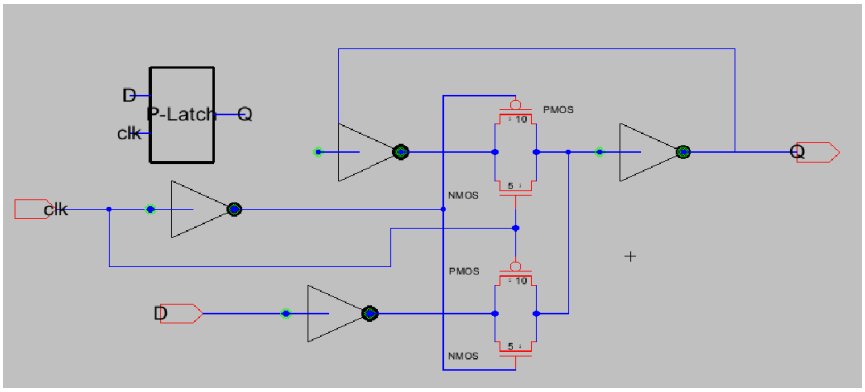


Figure 4: N-Latch Layout - Simulation.

2. P-Latch Schematic, Layout and Simulation.



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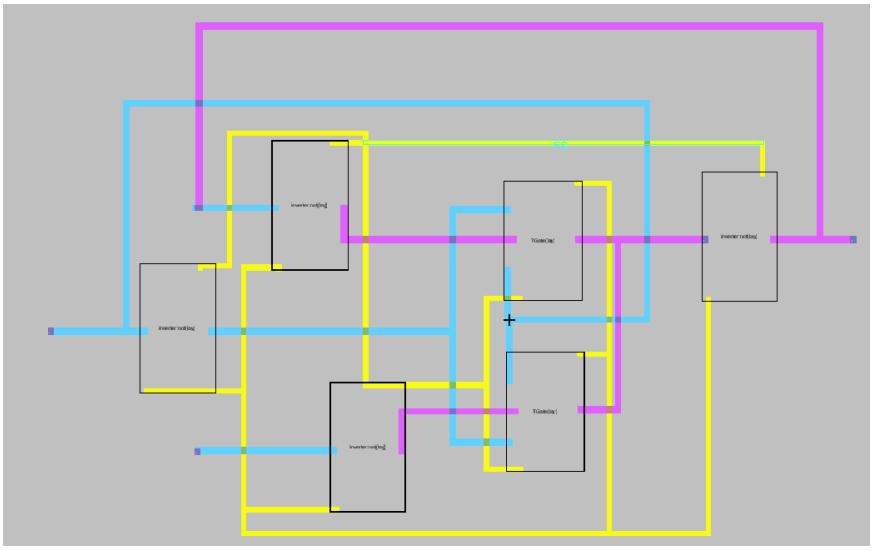

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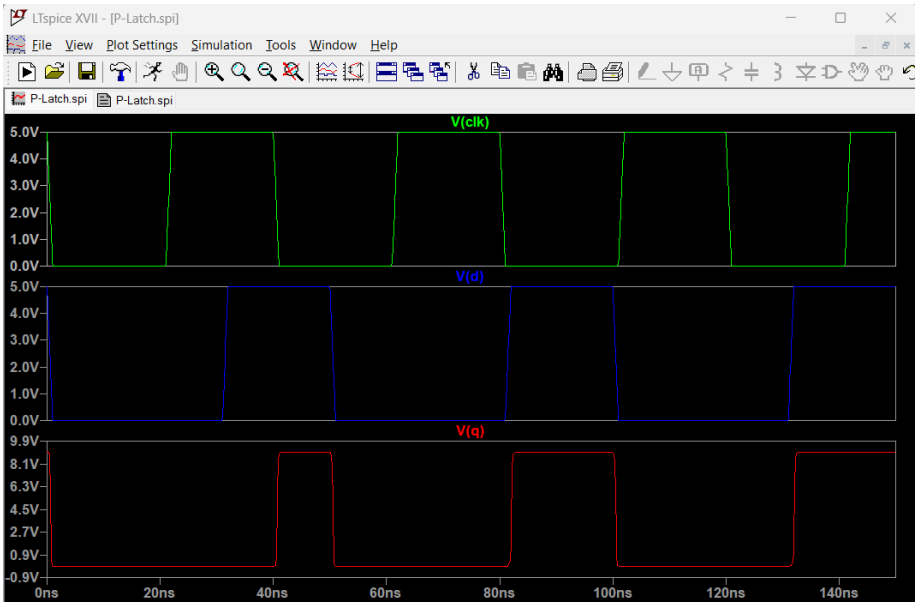

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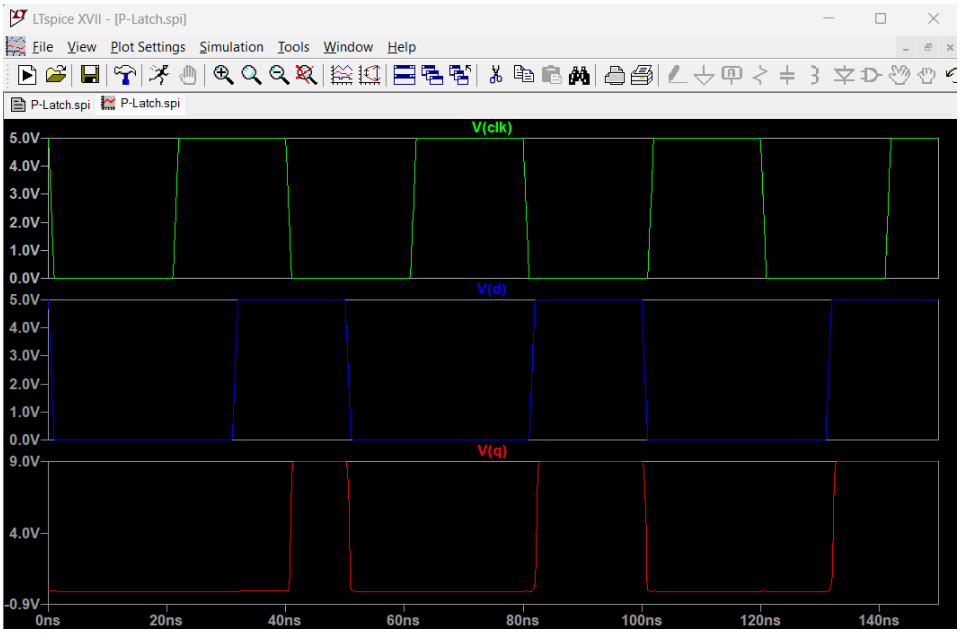

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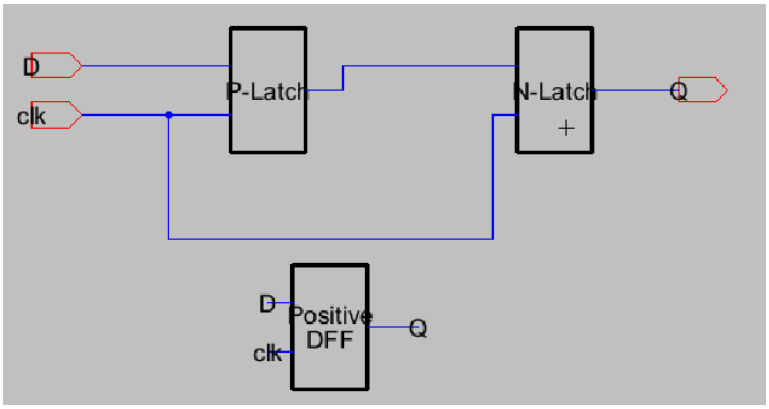
3. Rising Edge Flip Flop Schematic, Layout and Simulation.



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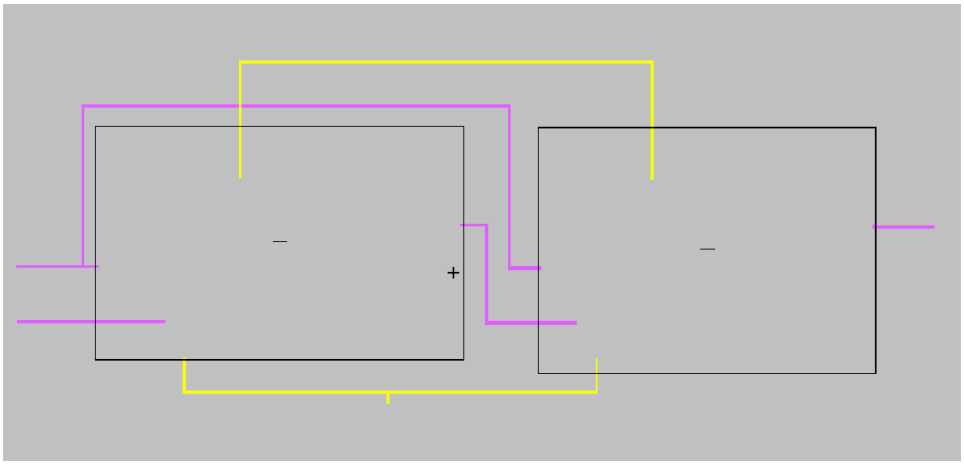

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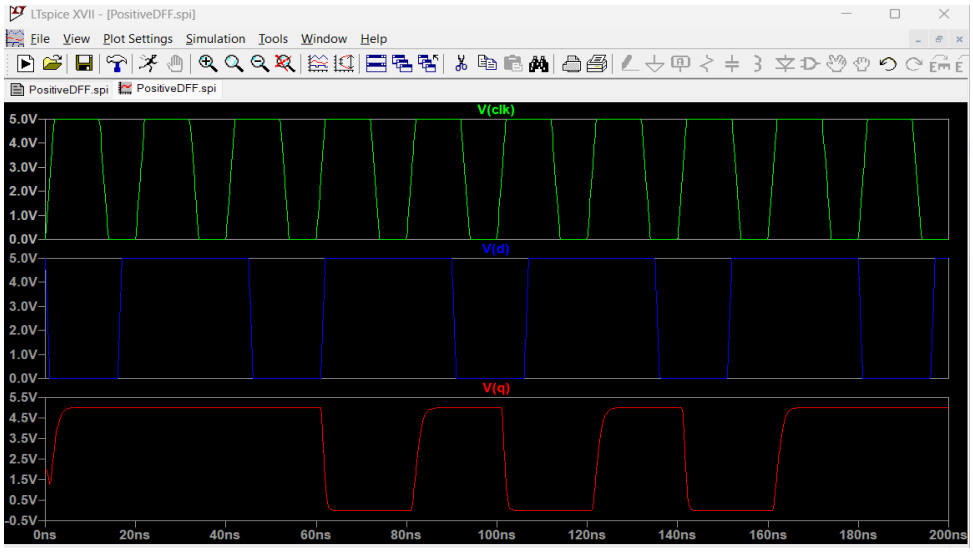

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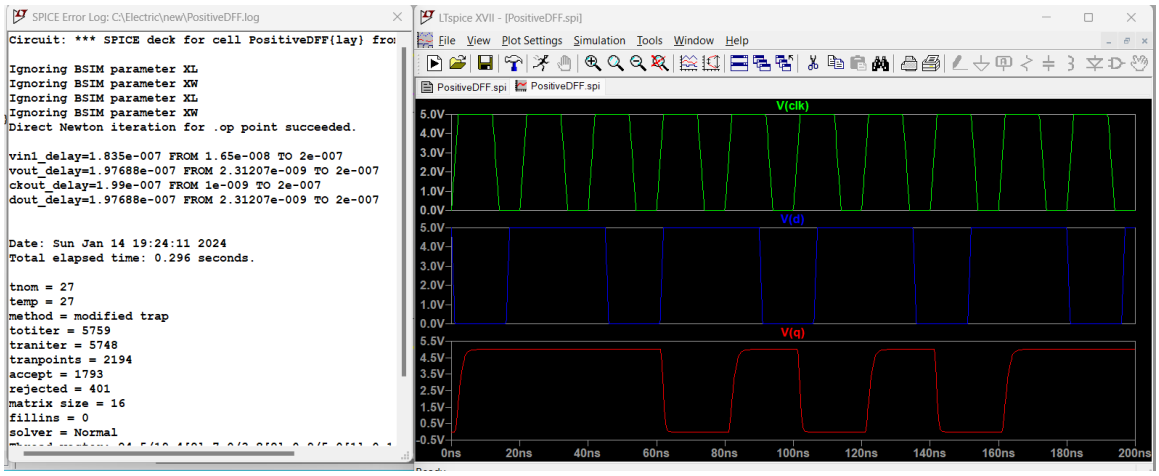

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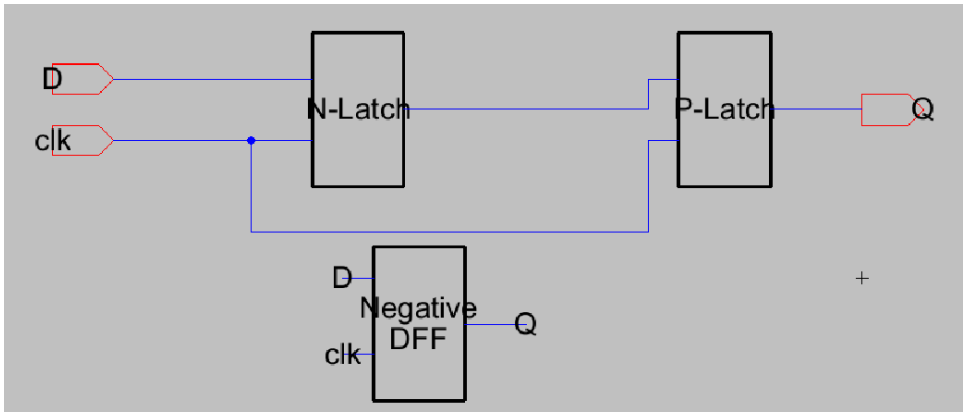

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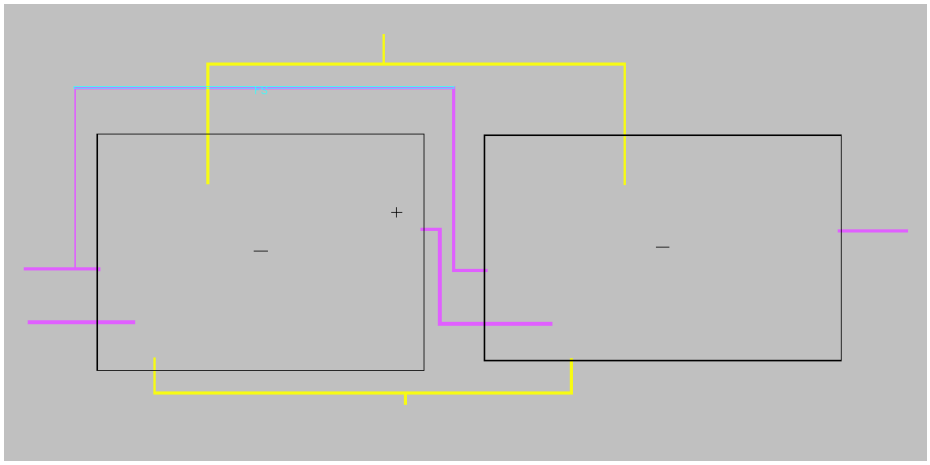

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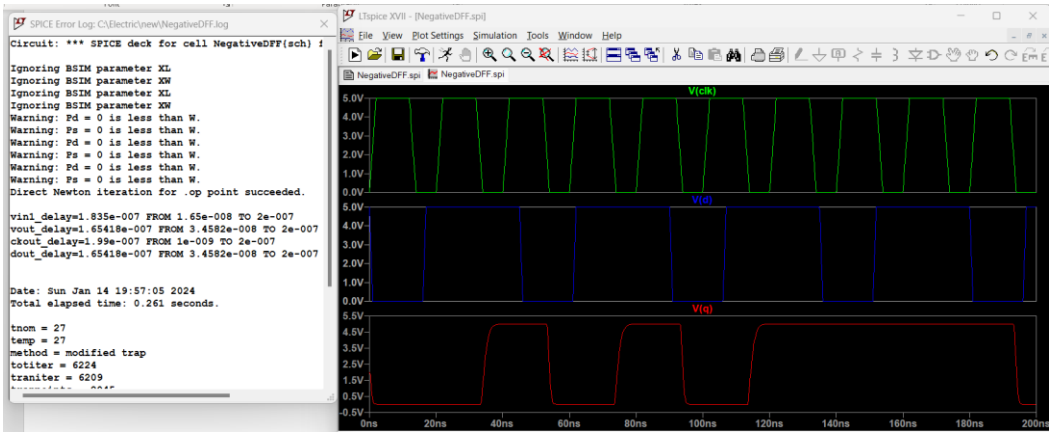

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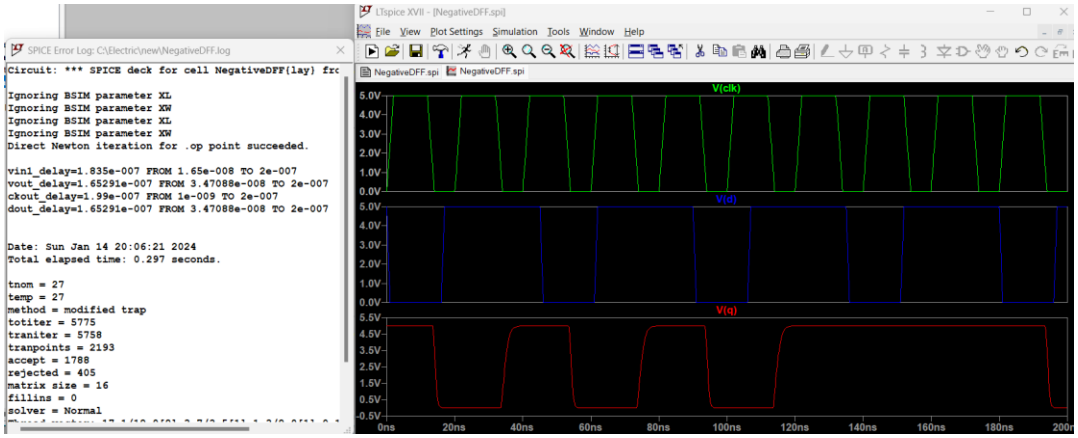

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5. Layout of the Transmission Gate used in the Design

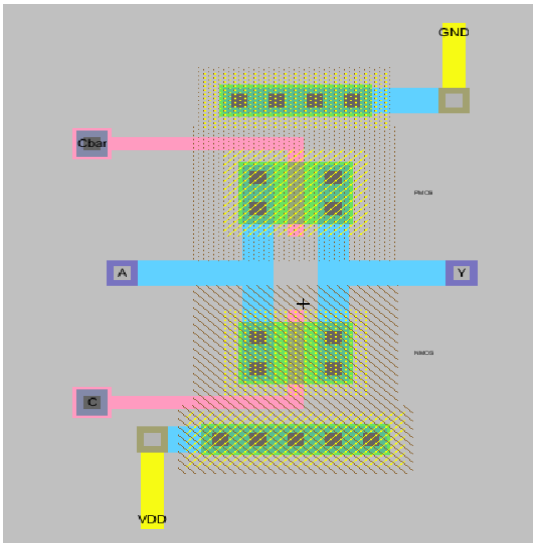

Figure 17: Transmission Gate Layout.