



Faculty Of Engineering and Technology

Electrical and Computer Engineering Department

ENCS3330, Digital Integrated Circuits

Assignment #2

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Section: 2

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Table of Contents

List of Figures.....	3
1. N-Latch Schematic, Layout and Simulation.	4
2. P-Latch Schematic, Layout and Simulation.....	5
3. Rising Edge Flip Flop Schematic, Layout and Simulation.	7
4. Falling Edge Flip Flop Schematic, Layout and Simulation.	8
5. Layout of the Transmission Gate used in the Design	9

List of Figures

Figure 1: N-Latch Schematic.-----	4
Figure 2: N-Latch Layout.-----	4
Figure 3: N-Latch Schematic - Simulation.-----	4
Figure 4: N-Latch Layout - Simulation.-----	5
Figure 5: P-Latch Schematic.-----	5
Figure 6: P-Latch Layout.-----	5
Figure 7: P-Latch Schematic - Simulation.-----	6
Figure 8: P-Latch Layout - Simulation.-----	6
Figure 9: Rising Edge Flip Flop Schematic.-----	7
Figure 10: Rising Edge Flip Flop Layout.-----	7
Figure 11: Rising FF Schematic - Simulation.-----	7
Figure 12: Rising FF Layout - Simulation.-----	8
Figure 13: Falling Edge Flip Flop Schematic.-----	8
Figure 14: Falling Edge Flip Flop Layout.-----	8
Figure 15: Falling Edge FF Schematic - Simulation.-----	9
Figure 16: Falling Edge FF Layout - Simulation.-----	9
Figure 17: Transmission Gate Layout.-----	9

1. N-Latch Schematic, Layout and Simulation.

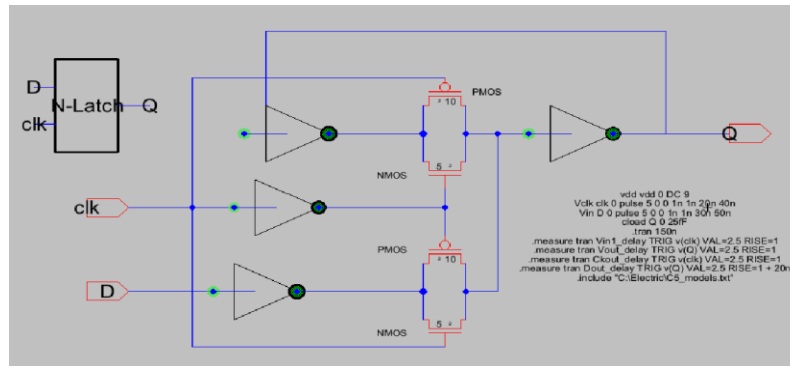


Figure 1: N-Latch Schematic.

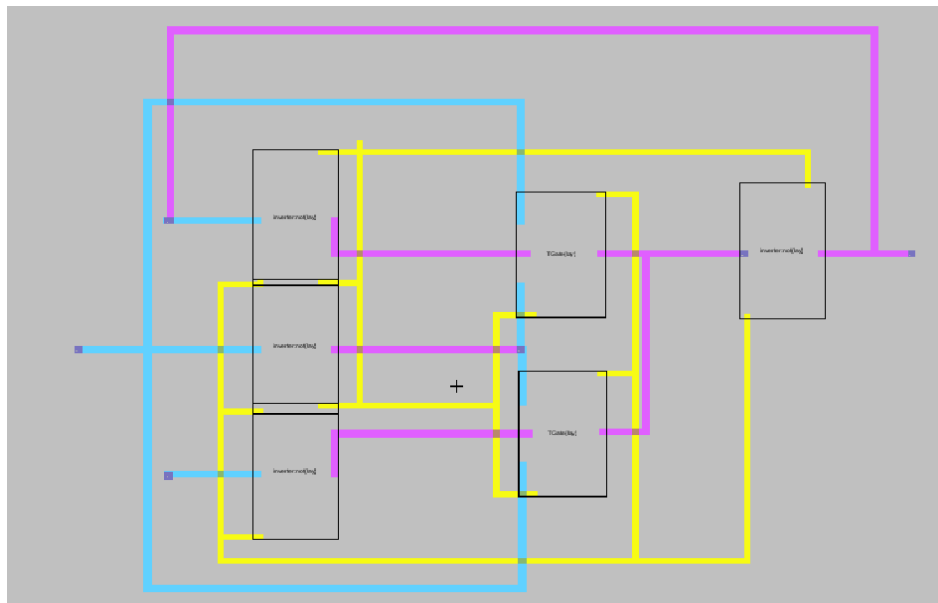


Figure 2: N-Latch Layout.

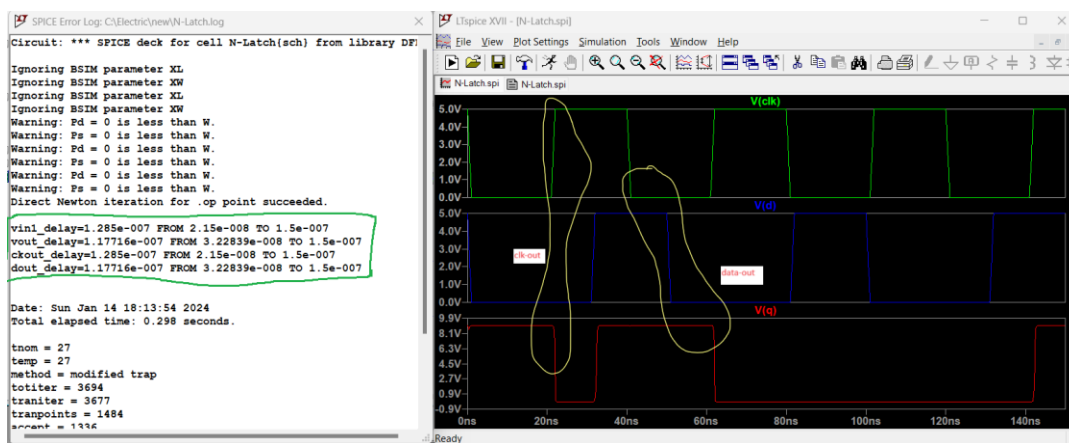


Figure 3: N-Latch Schematic - Simulation.

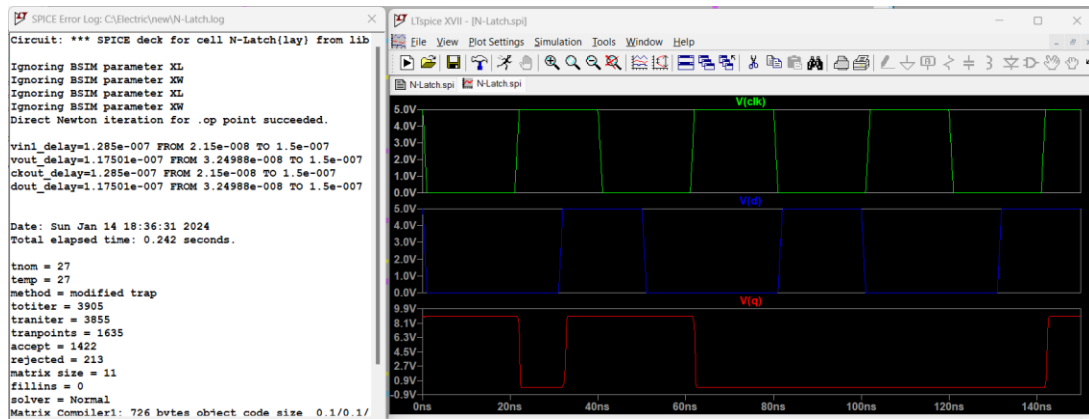


Figure 4: N-Latch Layout - Simulation.

2. P-Latch Schematic, Layout and Simulation.

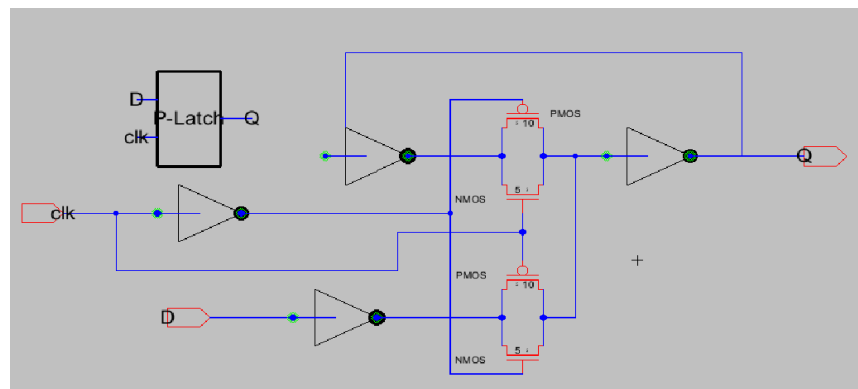


Figure 5: P-Latch Schematic.

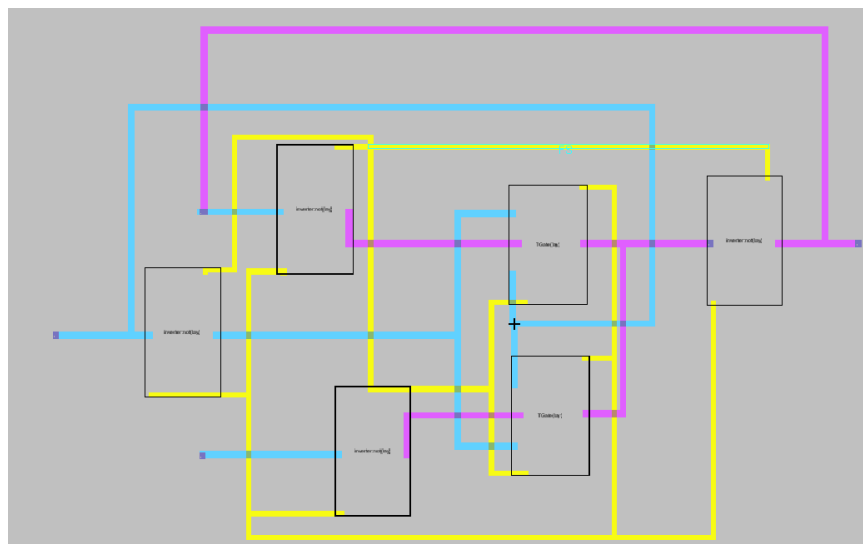


Figure 6: P-Latch Layout.

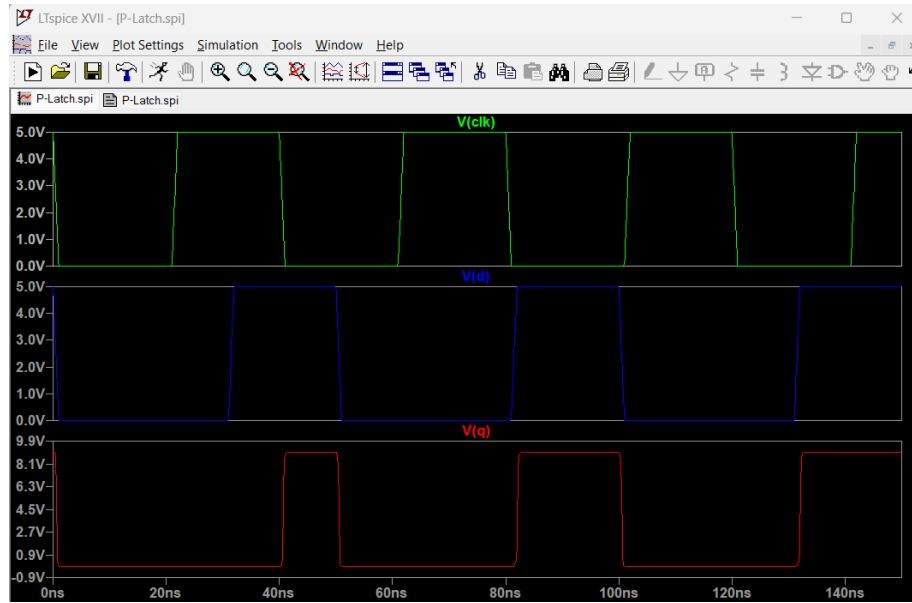


Figure 7: P-Latch Schematic - Simulation.

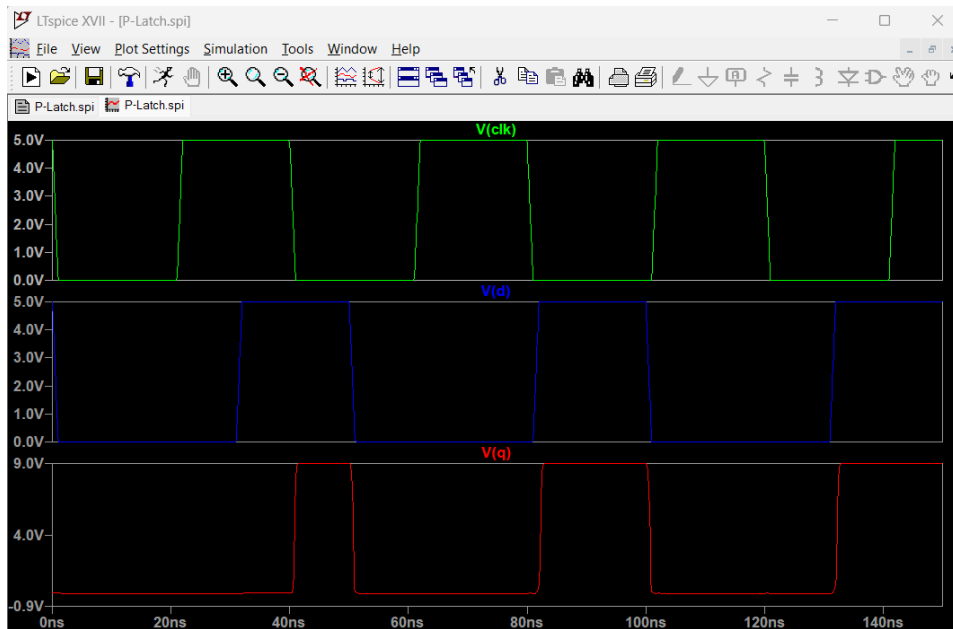


Figure 8: P-Latch Layout - Simulation.

3. Rising Edge Flip Flop Schematic, Layout and Simulation.

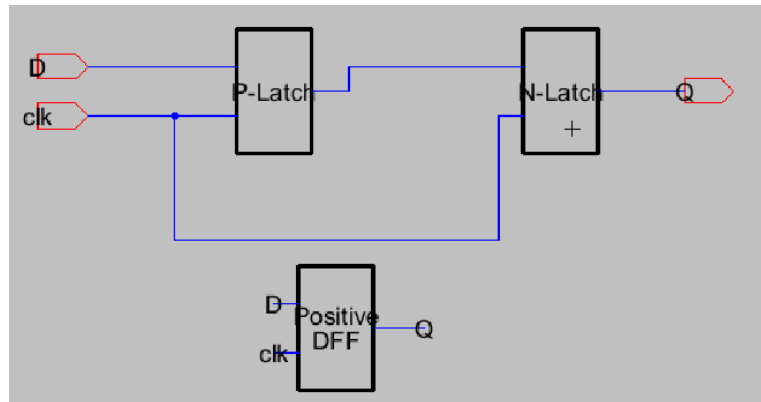


Figure 9: Rising Edge Flip Flop Schematic.

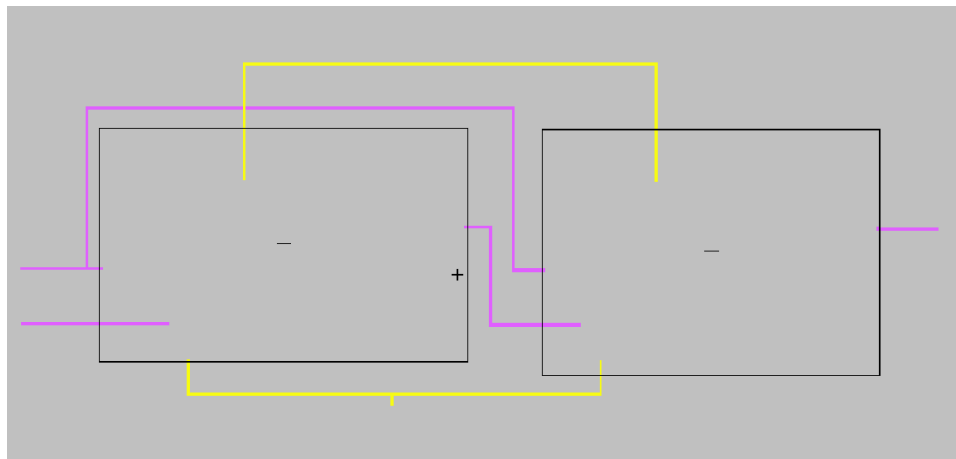


Figure 10: Rising Edge Flip Flop Layout.

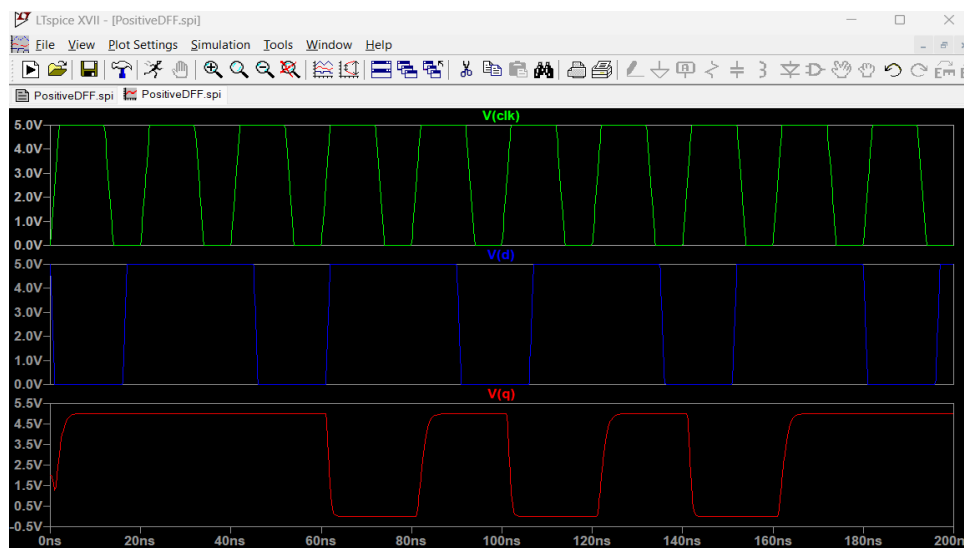


Figure 11: Rising FF Schematic - Simulation.

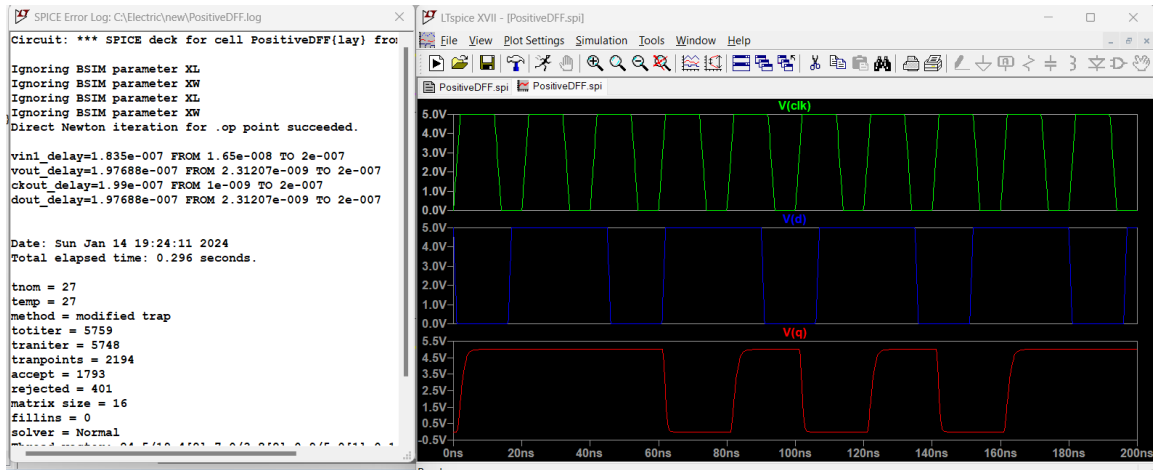


Figure 12: Rising FF Layout - Simulation.

4. Falling Edge Flip Flop Schematic, Layout and Simulation.

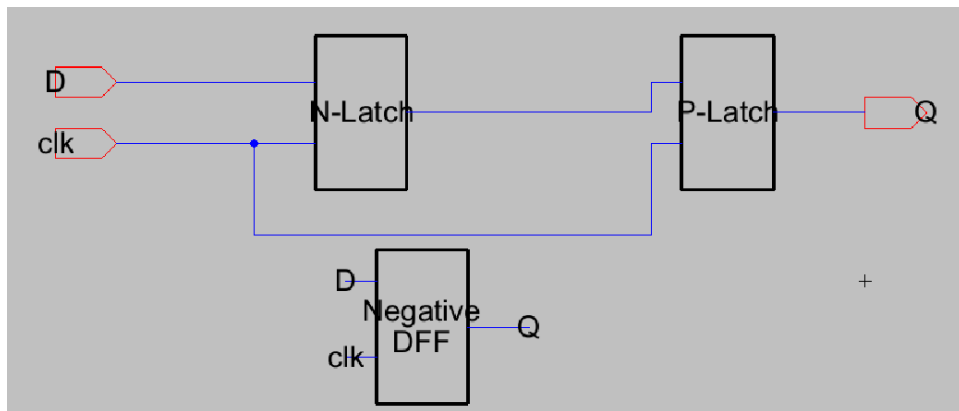


Figure 13: Falling Edge Flip Flop Schematic.

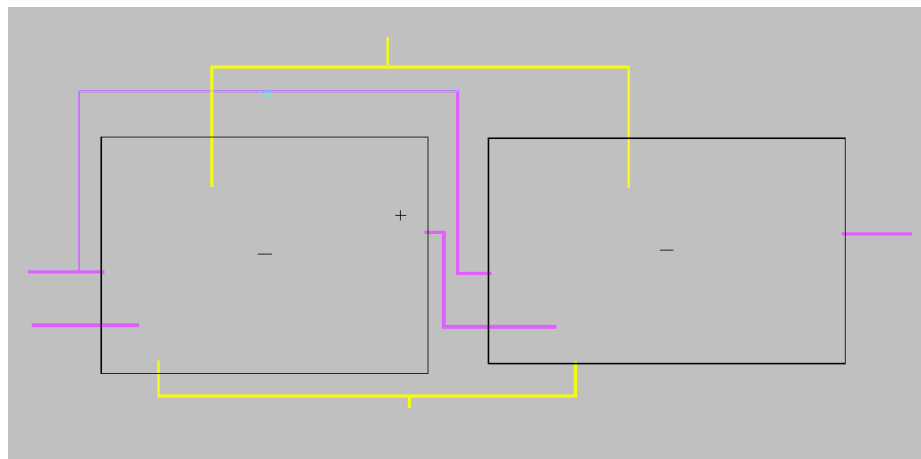


Figure 14: Falling Edge Flip Flop Layout.

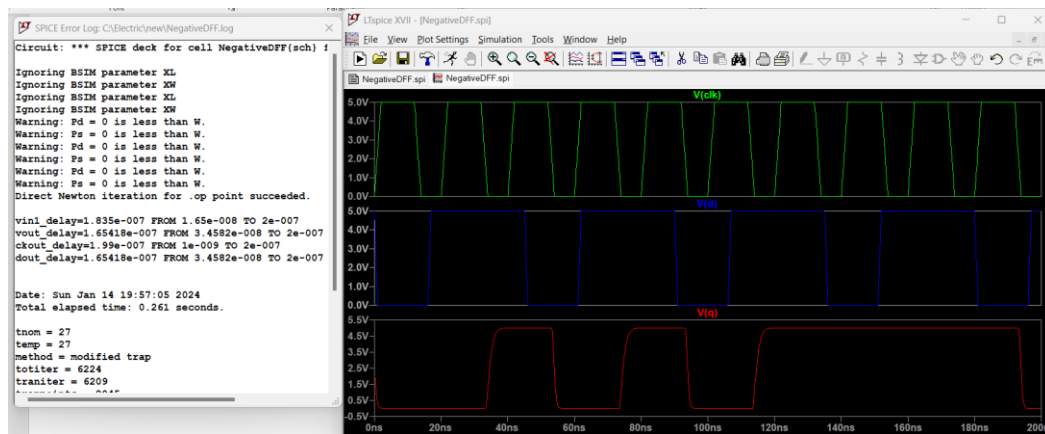


Figure 15: Falling Edge FF Schematic - Simulation.

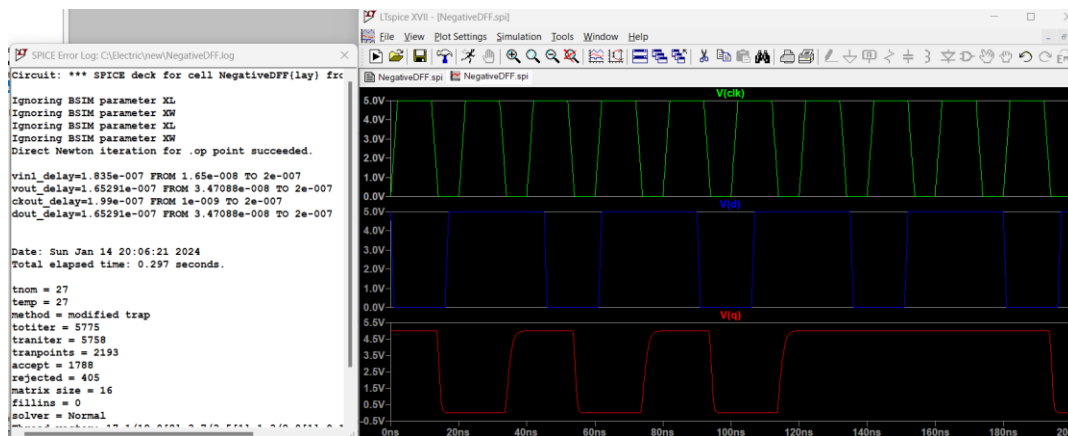


Figure 16: Falling Edge FF Layout - Simulation.

5. Layout of the Transmission Gate used in the Design

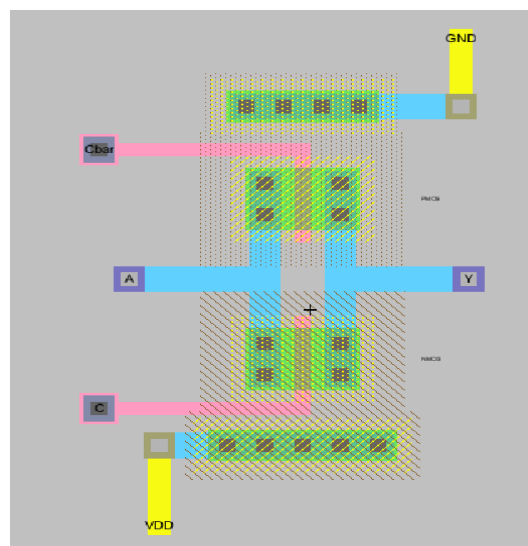


Figure 17: Transmission Gate Layout.