Pipeline_MIPS Project Status (11/13/2019 - 12:37:51)			
Project File:	pipeline.xise	**Parser Errors:**	No Errors
Module Name:	Pipeline_MIPS	**Implementation State:**	Placed and Routed
Target Device:	xc7vx485t-2ffg1761	• **Errors:**	
Product Version:	ISE 14.7	• **Warnings:**	
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	X 1 Failing Constraint
Environment:	System Settings	• **Final Timing Score:**	1195 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	333	607,200	1%	
Number used as Flip Flops	333			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	775	303,600	1%	
Number used as logic	728	303,600	1%	
Number using O6 output only	598			
Number using O5 output only	11			
Number using O5 and O6	119			
Number used as ROM	0			
Number used as Memory	44	130,800	1%	
Number used as Dual Port RAM	44			
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	44			
Number used as Single Port RAM	0			
Number used as Shift Register	0			
Number used exclusively as route-thrus	3			
Number with same-slice register load	1			
Number with same-slice carry load	2			
Number with other load	0			
Number of occupied Slices	338	75,900	1%	
Number of LUT Flip Flop pairs used	886			
Number with an unused Flip Flop	577	886	65%	
Number with an unused LUT	111	886	12%	
Number of fully used LUT-FF pairs	198	886	22%	
Number of unique control sets	5			
Number of slice register sites lost to control set restrictions	11	607,200	1%	
Number of bonded IOBs	69	700	9%	
Number of RAMB36E1/FIFO36E1s	16	1,030	1%	
Number using RAMB36E1 only	16			
Number using FIFO36E1 only	0			

Number of RAMB18E1/FIFO18E1s	0	2,060	0%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYs	0	700	0%	
Number of ILOGICE2/ILOGICE3/ISERDESE2s	0	700	0%	
Number of ODELAYE2/ODELAYE2_FINEDELAYs	0	700	0%	
Number of OLOGICE2/OLOGICE3/OSERDESE2s	0	700	0%	
Number of PHASER_IN/PHASER_IN_PHYs	0	56	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	56	0%	
Number of BSCANs	0	4	0%	
Number of BUFHCEs	0	168	0%	
Number of BUFRs	0	56	0%	
Number of CAPTUREs	0	1	0%	
Number of DNA_PORTs	0	1	0%	
Number of DSP48E1s	0	2,800	0%	
Number of EFUSE_USRs	0	1	0%	
Number of FRAME_ECCs	0	1	0%	
Number of GTXE2_CHANNELs	0	56	0%	
Number of GTXE2_COMMONs	0	14	0%	
Number of IBUFDS_GTE2s	0	28	0%	
Number of ICAPs	0	2	0%	
Number of IDELAYCTRLs	0	14	0%	
Number of IN_FIFOs	0	56	0%	
Number of MMCME2_ADVs	0	14	0%	
Number of OUT_FIFOs	0	56	0%	
Number of PCIE_2_1s	0	4	0%	
Number of PHASER_REFs	0	14	0%	
Number of PHY_CONTROLs	0	14	0%	
Number of PLLE2_ADVs	0	14	0%	
Number of STARTUPs	0	1	0%	
Number of XADCs	0	1	0%	
Average Fanout of Non-Clock Nets	4.41			

Performance Summary			[-]
Final Timing Score:	1195 (Setup: 1195, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	X 1 Failing Constraint		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Nov 13 12:31:31 2019			
Translation Report	Current	Wed Nov 13 12:34:24 2019	0	0	0
Map Report	Current	Wed Nov 13 12:36:07 2019	0	81 Warnings (81 new)	7 Infos (2 new)

Place and Route Report	Current	Wed Nov 13 12:37:19 2019	0	12 Warnings (0 new)	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed Nov 13 12:37:49 2019	0	0	4 Infos (0 new)
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	

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