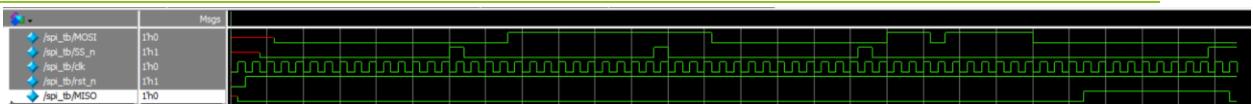


SPI

Name: Amr Essam Mahmoud Anwar

Name: Hazem Mohamed El Gharabawy

1) Snippets from the waveforms captured from QuestaSim

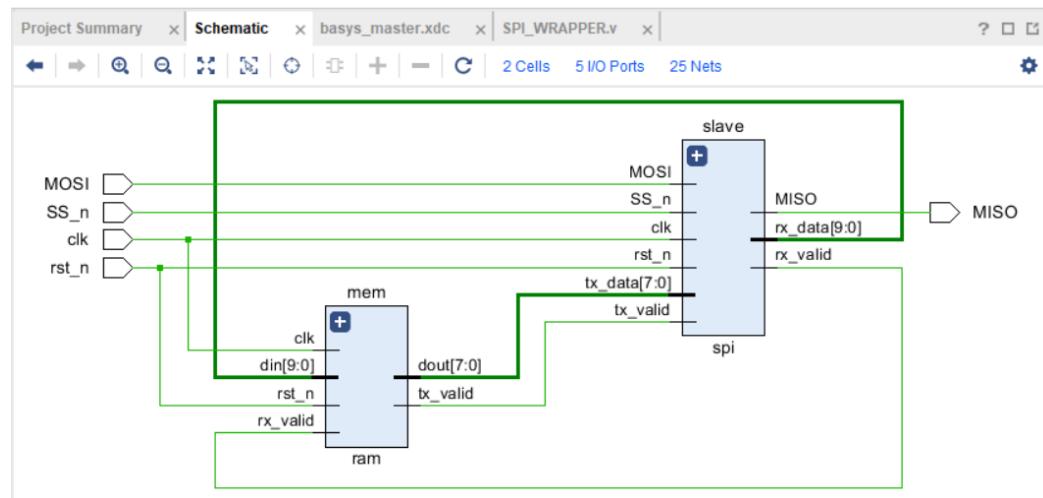


2) Synthesis snippets for each encoding

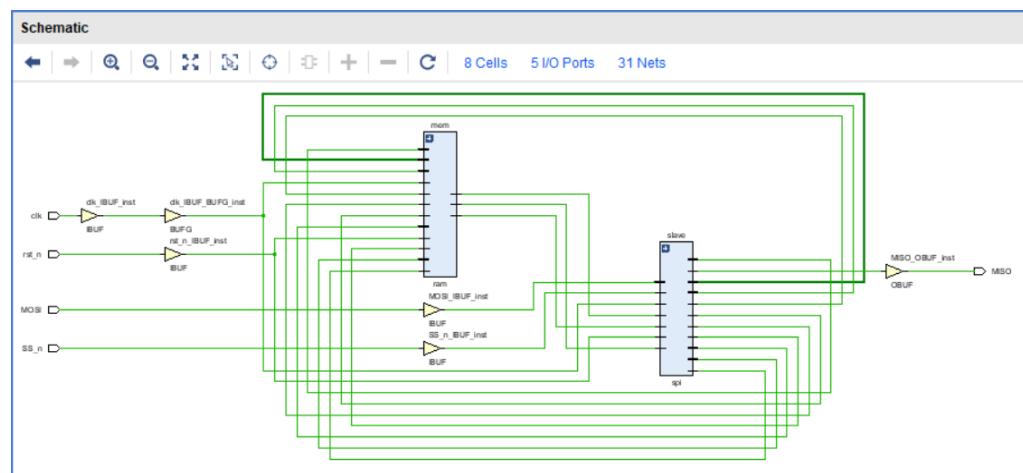
Grey

Schematic after the elaboration & synthesis

Elaborated



Synthesis



- *Synthesis report showing the encoding used*

```

xdc  x| SPI_WRAPPER.v  x| synth_1_synth_report_utilization_0 - synth_1  x| synth_1_synth_synthesis_report_0 - synth_1  x
F:/Digital/digital_course_projects/SPI_FINAL/SPI/SPI.runs/synth_1/spi_wrapper.vds
Read-only | settings

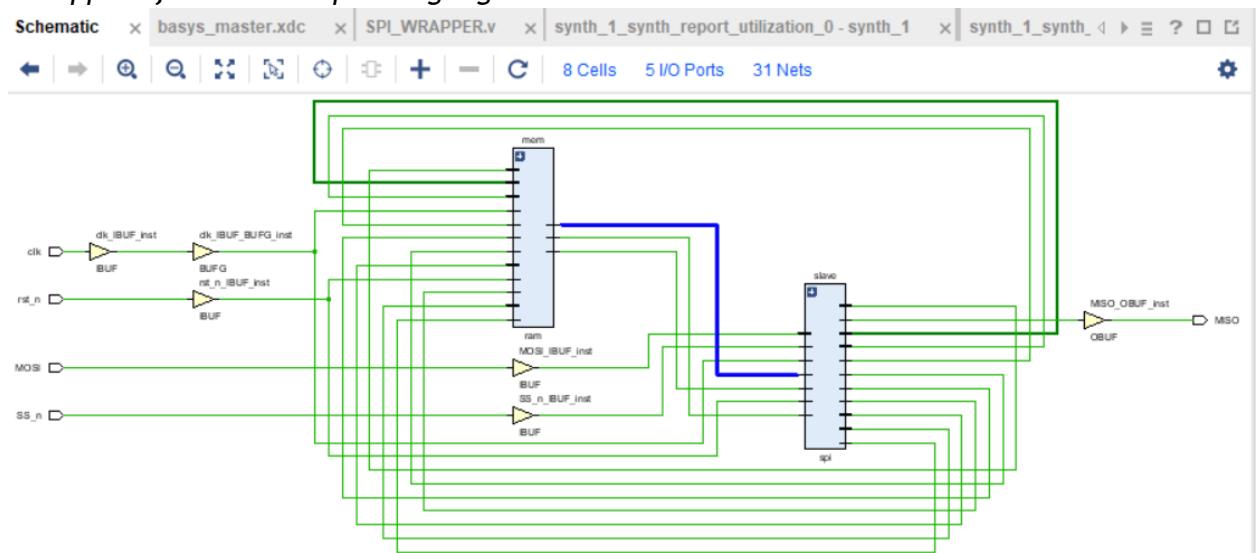
enc
Parameter IDLE bound to: 0 - type: integer
Parameter CHK_CMD bound to: 1 - type: integer
Parameter WRITE bound to: 2 - type: integer
Parameter READ_ADD bound to: 3 - type: integer
Parameter READ_DATA bound to: 4 - type: integer
INFO: [Synth 0-5534] Detected attribute (* fsm_encoding = "gray" *) [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_f
INFO: [Synth 0-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_f
WARNING: [Synth 0-567] referenced signal 'get_data' should be on the sensitivity list [F:/Digital/digital_course_proje
INFO: [Synth 0-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_f
INFO: [Synth 0-6155] done synthesizing module 'spi' (#1) [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_final.v:1
INFO: [Synth 0-6155] synthesizing module 'ram' [F:/Digital/digital_course_projects/SPI_FINAL/RAM.v:1]
INFO: [Synth 0-6155] done synthesizing module 'ram' (#1) [F:/Digital/digital_course_projects/SPI_FINAL/RAM.v:1]
Parameter MEM_DEPTH bound to: 256 - type: integer
Parameter ADDR_SIZE bound to: 8 - type: integer
INFO: [Synth 0-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/RAM.v:2
INFO: [Synth 0-6155] done synthesizing module 'ram' (2#1) [F:/Digital/digital_course_projects/SPI_FINAL/RAM.v:1]

```

- *Timing report snippet*

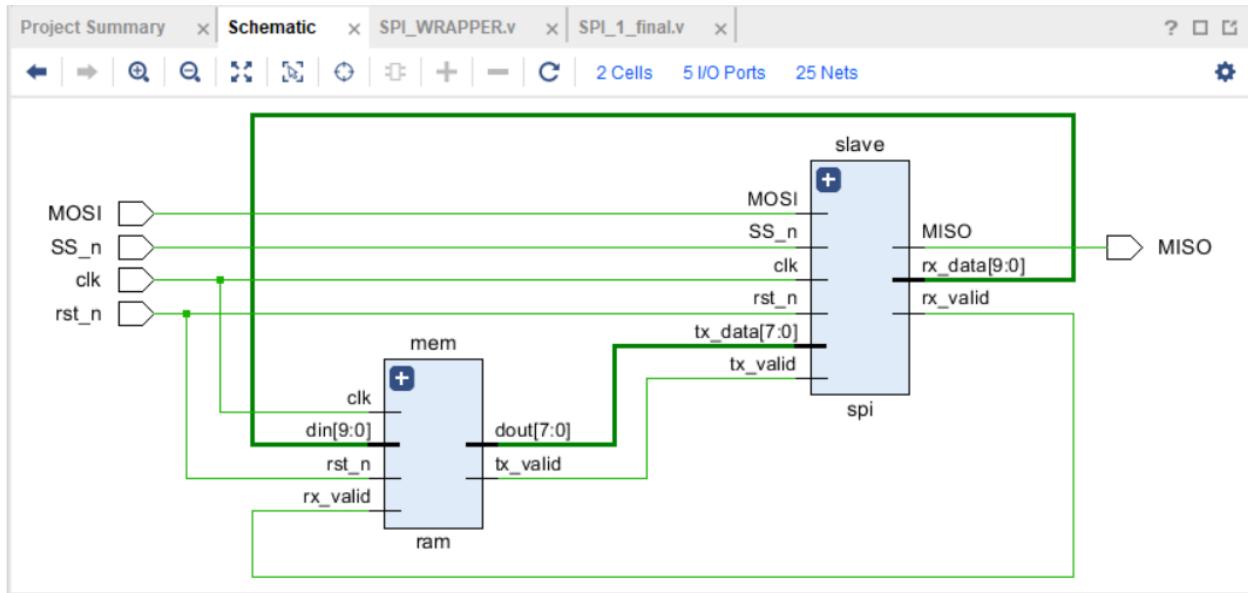
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	5.898	2	3	1	mem/mem_reg/CLKBWRCLK	slave/MISO_reg/D	3.951	2.702	1.249	10.
Path 2	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[0]/CE	2.798	0.875	1.923	10.
Path 3	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[1]/CE	2.798	0.875	1.923	10.
Path 4	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[2]/CE	2.798	0.875	1.923	10.
Path 5	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[3]/CE	2.798	0.875	1.923	10.
Path 6	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[4]/CE	2.798	0.875	1.923	10.

- *Snippet of the critical path highlighted in the schematic*

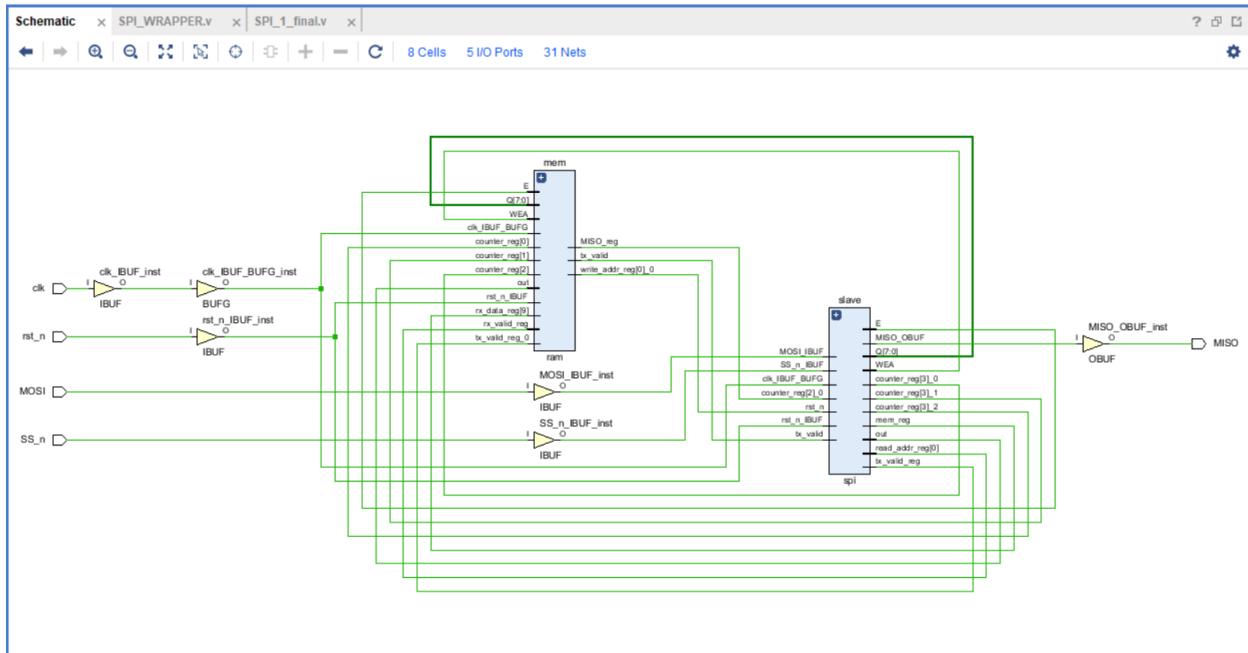


Hot one

Elaborated



Synthesis



- Synthesis report showing the encoding used

```

Schematic x SPI_WRAPPER.v x SPI_1_final.v x synth_1_synth_synthesis_report_0 - synth_1 x
F:/Digital/digital_course_projects/SPI_FINAL/SPI/SPI.runs/synth_1/spi_wrapper.vds
Read-only | Settings

enco Next Previous Highlight Match Case Whole Words 6 Match(es)

19 -----
20 Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 408.812 ; gain = 95.906
21 -----
22 INFO: [Synth 8-6157] synthesizing module 'spi_wrapper' [F:/Digital/digital_course_projects/SPI_FINAL/SPI_WRAPPER.v:1]
23 INFO: [Synth 8-6157] synthesizing module 'spi' [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_final.v:1]
24 Parameter IDLE bound to: 0 - type: integer
25 Parameter CHK_CMD bound to: 1 - type: integer
26 Parameter WRITE bound to: 2 - type: integer
27 Parameter READ_ADD bound to: 3 - type: integer
28 Parameter READ_DATA bound to: 4 - type: integer
29 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [F:/Digital/digital_course_projects/SPI_FINAL/SP
30 INFO: [Synth 8-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_f
31 WARNING: [Synth 8-567] referenced signal 'get_data' should be on the sensitivity list [F:/Digital/digital_course_proje
32 INFO: [Synth 8-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_f
33 INFO: [Synth 8-6155] done synthesizing module 'spi' (1#1) [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_final.v:1]

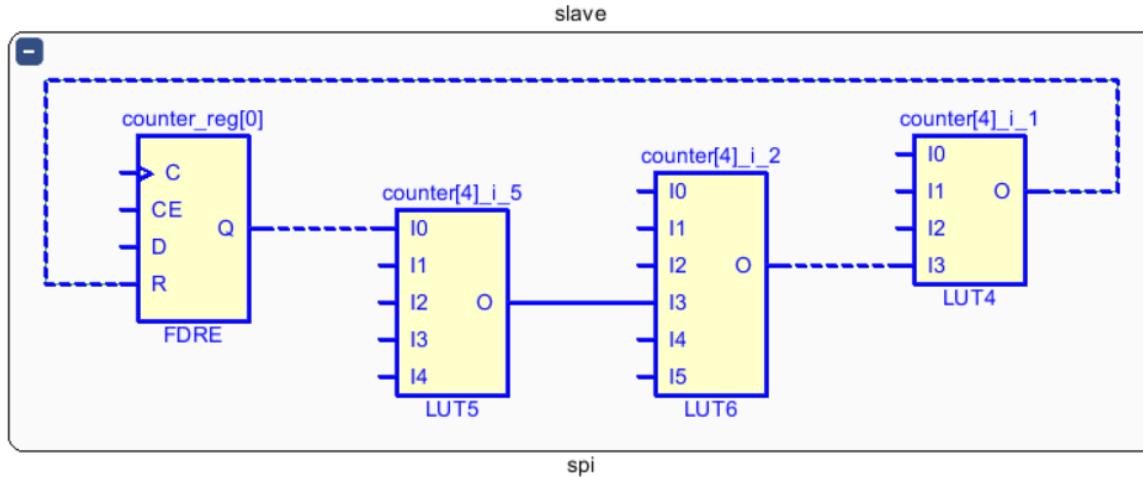
```

- Timing report snippet

The screenshot shows a timing analysis interface with a table titled "Intra-Clock Paths - sys_clk_pin - Setup". The table lists six paths with their respective parameters:

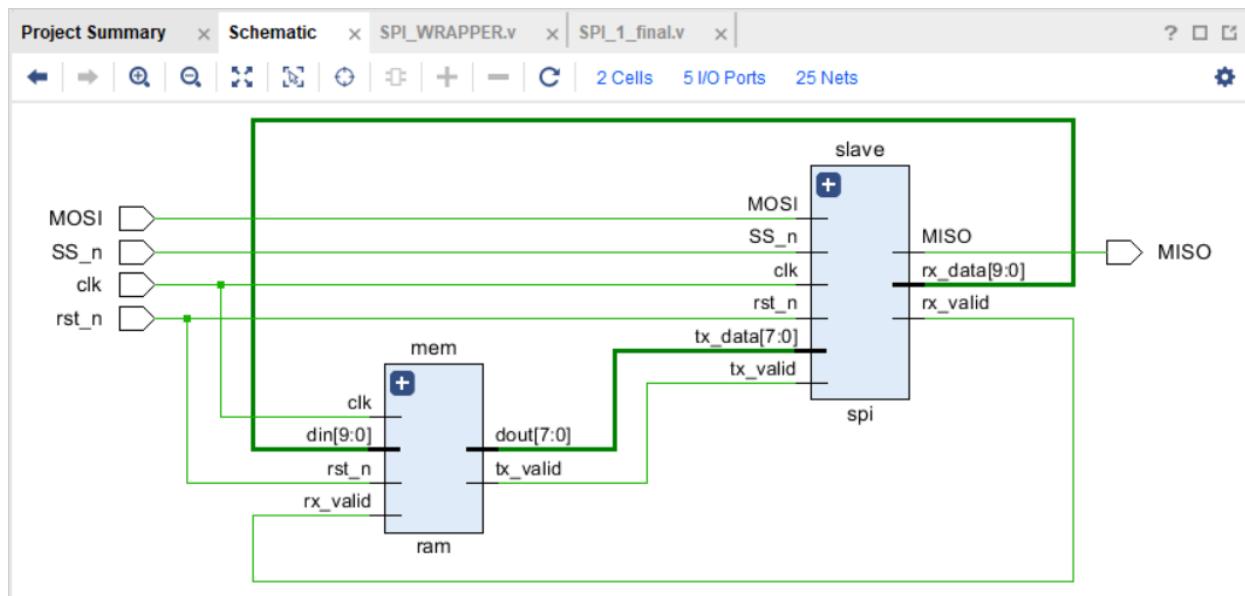
Name	Slack	^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	5.351		3	12	slave/counter_reg[0]/C	slave/counter_reg[0]/R	4.036	0.999	3.037	10.000	sys_d
Path 2	5.351		3	12	slave/counter_reg[0]/C	slave/counter_reg[1]/R	4.036	0.999	3.037	10.000	sys_d
Path 3	5.351		3	12	slave/counter_reg[0]/C	slave/counter_reg[2]/R	4.036	0.999	3.037	10.000	sys_d
Path 4	5.351		3	12	slave/counter_reg[0]/C	slave/counter_reg[4]/R	4.036	0.999	3.037	10.000	sys_d
Path 5	5.898		2	1	mem/mem_reg/CLKBWRCLK	slave/MISO_reg/D	3.951	2.702	1.249	10.000	sys_d
Path 6	6.482		2	12	slave/counter_real0/C	slave/counter_real0/ICE	3.136	0.875	2.261	10.000	sys_d

- Snippet of the critical path highlighted in the schematic

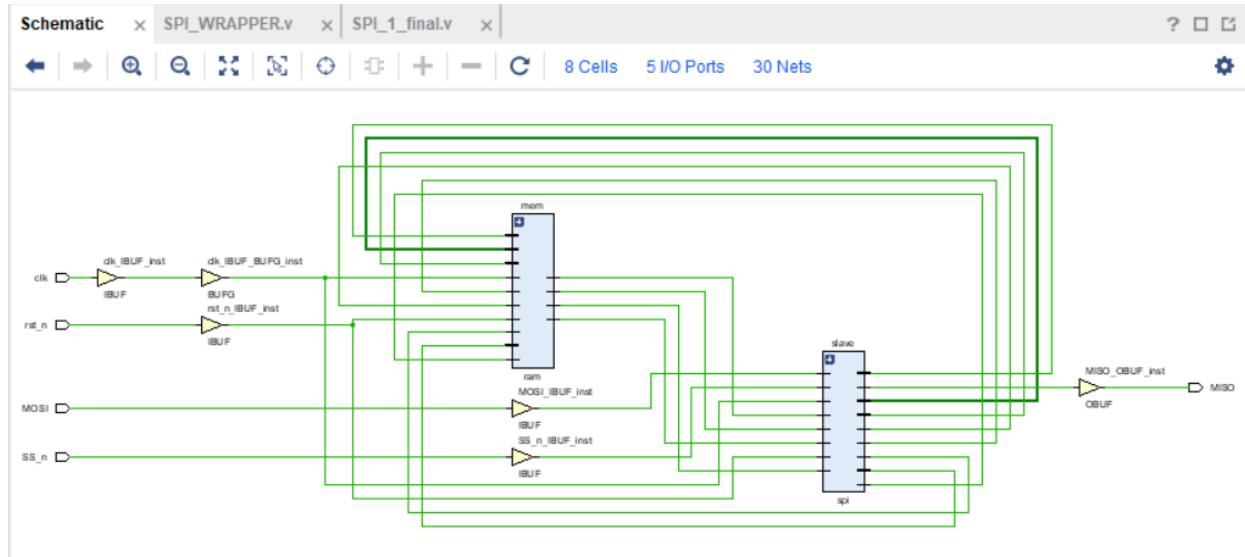


Seq

Elaborated



Synthesis



- Synthesis report showing the encoding used

```

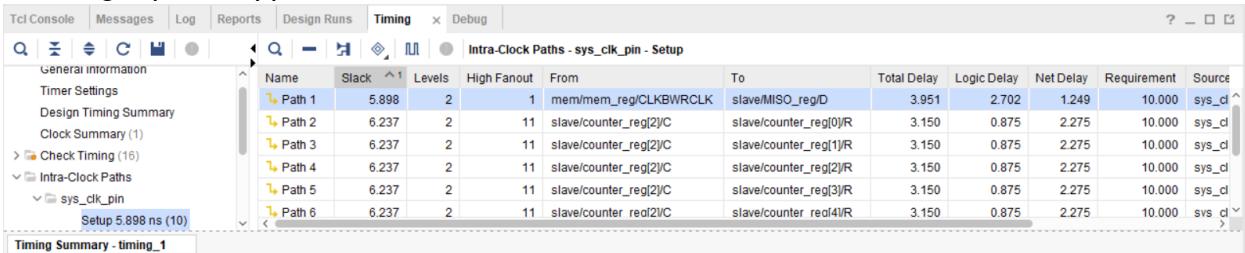
mary | Device | SPI_WRAPPER.v | SPI_1_final.v | Schematic | synth_1_synth_synthesis_report_0 - synth_1 |
F:/Digital/digital_course_projects/SPI_FINAL/SPI/runs/synth_1/spi_wrapper.vds
Read-only | Settings

enc
Next | Previous | Highlight | Match Case | Whole Words | 7 Match(es)

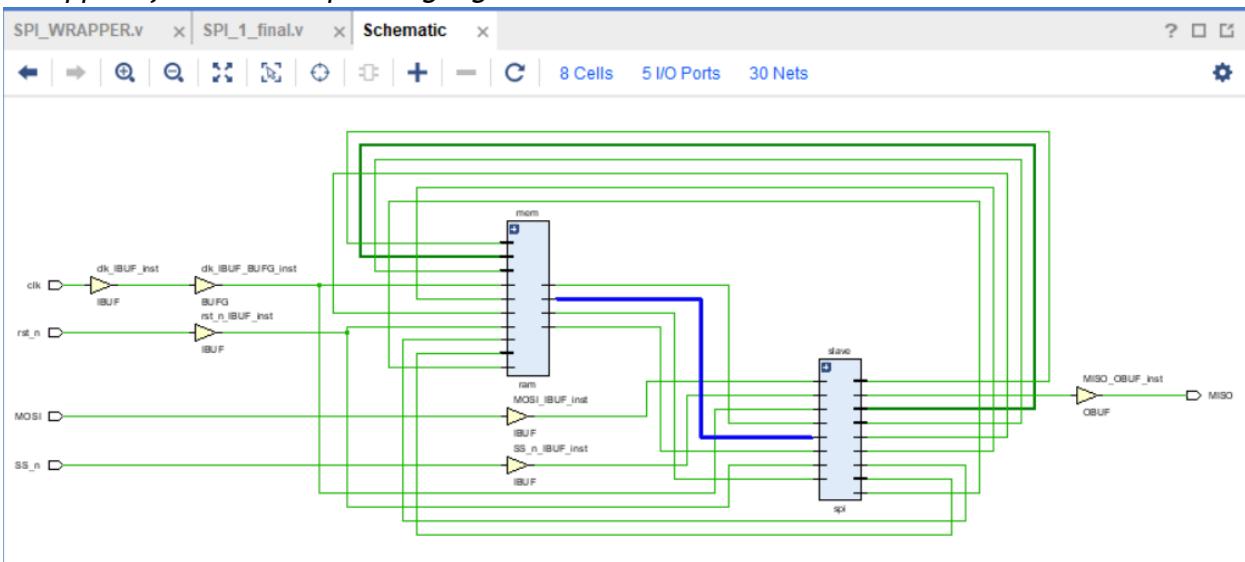
24 Parameter IDLE bound to: 0 - type: integer
25 Parameter CHK_CMD bound to: 1 - type: integer
26 Parameter WRITE bound to: 2 - type: integer
27 Parameter READ_ADD bound to: 3 - type: integer
28 Parameter READ_DATA bound to: 4 - type: integer
29 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [F:/Digital/digital_course_projects/SPI_FINAL
30 INFO: [Synth 8-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_f
31 WARNING: [Synth 8-567] referenced signal 'get_data' should be on the sensitivity list [F:/Digital/digital_course_proje
32 INFO: [Synth 8-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_f
33 INFO: [Synth 8-6155] done synthesizing module 'spi' (#1) [F:/Digital/digital_course_projects/SPI_FINAL/SPI_1_final.v:1
34 INFO: [Synth 8-6157] synthesizing module 'ram' [F:/Digital/digital_course_projects/SPI_FINAL/RAM.v:1]
35     Parameter MEM_DEPTH bound to: 256 - type: integer
36     Parameter ADDR_SIZE bound to: 8 - type: integer
37 INFO: [Synth 8-155] case statement is not full and has no default [F:/Digital/digital_course_projects/SPI_FINAL/RAM.v:2
38 INFO: [Synth 8-6155] done synthesizing module 'ram' (#1) [F:/Digital/digital_course_projects/SPI_FINAL/RAM.v:1]

```

- Timing report snippet



- Snippet of the critical path highlighted in the schematic

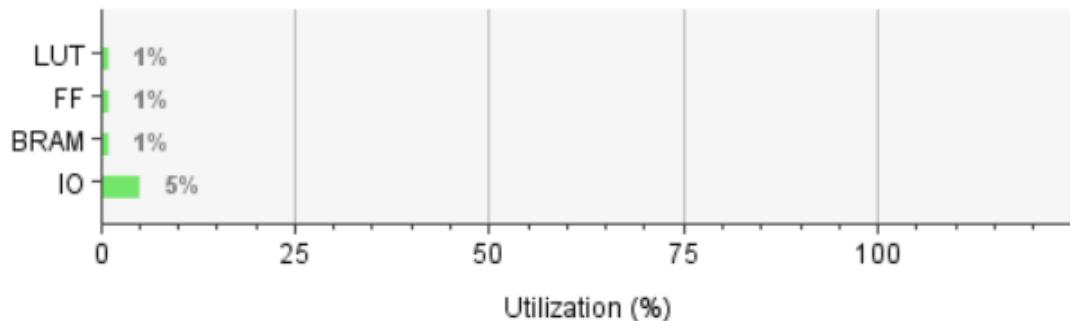


Implementation snippets for each encoding
grey

- Utilization report

Summary

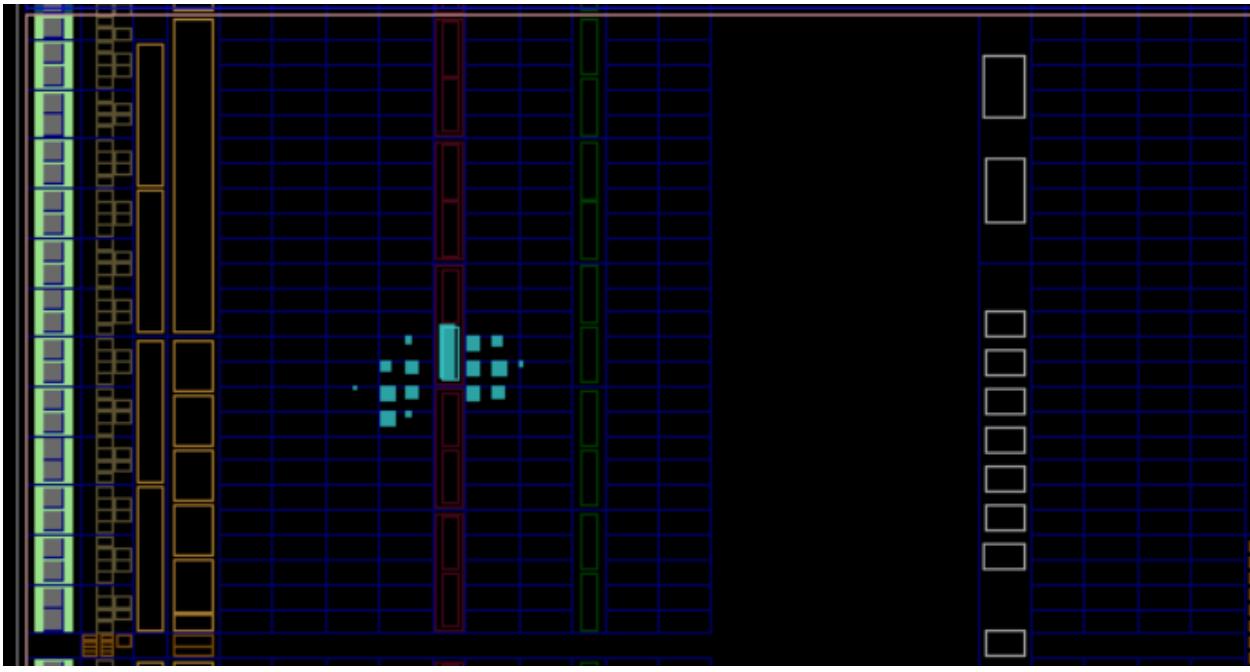
Resource	Utilization	Available	Utilization %
LUT	29	20800	0.14
FF	51	41600	0.12
BRAM	0.50	50	1.00
IO	5	106	4.72



- Timing report snippet

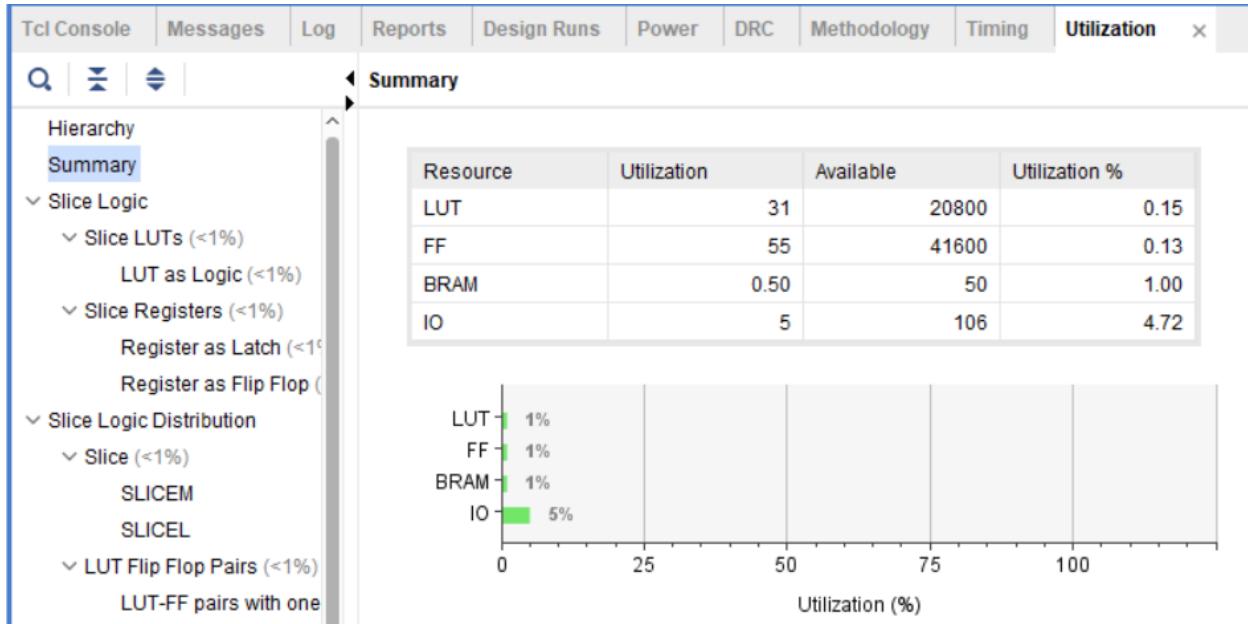
Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source C
Path 1	5.779	2	1	mem/mem_reg/CLKBWRCLK	slave/MISO_reg/D	4.250	2.702	1.548	10.000	sys_clk_
Path 2	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[0]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 3	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[2]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 4	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[3]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 5	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[4]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 6	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[5]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 7	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[6]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 8	6.795	2	14	slave/FSM_gray_cs_reg[2]/C	slave/counter_reg[4]/CE	2.939	0.766	2.173	10.000	sys_clk_
Path 9	6.808	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[1]/CE	2.885	0.956	1.929	10.000	sys_clk_
Path 10	6.808	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[7]/CE	2.885	0.956	1.929	10.000	sys_clk_

- FPGA device snippet



Hot one

- Utilization report



- Timing report snippet

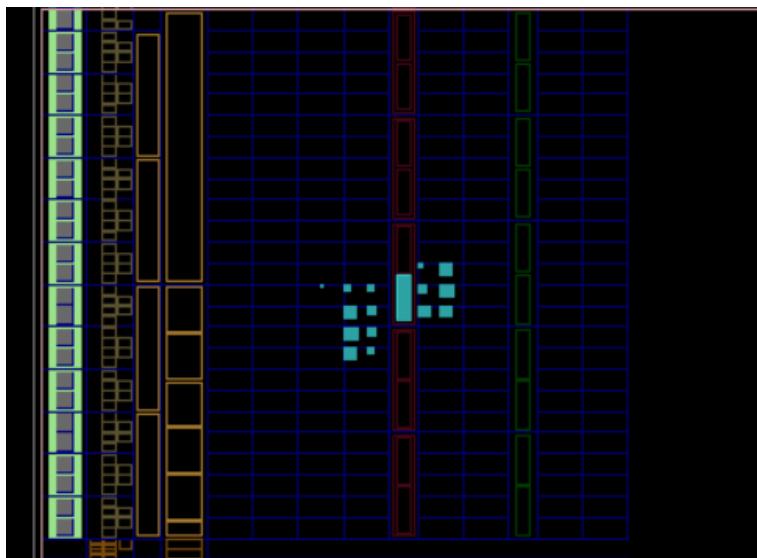
Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source C
Path 1	5.110		4	8	slave/FSM_onehot_cs_reg[4]/C	slave/counter_reg[0]/R	4.308	1.146	3.162	10.0	sys_clk_i
Path 2	5.110		4	8	slave/FSM_onehot_cs_reg[4]/C	slave/counter_reg[1]/R	4.308	1.146	3.162	10.0	sys_clk_i
Path 3	5.110		4	8	slave/FSM_onehot_cs_reg[4]/C	slave/counter_reg[2]/R	4.308	1.146	3.162	10.0	sys_clk_i
Path 4	5.110		4	8	slave/FSM_onehot_cs_reg[4]/C	slave/counter_reg[4]/R	4.308	1.146	3.162	10.0	sys_clk_i
Path 5	5.526		2	1	mem/mem_reg/CLKBWRCLK	slave/MISO_reg/D	4.501	2.702	1.799	10.0	sys_clk_i
Path 6	5.808		3	10	slave/FSM_onehot_cs_reg[4]/C	slave/temp_reg[2]/CE	3.850	1.022	2.828	10.0	sys_clk_i
Path 7	5.808		3	10	slave/FSM_onehot_cs_reg[4]/C	slave/temp_reg[3]/CE	3.850	1.022	2.828	10.0	sys_clk_i
Path 8	5.808		3	10	slave/FSM_onehot_cs_reg[4]/C	slave/temp_reg[4]/CE	3.850	1.022	2.828	10.0	sys_clk_i
Path 9	5.808		3	10	slave/FSM_onehot_cs_reg[4]/C	slave/temp_reg[5]/CE	3.850	1.022	2.828	10.0	sys_clk_i
Path 10	5.808		3	10	slave/FSM_onehot_cs_reg[4]/C	slave/temp_reg[6]/CE	3.850	1.022	2.828	10.0	sys_clk_i

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
> Check Timing (34)
Intra-Clock Paths
 sys_clk_pin
 Setup 5.110 ns (10)
 Hold 0.042 ns (10)
 Pulse Width 4.500 ns (30)
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

- FPGA device snippet



Messages after bitstream generation

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization | ? - □ ⊞

Q | H | E | T | M | B | Hide All

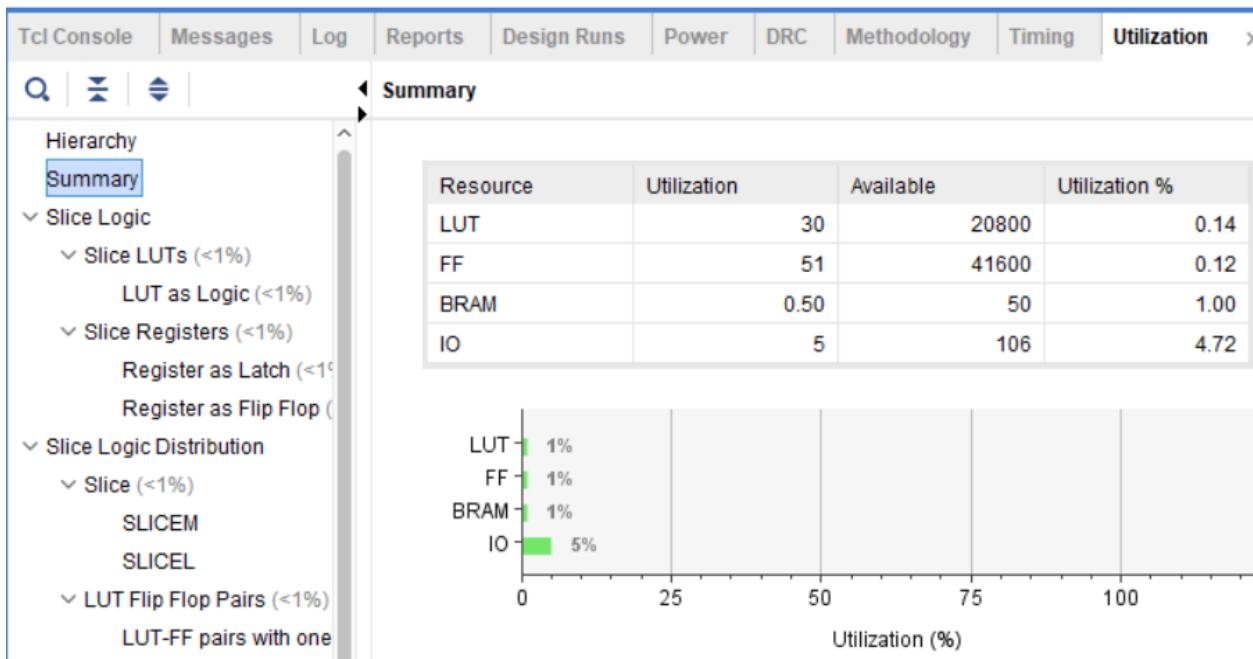
> Vivado Commands (3 infos, 28 status messages)

↳ Synthesis (3 warnings, 38 infos, 11 status messages)

- > Command: synth_design -top spi_wrapper -part xc7a35tcpg236-1L (10 more like this)
 - ⌚ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
 - ⌚ [Synth 8-6157] synthesizing module 'spi_wrapper' [SPI_WRAPPER.v1] (2 more like this)
 - ⌚ [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot") [SPI_1_final.v18]
 - ⌚ [Synth 8-567] referenced signal 'get_data' should be on the sensitivity list [SPI_1_final.v31]
 - ⌚ [Synth 8-155] case statement is not full and has no default [SPI_1_final.v32] (2 more like this)

Seq

- Utilization report



- Timing report snippet

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization ? - □ ⊞

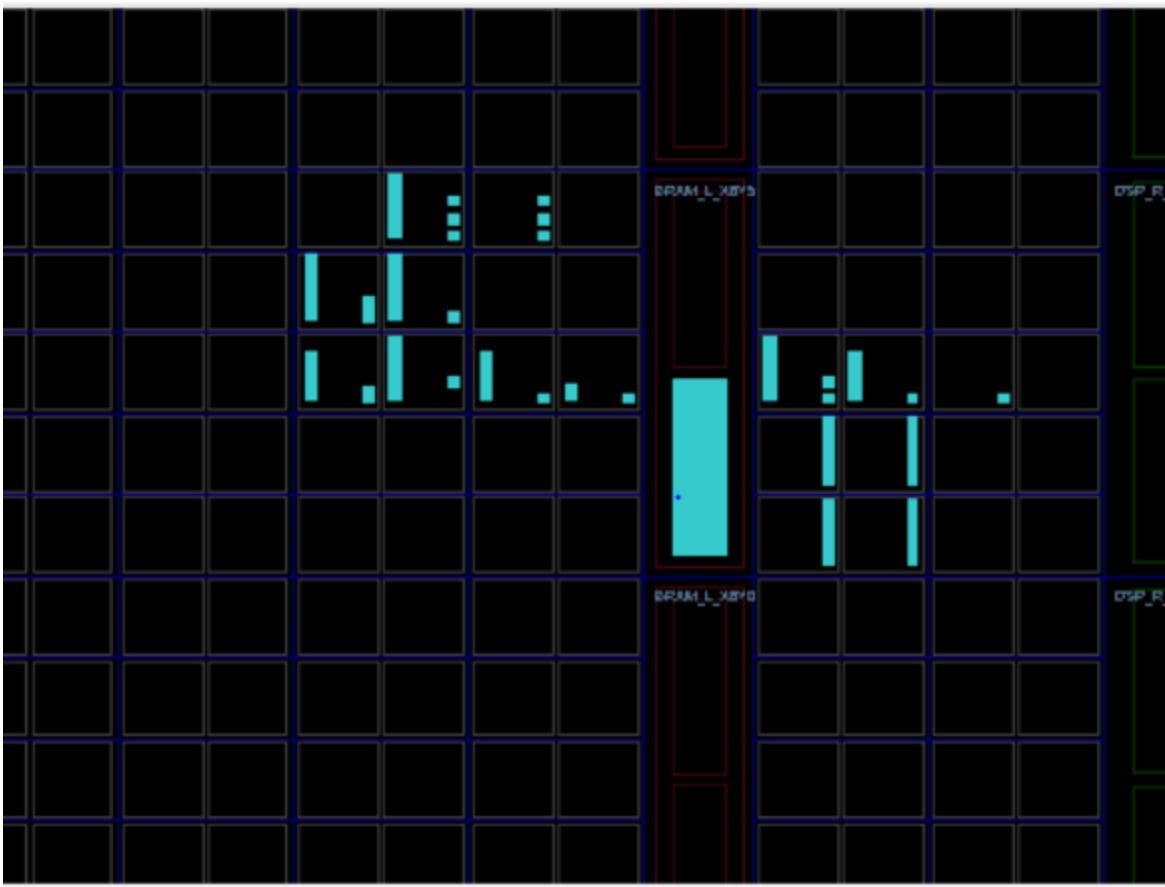
Q | H | E | C | B | General Information

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	5.547	2	1	mem/mem_reg/CLKBWRCLK	slave/MISO_reg/D	4.479	2.702	1.777	10.000	sys_clk	
Path 2	6.273	2	11	slave/counter_reg[2]/C	slave/rx_data_reg[0]/CE	3.382	1.078	2.304	10.000	sys_clk	
Path 3	6.273	2	11	slave/counter_reg[2]/C	slave/rx_data_reg[1]/CE	3.382	1.078	2.304	10.000	sys_clk	
Path 4	6.273	2	11	slave/counter_reg[2]/C	slave/rx_data_reg[2]/CE	3.382	1.078	2.304	10.000	sys_clk	
Path 5	6.273	2	11	slave/counter_reg[2]/C	slave/rx_data_reg[3]/CE	3.382	1.078	2.304	10.000	sys_clk	

Timing Summary - impl_1 (saved) × Timing Summary - timing_1 ×

- FPGA device snippet



Messages after bitstream generation

