SPI

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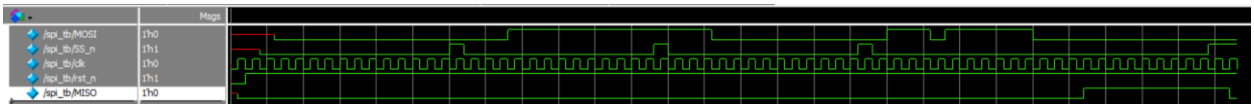
1) Snippets from the waveforms captured from QuestaSim

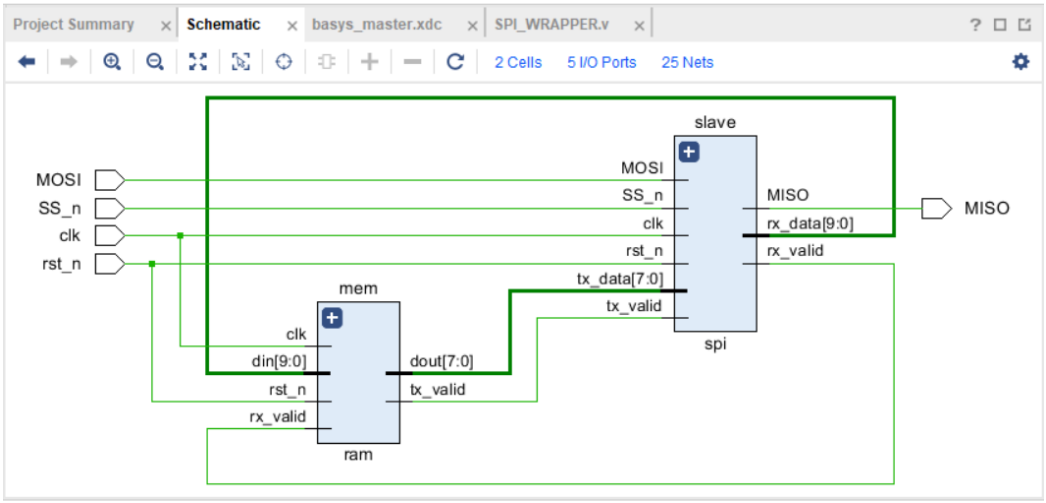


2) Synthesis snippets for each encoding

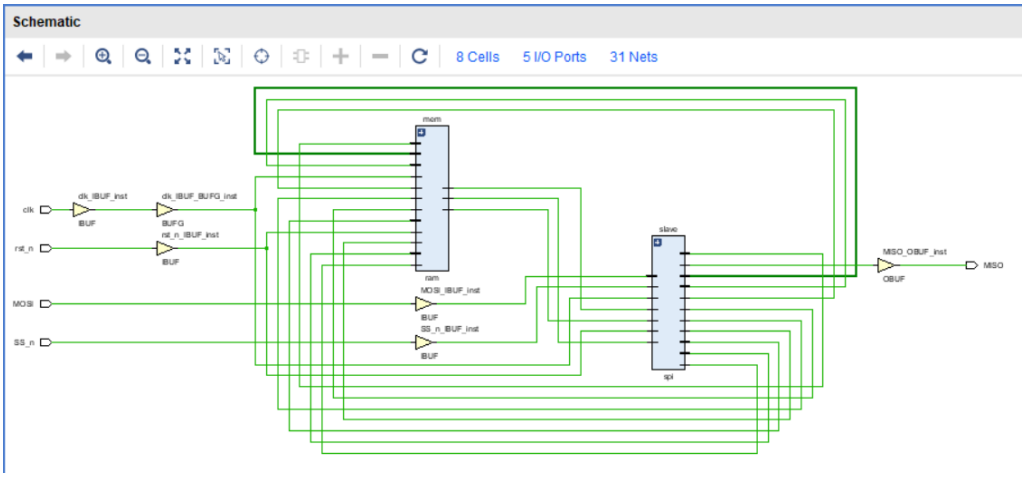
Grey

Schematic after the elaboration & synthesis

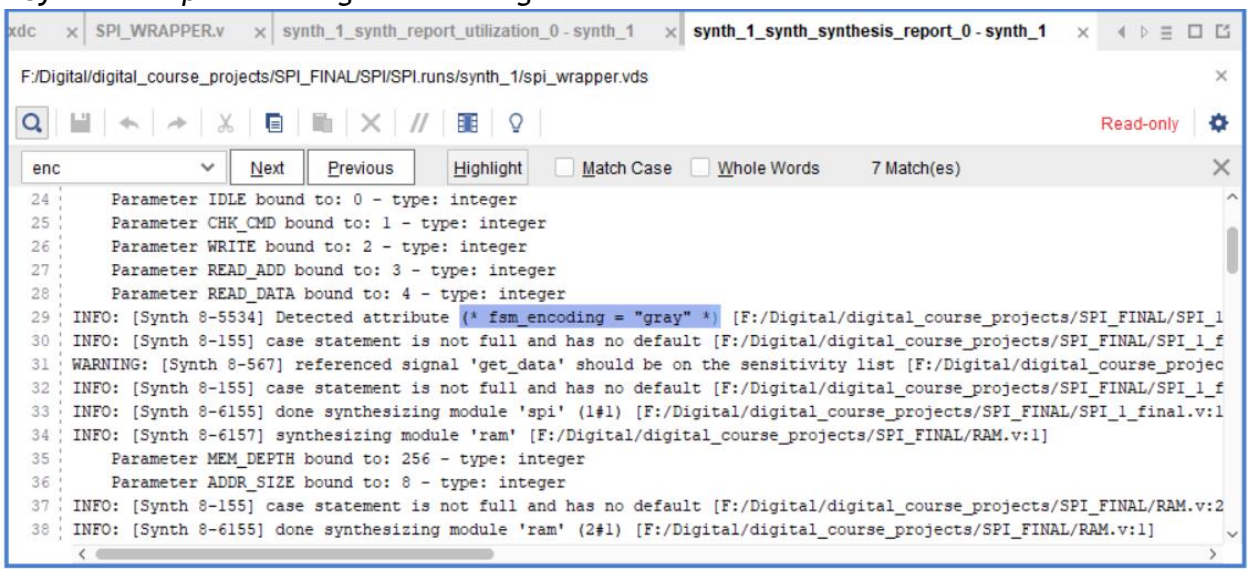
Elaborated



Synthesis



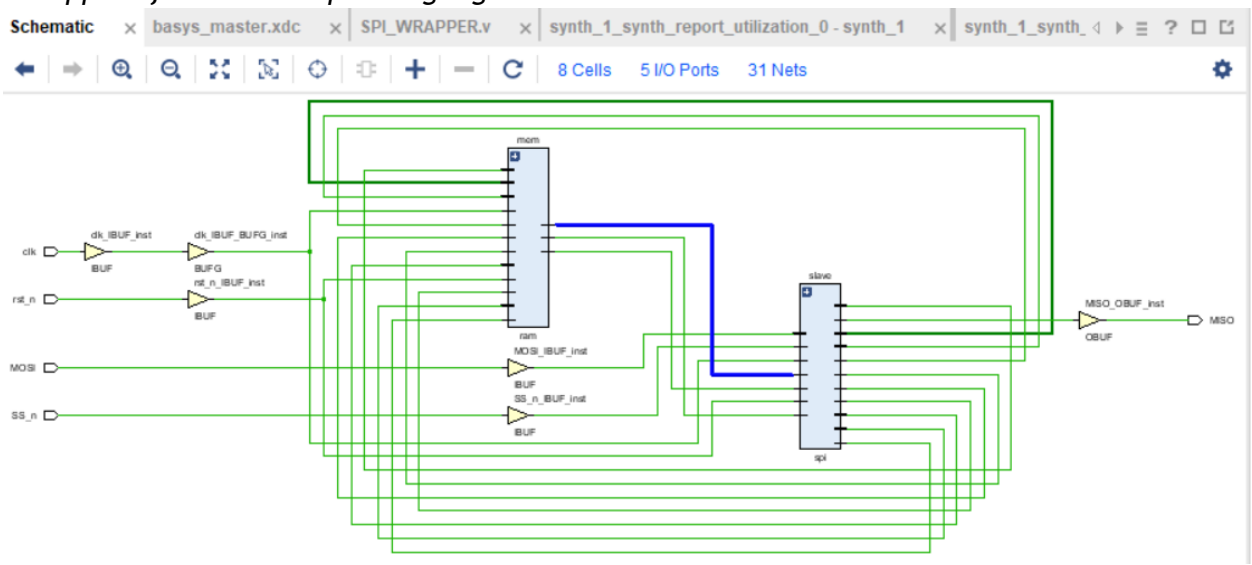
- *Synthesis report showing the encoding used*



- *Timing report snippet*

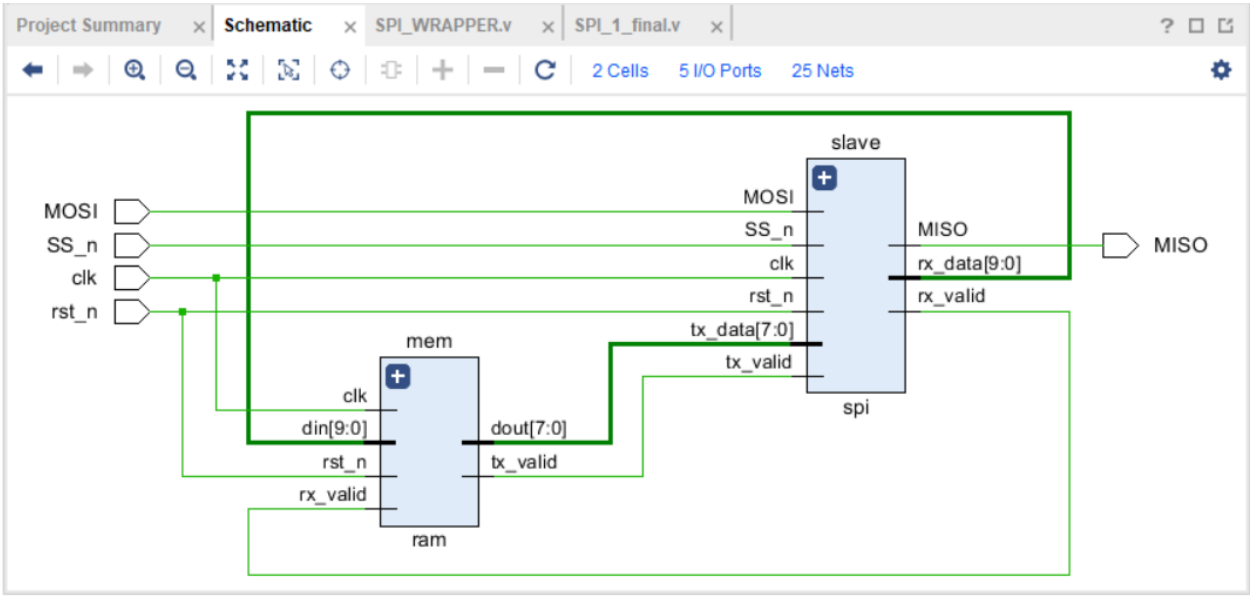
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requiremen
Path 1	5.898	2	3	1	mem/mem_reg/CLKBWRCLK	slave/MISO_reg/D	3.951	2.702	1.249	10.
Path 2	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[0]/CE	2.798	0.875	1.923	10.
Path 3	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[1]/CE	2.798	0.875	1.923	10.
Path 4	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[2]/CE	2.798	0.875	1.923	10.
Path 5	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[3]/CE	2.798	0.875	1.923	10.
Path 6	6.820	2	3	8	slave/counter_reg[4]/C	slave/counter_reg[4]/CE	2.798	0.875	1.923	10.

- *Snippet of the critical path highlighted in the schematic*

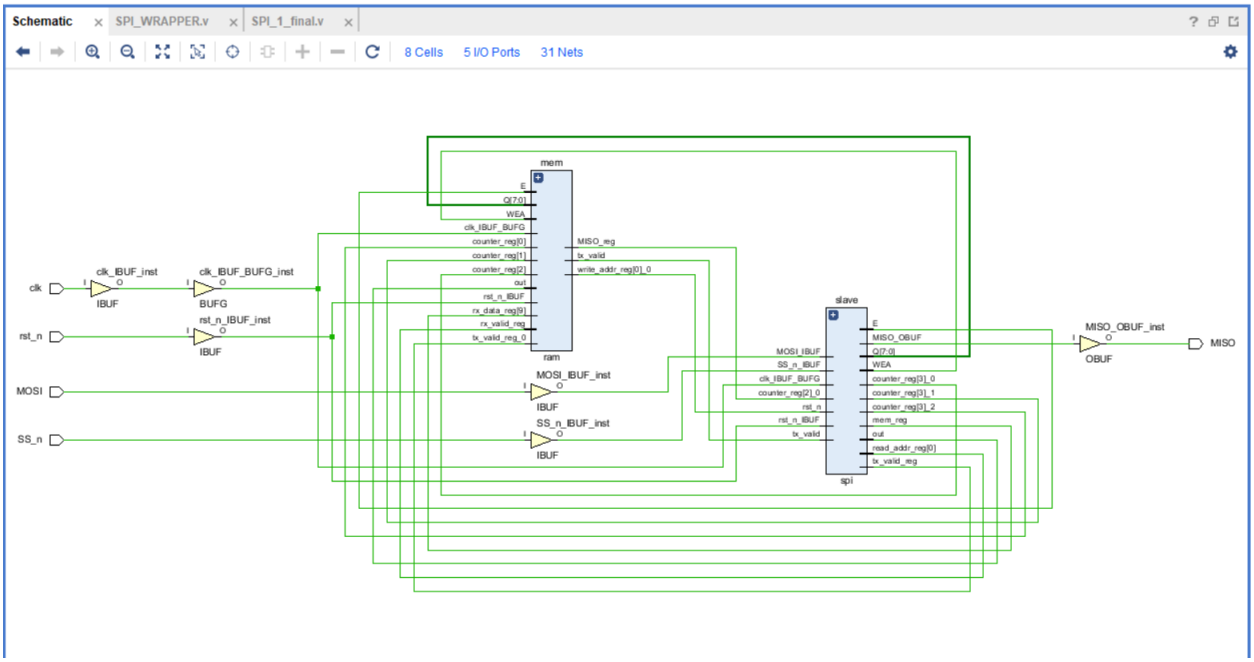


Hot one

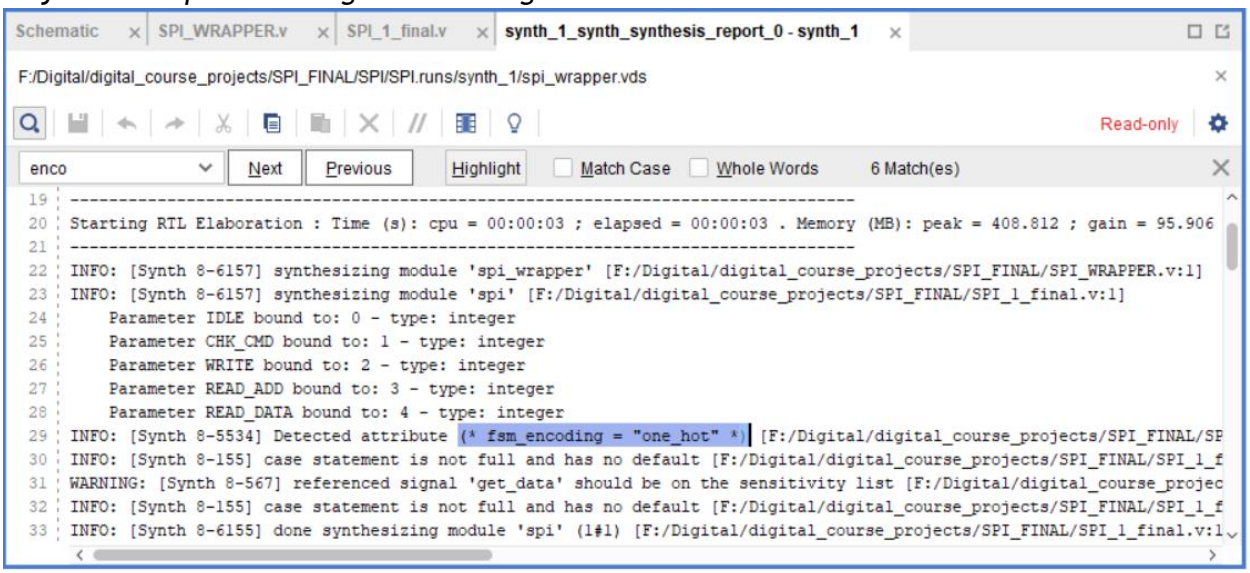
Elaborated



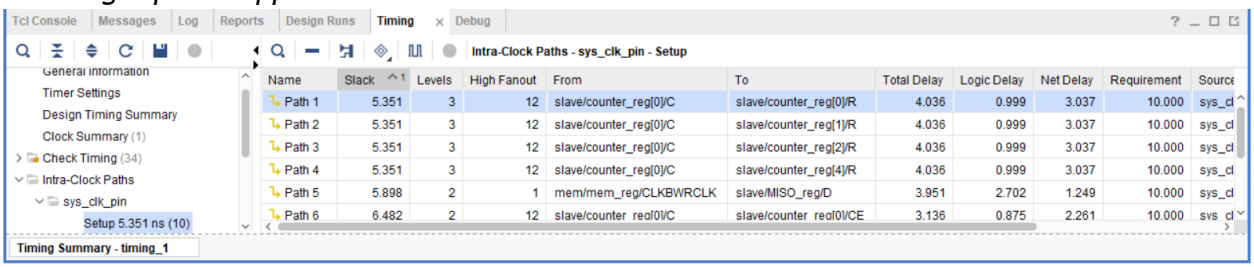
Synthesis



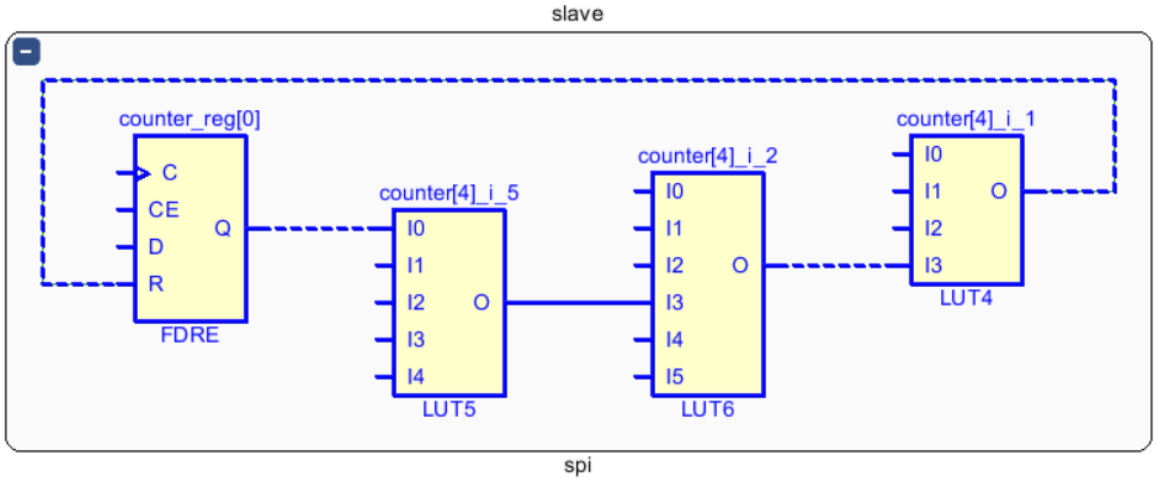
• *Synthesis report showing the encoding used*



• *Timing report snippet*

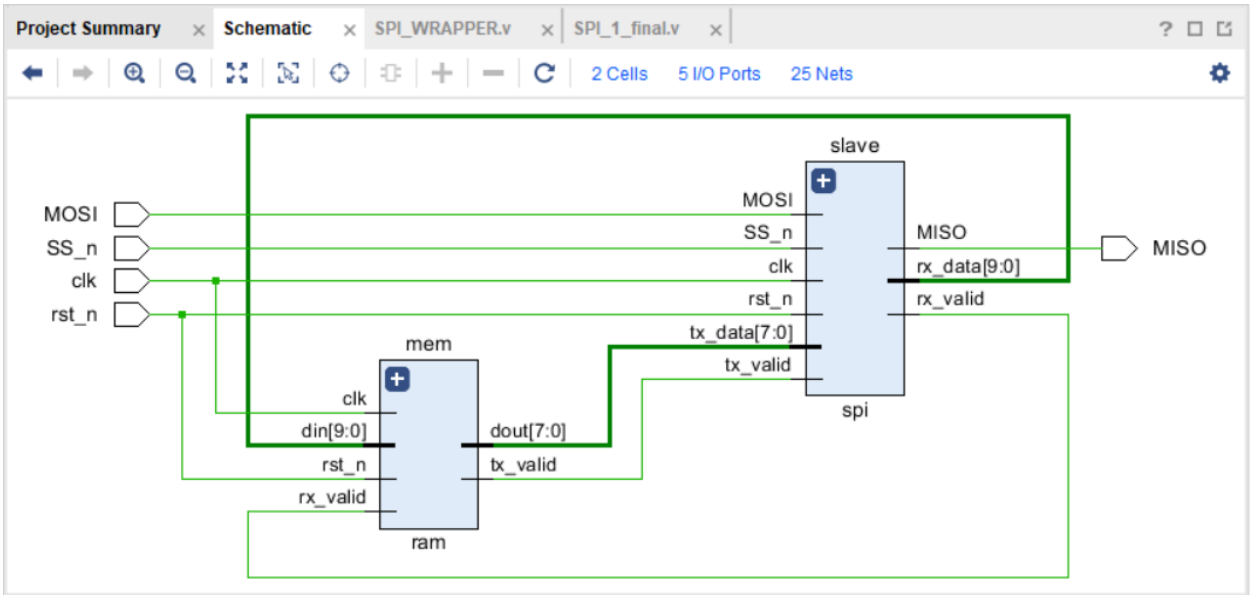


• *Snippet of the critical path highlighted in the schematic*

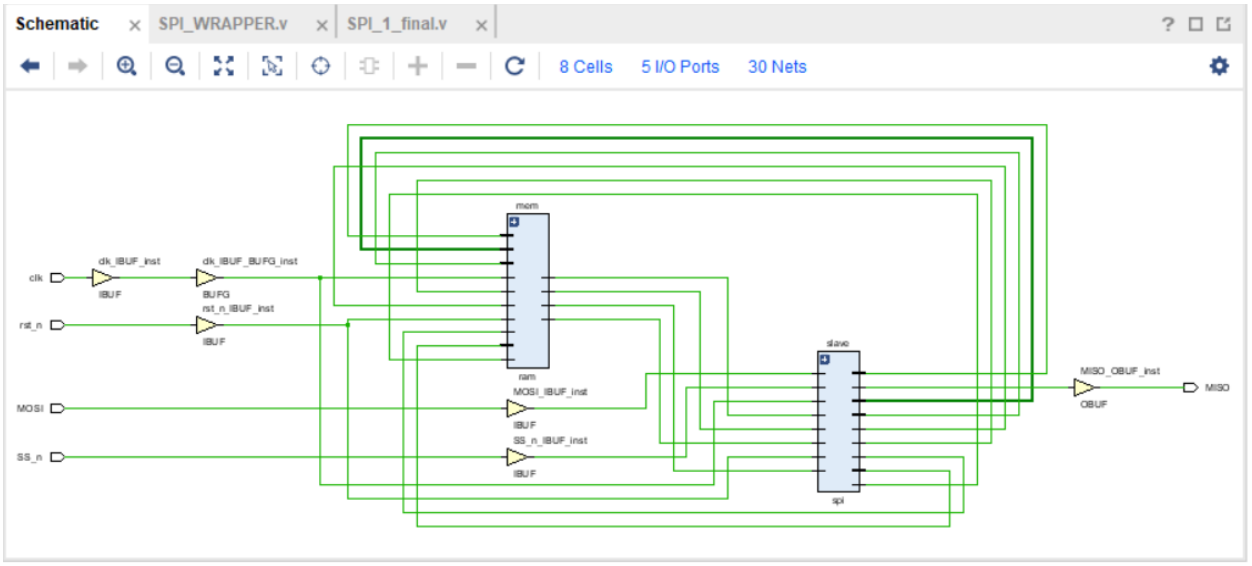


Seq

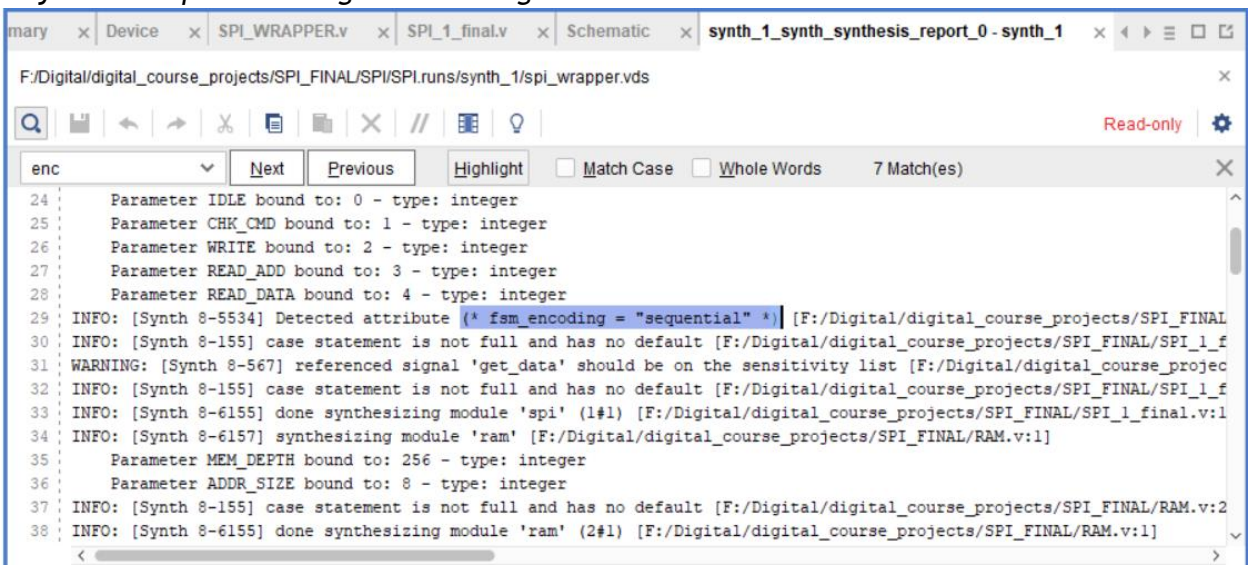
Elaborated


Project Summary
Schematic
SPI_WRAPPER.v
SPI_1_final.v
2 Cells
5 I/O Ports
25 Nets
slave
MOSI
SS_n
clk
rst_n
tx_data[7:0]
tx_valid
MISO
rx_data[9:0]
rx_valid
spi
mem
clk
din[9:0]
rst_n
rx_valid
dout[7:0]
tx_valid
ram
MOSI
SS_n
clk
rst_n
MISO

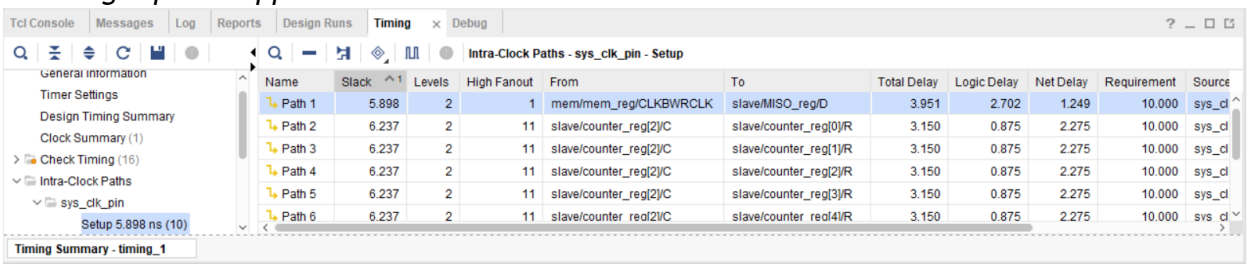
Synthesis


Schematic
SPI_WRAPPER.v
SPI_1_final.v
8 Cells
5 I/O Ports
30 Nets
mem
slave
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
rst_n
rst_n_IBUF_inst
IBUF
MOSI
MOSI_IBUF_inst
IBUF
SS_n
SS_n_IBUF_inst
IBUF
ram
spi
MISO_OBUF_inst
OBUF
MISO

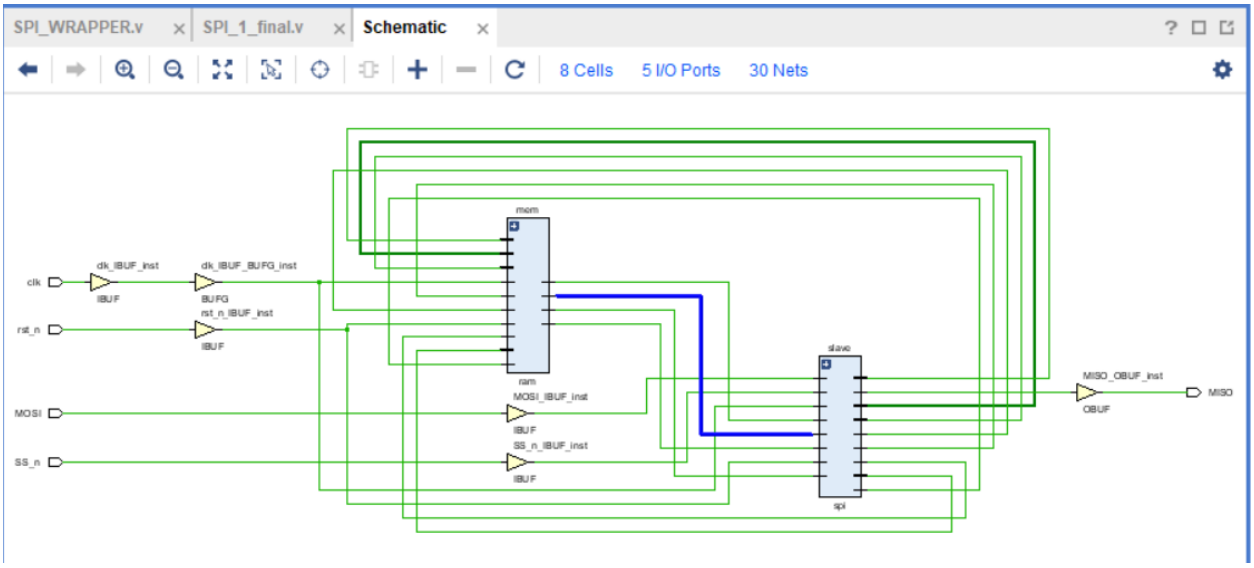
- *Synthesis report showing the encoding used*



- *Timing report snippet*



- *Snippet of the critical path highlighted in the schematic*



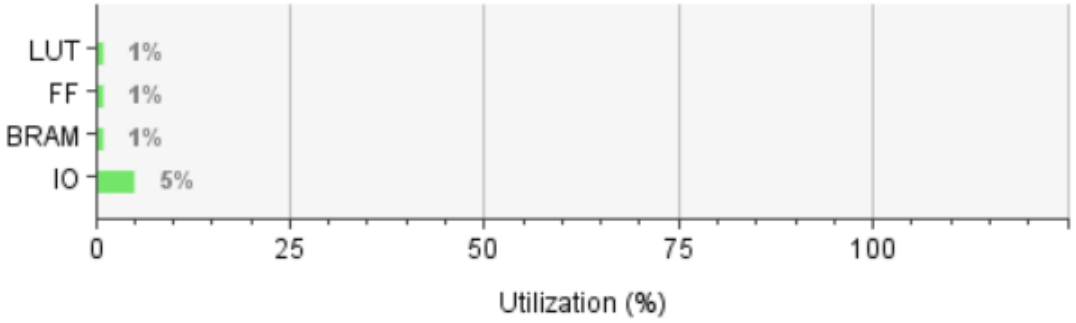
Implementation snippets for each encoding

grey

- Utilization report

Summary

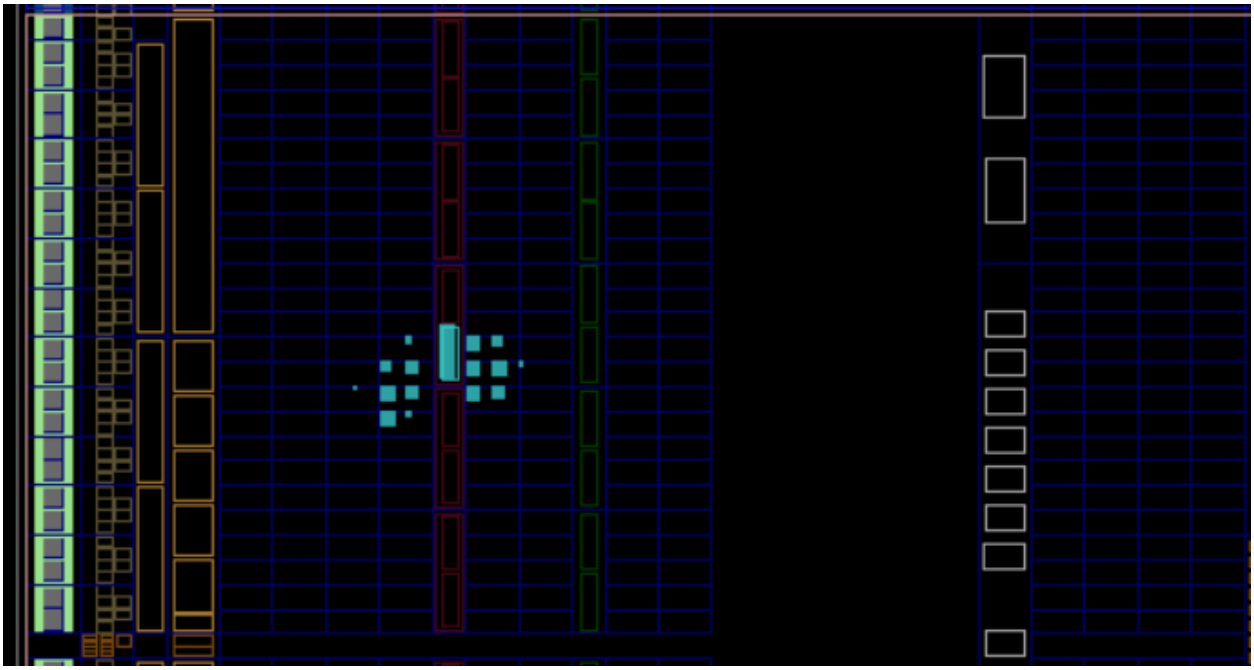
Resource	Utilization	Available	Utilization %
LUT	29	20800	0.14
FF	51	41600	0.12
BRAM	0.50	50	1.00
IO	5	106	4.72



- Timing report snippet

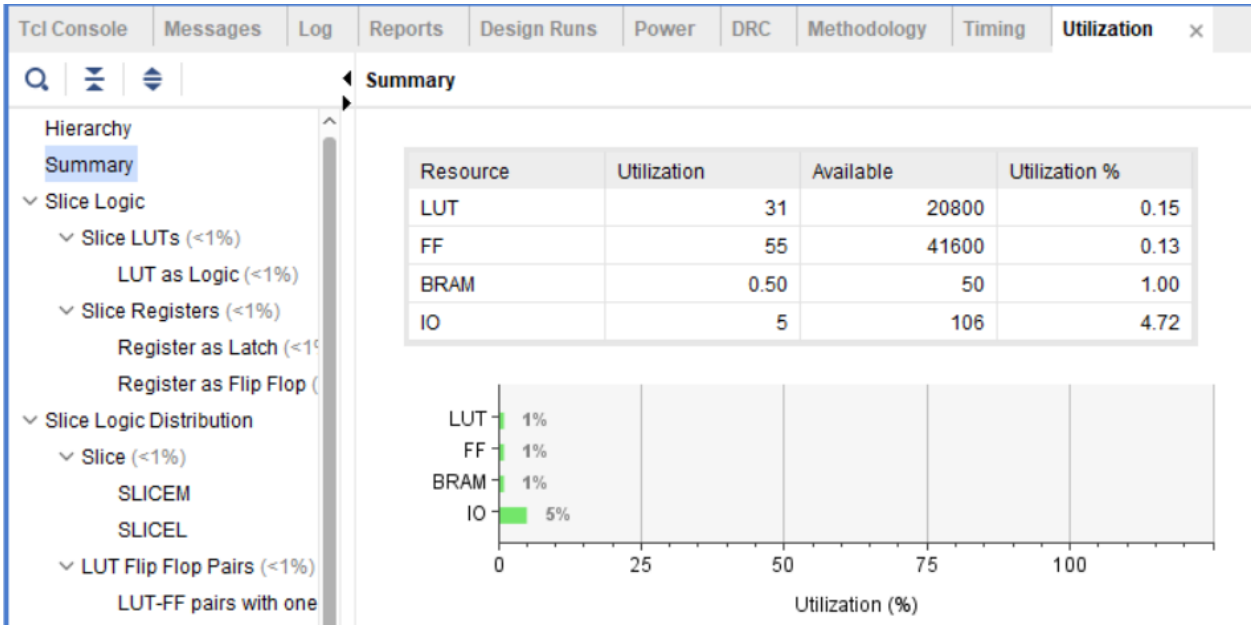
Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source C
Path 1	5.779	2	1	mem/mem_reg/CLKBWRCLK	slave/MISO_reg/D	4.250	2.702	1.548	10.000	sys_clk_
Path 2	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[0]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 3	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[2]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 4	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[3]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 5	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[4]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 6	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[5]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 7	6.624	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[6]/CE	3.033	0.956	2.077	10.000	sys_clk_
Path 8	6.795	2	14	slave/FSM_gray_cs_reg[2]/C	slave/counter_reg[4]/CE	2.939	0.766	2.173	10.000	sys_clk_
Path 9	6.808	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[1]/CE	2.885	0.956	1.929	10.000	sys_clk_
Path 10	6.808	2	10	slave/counter_reg[4]/C	slave/rx_data_reg[7]/CE	2.885	0.956	1.929	10.000	sys_clk_

- FPGA device snippet

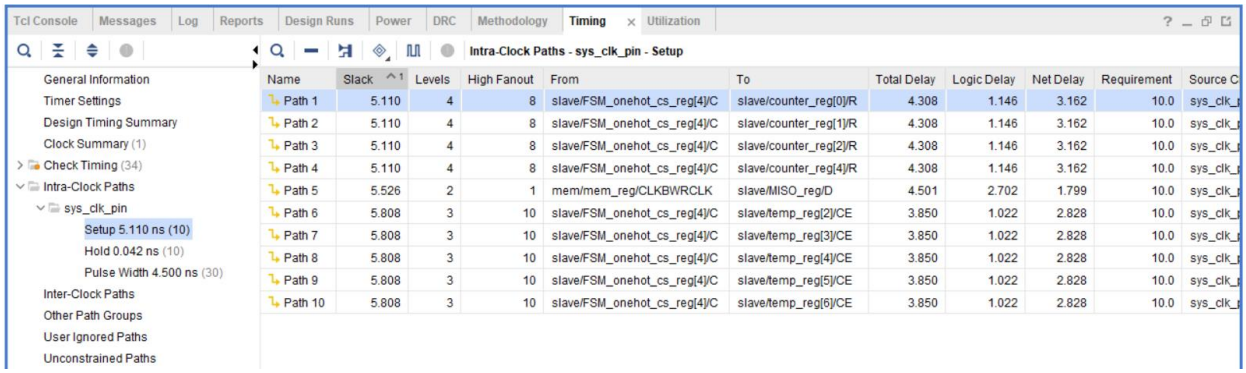


Hot one

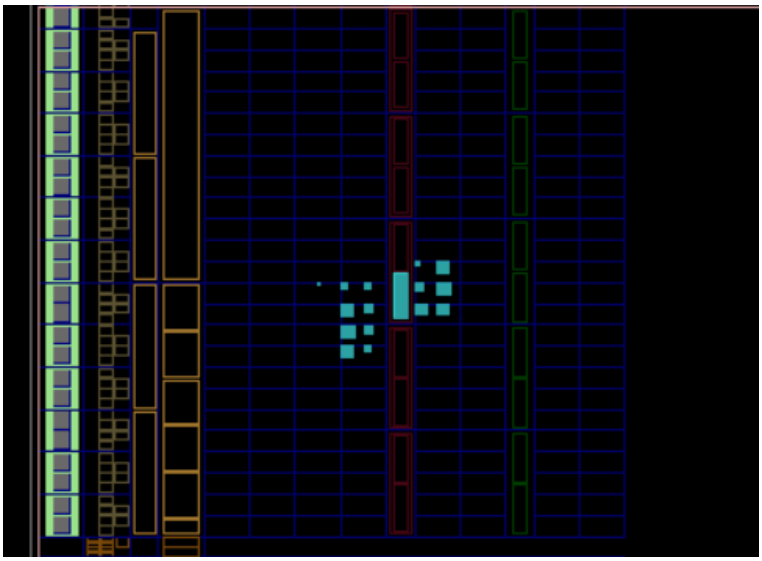
- Utilization report



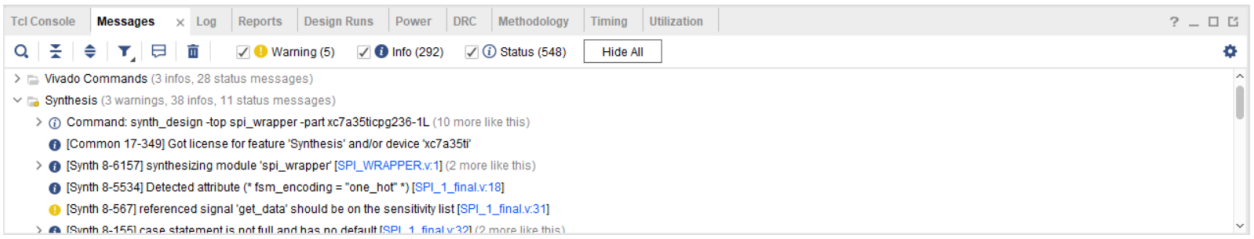
- Timing report snippet



- FPGA device snippet

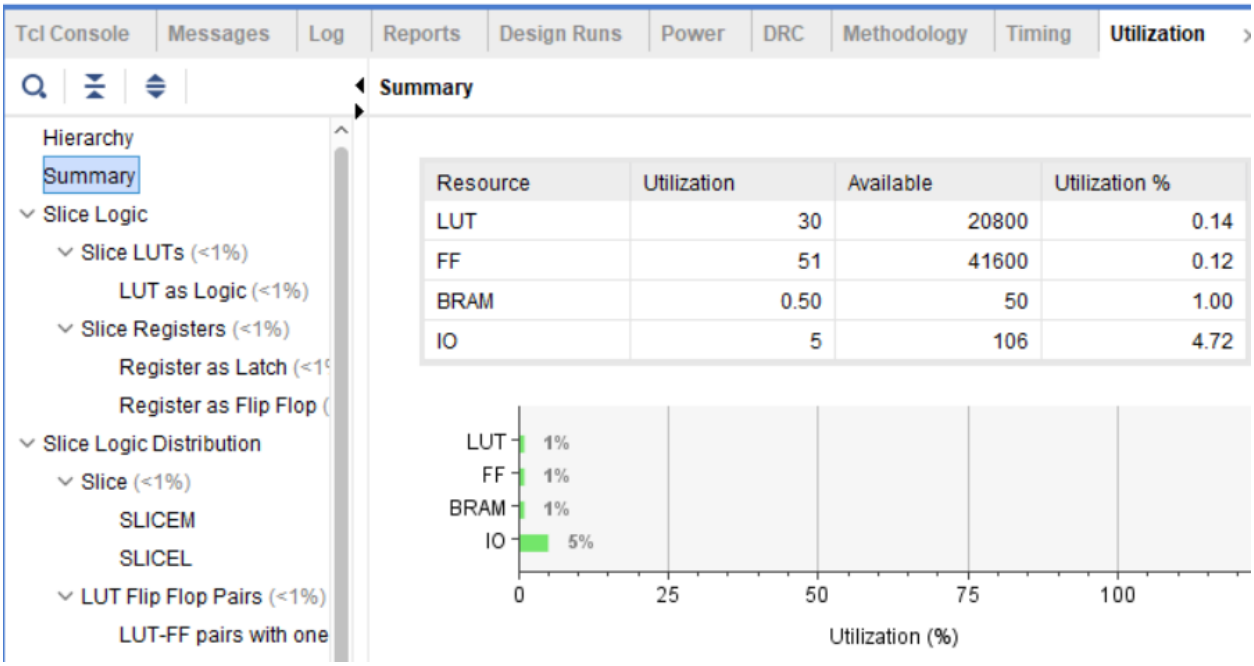


Messages after bitstream generation

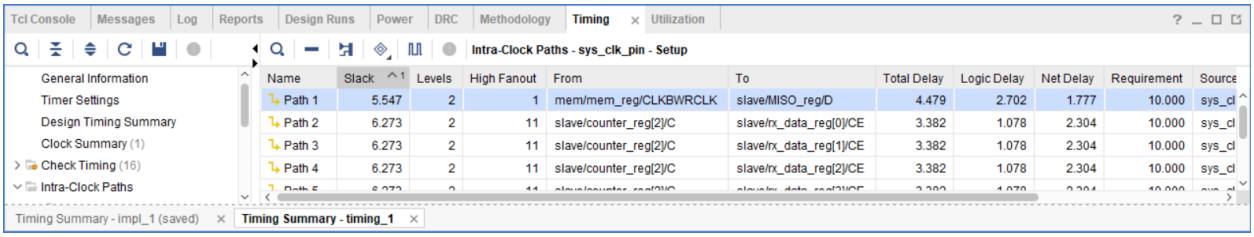


Seq

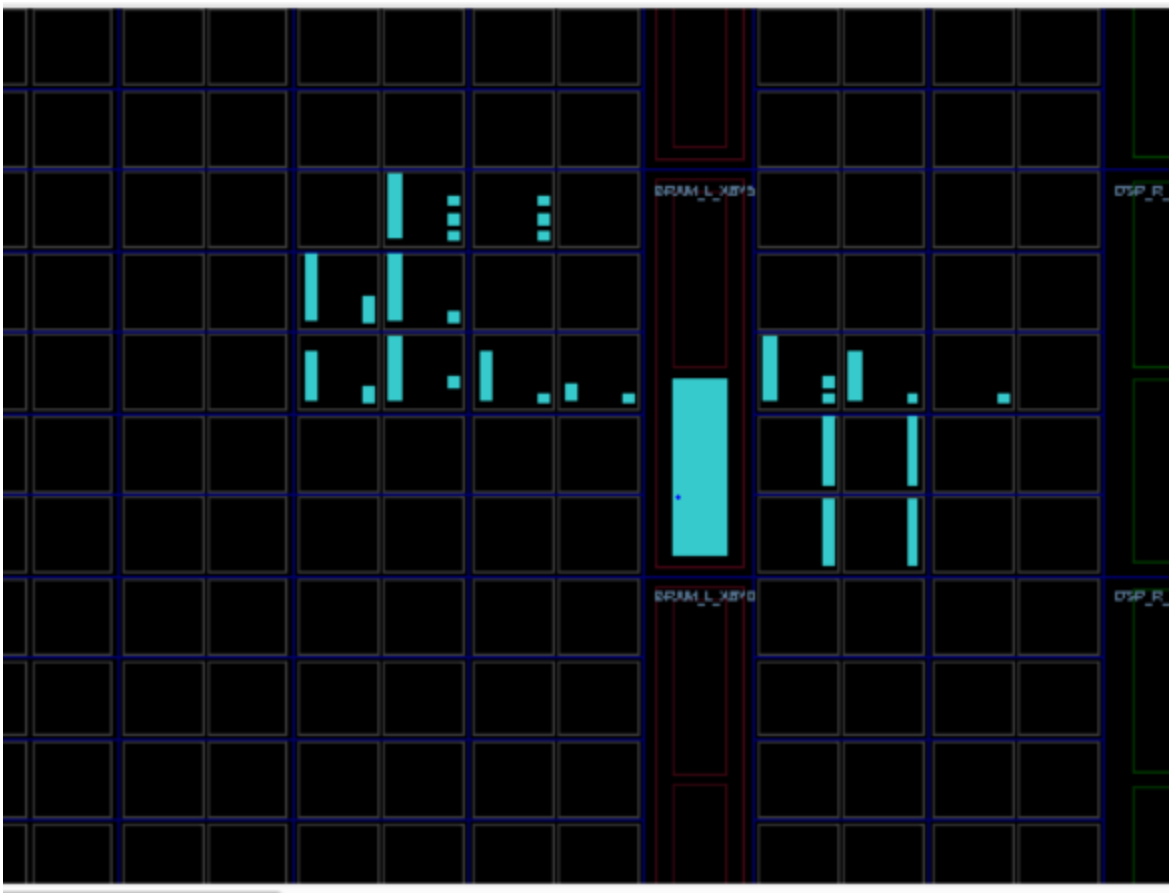
- Utilization report



- Timing report snippet



- FPGA device snippet



Messages after bitstream generation