

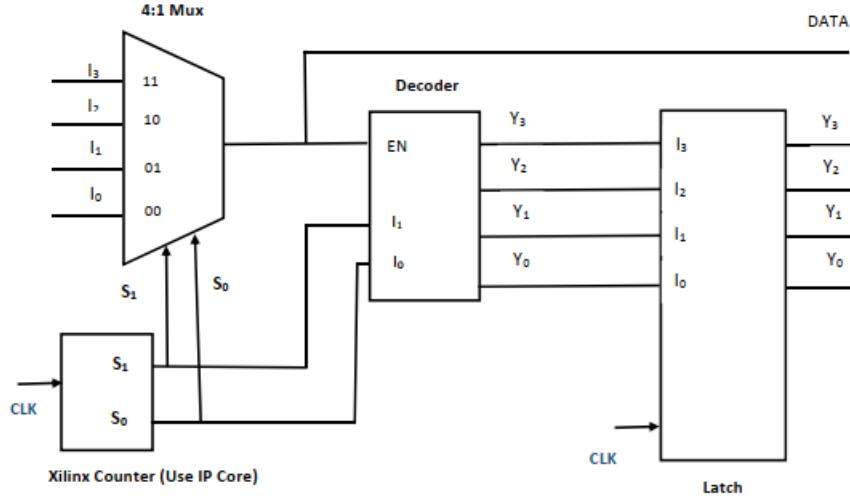
LAB Workshop on 'FPGA Architecture and Programming using Verilog HDL'

MINIPROJECT SUBMISSION

AMREEN KAUR

(fpga0722-amre62)

MINI PROJECT



Code the above design in verilog HDL and implement the same on the FPGA Kit allotted to you

Use Virtual input and Output IP Core for giving input I_3, I_2, I_1, I_0

CLK from the Kit.

Y₃ Y₂ Y₁ Y₀ need to be displayed on Chipscope IP Core.

1. *4-1 Mux use dataflow*
2. *Decoder use behaviour modeling*
3. *Latch use behaviour modeling*
4. *Counter- Use Xilinx IP Core.*
5. *Connect everything as miniproject.v and implement on the Kit*

1. 4-1 Mux (use dataflow).

Flow Navigator

Add Sources

Language Templates

 IP Catalog

Create Block Design

Open Block Design

Generate Block Design

▼ SIMULATION

Run Simulation

▼ RTI ANALYSIS

> Open Elaborated Design

▼ SYNTHESIS

Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1|

Project Summary x counter mini.v x mini proj.v * x

D:\IATEST PROGRAMS\Counter_top\Counter_top_srcs\sources_1\new\mini_proj.v

```
Q |  |  |  |  |  |  |  |  |  |  |  |   
7 // Design Name:  
8 // Module Name: mini_proj  
9 // Project Name:  
10 // Target Devices:  
11 // Tool Versions:  
12 // Description:  
13 //  
14 // Dependencies:  
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////////////////////////////////  
21  
22  
23 module mini_proj(  
24  
25  
26 );  
27 // counter ip  
28 c_counter_binary_0 counter(  
29 .CLK(clk), // input wire CLK  
30 .Q(count) // output wire [1 : 0] count  
31 );  
32  
33 //mux  
34 assign s1 = count[1]; //o/p of counter to select line of mux  
35 assign s0 = count[0];  
36 assign output_mux = (!s1&(!s0)&i0) | (!s1&s0&i1) | (s1&(!s0)&i2) | (s1&s0&i3); //output of mux using dataflow  
37 assign en = output_mux; //o/p of mux to enable of decoder
```

Tcl Console Messages Log Reports Design Runs

38:1 Insert Verilog

2. Decoder use (behavioral modeling)

Flow Navigator

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

► Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary x counter_mini.v x mini_proj.v *

D:/LATEST PROGRAMS/Counter_top/Counter_top.srsc/sources_1/new/mini_proj.v



```
35 assign s0 = count[0];
36 assign output_mux = (! (s1) & (! (s0)) & (i0)) | (! (s1) & (s0) & (i1)) | (s1 & (! (s0)) & i2) | (s1 & s0 & i3); //output of mux using dataflow
37 assign en = output_mux; //o/p of mux to enable of decoder
38
39 // decoder
40 always @(s1,s0) //sensitive to decoder i/p
41 begin
42 if (en == 0)
43 begin
44 k0 = 1'b0; k1 = 1'b0 ; k2 = 1'b0 ; k3 = 1'b0; //o/p using behavioral
45 end
46 else
47 begin
48 if ( s1 == 0 & s0 == 0) begin
49 k0 = 1; k1 = 0; k2 = 0; k3 = 0;
50 end
51 else if ( s1 == 0 & s0 == 1) begin
52 k0 = 0; k1 = 1; k2 = 0; k3 = 0;
53 end
54 else if ( s1 == 1 & s0 == 0) begin
55 k0 = 0; k1 = 0; k2 = 1; k3 = 0;
56 end
57 else begin
58 k0 = 0; k1 = 0; k2 = 0; k3 = 1;
59 end
60 end
61 end
62
63
64 endmodule
65
```

3. Latch use (behavioral modeling)

Flow Navigator

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

► Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary x counter_mini.v x mini_proj.v *

D:/LATEST PROGRAMS/Counter_top/Counter_top.srsc/sources_1/new/mini_proj.v



```
63 //latch
64 always @(*)
65 begin
66 if ( k0 == 1 )
67 begin
68 if ( clk == 1)
69 y0 <= k0;
70 else
71 y0 <= y0;
72 end
73 else if ( k1 == 1 ) //latch i/p=o/p of decoder
74 begin
75 if ( clk == 1)
76 y1 <= k1; //o/p using behavioral
77 else
78 y1 <= y1;
79 end
80 else if ( k2 == 1 )
81 begin
82 if ( clk == 1)
83 y2 <= k2;
84 else
85 y2 <= y2;
86 end
87 else if ( k3 == 1)
88 begin
89 if ( clk == 1)
90 y3 <= k3;
91 else
92 y3 <= y3;
93 end
```

4. Counter- Use Xilinx IP Core.

- The slides(3 &4) that follow show the code made for the **counter** used in the miniproject(made using **IP Core**)and its **simulation and synthesis results**. It is once done separately to show how to use a counter from Xilinx IP Core. It is then followed by the code used in the miniproject.

Flow Navigator

PROJECT MANAGER - Counter_top

PROJECT MANAGER

Settings

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

Run Synthesis

> Open Synthesized Design

IMPLEMENTATION

Run Implementation

> Open Implemented Design

PROGRAM AND DEBUG

Project Summary

counter_mini.v *

IP Catalog

c_counter_binary_0.vo

D:/LATEST PROGRAMS/Counter_top/Counter_top.srsc/sources_1/new/counter_mini.v



```
2 //////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 20.08.2022 19:57:08
7 // Design Name:
8 // Module Name: counter_mini
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:|
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////
21
22
23 module counter_mini(
24     input clk,
25     output [1:0] count
26 );
27 c_counter_binary_0 minip (
28     .CLK(clk), // input wire CLK
29     .Q(count) // output wire [1 : 0] Q
30 );
31 endmodule
32
```

File Edit Flow Tools Reports Window Layout View Run Help Q: Quick Access

10 us

Default Layout

Flow Navigator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

SIMULATION - Behavioral Simulation - Functional - sim_1 - counter_mini

counter_mini.v c_counter_binary_0.vo Untitled 1

Scope Sources Objects Protocol Instances

Name Value

Name	Value
clk	0
co...	00

9,000.000 ns 9,500.000 ns 10,000.000 ns 10,500.000 ns 11,000.000 ns 11,500.000 ns

Tcl Console Messages Log

Sim Time: 11 us

The screenshot shows the Vivado 2021.2 simulation interface for a behavioral simulation of a counter. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Run, Help, and a Quick Access search bar. The main window title is "SIMULATION - Behavioral Simulation - Functional - sim_1 - counter_mini". The left sidebar contains sections for Project Manager, IP Integrator, Simulation, RTL Analysis, Synthesis, Implementation, and Program and Debug. The "SIMULATION" section is currently selected. The main workspace displays a waveform for "counter_mini.v" and "c_counter_binary_0.vo". A table shows the values for "clk" and "co...". The waveform shows a binary counter starting at 00 and incrementing by 1 every 500ns. The simulation time is set to 11 us. The bottom status bar shows the current simulation time as 11 us.

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Synthesis Complete ✓

Default Layout

Flow Navigator

- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design**
- Constraints Wizard
- Edit Timing Constraints
- Set Up Debug
- Report Timing Summary
- Report Clock Networks
- Report Clock Interaction
- Report Methodology

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary Device counter_mini.v c_counter_binary_0.veo

Netlist IP Properties Sources

Tcl Console Messages Log Reports Design Runs

Flow Navigator

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

▶ Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary x counter_mini.v x mini_proj.v *

D:/LATEST PROGRAMS/Counter_top/Counter_top.srsc/sources_1/new/mini_proj.v



```
4 // Engineer:  
5 //  
6 // Create Date: 20.08.2022 20:52:13  
7 // Design Name:  
8 // Module Name: mini_proj  
9 // Project Name:  
10 // Target Devices:  
11 // Tool Versions:  
12 // Description:  
13 //  
14 // Dependencies:  
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////////////////////////////////  
21  
22  
23 module mini_proj(  
24  
25  
26 );  
27 // counter ip  
28 c_counter_binary_0 counter(  
29 .CLK(clk), // input wire CLK  
30 .Q(count) // output wire [1 : 0] count|  
31 );  
32  
33 endmodule  
34
```

Tcl Console Messages Log Reports Design Runs

30:40 Insert Verilog

5. Connect everything as miniproject.v and implement on the Kit

Flow Navigator

[Add Sources](#)[Language Templates](#)[IP Catalog](#)

IP INTEGRATOR

[Create Block Design](#)[Open Block Design](#)[Generate Block Design](#)

SIMULATION

[Run Simulation](#)

RTL ANALYSIS

[Open Elaborated Design](#)

SYNTHESIS

[Run Synthesis](#)

Open Synthesized Design

[Constraints Wizard](#)[Edit Timing Constraints](#)[Set Up Debug](#)[Report Timing Summary](#)[Report Clock Networks](#)[Report Clock Interaction](#)[Report Methodology](#)

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary

counter_mini.v

mini_proj.v *

D:/LATEST PROGRAMS/Counter_top/Counter_top.srsc/sources_1/new/mini_proj.v

[Source File Properties](#)[Netlist](#)[Sources](#)[Search](#)[Find](#)[Find Next](#)[Find Previous](#)[Replace](#)[Delete](#)[Copy](#)[Paste](#)[Delete](#)[Comment](#)[Uncomment](#)[Format](#)[Select All](#)[Select Line](#)[Select Block](#)[Select Column](#)[Select Range](#)[Select All Lines](#)[Select All Columns](#)[Select All Ranges](#)[Select All Lines and Columns](#)[Select All Ranges and Columns](#)[Select All Lines and Ranges](#)[Select All Lines, Columns, and Ranges](#)[Select All Lines, Columns, Ranges, and Columns](#)[Select All Lines, Ranges, and Ranges](#)[Select All Lines, Columns, and Ranges](#)[Select All Lines, Columns, Ranges, and Ranges](#)

```
75 if ( clk == 1)
76     y1 <= k1; //o/p using behavioral
77     else
78     y1 <= y1;
79 end
80 else if ( k2 == 1 )
81 begin
82     if ( clk == 1)
83         y2 <= k2;
84     else
85         y2 <= y2;
86 end
87 else if ( k3 == 1 )
88 begin
89     if ( clk == 1)
90         y3 <= k3;
91     else
92         y3 <= y3;
93 end
94 end
95
96 assign Y0 = y0; //latch fin
97 assign Y1 = y1;
98 assign Y2 = y2;
99 assign Y3 = y3;
100 assign data_out = output_mux; //data output
101
102
103
104 endmodule
105
```

Tcl Console Messages Log Reports Design Runs

95:1 Insert Verilog

**Use Virtual input and Output IP Core for giving input
I3, I2, I1, I0**

Flow Navigator

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

► Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary

counter_mini.v

mini_proj.v *

D:/LATEST PROGRAMS/Counter_top/Counter_top.srsc/sources_1/new/mini_proj.v

```
23 module mini_proj(
24   clk,Y0,Y1,Y2,Y3,data_out
25 );
26
27   input clk ;
28   wire [1:0] count;
29   wire output_mux;
30   wire en;
31   reg k0,k1,k2,k3;
32   reg y0,y1,y2,y3;
33   output Y0,Y1,Y2,Y3,data_out;
34
35 // counter ip
36 c_counter_binary_0 counter(
37   .CLK(clk), // input wire CLK
38   .Q(count) // output wire [1 : 0] count
39 );
40
41 ///inputs for virtual input and output -- vio ip
42 vio_0 inputs (
43   .clk(clk), // input wire clk
44   .probe_out0(i3), // output wire probes
45   .probe_out1(i2),
46   .probe_out2(i1),
47   .probe_out3(i0)
48 );
49
50 //mux
51 assign s1 = count[1]; //o/p of counter to select line of mux
52 assign s0 = count[0];
53 assign output_mux = (! (s1)&(! (s0))&(i0)) | (! (s1)&(s0)&(i1)) | (s1&(! (s0))&i2) | (s1&s0&i3) ; //output of mux using dataflow
54 assign output_mux = !output_mux; //in of mux to enable of decoder
```

Tcl Console Messages Log Reports Design Runs

127:1 Insert Verilog

Y3 Y2 Y1 Y0 need to be displayed on Chipscope IP Core.

Flow Navigator

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

► Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary x counter_mini.v x mini_proj.v *

D:/LATEST PROGRAMS/Counter_top/Counter_top.srsc/sources_1/new/mini_proj.v



```
102     y2 <= y2;
103 end
104 else if ( k3 == 1)
105 begin
106     if ( clk == 1)
107         y3 <= k3;
108     else
109         y3 <= y3;
110 end
111 end
112
113 assign Y0 = y0; //latch fin
114 assign Y1 = y1;
115 assign Y2 = y2;
116 assign Y3 = y3;
117 assign data_out = output_mux; //data output
118
119 // Integrated Logic Analyzer (ILA) for outputs
120 ila_3 latch_output (
121     .clk(clk), // input wire clk
122     .probe0(Y0), // input wire probes
123     .probe1(Y1),
124     .probe2(Y2),
125     .probe3(Y3),
126     .probe4(data_out)
127 );
128
129 endmodule
130
```

Tcl Console Messages Log Reports Design Runs

130:1 Insert Verilog

File Edit Flow Tools Reports Window Layout View Run Help Quick Access

Synthesis and Implementation Out-of-date details !

Default Layout

Flow Navigator Add Sources Language Templates IP Catalog

IP INTEGRATOR Create Block Design Open Block Design Generate Block Design

SIMULATION Run Simulation

RTL ANALYSIS Open Elaborated Design

SYNTHESIS Run Synthesis Open Synthesized Design

IMPLEMENTATION Run Implementation Open Implemented Design

PROGRAM AND DEBUG Generate Bitstream Open Hardware Manager

SIMULATION - Behavioral Simulation - Functional - sim_1 - mini_proj

mini_proj.v Untitled 1

Scope Sources Objects Protocol Instances

Name Value

Name	Value
clk	1
count[1:0]	01
output_mux	1
en	1
k0	0
k1	1
k2	0
k3	0
y0	1
y1	1
y2	X
y3	X
Y0	1
Y1	1
Y2	X
Y3	X
data_out	1
i3	0
i2	0
i1	1

508,434,200.000 ns 508,434,300.000 ns 508,434,400.000 ns 508,434,500.000 ns 508,434,600.000 ns 508,434,650.000 ns 508,434,700.000 ns

Tcl Console Messages Log

Current time: 516282550 ns... Cancel Sim Time: 517924750 ns

83°F Cloudy ENG IN 20:20 21-08-2022 1

Flow Navigator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates

IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

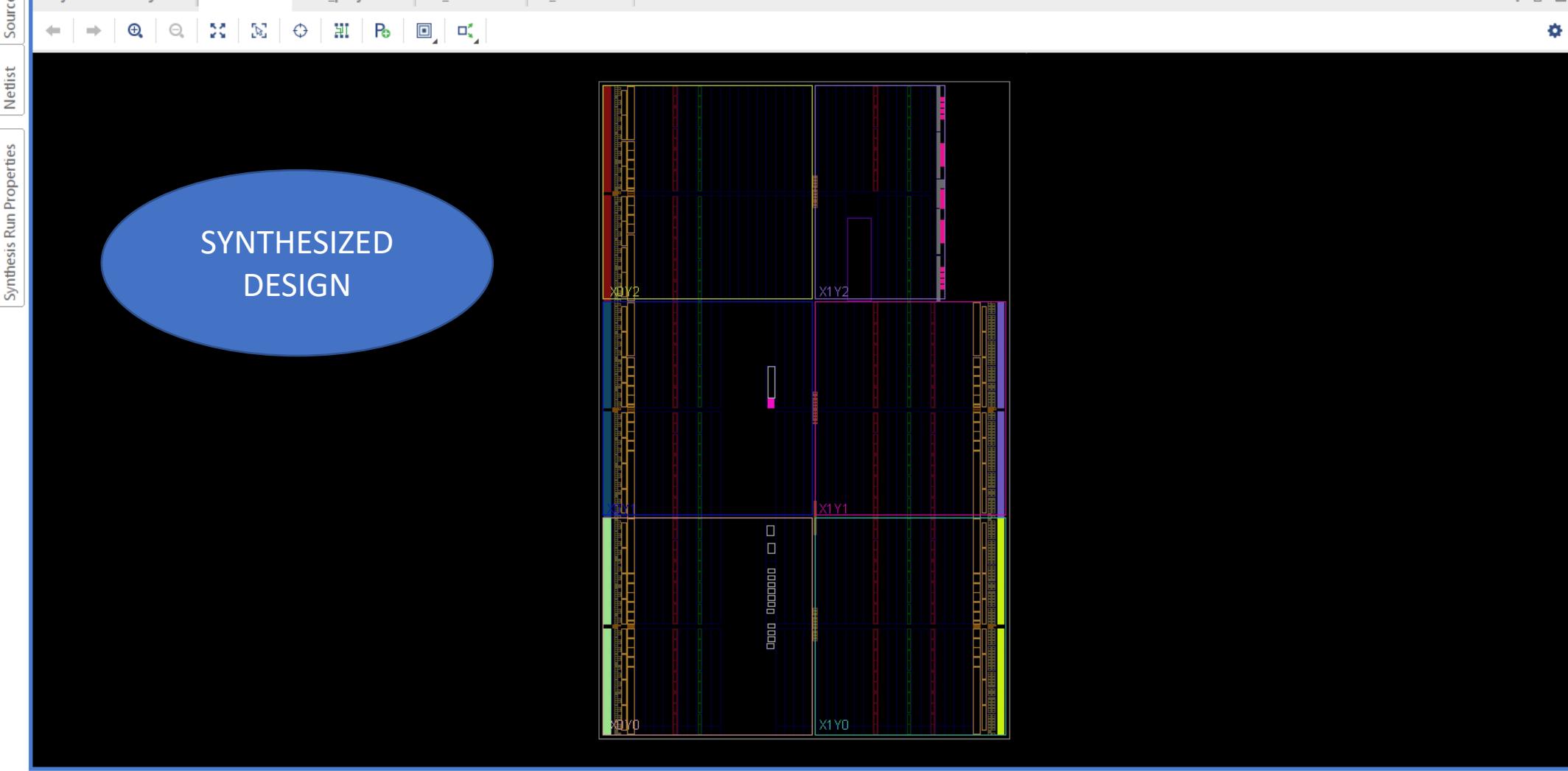
- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary Device mini_proj.v vio_0.veo ila_0.veo



Tcl Console Messages Log Reports Design Runs

Flow Navigator

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

SYNTHESIS

> Run Synthesis

Open Synthesized Design

Constraints Wizard

Edit Timing Constraints

Set Up Debug

Report Timing Summary

Report Clock Networks

Report Clock Interaction

Report Methodology

Report DRC

Report Noise

Report Utilization

Report Power

Schematic

IMPLEMENTATION

> Run Implementation

SYNTHESIZED DESIGN - synth_1 | xc7a35ticsg324-1L

Project Summary Device mini_proj.v Schematic

19 Cells 6 I/O Ports 132 Nets

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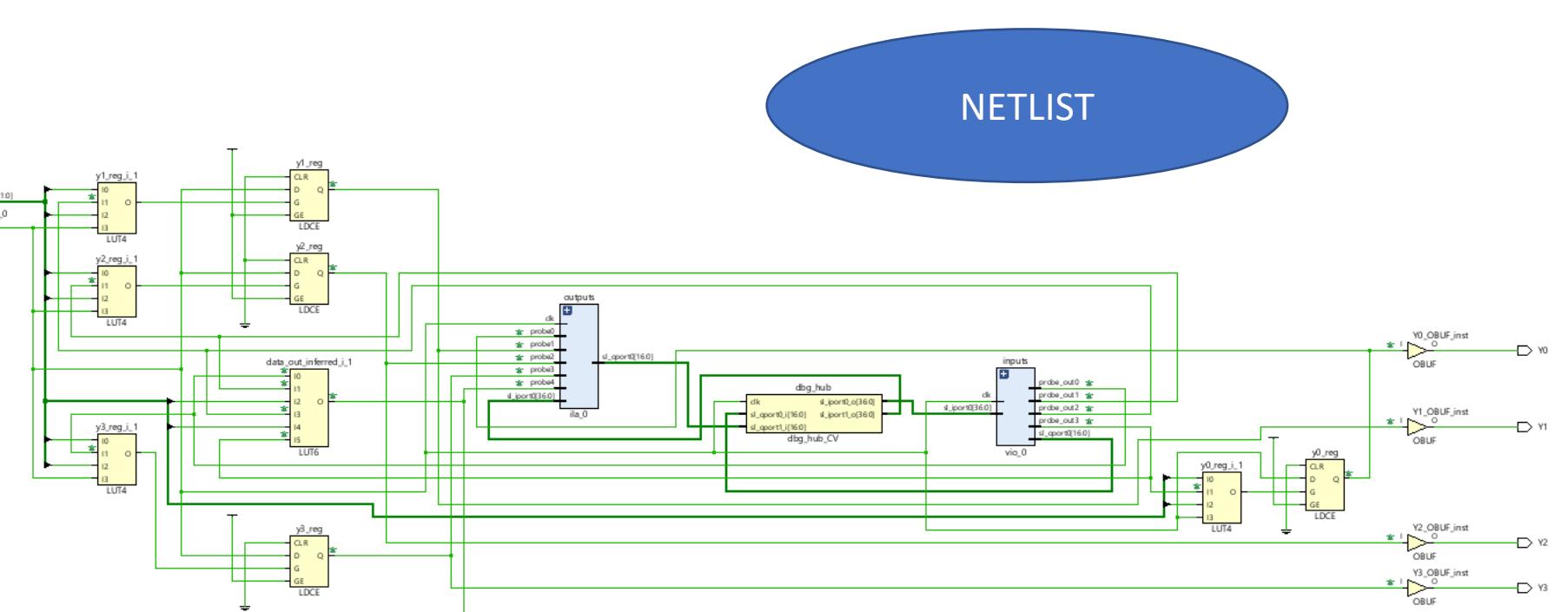
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Tcl Console Messages Log Reports Design Runs

mini_proj_1 - [D:/LATEST PROGRAMS/mini_proj_1/mini_proj_1.xpr] - Vivado 2021.2

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access Implementation Complete ✓ I/O Planning ? x

Flow Navigator Add Sources Language Templates IP Catalog

IP INTEGRATOR Create Block Design Open Block Design Generate Block Design

SIMULATION Run Simulation

RTL ANALYSIS > Open Elaborated Design

SYNTHESIS ▶ Run Synthesis > Open Synthesized Design

IMPLEMENTATION ▶ Run Implementation ▶ Open Implemented Design Constraints Wizard Edit Timing Constraints Report Timing Summary Report Clock Networks

IMPLEMENTED DESIGN - xc7a35ticsg324-1L

Package Device mini_proj.v

Sources Netlist Device Constraints Source File Properties Clock Regions

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

A B C D E F G H J K L M N P R T U V

IMPLEMENTED DESIGN

Tcl Console Messages Log Reports Design Runs Timing Power Methodology DRC Package Pins I/O Ports

Flow Navigator

RTL ANALYSIS
Open Elaborated Design

SYNTHESIS
Run Synthesis
Open Synthesized Design

IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic

PROGRAM AND DEBUG
Generate Bitstream

IMPLEMENTED DESIGN - xc7a35ticsg324-1L

Package Device mini_proj.v pins.xdc

D:/LATEST PROGRAMS/mini_proj_1/mini_proj_1.srcts/constrs_1/new/pins.xdc



```
1 set_property IOSTANDARD LVCMOS33 [get_ports clk]
2 set_property PACKAGE_PIN H5 [get_ports data_out]
3 set_property PACKAGE_PIN J5 [get_ports Y0]
4 set_property PACKAGE_PIN T9 [get_ports Y1]
5 set_property PACKAGE_PIN T10 [get_ports Y2]
6 set_property PACKAGE_PIN G6 [get_ports Y3]
7 set_property IOSTANDARD LVCMOS33 [get_ports data_out]
8 set_property IOSTANDARD LVCMOS33 [get_ports Y0]
9 set_property IOSTANDARD LVCMOS33 [get_ports Y1]
10 set_property IOSTANDARD LVCMOS33 [get_ports Y2]
11 set_property IOSTANDARD LVCMOS33 [get_ports Y3]
12
13 set_property PACKAGE_PIN E3 [get_ports clk]
14 set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
15 set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
16 set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
17 connect_debug_port dbg_hub/clk [get_nets clk_IBUF_BUFG]
18
```

CONSTRAINTS
FILE

Tcl Console Messages Log Reports Design Runs Timing Power Methodology DRC Package Pins I/O Ports

1:1 Insert XDC

NPTEL-NIELIT-ARM#FPGA#B4: La | NPTEL-NIELIT-ARM#FPGA#B4: La | NIELIT calicut Remote Hardware | +

Not secure | iep.nielit:33305/index.html

mini_proj - [/home/fpga0722-amre62/mini_proj/mini_proj.xpr] - Vivado 2020.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210319AB5935A

Hardware

Name	Status
localhost (20)	Connected
xilinx_tcf/Digilent/210319AB5935A (20)	Closed
xilinx_tcf/Digilent/210319AB5935A (20)	Open
xc7a35t_0_1 (3)	Programmed
XADC (System Monitor)	
hw_vio_1 (inputs)	OK - Output
hw_il_1 (outputs)	Idle
xilinx_tcf/Digilent/210292AD2I (20)	Closed
xilinx_tcf/Digilent/210319AB5935A (20)	Closed
xilinx_tcf/Digilent/210319AB5935A (20)	Closed
xilinx_tcf/Digilent/210292AD2I (20)	Closed
xilinx_tcf/Digilent/210292AD2I (20)	Closed

Debug Probe Properties

hw_il_1 x hw_vios x

hw_vio_1

Name	Value	Activity	Direction	VIO
i0	[B] 0		Output	hw_vio_1
i1	[B] 0		Output	hw_vio_1
i2	[B] 0		Output	hw_vio_1
i3	[B] 0		Output	hw_vio_1

VIO

Tcl Console

- program_hw_devices [get_hw_devices xc7a35t_0_1]
- INFO: [Labtools 27-3164] End of startup status: HIGH
- refresh_hw_device [lindex [get_hw_devices xc7a35t_0_1] 0]
- INFO: [Labtools 27-2302] Device xc7a35t (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
- INFO: [Labtools 27-2302] Device xc7a35t (JTAG device index = 0) is programmed with a design that has 1 VIO core(s).
- INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
- display_hw_il_data [get_hw_il_data hw_il_data_1 -of_objects [get_hw_ilas -of_objects [get_hw_devices xc7a35t_0_1] -filter {CELL_NAME=~"outputs"}]]

Type a Tcl command here

NPTEL-NIELIT-ARM#FPGA#B4: La | NPTEL-NIELIT-ARM#FPGA#B4: La | NIELIT calicut Remote Hardware | +

Not secure | iep.nielit:33305/index.html

mini_proj - [/home/fpga0722-amre62/mini_proj/mini_proj.xpr] - Vivado 2020.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210319AB5935A

Hardware

Name	Status
localhost (20)	Connected
xilinx_tcf/Digilent/210319AB5935A (20)	Closed
xilinx_tcf/Digilent/210319AB5935A (20)	Open
xc7a35t_0_1 (3)	Programmed
XADC (System Monitor)	
hw_vio_1 (inputs)	OK - Output
hw_ilas_1 (outputs)	Idle
xilinx_tcf/Digilent/210292AD2I (20)	Closed
xilinx_tcf/Digilent/210319AB5935A (20)	Closed
xilinx_tcf/Digilent/210319AB5935A (20)	Closed
xilinx_tcf/Digilent/210292AD2I (20)	Closed
xilinx_tcf/Digilent/210292AD2I (20)	Closed

hw_ilas_1 x hw_vios x

Trigger Setup - hw_ilas_1

Name	Operator	Radix	Value	Port	Comparator Usage
data_out_OBUF	==	[B]	X	probe4[0]	
Y0_OBUF	==	[B]	X	probe0[0]	
Y1_OBUF	==	[B]	X	probe1[0]	
Y2_OBUF	==	[B]	X	probe2[0]	
Y3_OBUF	==	[B]	X	probe3[0]	

ILA

Tcl Console x Messages Serial I/O Links Serial I/O Scans

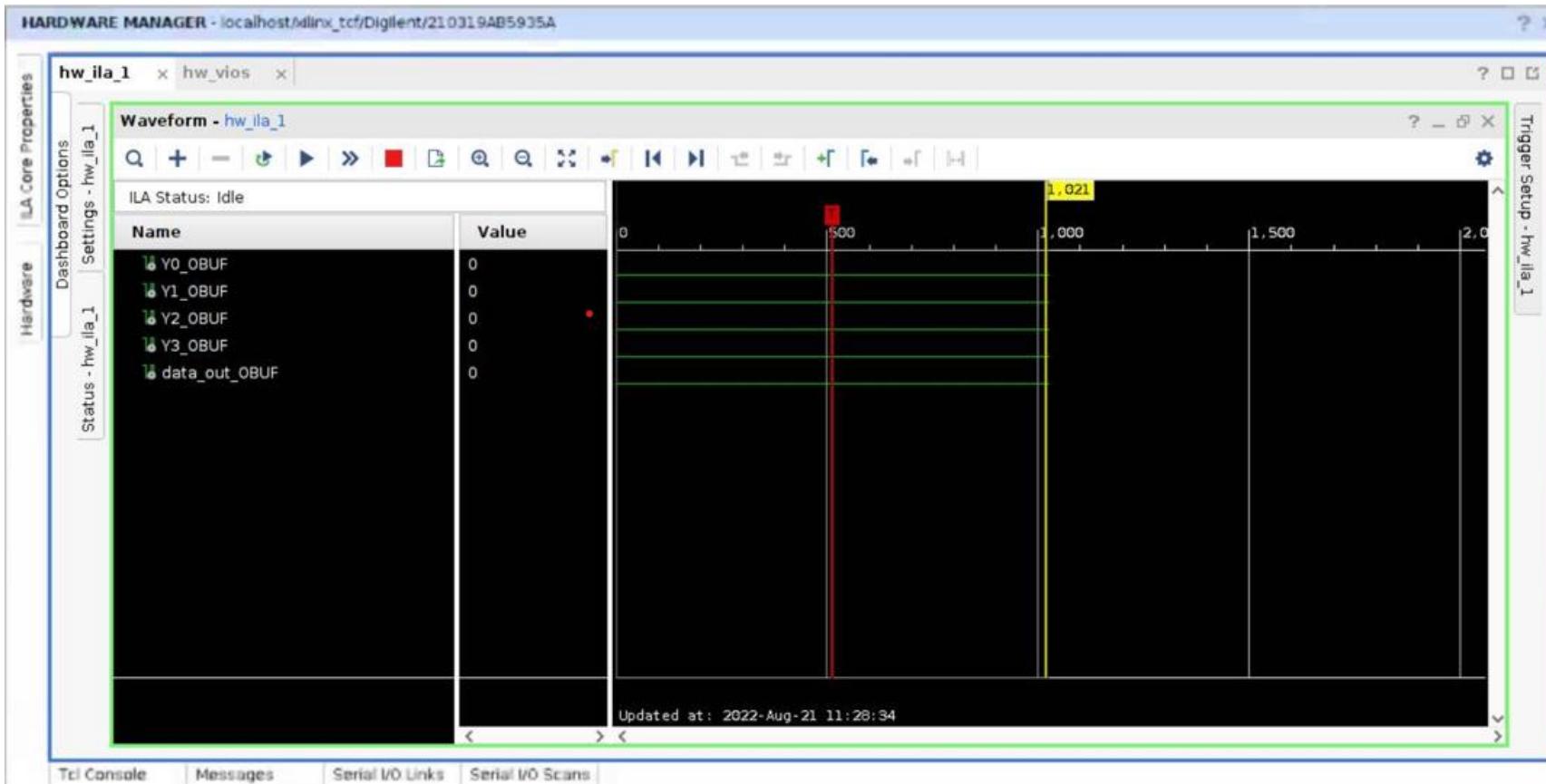
```
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices xc7a35t_0_1] 0]
INFO: [Labtools 27-2302] Device xc7a35t (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xc7a35t (JTAG device index = 0) is programmed with a design that has 1 VIO core(s).
set_property PROBES.FILE [/home/fpga0722-amre62/Downloads/mini_proj.ltx] [get_hw_devices xc7a35t_0_1]
set_property FULL_PROBES.FILE [/home/fpga0722-amre62/Downloads/mini_proj.ltx] [get_hw_devices xc7a35t_0_1]
set_property PROGRAM.FILE [/home/fpga0722-amre62/Downloads/mini_proj.bit] [get_hw_devices xc7a35t_0_1]
program_hw_devices [get_hw_devices xc7a35t_0_1]
INFO: [Labtools 27-3164] End of startup status: HIGH
```

Type a Tcl command here

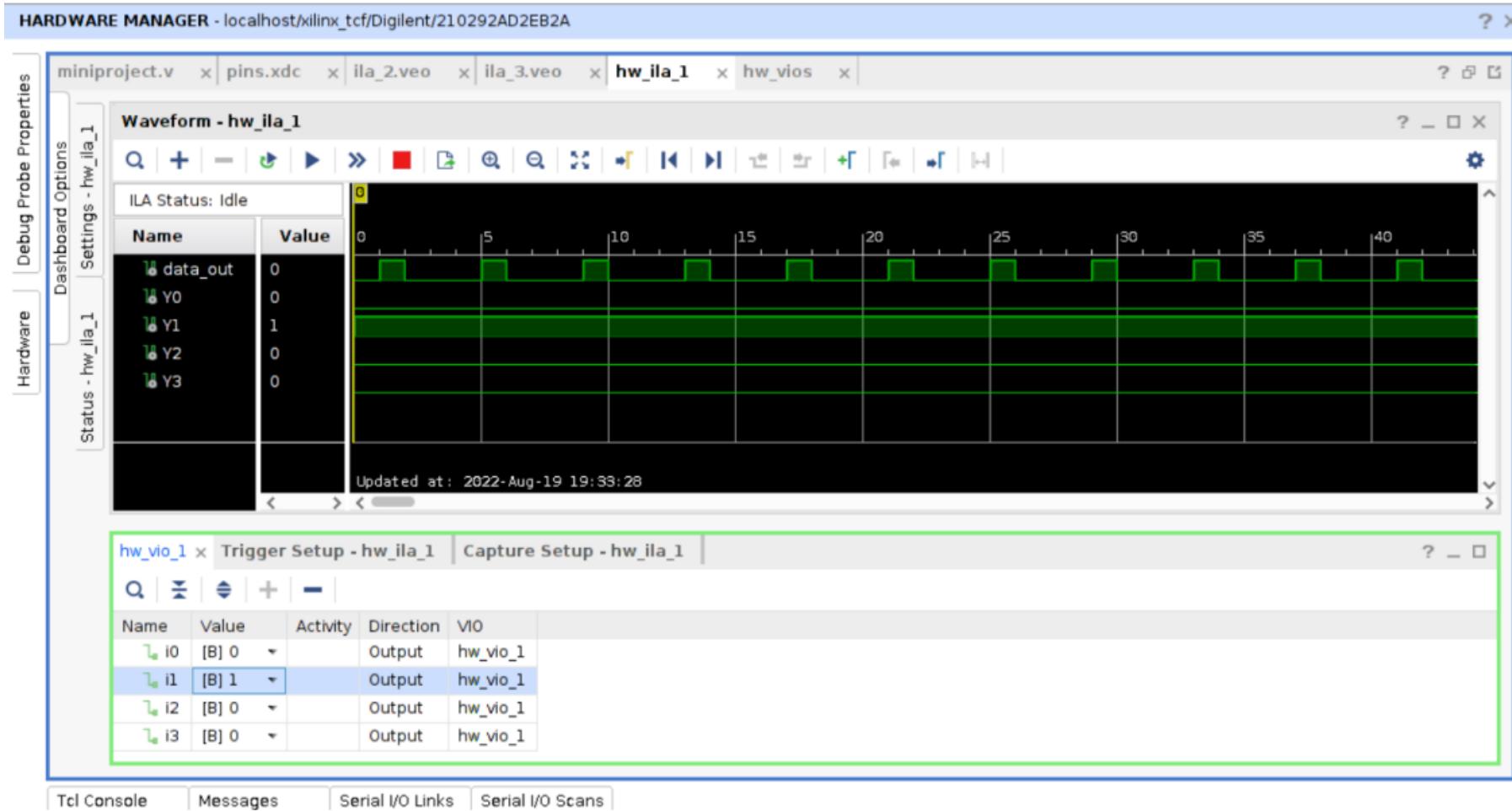
85°F Cloudy

11:27 21-08-2022

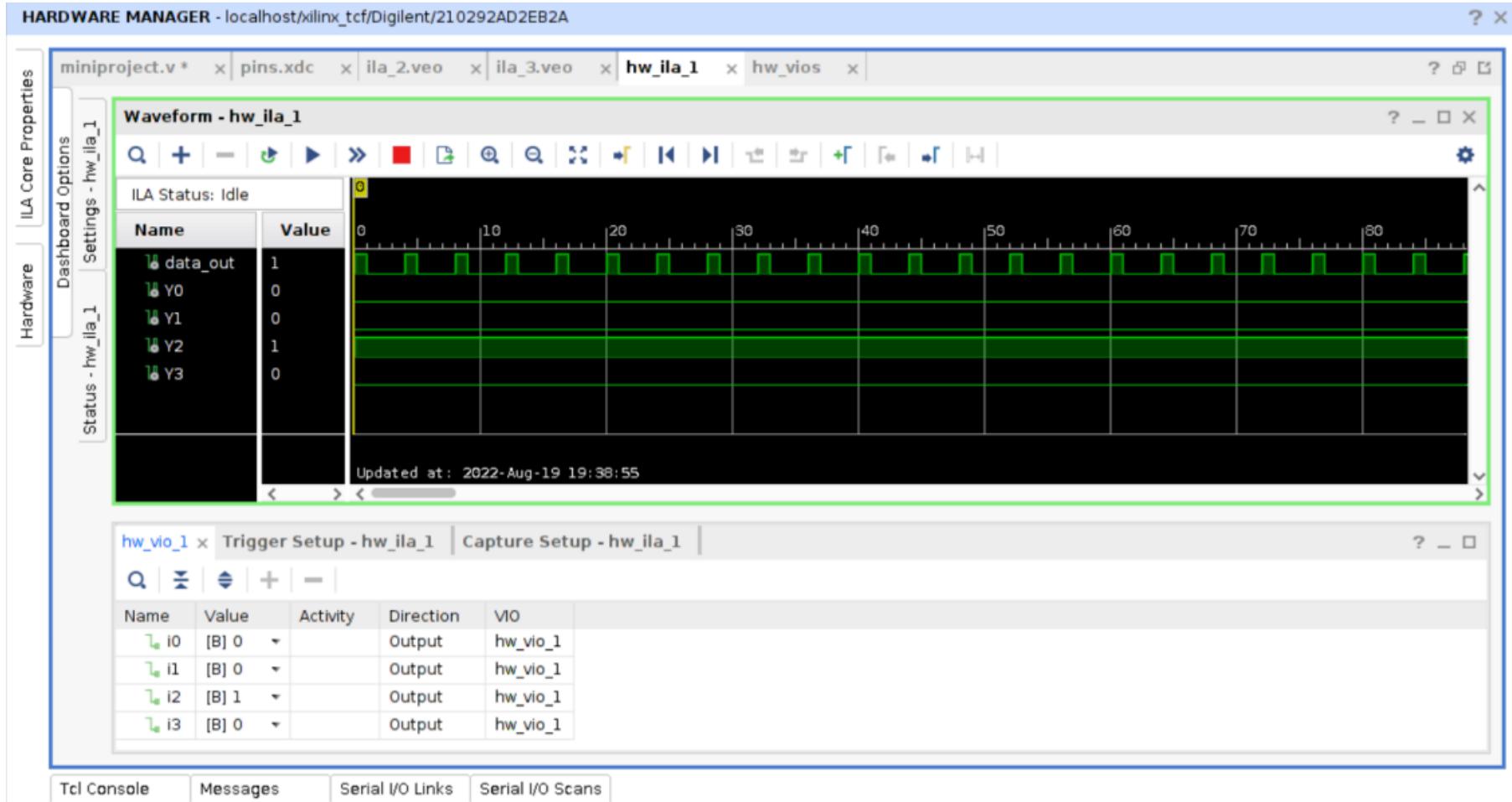
NO INPUTS
GIVEN



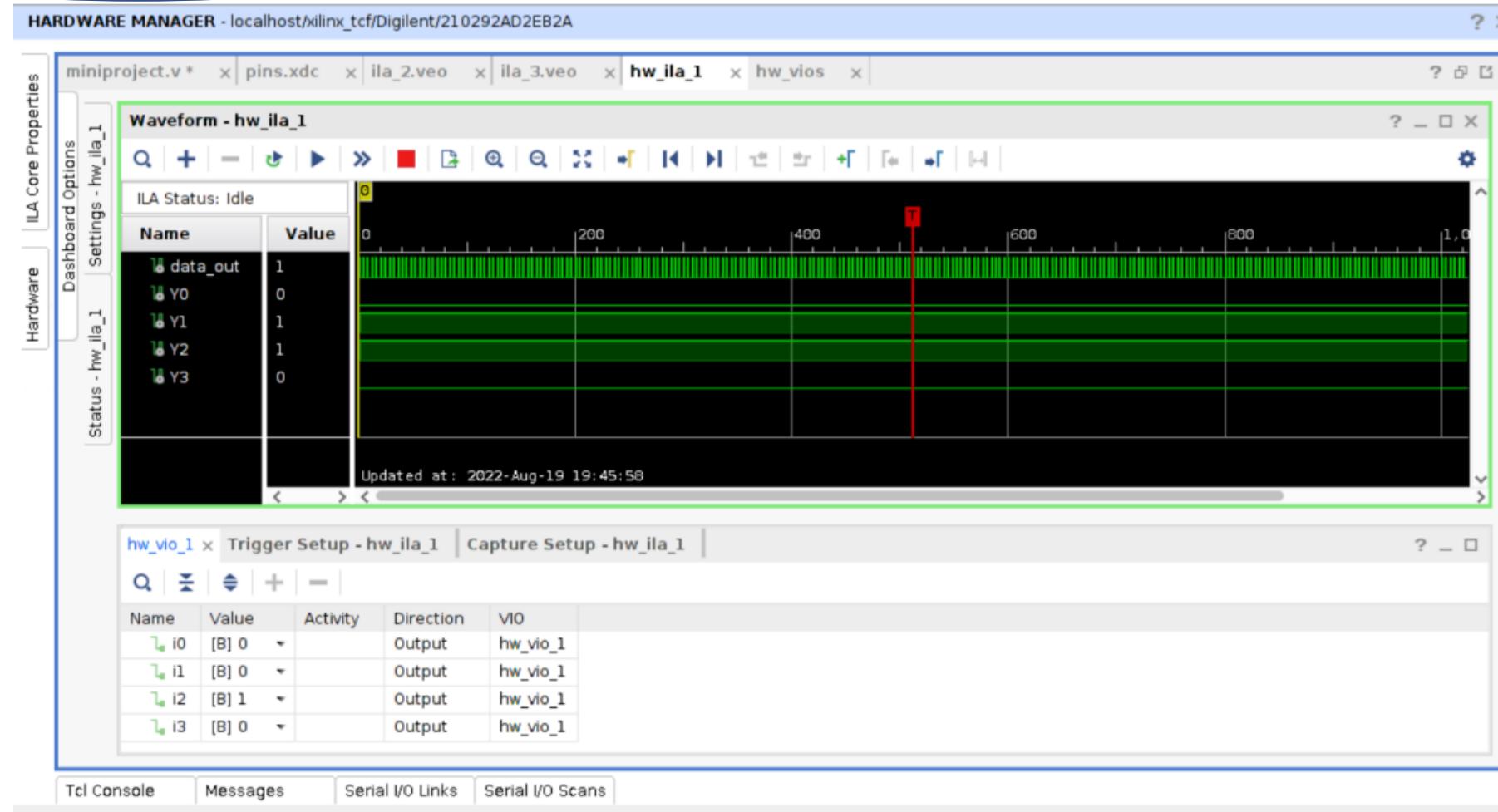
i1 TRIGGERED



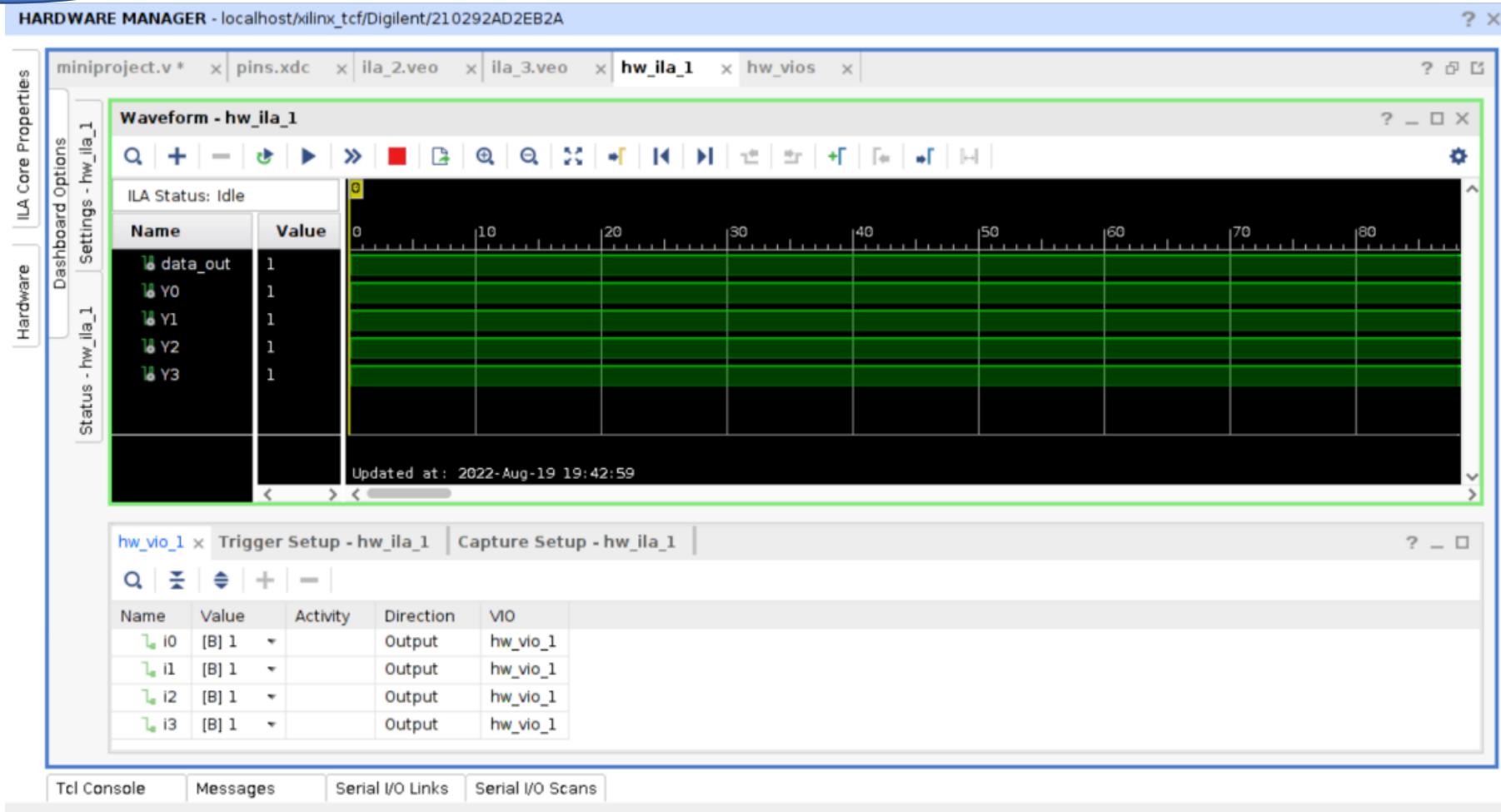
12 TRIGGERED

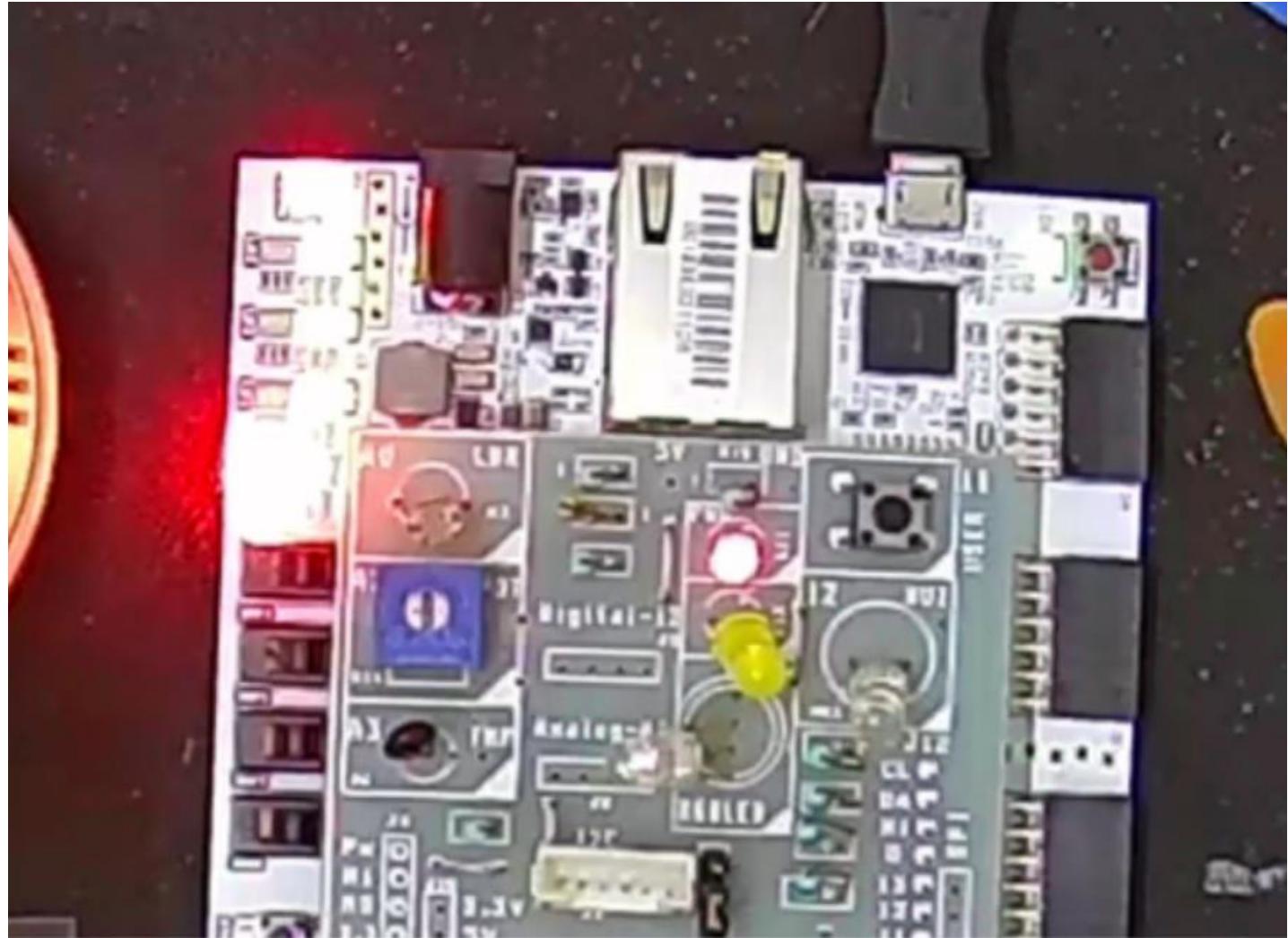


i2 TRIGGERED WITHOUT REPROGRAMMING AFTER PREVIOUS OUTPUT



ALL OUTPUTS





FPGA
OUTPUT

THANKYOU