ECEN 5623
Homework set 4

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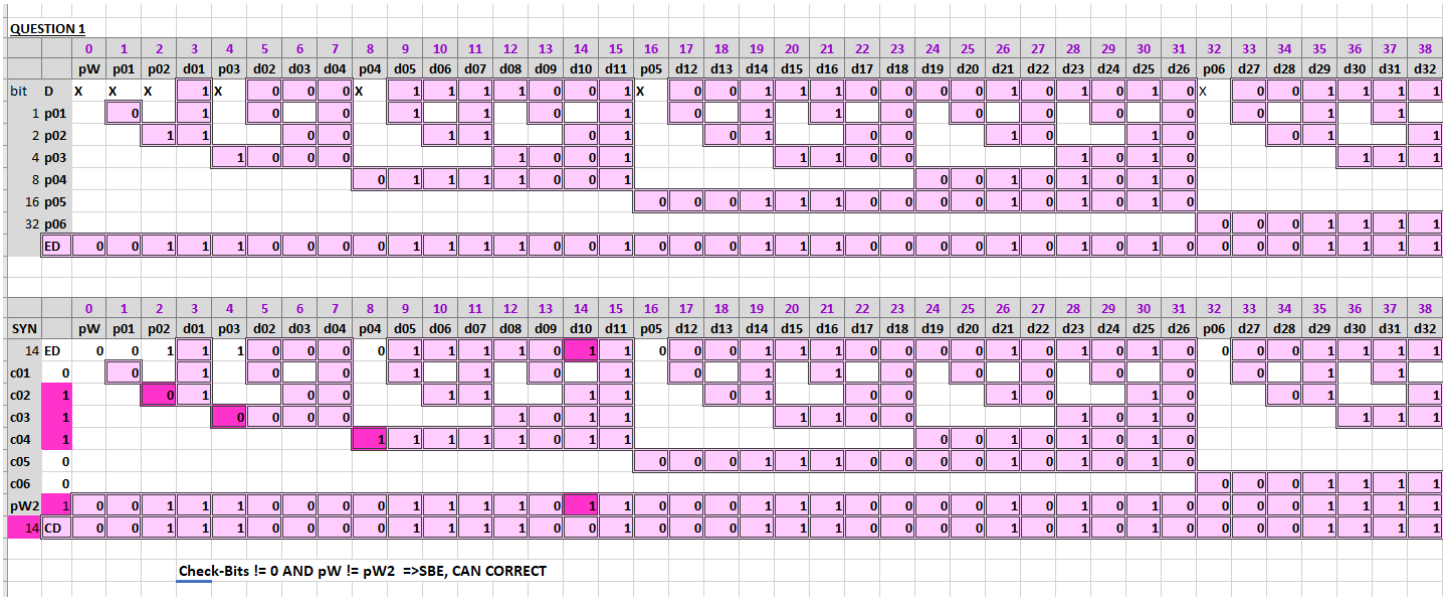
1. **Develop an example of a 32-bit Hamming encoded word (39 bits total) and show a correctable SBE scenario. Show the data word in a table like Figure 5.6 in the book.**



QUESTION 1

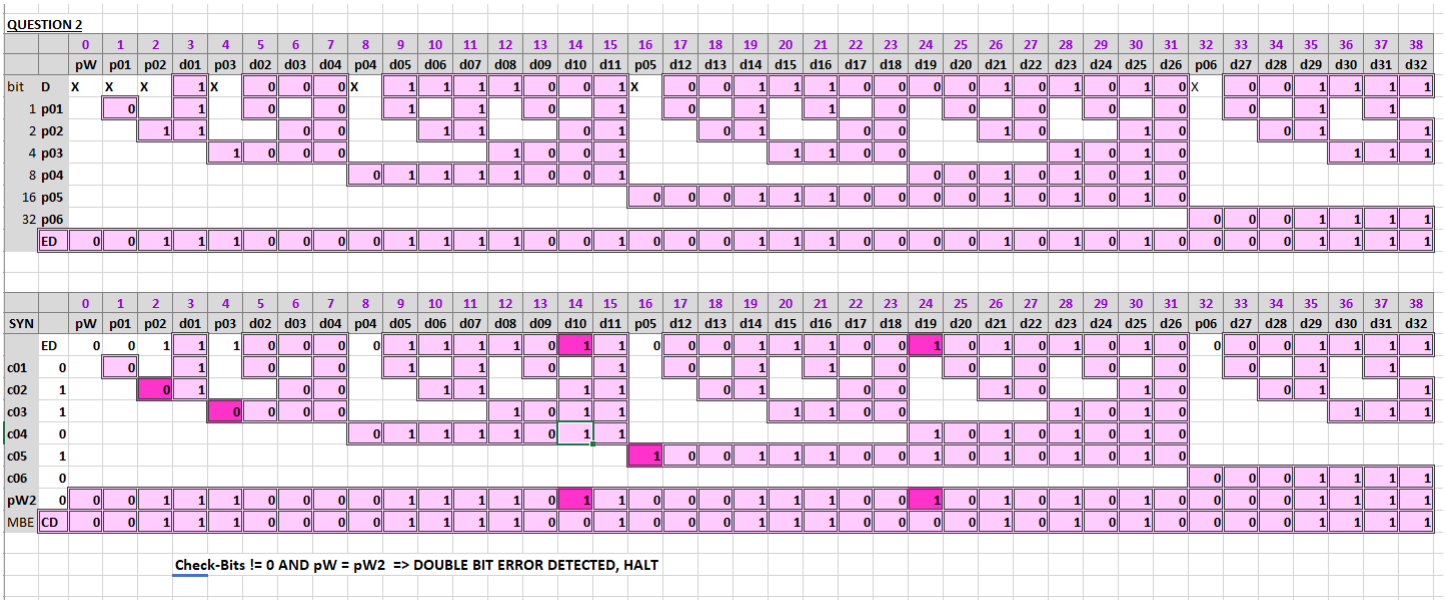
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
		pW	p01	p02	d01	p03	d02	d03	d04	p04	d05	d06	d07	d08	d09	d10	d11	p05	d12	d13	d14	d15	d16	d17	d18	d19	d20	d21	d22	d23	d24	d25	d26	p06	d27	d28	d29	d30	d31	d32
bit	D	X	X	X	1	X	0	0	0	X	1	1	1	1	0	0	1	X	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	X	0	0	1	1	1	1
1	p01		0		1		0		0		1		1		0		1		0		1		1		0		0		0		0		0		0		1		1	
2	p02			1	1			0	0			1	1			0	1			0	1			0	0			1	0			1	0			0	1			1
4	p03					1	0	0	0					1	0	0	1					1	1	0	0					1	0	1	0					1	1	1
8	p04									0	1	1	1	1	0	0	1									0	0	1	0	1	0	1	0							
16	p05																	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0							
32	p06																																	0	0	0	1	1	1	1
	ED	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	1	1

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
SYN		pW	p01	p02	d01	p03	d02	d03	d04	p04	d05	d06	d07	d08	d09	d10	d11	p05	d12	d13	d14	d15	d16	d17	d18	d19	d20	d21	d22	d23	d24	d25	d26	p06	d27	d28	d29	d30	d31	d32
14	ED	0	0	1	1	1	0	0	0	0	1	1	1	1	0	1	1	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	1	1
c01	0		0		1		0		0		1		1		0		1		0		1		1		0		0		0		0		0		0		1		1	
c02	1			0	1			0	0			1	1			1	1			0	1			0	0			1	0			1	0			0	1			1
c03	1					0	0	0	0					1	0	1	1					1	1	0	0					1	0	1	0					1	1	1
c04	1									1	1	1	1	1	0	1	1									0	0	1	0	1	0	1	0							
c05	0																	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0							
c06	0																																	0	0	0	1	1	1	1
pW2	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	1	1	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	1	1
14	CD	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	1	1

Check-Bits != 0 AND pW != pW2 =>SBE, CAN CORRECT

Bit d10 is changed to 1 to introduce single bit error (SBE). In the calculated syndrome, check bits are non-zero and pW is not equal to pW2 which shows SBE and this can be corrected. Value of check bits is 14 which is the erroneous bit.

2. **For the foregoing problem, now show an uncorrectable MBE scenario.**



QUESTION 2

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
		pW	p01	p02	d01	p03	d02	d03	d04	p04	d05	d06	d07	d08	d09	d10	d11	p05	d12	d13	d14	d15	d16	d17	d18	d19	d20	d21	d22	d23	d24	d25	d26	p06	d27	d28	d29	d30	d31	d32
bit	D	X	X	X	1	X	0	0	0	X	1	1	1	1	0	0	1	X	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	X	0	0	1	1	1	1
1	p01		0		1		0		0		1		1		0		1		0		1		1		0		0		0		0		0		0		1		1	
2	p02			1	1			0	0			1	1			0	1			0	1			0	0			1	0			1	0			0	1			1
4	p03					1	0	0	0					1	0	0	1					1	1	0	0					1	0	1	0					1	1	1
8	p04									0	1	1	1	1	0	0	1									0	0	1	0	1	0	1	0							
16	p05																	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0							
32	p06																																	0	0	0	1	1	1	1
	ED	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	1	1

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
SYN		pW	p01	p02	d01	p03	d02	d03	d04	p04	d05	d06	d07	d08	d09	d10	d11	p05	d12	d13	d14	d15	d16	d17	d18	d19	d20	d21	d22	d23	d24	d25	d26	p06	d27	d28	d29	d30	d31	d32
	ED	0	0	1	1	1	0	0	0	0	1	1	1	1	0	1	1	0	0	0	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	0	1	1	1	1
c01	0		0		1		0		0		1		1		0		1		0		1		1		0		0		0		0		0		0		1		1	
c02	1			0	1			0	0			1	1			1	1			0	1			0	0			1	0			1	0			0	1			1
c03	1					0	0	0	0					1	0	1	1					1	1	0	0					1	0	1	0					1	1	1
c04	0									0	1	1	1	1	0	1	1									1	0	1	0	1	0	1	0							
c05	1																	1	0	0	1	1	1	0	0	1	0	1	0	1	0	1	0							
c06	0																																	0	0	0	1	1	1	1
pW2	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	1	1	0	0	0	1	1	1	0	0	1	0	1	0	1	0	1	0	0	0	0	1	1	1	1
MBE	CD	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	1	1	1	1

Check-Bits != 0 AND pW = pW2 => DOUBLE BIT ERROR DETECTED, HALT

Bit d10 and bit d19 are changed to 1 to introduce multiple bit error (MBE). In the calculated syndrome, check bits are non-zero and pW is equal to pW2 which shows MBE and this cannot be corrected.

3. **For the following Nand flash block update history for 2 sectors that contain 4 blocks each (e.g. 16K sectors, with 4K blocks), fill in the missing WRITE operations as needed and compute write-amplification.**

		#1 - Start	#2	#3	#4	#5	#6	#7
Sector Erased (S0, S1)		0,0	1,1	1,1	1,1	1,1	2,1	2,1
S1								
	PB7	FREE	FREE	FREE	LB3	LB3	LB3	LB3
	PB6	FREE	FREE	LB2	LB2	INVLD	INVLD	INVLD
	PB5	FREE	LB3	LB3	INVLD	INVLD	INVLD	INVLD
	PB4	FREE	LB2	INVLD	INVLD	INVLD	INVLD	INVLD
S0								
	PB3	FREE	FREE	FREE	LB1	LB1	FREE	LB1
	PB2	FREE	FREE	LB0	LB0	INVLD	FREE	FREE
	PB1	FREE	LB1	LB1	INVLD	INVLD	FREE	LB2
	PB0	FREE	LB0	INVLD	INVLD	INVLD	FREE	LB0
FS LBs Updated			0,1,2,3	0,2	1,3	0,2	0,2	0,2
FS LBs Cached						0,2	0,2	
Sector LBs Buffered							1	
		#8	#9	#10	#11	#12	#13	#14
Sectors Erased (S0, S1)	2,1	2,1	2,2	2,2	2,2	2,2	3,2	3,2
S1								
	LB3	INVLD	FREE	FREE	LB2	LB2	LB2	LB2
	INVLD	INVLD	FREE	FREE	LB0	LB0	LB0	LB0
	INVLD	INVLD	FREE	LB3	LB3	INVLD	INVLD	INVLD
	INVLD	INVLD	FREE	LB1	LB1	INVLD	INVLD	INVLD
S0								
	LB1	INVLD	INVLD	INVLD	INVLD	INVLD	FREE	FREE
	FREE	FREE	FREE	FREE	FREE	FREE	FREE	FREE
	LB2	LB2	LB2	LB2	INVLD	INVLD	FREE	LB3
	LB0	LB0	LB0	LB0	INVLD	INVLD	FREE	LB1
FS LBs Updated	0,2	1,3	1,3	1,3	0,2	1,3	1,3	1,3
FS LBs Cached		1,3	1,3			1,3	1,3	
Sector LBs Buffered								

#1 – All blocks FREE
#2 – Erase S0 & S1, WRITE LB 0, 1, 2, 3
#3 – Read LB 0, 2, Modify, WRITE LB 0, 2
#4 – Read LB 1, 3, Modify, WRITE LB 1, 3
#5 – Read LB 0, 2, Modify and Cache
#6 – Buffer LB 0, 1, 2, Erase S0
#7 – WRITE LB 0, 1, 2 S0

Write Amplification = 11/10 = 1.1

#8 - Read LB 1, 3, Modify and Cache
#9 – Erase S1
#10 – WRITE LB 1, 3
#11 – Read LB 0, 2, Modify, WRITE LB 0, 2
#12 – Read LB 1, 3, Modify and Cache
#13 – Erase S0
#14 – WRITE LB 1, 3

Write Amplification = 17/16 = 1.0625
Total sector erases for both S0 and S1 = 5 (3 S0 + 2 S1)