Stand: 12.11.2011

Stand: 12.11.2011	3V Side A			AGP 3.3 V	olt Roards			PCI 3V S	Side R
Description	+3.3V	Pin	Pin #	Side A	Side B	Pin #	Pin		Description
Test Logic Reset	TRST	A1	1	+12V	//expente		B1		-12 VDC
+12 VDC	+12V	A2 <		***PEDETH	#5.0V	2	B2		Test Clock
Test Mde Select	TMS	A3	7 2	Reserved	5.0V	3	→B3	GND	
Test Data Input	TDI	A4		usp.	<u> </u>	A CONTRACTOR	B4	TDO	
+5 VDC	+5V	A5	//////////////////////////////////////	Ground	Ground	5 —	⇒B5	+5V	
Interrupt A	INTA	A6 <		INTA#	////AKY###//	<u> </u>	→ B6	+5V	
Interrupt C	INTC	A7	/ 7	RST#	CLK	7 .	B7	INTB	
+5 VDC	+5V	A8	8	GNT#	REQ#	8	B8	INTD	•
Reserved VDC	RESV01	A9	9	VCC 3.3	VCC 3.3	9	В9		Reserved
+V I/O (+5 V or +3.3 V)	+3.3V	A10	W/////////////////////////////////////	<u>-\$74</u>	<u> </u>	<u> 140</u>	B10		+V I/O (+5 V or +3.3 V)
Reserved VDC	RESV03	A11	43	Reserved	<u>\$72</u>	24	B11	PRSNT2	
Ground or Open (Key)	(OPEN)	A12	<u> </u>	.PIPE#	RBF#	32	B12	(OPEN)	Ground or Open (Key)
Ground or Open (Key)	(OPEN)	A13	/ ''''''''''''''''''''''''''''''''''''	Ground	Ground	13	B13		Ground or Open (Key)
Reserved VDC	RESV05	A14	<u> </u>	Reserved	Xeterved	(1) <u>4</u> 4(((()))	B14	RES	
Reset	RESET	A15	<u> 45</u>	-SBA1	SBAD	<u> 15</u>	B15	GND	Reset
+V I/O (+5 V or +3.3 V)	+3.3V	A16	/mmmmmmm 16	VCC 3.3	vcc 3.3	16 🔪	B16	CLK	Clock
Grant PCI use	GNT	A17	- ''///////////////////////////////////	-\$BA3	<u> </u>	(1 <u>4.3</u> 4 (1)	→ B17	GND	Ground
Ground	GND08	A18 🗸	48	-Reserved	SB STB	18	B18	REQ	Request
Reserved VDC	RESV06	A19	, 19	Ground	Ground	19	B19	+3.3V	•
Address/Data 30	AD30	A20 <		-SBA5	SBAA	29	>> B20	AD31	
+3.3 VDC	+3.3V01	A21	24	-SBA7	SBAS	24	B21	AD29	·
Address/Data 28	AD28	A22	22	Key	Key	22	→B22	GND	Ground
Address/Data 26	AD26	A23	23	Key	Key	23	B23	AD27	Address/Data 27
Ground	GND10	A24 Z	24	Key	Key	24	B24	AD25	Address/Data 25
Address/Data 24	AD24	A25	25	Key	Key	25	B25	+3.3V	+3.3VDC
Initialization Device Select	IDSEL	A26	26	AD30	AD31	26	B26	C/BE3	Command, Byte Enable 3
+3.3 VDC	+3.3V03	A27 🗸	27	AD28	AD29	27	B27	AD23	Address/Data 23
Address/Data 22	AD22	A28	28	VCC 3.3	VCC 3.3	28	→B28	GND	
Address/Data 20	AD20	A29	29	AD26	AD27	29	B29	AD21	Address/Data 21
Ground	GND12	A30 🗹	30	AD24	AD25	30	B30	AD19	Address/Data 19
Address/Data 18	AD18	A31	31	Ground	Ground	31	B31	+3.3V	+3.3 VDC
Address/Data 16	AD16	A32		Reserved	AD STB1	32	7B32	AD17	Address/Data 17
+3.3 VDC	+3.3V05	A33	_33	C/BE3#	AD23	33	B33	C/BE2	Command, Byte Enable 2
Address or Data phase	FRAME	A34	34	Vddq 3.3	Vddq 3.3	34	→ B34	GND13	Ground
Ground	GND14	A35 🗸	35	AD22	AD21	35	B35	IRDY	Initiator Ready
Target Ready	TRDY	A36	36	AD20	AD19	36	▶B36	+3.3V06	+3.3 VDC
Ground	GND15	A37	37	Ground	Ground	37	/7 B37	DEVSEL	Device Select
Stop Transfer Cycle	STOP	A38	38	AD18	AD17	38	>B38	GND16	Ground
+3.3 VDC	+3.3V07	A39	39	AD16	C/BE2#	39	B39	LOCK	Lock bus
Snoop Done	SDONE	A40	40	Vddq 3.3	Vddq 3.3	40	B40	PERR	Parity Error
Snoop Backoff	SBO	A41	41	FRAME#	IRDY#	41	→ B41	+3.3V08	+3.3 VDC
Ground	GND17	A42 <	42	Reserved	3.3Vaux	(4)	B42	SERR	System Error
Parity	PAR	A43	43	Ground	Ground	43	B43	+3.3V09	+3.3 VDC
Address/Data 15	AD15	A44	44	Reserved	Reserved	144	B44	C/BE1	Command, Byte Enable 1
+3.3 VDC	+3.3V10	A45	45	VCC 3.3	VCC 3.3	45	B45	AD14	Address/Data 14
Address/Data 13	AD13	A46	46	TRDY#	DEVSEL#	46	→ B46	GND18	Ground
Address/Data 11	AD11	A47	47	STOP#	Vddq 3.3	47	7 B47	AD12	Address/Data 12
Ground	GND19	A48	48	DNAEH	DERR#	18	7 B48	AD10	Address/Data 10

