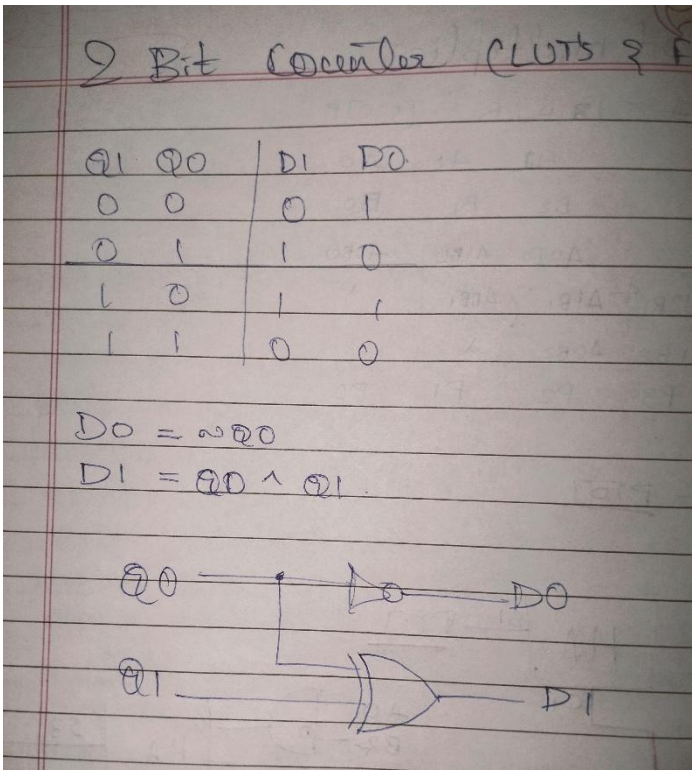
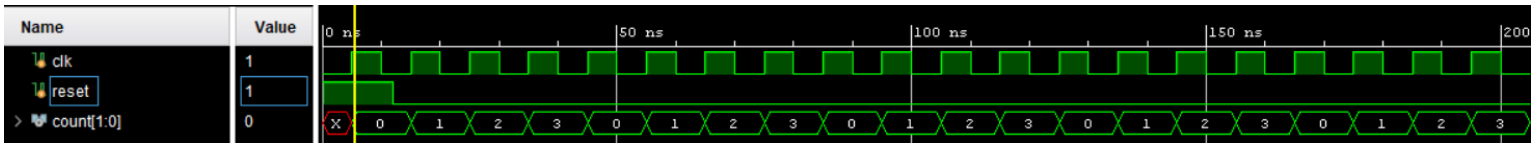
2-Bit Counter

```
//Verilog code for 2-Bit Counter
module counter_2bit (clk, reset, count);
   input wire clk;
   input wire reset;
   output reg [1:0] count;
   wire d0, d1;

   assign d0 = ~count[0];
   assign d1 = count[1] ^ count[0];

   always @(posedge clk) begin
      if (reset)
         count <= 2'b00;
      else
         count <= {d1, d0};
   end

endmodule
```



Waveform:



Synthesis analysis schematic:

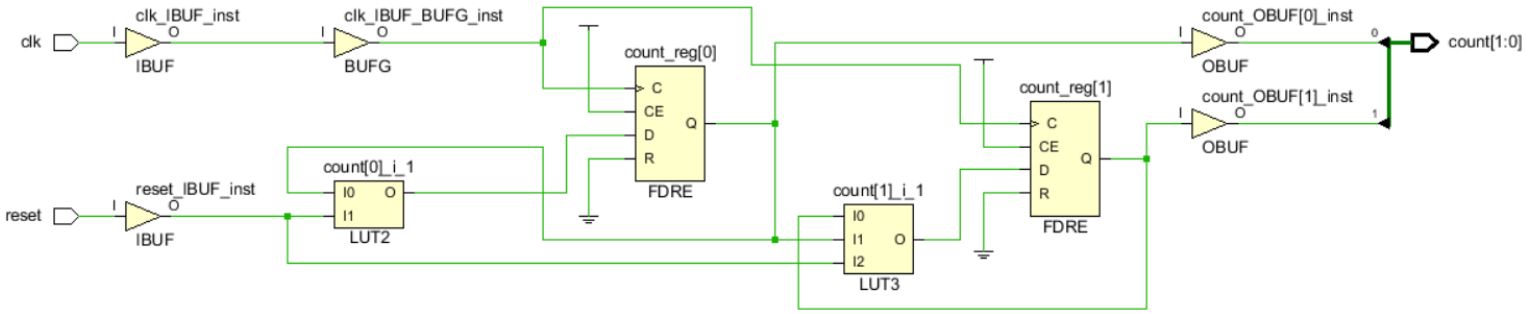


Figure 1: Synthesis analysis schematic

RTL analysis schematic:

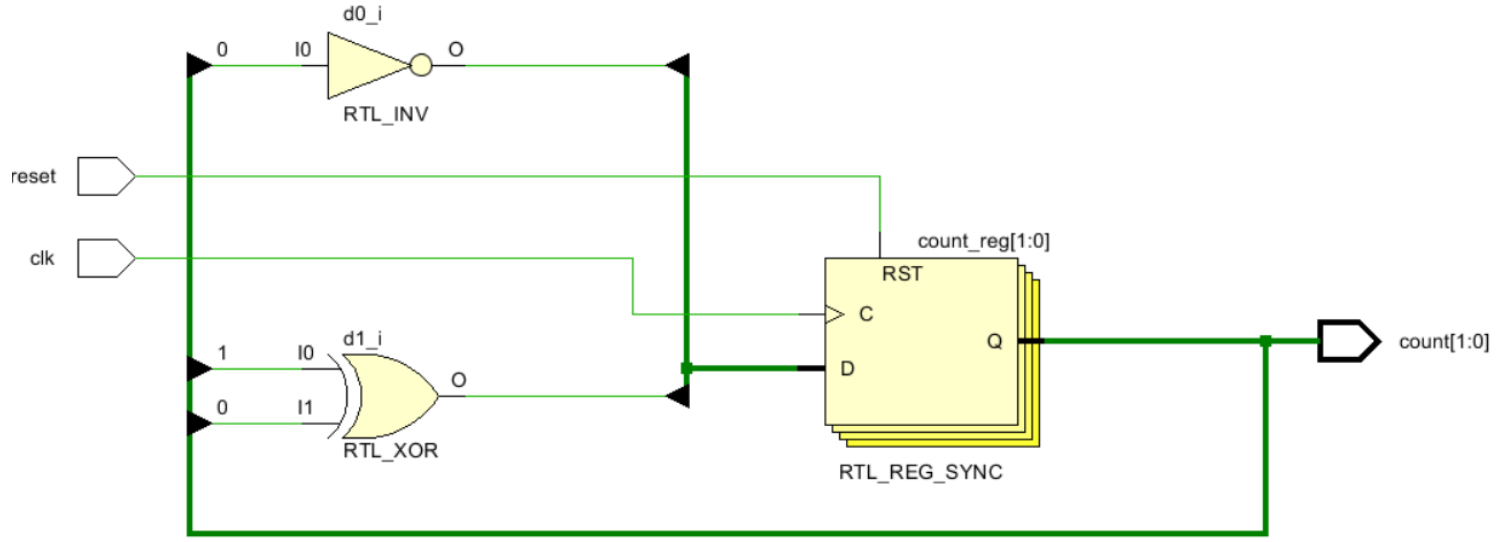


Figure 2: RTL analysis schematic

Look Up Tables:

Cell Properties

count[0]_i_1

I1	I0	O=!I0 & !I1
0	0	1
0	1	0
1	0	0
1	1	0

Table 1: LUT2

Cell Properties

count[1]_i_1

I2	I1	I0	O=I0 & !I1 & !I2 + !I0 & I1 & !I2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Table 2: LUT3