AND gate

```
//Verilog code for AND gate for positive-edge clk trigger
module gate_AND(a, b, y, clk);
 input a, b, clk;
 output reg y;
 always @(posedge clk)
  begin
   y <= a& b;
  end
endmodule
```

Synthesis Schematic:

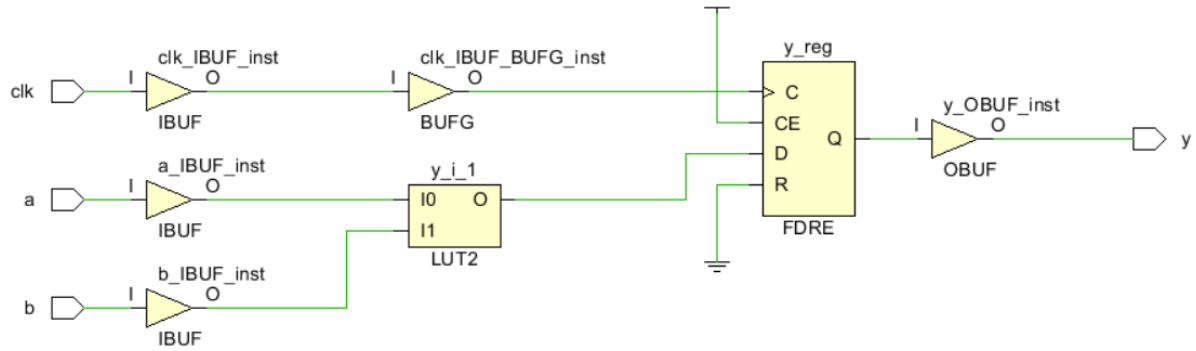

Figure 1: Synthesis schematic

RTL analysis schematic:

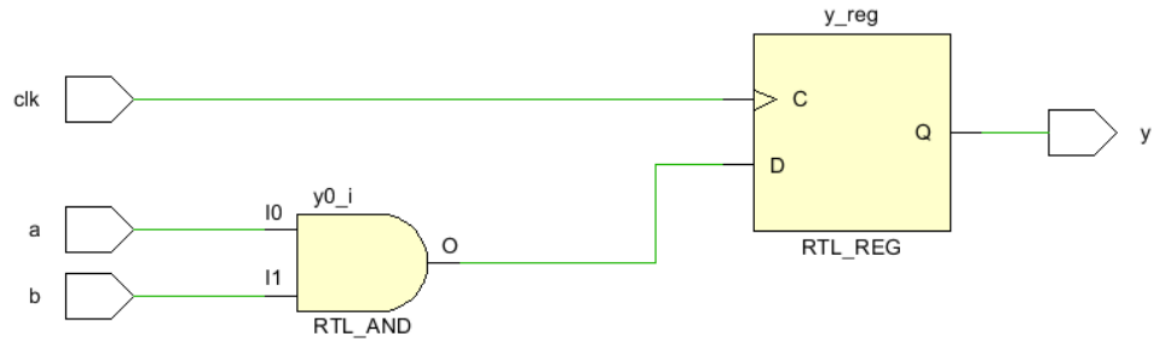

Figure 2: RTL Analysis schematic

Look Up Table:

Cell Properties

y_i_1

I1	I0	O=I0 & I1
0	0	0
0	1	0
1	0	0
1	1	1

Waveform: