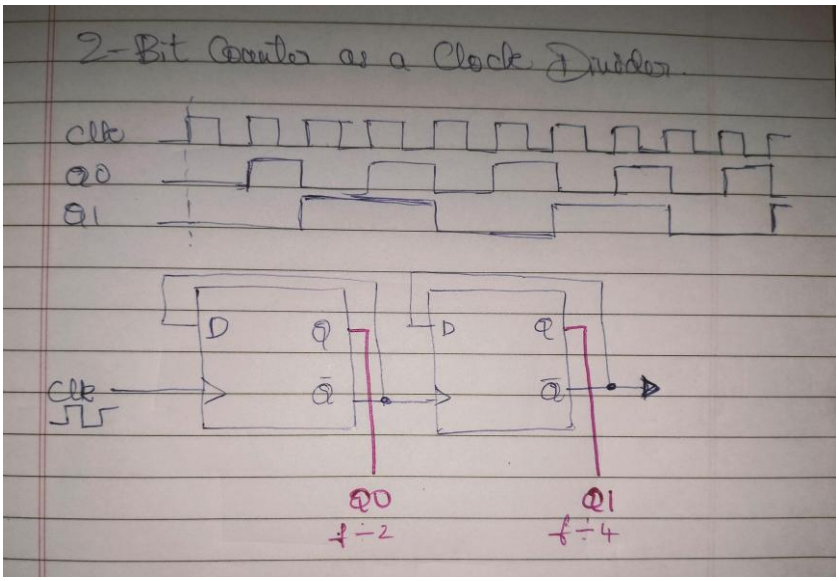
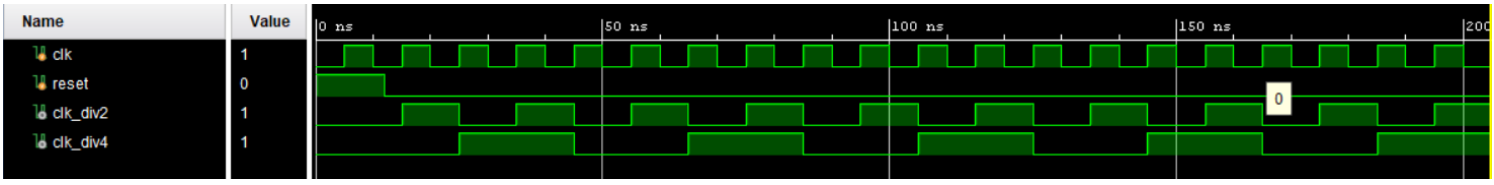
2-Bit Counter as a Clock Divider

//Verilog code

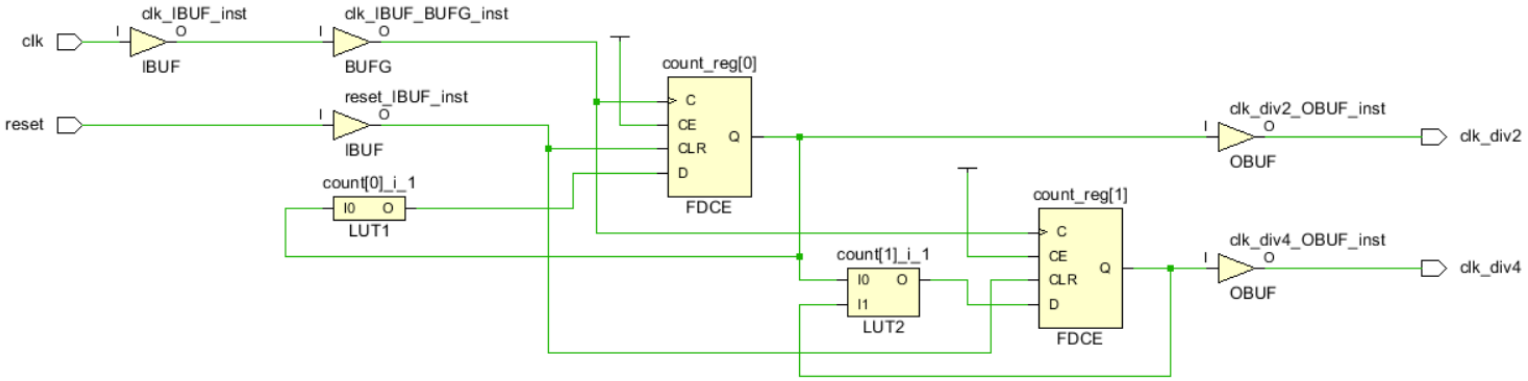
```
module counter_clk_div (clk, reset, clk_div2, clk_div4);
   input wire clk;
   input wire reset;
   output wire clk_div2;
   output wire clk_div4;
   reg [1:0] count;

   always @(posedge clk or posedge reset) begin
      if (reset)
         count <= 2'b00;
      else
         count <= count + 1;
   end
   assign clk_div2 = count[0];
   assign clk_div4 = count[1];
endmodule
```



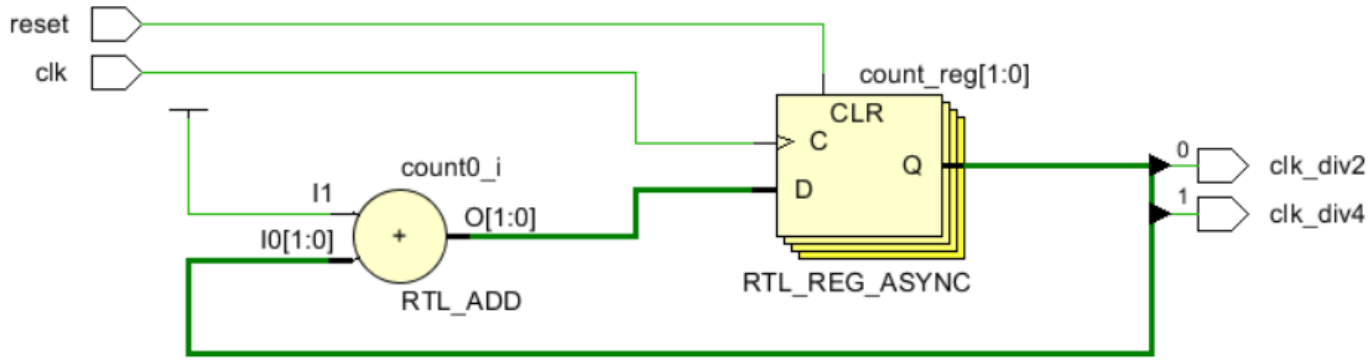
Waveform:



Synthesis schematic:



RTL Analysis schematic:



Look Up Tables:

Cell Properties

count[0]_i_1

I0	O=!I0
0	1
1	0

Table 1: LUT1

Cell Properties

count[1]_i_1

I1	I0	O=I0 & !I1 + !I0 & I1
0	0	0
0	1	1
1	0	1
1	1	0

Table 2: LUT2