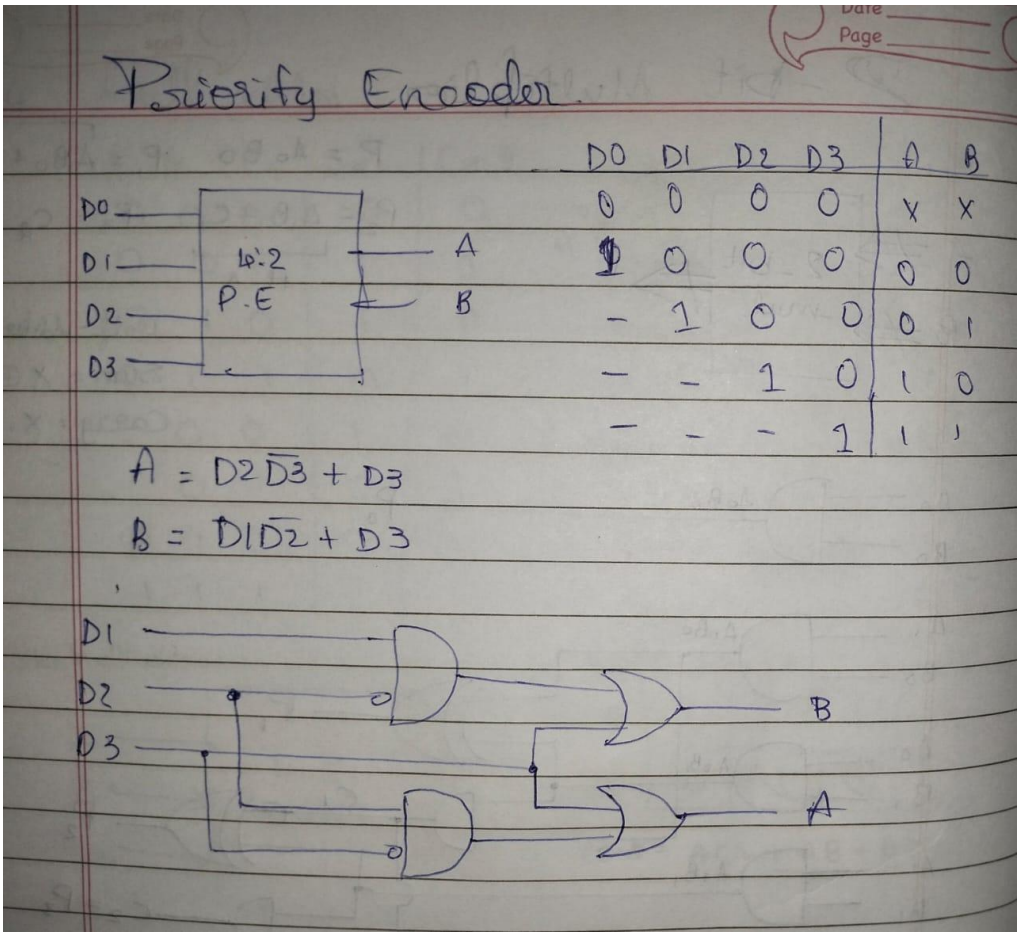
Priority Encoder




```
//Verilog code for priority encoder
module priority_encoder(D, A, B);
 input [3:0]D;
 output A, B;

  assign A = (D[2] &~D[3]) | D[3];
  assign B = (D[1] & ~D[2]) | D[3];

endmodule
```

Synthesis Schematic:

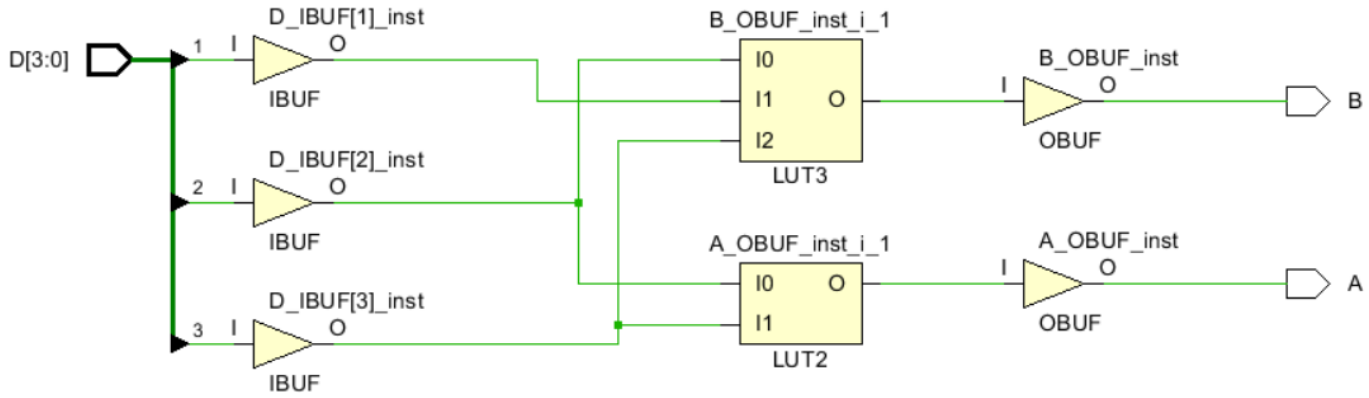


Figure 1: Synthesis schematic

RTL analysis schematic:

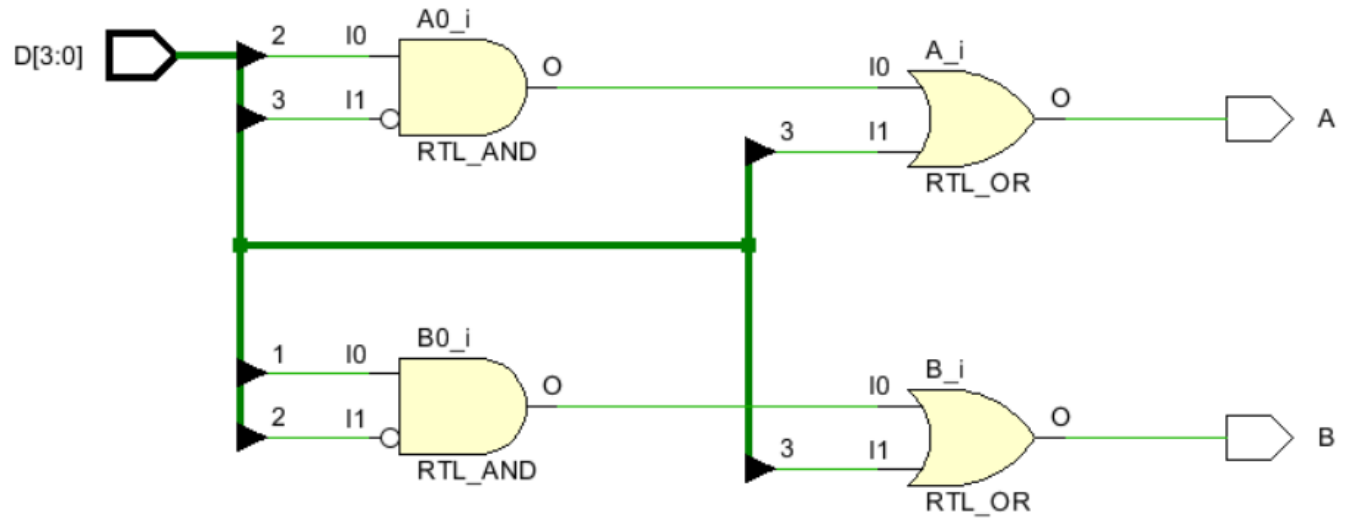


Figure 2: RTL analysis schematic

Look Up Table:

Cell Properties

A_OBUF_inst_i_1

I1	I0	O=I0 + I1
0	0	0
0	1	1
1	0	1
1	1	1

Table 1: LUT for A

Cell Properties

B_OBUF_inst_i_1

I2	I1	I0	O=!I0 & I1 + I2
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table 2: LUT for B