

# System Layout Design

## Front Side

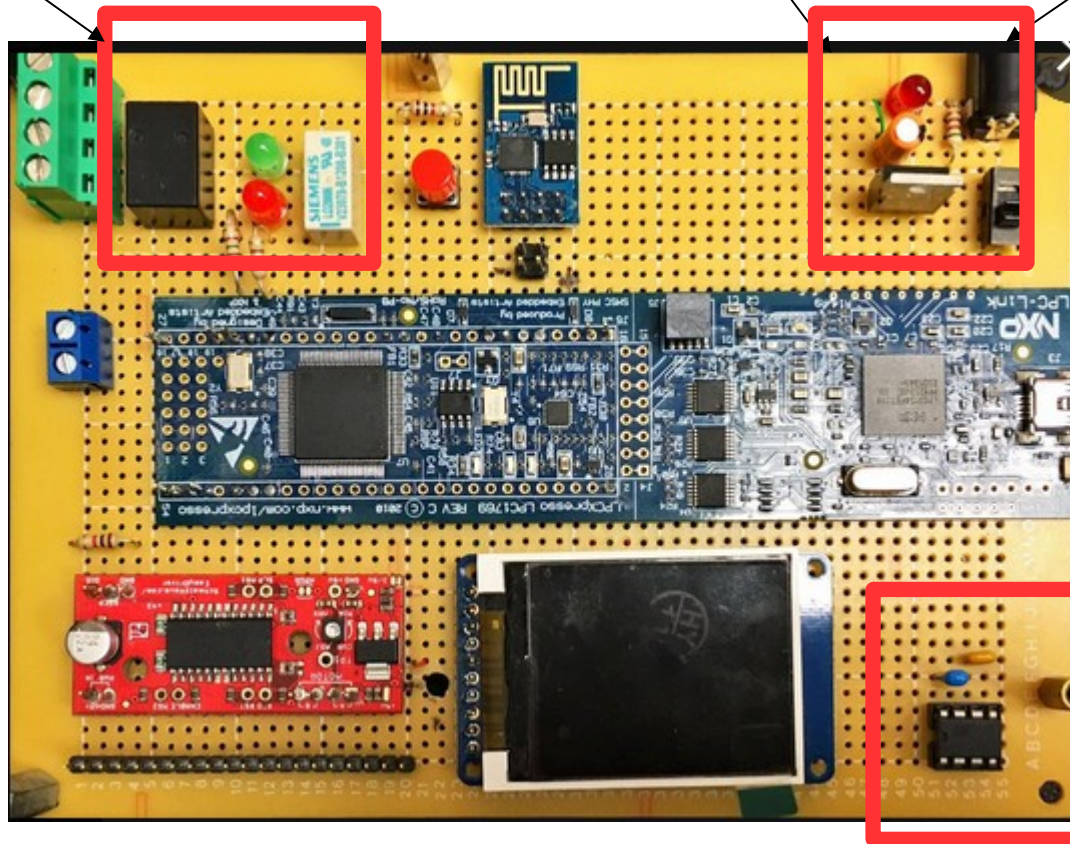
GPIO testing circuit  
with solid state relay

PWR circuit unit

J1: PWR  
Connector

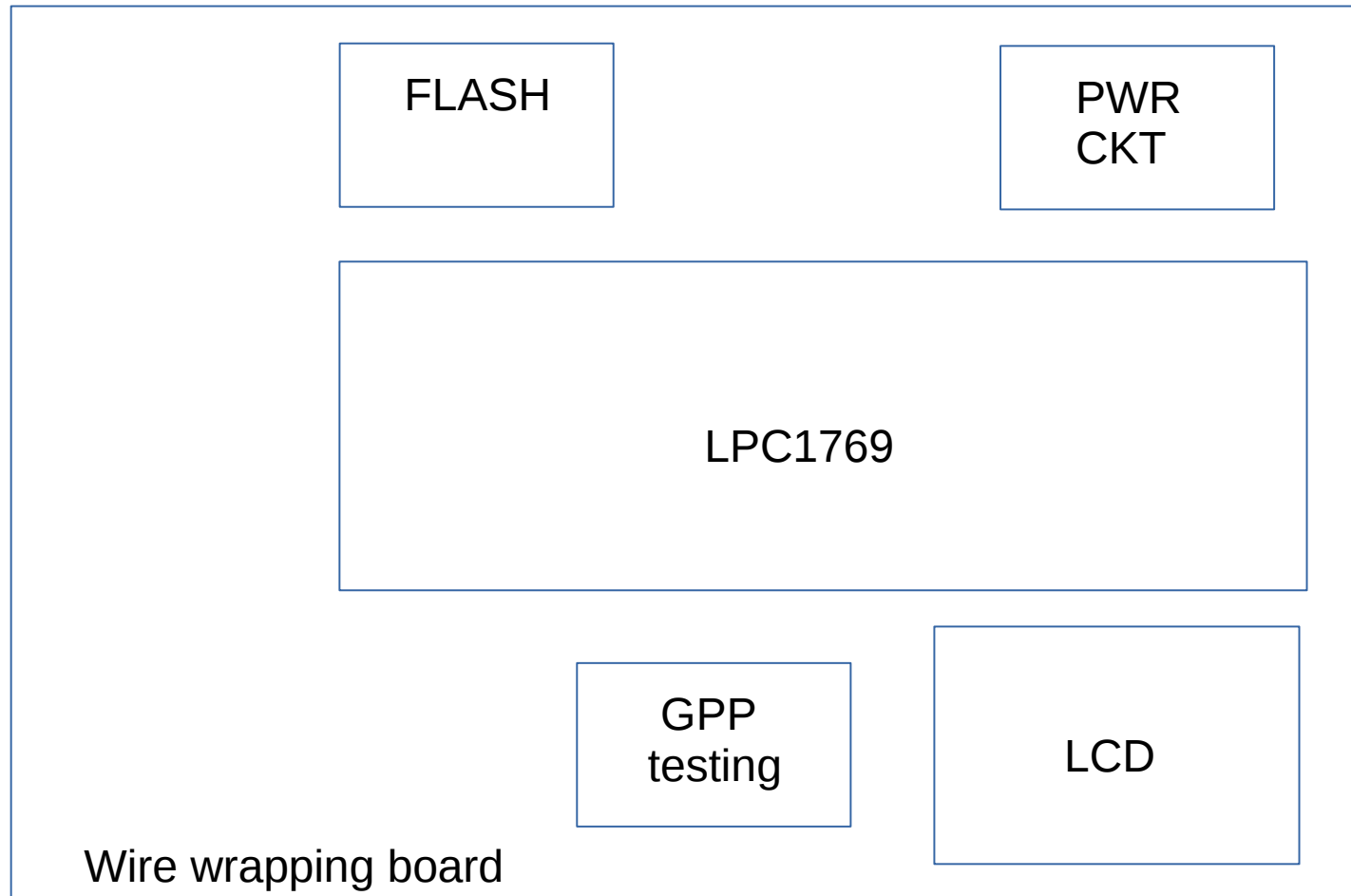
LPC1769

SPI I/F Flash



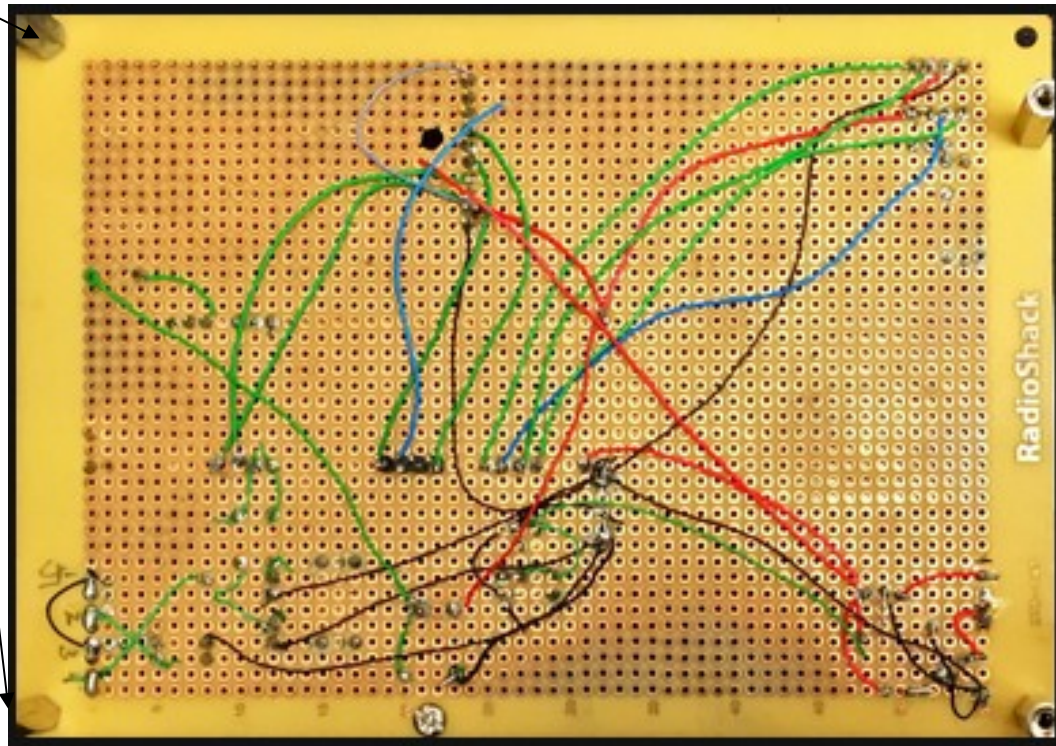
Dimension: 16 x 11 mm or 6.25 x 4.50 inch

# First Thing First, Layout Design



# System Layout Design Back Side

Standoffs



Standoffs

Wire Wrapping: 18g to 24G

|               |  |
|---------------|--|
| 10G - 0.1019" |  |
| 12G - 0.0808" |  |
| 14G - 0.0641" |  |
| 16G - 0.0508" |  |
| 18G - 0.0403" |  |
| 20G - 0.0320" |  |
| 22G - 0.0253" |  |
| 24G - 0.0201" |  |
| 26G - 0.0159" |  |
| 28G - 0.0126" |  |
| 30G - 0.0100" |  |
| 32G - 0.0080" |  |
| 34G - 0.0063" |  |

Wire soldered or wire wrapped

[http://www.softflexcompany.com/WSWrapper.jsp?mypage=Tips\\_Wire\\_Temper.html](http://www.softflexcompany.com/WSWrapper.jsp?mypage=Tips_Wire_Temper.html)

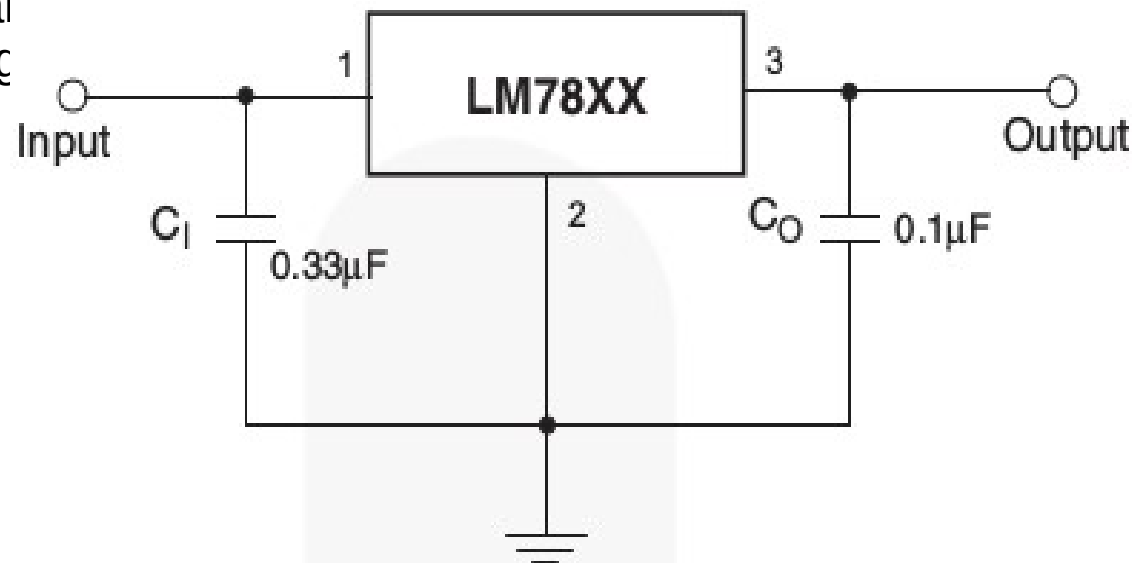
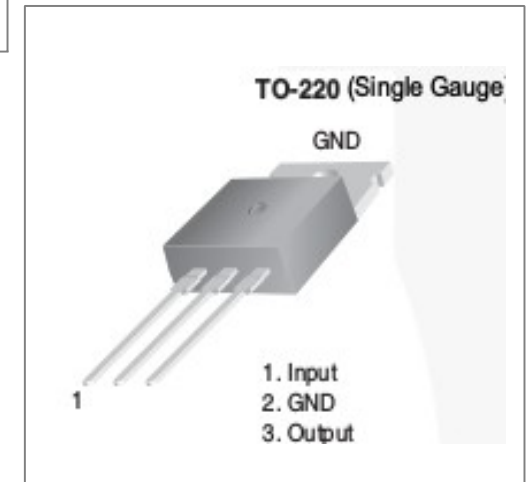
# PWR Regulator LM7805



LM78XX / LM78XXA

3-Terminal 1 A Positive Voltage Regulator

The LM78XX series of three-terminal positive regulators is available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down, and safe operating area protection. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed-voltage regulators, these devices can also be used as adjustable voltage regulators.



Note: 1. Voltage drop 1.5 volt;  
2. current output 1 A.



# 8-30-2018 PWR And Debugging Unit Design

CMPE240 Advanced Microprocessor Systems  
August 29, 2018 Harry Li 1/.

Today's Topics: 1° Spec for the Prototype Board Design. 2° Start the Layout Design.

New Posting @ github.

Note: Make Purchase of LPC1769 Today.

NXP IDE. Software Dev. Tool → Patch 1769. (Today)  
CPU Datasheet

Home: Build Spec. Table for the Prototype System (Lab Report)

From the Table, S.P.I. Device

Serial Peripheral I/F

Example: Bring Up the System. → "Hello, the World"

Step 1: Bring up the System. → Step 2: S.P.I. I/F → Step 3.

3 1/2 weeks.

2D G.E.



Naming convention on the SCH datasheet, (1) CPU manufacture + (2) industry Protocol + (3) 3<sup>rd</sup> Party



CPU. Ref: 1° CPU Datasheet .pp.9.  
2° GPP (General Purpose Port) SCH. Table.

Objectives:

1° Identify the pins for Items 5 Debugging.

2° SCH → CPU → Protocol  
Phy Datasheet Architecture

Note: 1° Naming Conventions.

CPU ✓ → Industrial ✓  
Datasheet → Protocol  
3<sup>rd</sup> Party

2° Ref. Pin "J2-1"  
1st pin

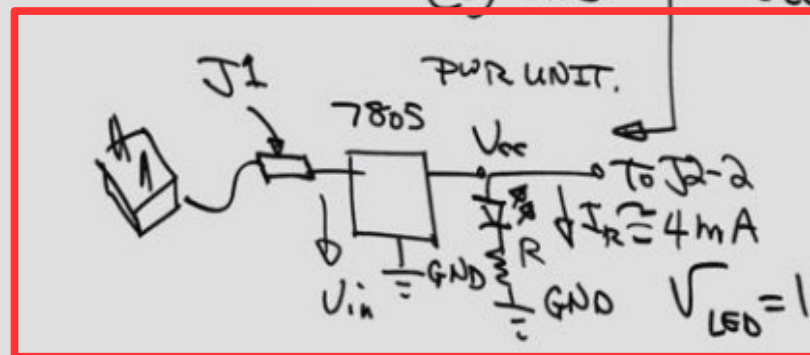
# 8-30-2018 PWR And Debugging Unit Design

CMPE240 Adv. Micro Aug 29, 18 Harry Li

Table 2 Pin Assignment for GPP I/O Debugging.

| CPU Pin         | Description                        | Connector Pin |
|-----------------|------------------------------------|---------------|
| GPP O/P<br>P0.2 | General Purpose Port<br>Output Pin | J2-21         |
| GPP I/P<br>P0.3 | General Purpose Port<br>Input Pin  | J2-22         |
| PWR/VIN         | SVDC                               | J2-2          |

Note: 3° Power up the CPU module.



Complete this table for the rest of the components needed for GPP I/P (input) and O/P (output) testing circuit

|    |                                       | Note                  |
|----|---------------------------------------|-----------------------|
| J1 | Connector (PWR)<br>Wall mount Adaptor | 7805 or<br>Equivalent |

Add the part of the input/output testing circuit

$$V_{CC} = I_R R + V_{LED} \dots (1)$$

4° I/P Testing CKT.  
I/P Testing CKT

