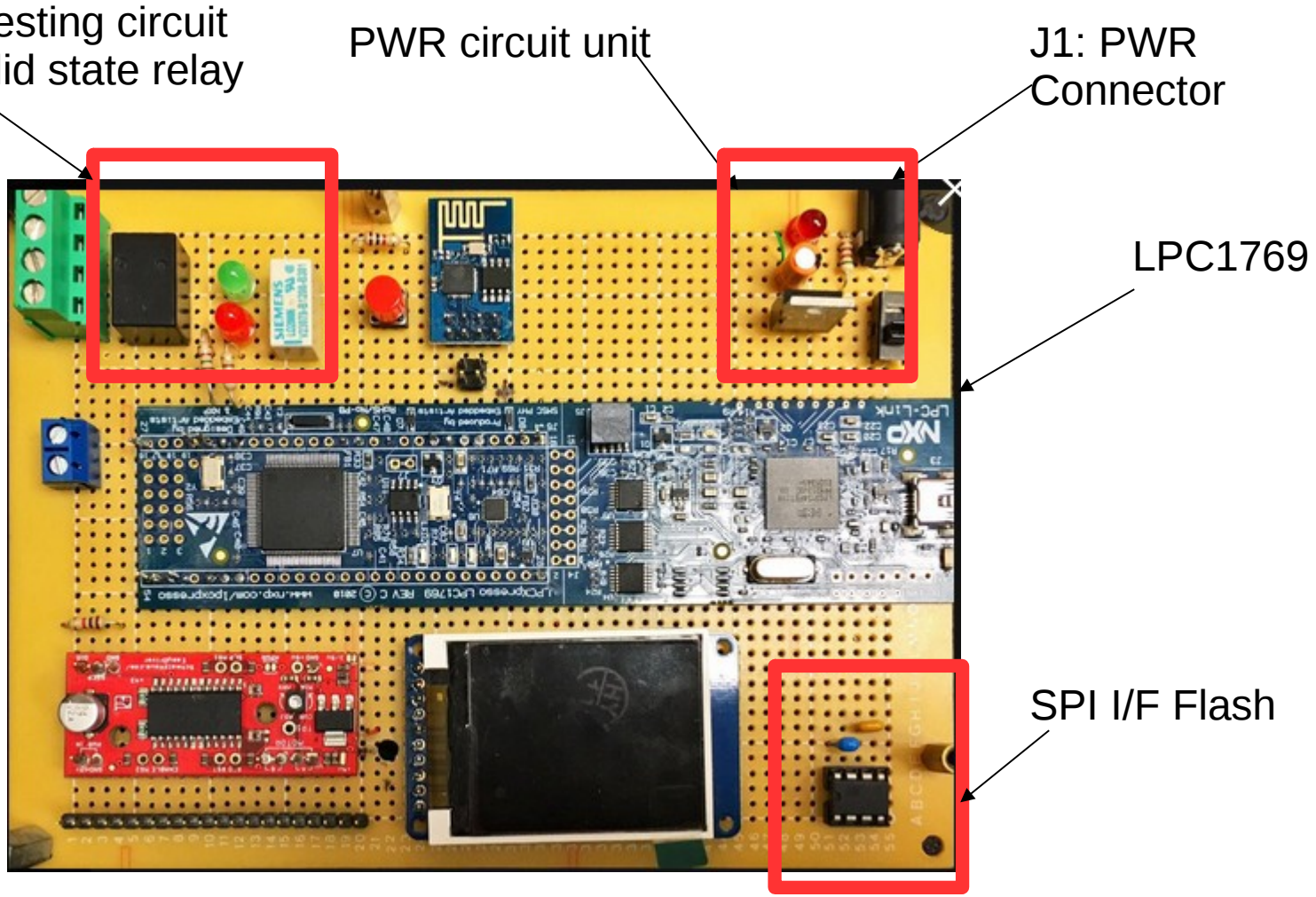
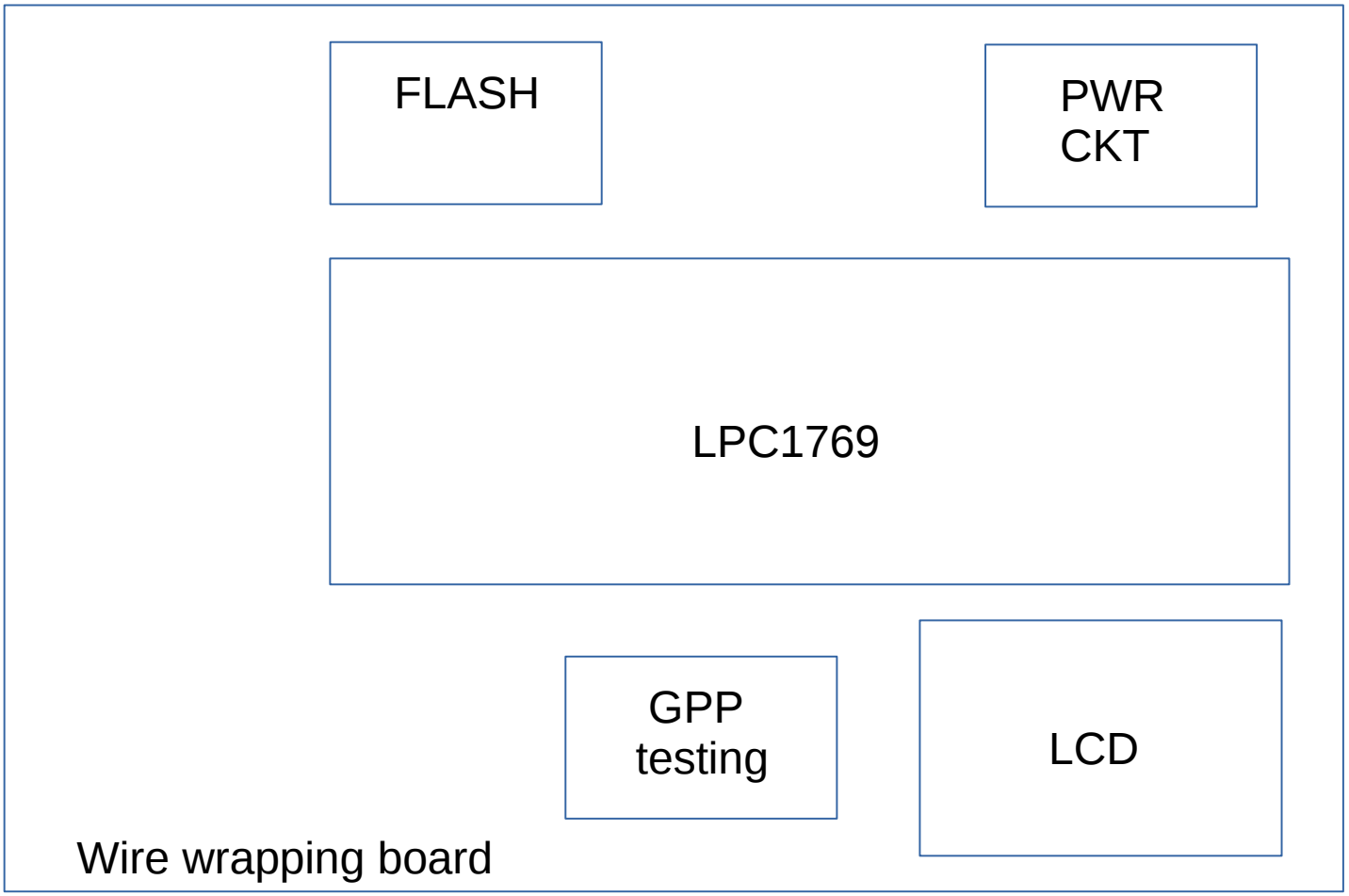
System Layout Design
Front Side



Dimension: 16 x 11 mm or 6.25 x 4.50 inch

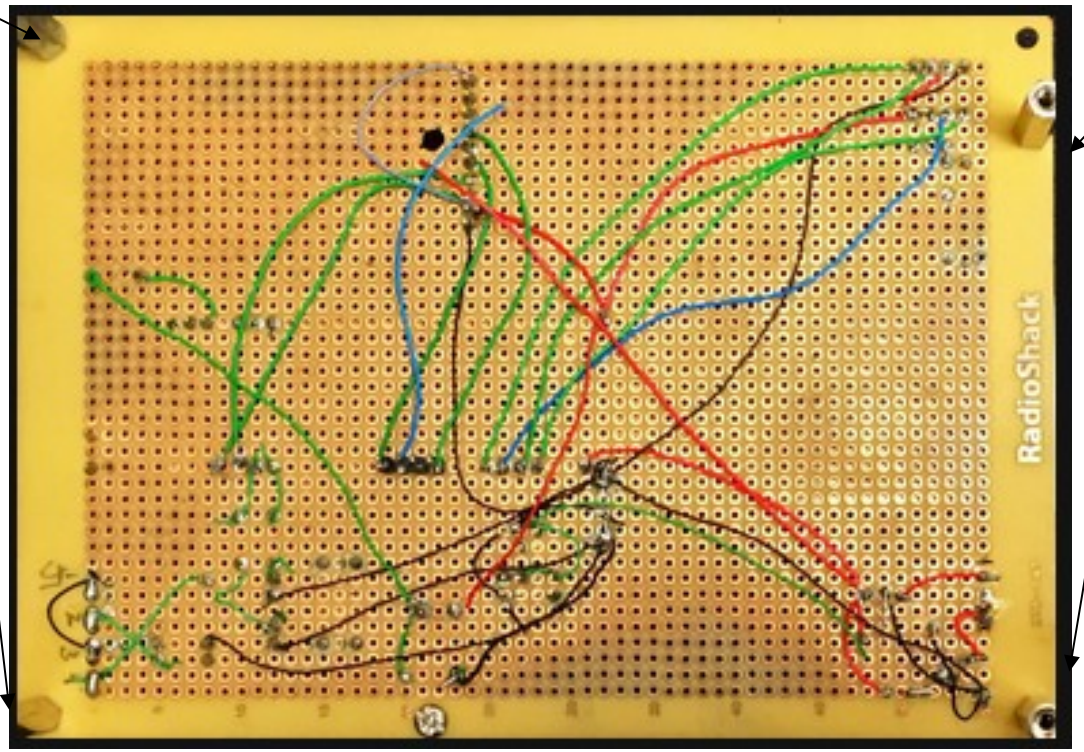
First Thing First, Layout Design



System Layout Design Back Side

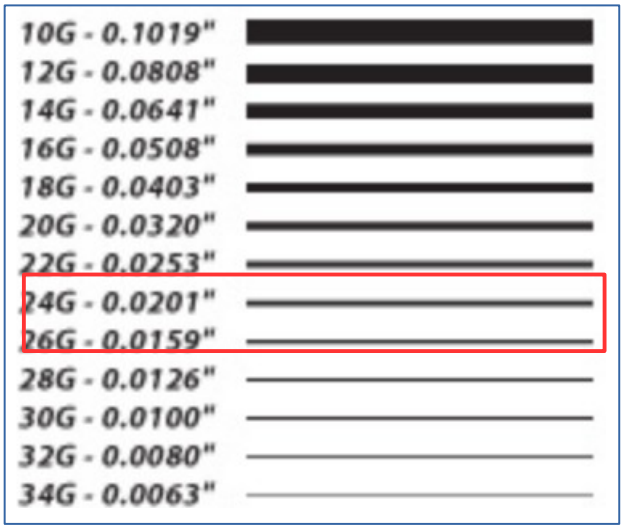
Standoffs

Standoffs



Wire soldered or wire wrapped

Wire Wrapping: 18g to 24G

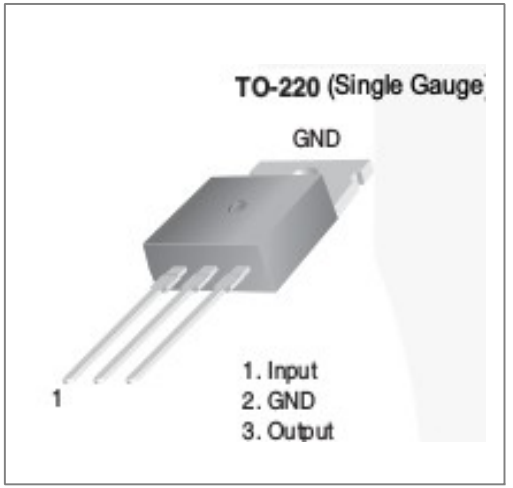


http://www.softflexcompany.com/WSWrapper.jsp?mypage=Tips_Wire_Temper.html

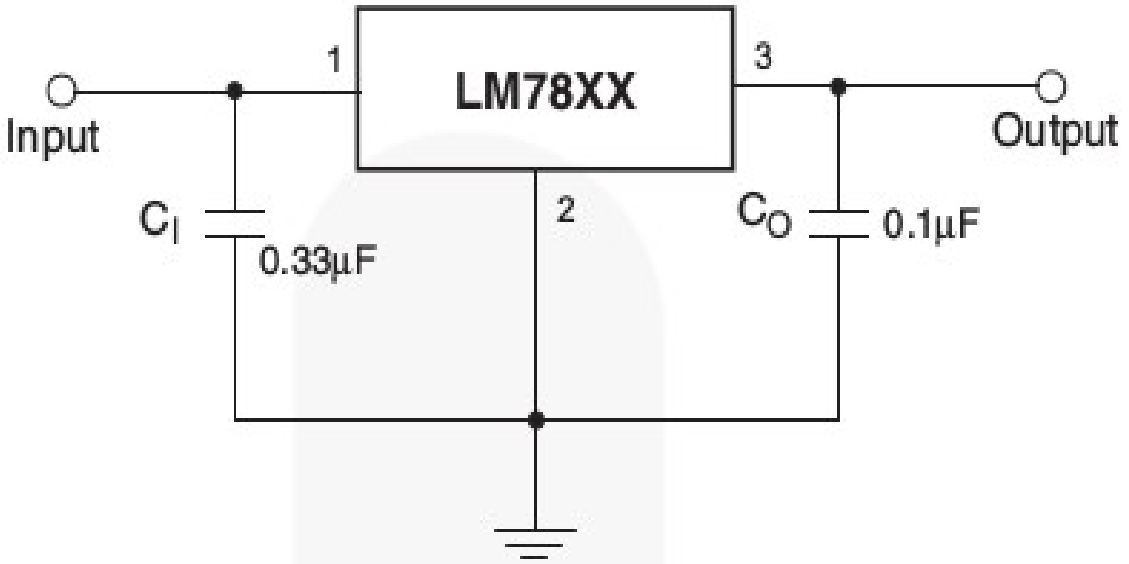
PWR Regulator LM7805

FAIRCHILD SEMICONDUCTOR

LM78XX / LM78XXA
3-Terminal 1 A Positive Voltage Regulator

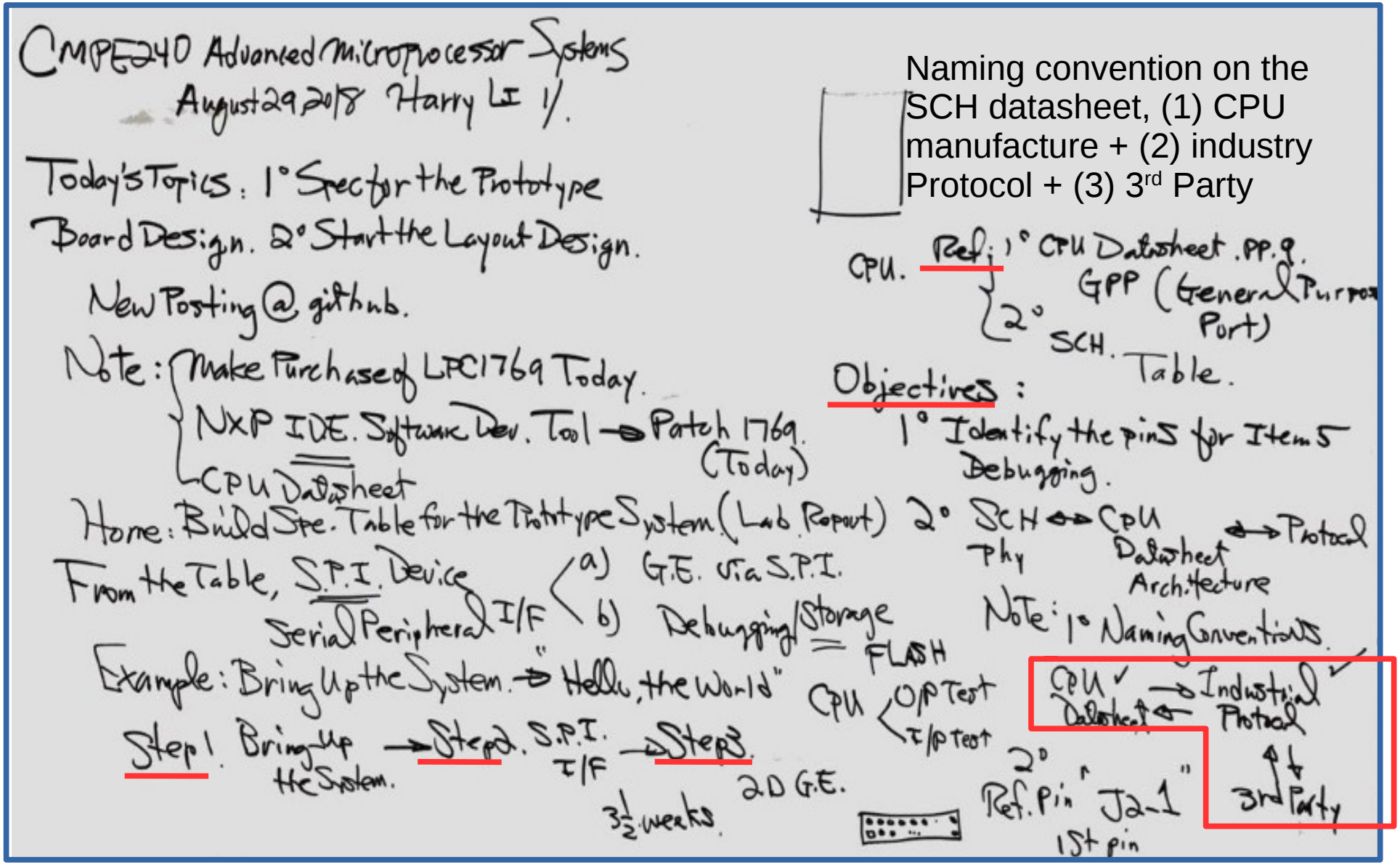


The LM78XX series of three-terminal positive regulators is available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down, and safe operating area protection. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed-voltage regulators, these devices ca
nal components for adjustable voltag



Note: 1. Voltage drop 1.5 volt;
2. current output 1 A.

8-30-2018 PWR And Debugging Unit Design



Harry Li, Ph.D. SJSU

8-30-2018 PWR And Debugging Unit Design

CMPE240 Adv. Micro Aug 29, 18 Harry Li

Table2 Pin Assignment for GPP I/O Debugging

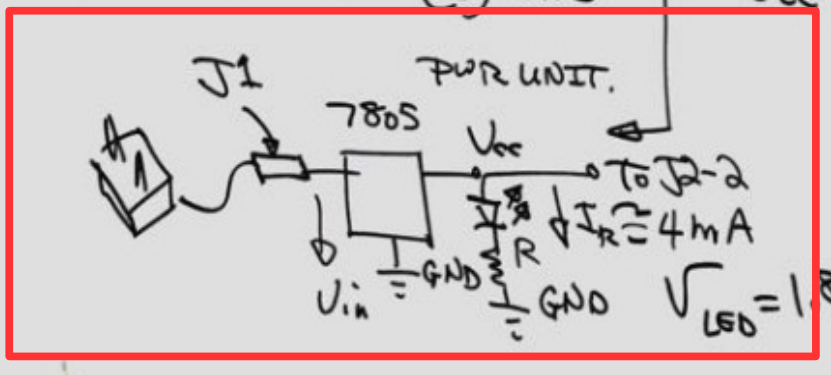
CPU Pin	Description	Connector Pin
GPP O/P P0.2	General Purpose Port Output Pin	J2-21
GPP I/P P0.3	General Purpose Port Input Pin.	J2-22
PWR/VIN	SVDC	J2-2 a) PWR/VIN b) GND

Note: 3. Power up the CPU module.

Complete this table for the rest of the components needed for GPP I/P (input) and O/P (output) testing circuit

J1	Connector (PWR) Wall-mount Adaptor	Note 7805 OR Equivalent

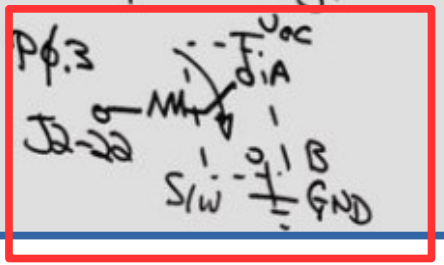
Add the part of the input/output testing circuit

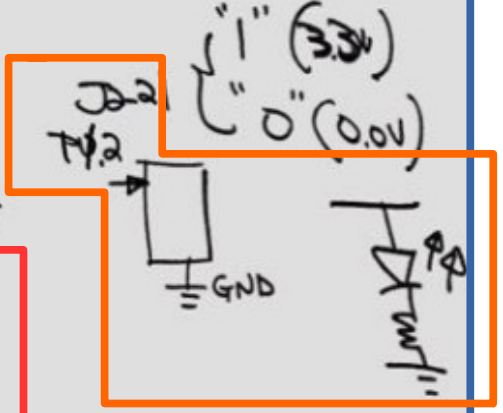


$V_{cc} = I_R R + V_{LED} \ldots (1)$

4. O/P Testing CKT.

I/P Testing CKT.

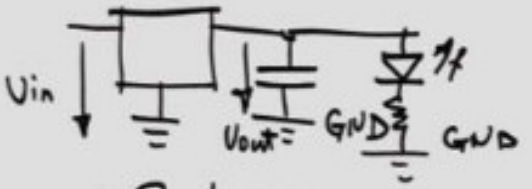




9-5-2018 Design Requirements

CMPE24D Advanced Micro Processor Systems
Sept. 5th 2018. Harry LI //.

Today's Topics: 1° Design & Build Prototype Board.
Colour LCD Modules: 1° ST.I. 2° Through-Hole Connector (Easy to Solder) 3°. Driver Software Lib. ST7735R
Note: On Line, github/hualili ① Software IDE Installation, No.103; ② No104. Layout Design ③ No.105 S.P.I. Glour LCD. ④ No.106 B.O.M ⑤ lpc1769 Patch.
Homework
Homework: Layout for the Board. System Block Diagram. for the Prototype System.
Note: PWR 1° Unit w/ Cap 4.7uF



RC LP.F
2° System Block Diagram(s) w/ Clear Connectivity & Functional Name. (GPP, SPI/MOSI..)
3° Wire Wrapping (Due Next Wednesday)
4° Homework w/ 3 Tables
Naming Convention 2018-9-5
① 240Repo ② HL ③ V3 ④ Name
5° O.P.T./IPT. CKT.
SCH → Good Engn. Practice.

9-5-2018 Design Requirements