

System Layout Design

Front Side

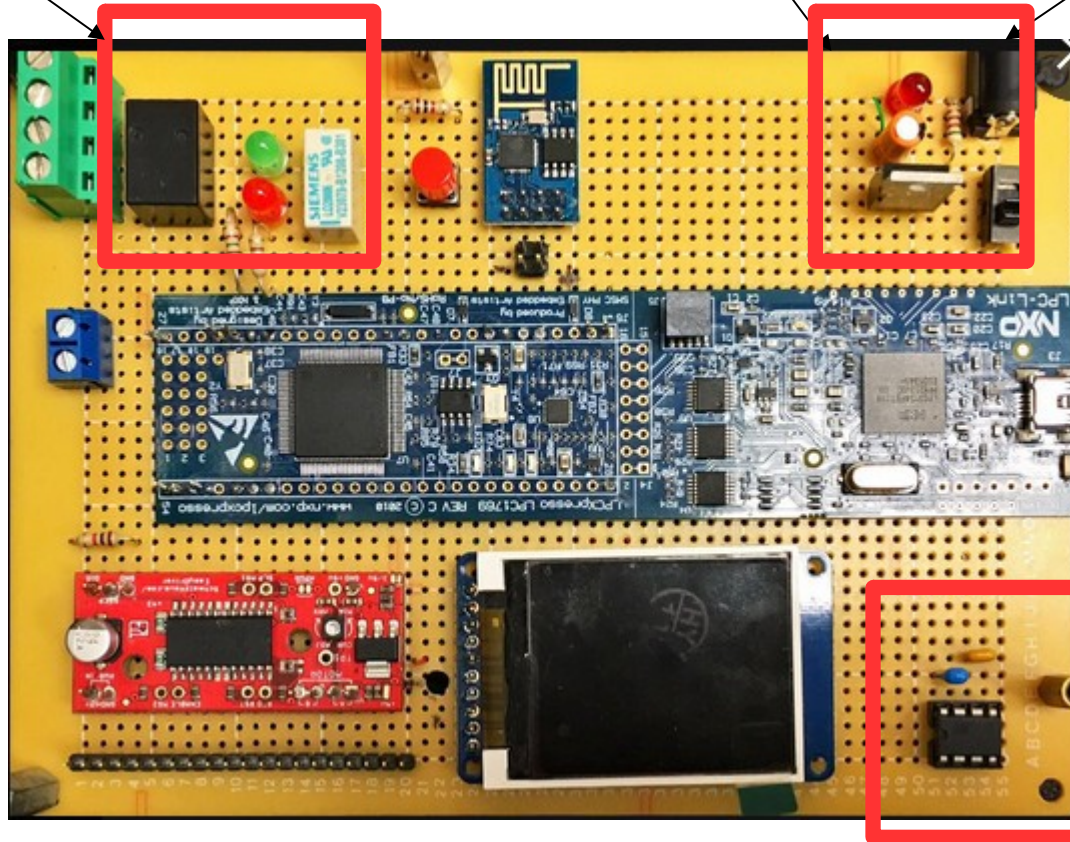
GPIO testing circuit
with solid state relay

PWR circuit unit

J1: PWR
Connector

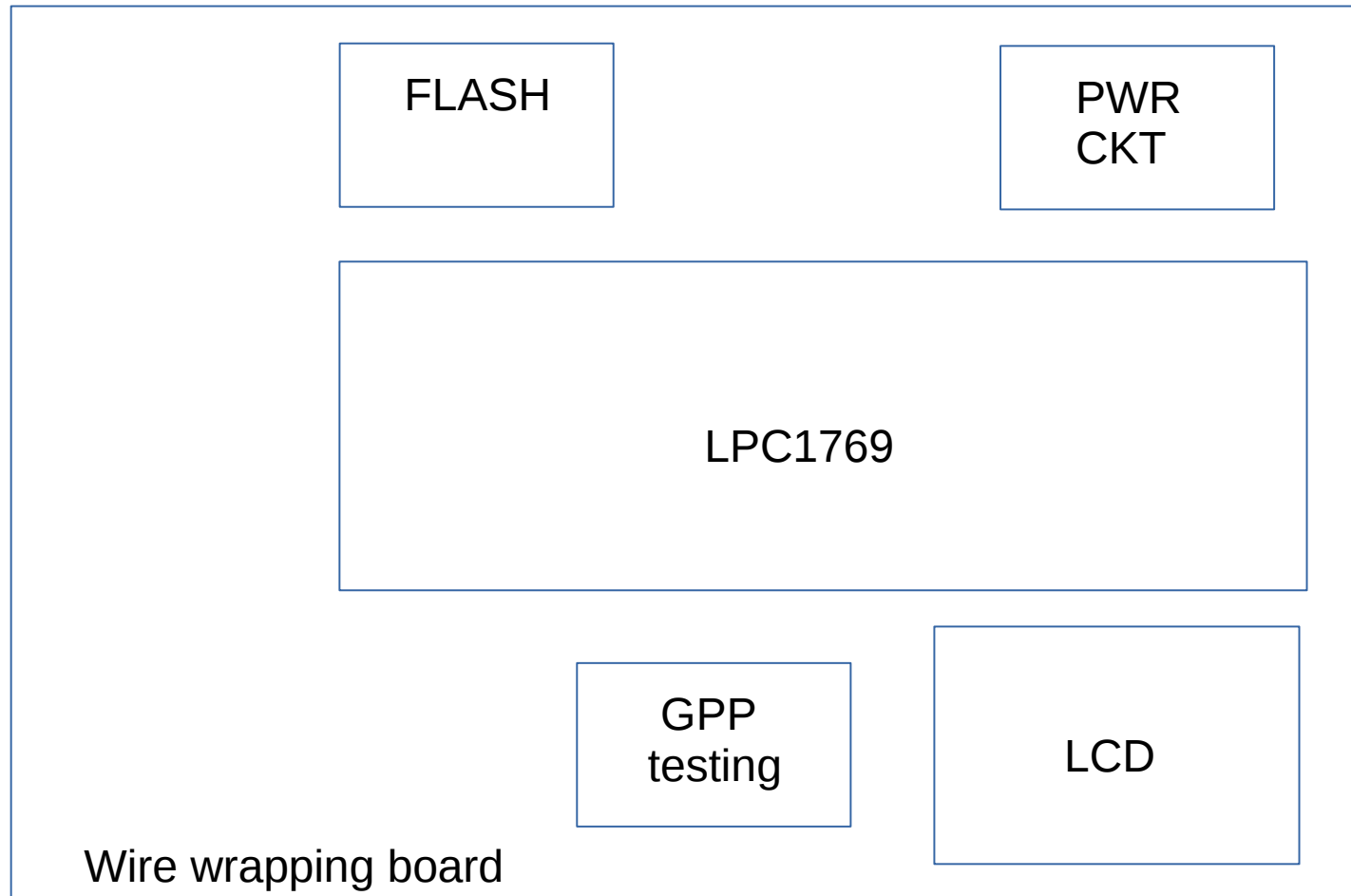
LPC1769

SPI I/F Flash



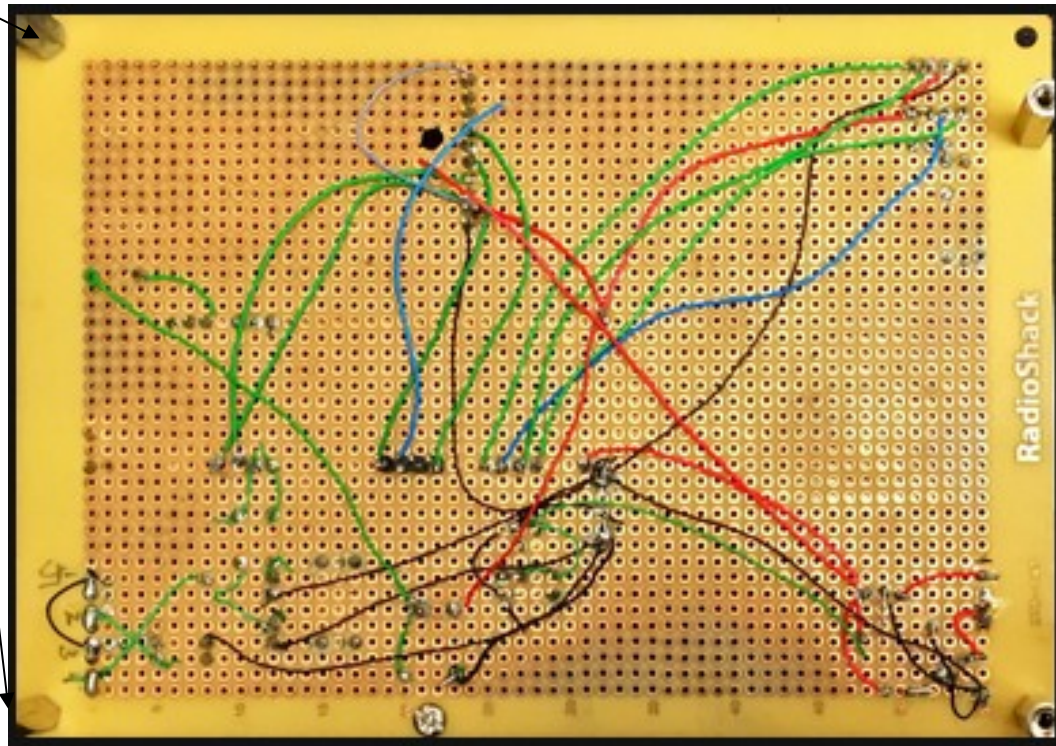
Dimension: 16 x 11 mm or 6.25 x 4.50 inch

First Thing First, Layout Design



System Layout Design Back Side

Standoffs



Standoffs

Wire Wrapping: 18g to 24G

| | |
|---------------|--|
| 10G - 0.1019" | |
| 12G - 0.0808" | |
| 14G - 0.0641" | |
| 16G - 0.0508" | |
| 18G - 0.0403" | |
| 20G - 0.0320" | |
| 22G - 0.0253" | |
| 24G - 0.0201" | |
| 26G - 0.0159" | |
| 28G - 0.0126" | |
| 30G - 0.0100" | |
| 32G - 0.0080" | |
| 34G - 0.0063" | |

Wire soldered or wire wrapped

http://www.softflexcompany.com/WSWrap per.jsp?mypage=Tips_Wire_Temper.html

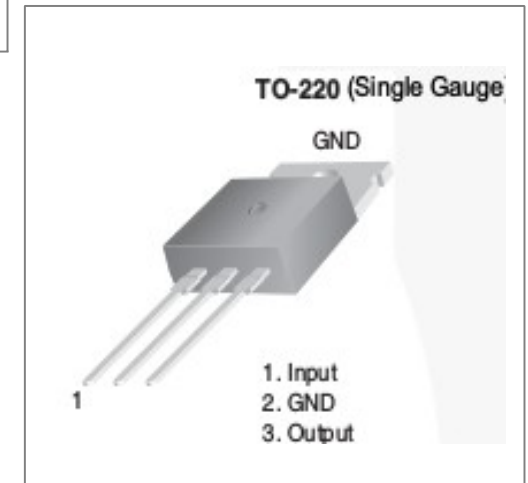
PWR Regulator LM7805



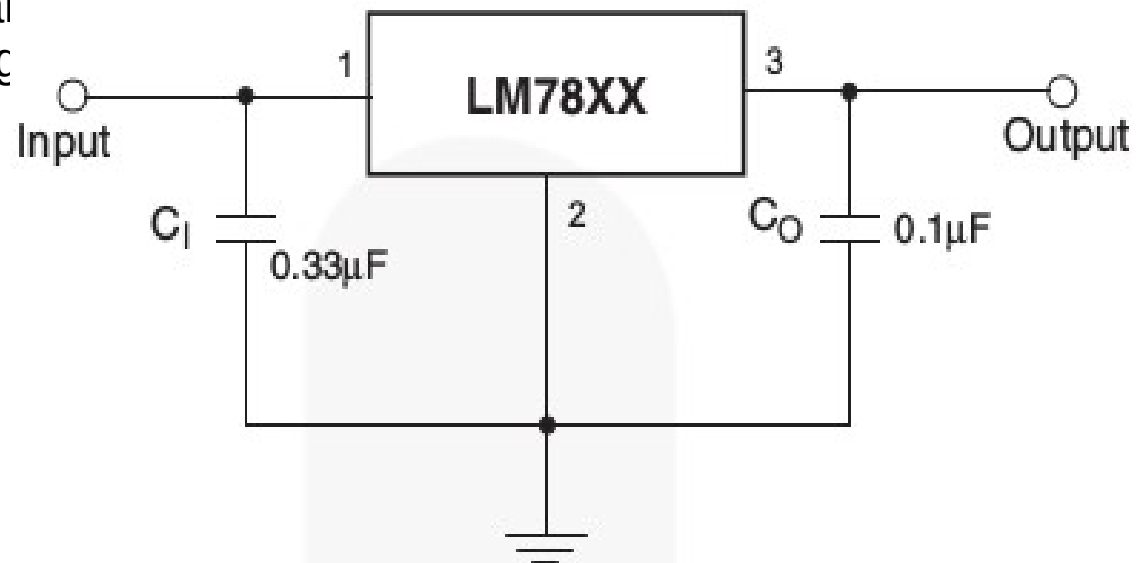
LM78XX / LM78XXA

3-Terminal 1 A Positive Voltage Regulator

The LM78XX series of three-terminal positive regulators is available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down, and safe operating area protection. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed-voltage regulators, these devices can be used as adjustable voltage regulators with external components for adjustable voltage.



Note: 1. Voltage drop 1.5 volt;
2. current output 1 A.



8-30-2018 PWR And Debugging Unit Design

CMPE240 Advanced Microprocessor Systems
August 29, 2018 Harry Li 1/.

Today's Topics: 1° Spec for the Prototype Board Design. 2° Start the Layout Design.

New Posting @ github.

Note: Make Purchase of LPC1769 Today.

NXP IDE. Software Dev. Tool → Patch 1769. (Today)
CPU Datasheet

Home: Build Spec. Table for the Prototype System (Lab Report)

From the Table, S.P.I. Device

Serial Peripheral I/F

Example: Bring Up the System. → "Hello, the World"

Step 1: Bring up the System. → Step 2: S.P.I. I/F → Step 3.

3½ weeks.

2D G.E.



Naming convention on the SCH datasheet, (1) CPU manufacture + (2) industry Protocol + (3) 3rd Party



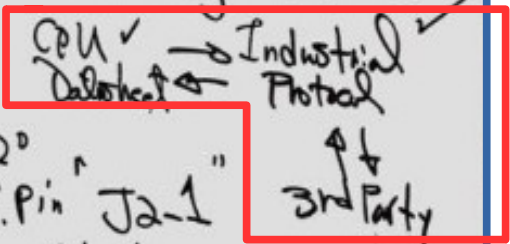
CPU. Ref: 1° CPU Datasheet .pp.9.
2° GPP (General Purpose Port) SCH. Table.

Objectives:

1° Identify the pins for Item 5 Debugging.

2° SCH → CPU → Protocol
Phy Datasheet Architecture

Note: 1° Naming Conventions.



2° Ref. Pin "J2-1" 1st pin

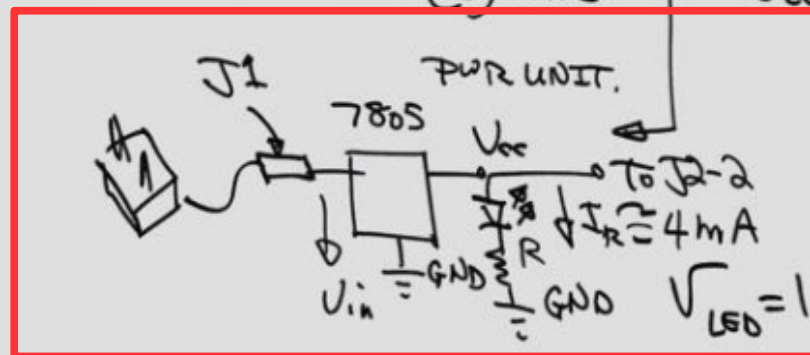
8-30-2018 PWR And Debugging Unit Design

CMPE240 Adv. Micro Aug 29, 18 Harry Li

Table 2 Pin Assignment for GPP I/O Debugging.

| CPU Pin | Description | Connector Pin |
|----------------------------|---|---------------|
| GPP O/P P0.2 | General Purpose Port Output Pin | J2-21 |
| GPP I/P P0.3 PWR/VIN | General Purpose Port Input Pin SVDC | J2-22 J2-2 |

Note: 3. Power up the CPU module.



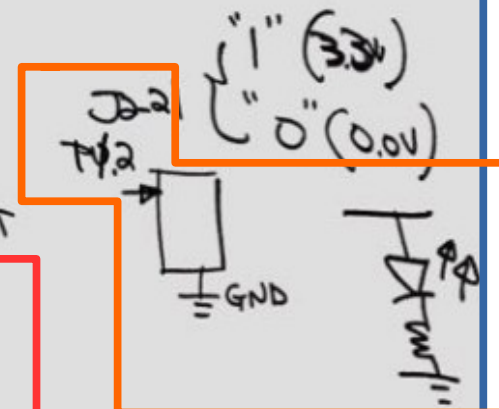
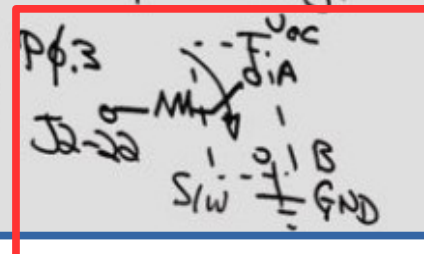
Complete this table for the rest of the components needed for GPP I/P (input) and O/P (output) testing circuit

| | | Note |
|----|---------------------------------------|-----------------------|
| J1 | Connector (PWR) Wall mount Adaptor | 7805 or Equivalent |

Add the part of the input/output testing circuit

$$V_{CC} = I_R R + V_{LEO} \dots (1)$$

4. I/P Testing CKT.
I/P Testing CKT



9-5-2018 Design Requirements

CMPE24D Advanced Microprocessor Systems
Sept. 5th, 2018. Harry Li 1/.

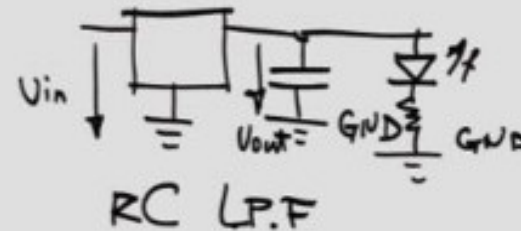
Today's Topics: 1° Design & Build Prototype Board.

Colour LCD Modules: 1° S.T.I. 2° Through-Hole Connector (Easy to Solder) 3° Driver Software Lib. ST7735R

Note: On Line, github/huaili ① Software IDE Installation, No. 103; ② No. 104. Layout Design ③ No. 105 S.T.I. Colour LCD. ④ No. 106 B.O.M. ⑤ lpc1769 Patch.

Homework: Layout for the Board.

Note: PWR
1° Unit w/ Cap 4.7uF
System Block Diagram.
for the Prototype System.



2° System Block Diagrams
w/ clear connectivity & Functional Name. (GPP, SPI/MOSI, ...)

3° Wire Wrapping (Due Next Wednesday)

4° Homework w/ 3 Tables

Naming Convention

2018-9-5

① 240Repo ② HL ③ U3 ④

5° O.P.T./I.P.T. CKT. Name

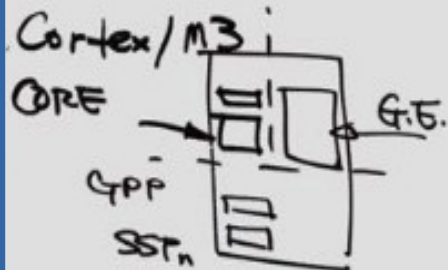
SCH → Good Engn. Practice.

9-5-2018 Design Requirements

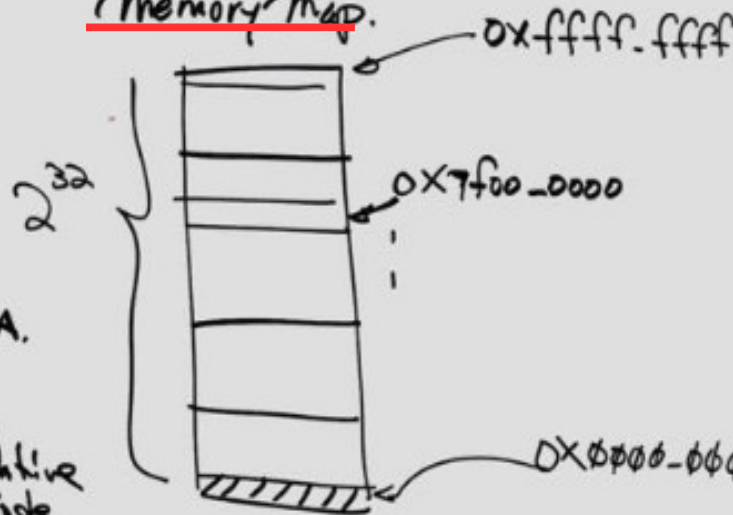
CMPE240 Adv. Micro. Sept. 5, 2018

Software Aspects for the Prototype System.

CPU Datasheet. P.P. 9 + P.P. 13. → IDE.



Memory map.



⑥ 3 bits to uniquely
define A memory Bank.

$a_{31} a_{30} \dots a_2 a_1 a_0$

Little Endian.

$a_{31} a_{30} a_{29}$

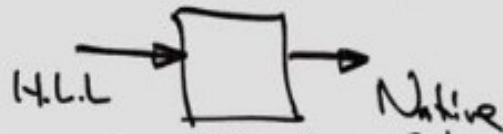
BANK0 BANK1 BANK2

Example: find
Bank2 starting
addr

0x4000-0000

$a_{31} a_{30} a_{29} | a_{28}$
0 0 0 1 0
0 0 1 0
0 1 0 0 →

① RISC ISA.



32 bits. Compiler

Architecture.

② 4GB.

③ Byte Addressable
Machine

⑤ PWR-up Address.

0x0000-0000

+ the addr. when CPU
powered up,

④ 8 Equal Banks

1st BANK → BANK0; 0x0000-0000