SSP_Test.c SPI FLASH Interface

1

Write data to buffer
1. Select (CS =0)
2. Command (Buffer 1=0x84, Buffer 2=0x87)
3. Three bytes address
Data (1-256 bytes)
4. Deselect (CS=1)

2

Write buffer to flash
1. Select (CS =0)
2. Command (Buffer 1=0x83, Buffer 2=0x86)
3. Three bytes address
4. Deselect (CS=1)

3

Read flash to buffer
1 Select (CS=0)
2 Command (Buffer 1=0x53, Buffer 2=0x55)
3 Three bytes address
4 Deselect (CS=1)

4

Read buffer
1. Select (CS =0)
2. Command (Buffer 1=0xd4, Buffer 2=0xd6)
3. Three bytes address
4. Unnecessary byte(1 byte)
- Data (1-256 bytes)
5. Deselect (CS=1)

5

Erase Flash
1. Select (CS =0)
2. 0xc7
3. 0x94
4. 0x80
5. 0x9a
6. Deselect (CS=1

uint8_t SSP1exchangeByte(uint8_t out)

```
uint8_t SSP1exchangeByte(uint8_t out){
    LPC_SSP1->DR = out;
    while(LPC_SSP1->SR & (1<<4));
    return LPC_SSP1->DR;
}
```

Table 374: SSPn Status Register

0	TFE	Transmit FIFO Empty. This bit is 1 is the Transmit FIFO is empty, 0 if not.
1	TNF	Transmit FIFO Not Full. This bit is 0 if the Tx FIFO is full, 1 if not.
2	RNE	Receive FIFO Not Empty. This bit is 0 if the Receive FIFO is empty, 1 if not.
3	RFF	Receive FIFO Full. This bit is 1 if the Receive FIFO is full, 0 if not.
4	BSY	Busy. This bit is 0 if the SSPn controller is idle, or 1 if it is currently sending/receiving a frame and/or the Tx FIFO is not empty.

Table 373: SSPn Data Register (SSP0DR)

Bit	Symbol	Description
15:0	DATA	**Write:** software can write data to be sent in a future frame to this register whenever the TNF bit in the Status register is 1, indicating that the Tx FIFO is not full. If the Tx FIFO was previously empty and the SSP controller is not busy on the bus, transmission of the data will begin immediately. Otherwise the data written to this register will be sent as soon as all previous data has been sent (and received). If the data length is less than 16 bits, software must right-justify the data written to this register. **Read:** software can read data from this register whenever the RNE bit in the Status register is 1, indicating that the Rx FIFO is not empty. When software reads this register, the SSP controller returns data from the least recent frame in the Rx FIFO. If the data length is less than 16 bits, the data is right-justified in this field with higher order bits filled with 0s.

Table 370. SSP Register Map

DR	Data Register. Writes fill the transmit FIFO, and reads empty the receive FIFO.	R/W
SR	Status Register	RO