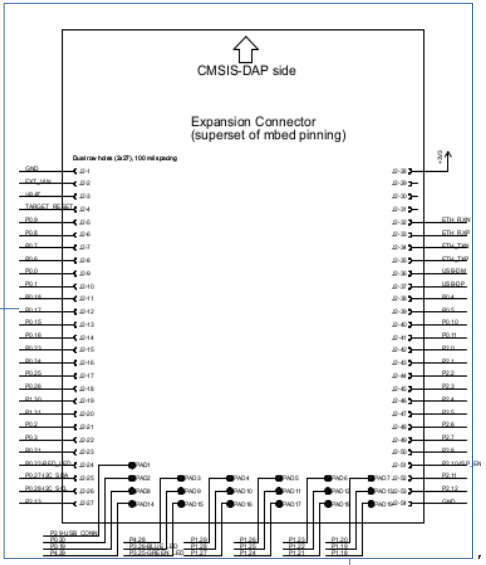
Overview: Three Aspects Into One

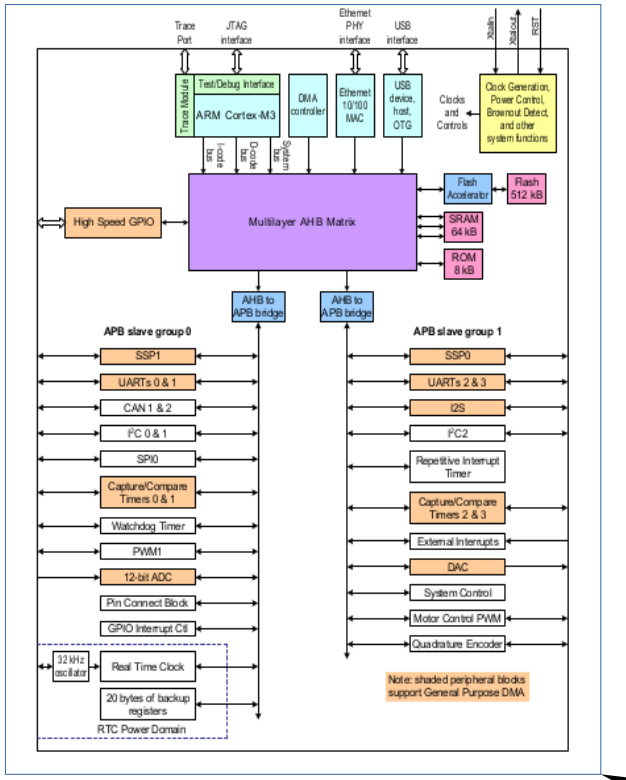
For Advanced Microprocessor Systems

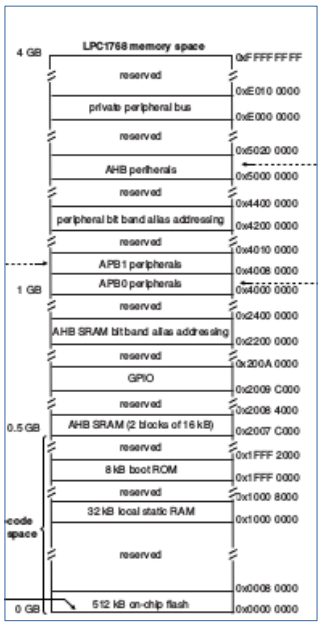
1. CPU data sheet UM10360
NXP Semiconductors
LPC17xx user manua
(1) CPU Block Diagram: pp. 9
(2) Memory map: pp. 14

2. Schematics of the board design

LPCXpresso1769_CD_revD(1)







3. Compiler (IDE: integrated development platform)

The MCUXpresso IDE

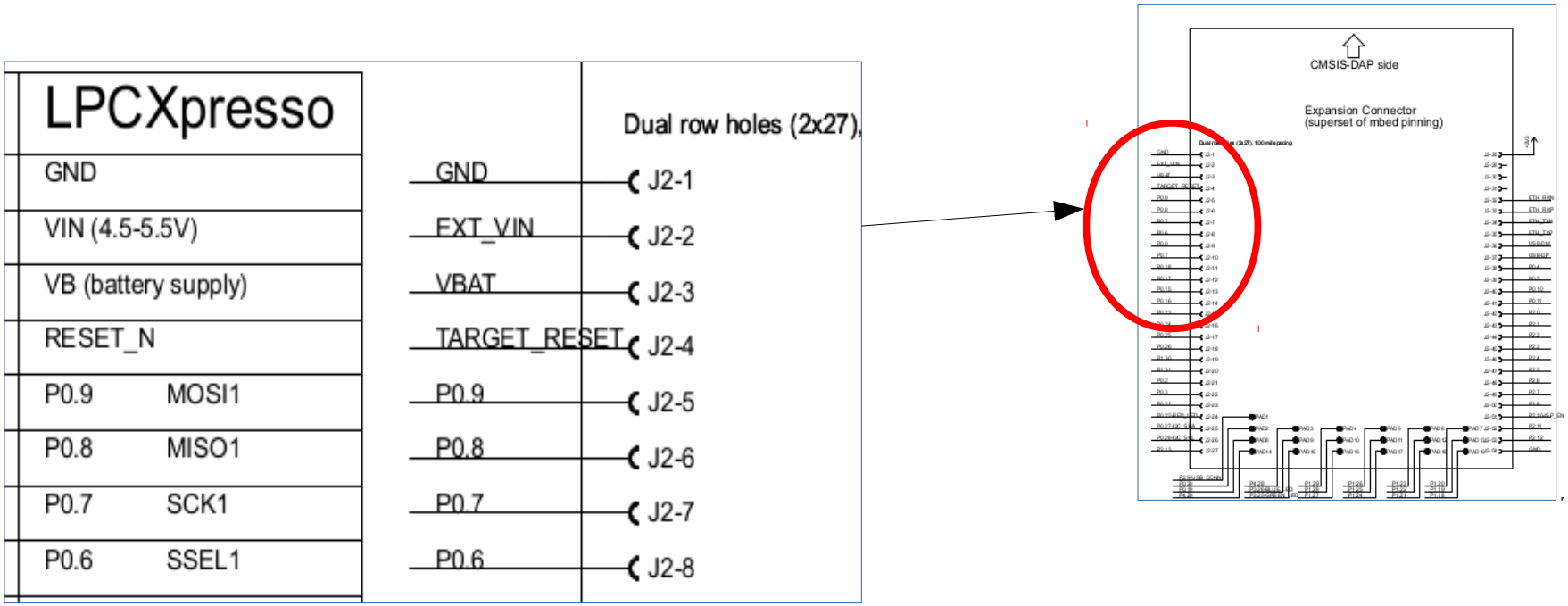
3.1 GUI
3.2 Cross compiler
3.3 flash writer
3.4 processor specific source code to port the compiler to the CPU

lpcopen_2_10_lpcxpresso_nxp_lpcxpresso_1769

Harry Li, Ph.D.

Identify CPU Pins From The Connector

For SPI Interface Design



Mapping Cross Compiler to LPC17xx

https://raw.githubusercontent.com/ajhc/demo-cortex-m3/master/lpcxpresso-lpc1769/lpc1769/drivers/LPC17xx.h

```
// specital purpose registers  typedef struct
IRQn_Type;
LPC_SC_TypeDef;
LPC_PINCON_TypeDef;
LPC_GPIO_TypeDef;
LPC_GPIOINT_TypeDef;
LPC_TIM_TypeDef;
LPC_PWM_TypeDef;
LPC_UART_TypeDef;
LPC_UART0_TypeDef;
LPC_UART1_TypeDef;
LPC_SPI_TypeDef;
LPC_SSP_TypeDef;
LPC_I2C_TypeDef;
LPC_I2S_TypeDef;
LPC_RIT_TypeDef; //Repetitive Interrupt Timer (RIT) register structure definition
LPC_RTC_TypeDef;
LPC_WDT_TypeDef;
LPC_ADC_TypeDef;
LPC_DAC_TypeDef;
LPC_MCPWM_TypeDef;//Motor Control Pulse-Width Modulation (MCPWM)
LPC_QEI_TypeDef;  //Quadrature Encoder Interface (QEI)
LPC_CANAF_TypeDef;//Controller Area Network Acceptance Filter
LPC_CANCR_TypeDef;//CAN control register
LPC_GPDMA_TypeDef;
LPC_GPDMACH_TypeDef;//General Purpose Direct Memory Access Channel
LPC_USB_TypeDef;
LPC_EMAC_TypeDef;
```

Mapping Cross Compiler to LPC17xx

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```
/*********************************************************************/
/*                  Peripheral memory map                            */
/*********************************************************************/
/* Base addresses                                                    */
#define LPC_FLASH_BASE       (0x00000000UL)
#define LPC_RAM_BASE         (0x10000000UL)
#ifdef __LPC17XX_REV00
#define LPC_AHBRAM0_BASE     (0x20000000UL)
#define LPC_AHBRAM1_BASE     (0x20004000UL)
#else
#define LPC_AHBRAM0_BASE     (0x2007C000UL)
#define LPC_AHBRAM1_BASE     (0x20080000UL)
#endif
```

```
/*********************************************************************/
/*                  Peripheral declaration                           */
/*********************************************************************/
#define LPC_SC               ((LPC_SC_TypeDef       *) LPC_SC_BASE       )
#define LPC_GPIO0              ((LPC_GPIO_TypeDef     *) LPC_GPIO0_BASE    )
#define LPC_GPIO1              ((LPC_GPIO_TypeDef     *) LPC_GPIO1_BASE    )
#define LPC_GPIO2              ((LPC_GPIO_TypeDef     *) LPC_GPIO2_BASE    )
```