Jan 27 (Wed), 2021 | Harry Li

CMPE240 Welcome to 240 Section 2

Email: hua.li@sjsu.edu
Office Hours: M.W. 4:30-5:30 pm.
~~Zoom Based~~
Greensheet github/hualili
CMPE240/2018F

References:
1. Greensheet on github
(650) 400-1116 Text message
Prerequit Requirements 180D

Advanced Microprocessor Systems
Smart phones ↑ RISC Architecture
5G, Edge AI → IoT, AI → GPU Architectural Aspects

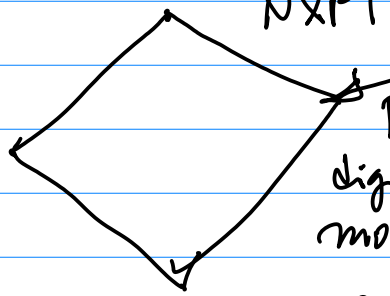
Prototype System
Fully Functional Microprocessor System

Action Items:
1° github/hualili/cmpe240
2° Pre-requit Requirements, 180D
3° LPC1769 CPU module
digi-key.com or mouser.com

Handson: multiple projects, 3 miles stones

4° CPU Datasheet 5° MCU expresso

CMPE240 Feb1 (Mon)
Todays Topics: 1° System Level Architecture — LPC1769
Ref: github/hualili/cmpe240/2018F-102 2° CPU Datasheet
Example:
1° CPU Module @ center of the System layout Design
NXP1769



2° Wirewrapping Board
Dimension: 6"x4"
with Through-Holes, and one side of Board whose through-Holes with metal plating; But not the entire Board (just the throug-Holes)

3° PWR CKT: J1 Connector
Right Angle Connector; S/W Toggle Switch; IC Regulator 7805, 1117
Red LED 4mA 10mA
Resistor, Cap. (LPF)
Note: Debug/Development No External PWR CKT
NXP.com

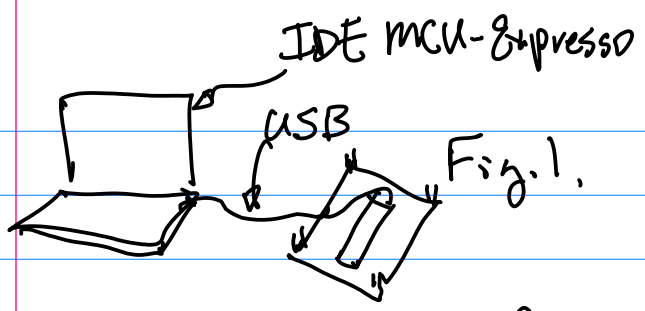
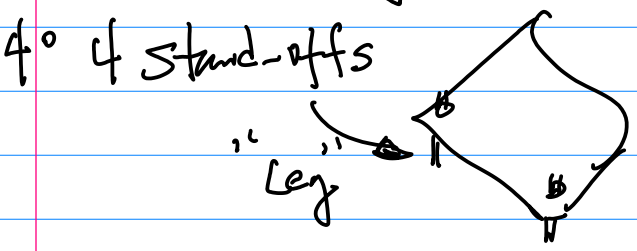


Fig. 1.



Ref: CPU module Design. pdf
github, Rev. D. OR higher

From the Datasheet, Two tables on Each side of the CPU module
First, Left side, the outter table is for mbed, Not interested.

Naming Convention:

① CPU pin is named identical as the name appened in the CPU Datasheet;

② The physical connector Label(s) are given on the SCH to match up the physical Board

Question: Find the pin for GND

From SCH,

Connectivity Table ← Connector J2 Position 1

Functional Pin	Physical Pin	Note
GND	J2-1	
VIN	J2-2	4.5~5.5VDC

Enumeration of the pin(s)
CPU pin (1st pin) starts as "0";

CPU Datasheet 2018S-3-UM10360
CPU Architecture, pp. 9

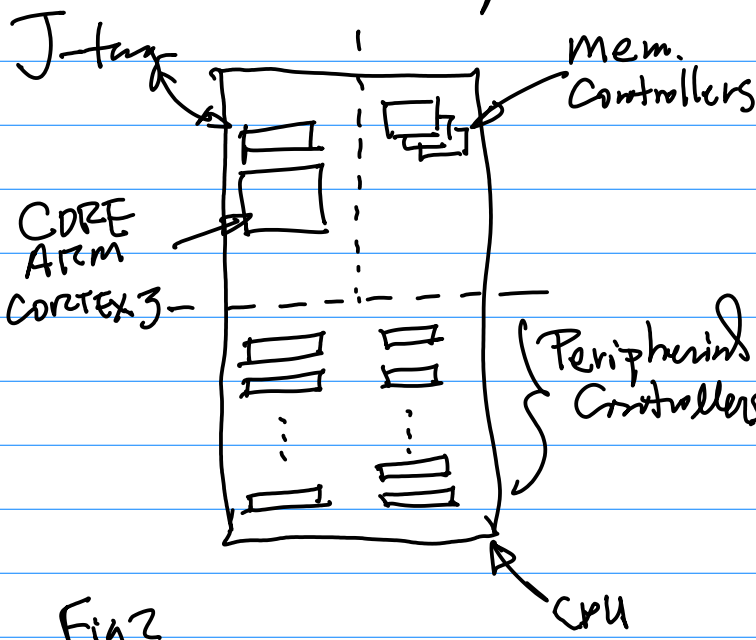


Fig 2.
Peripheral controllers (SCH, CPU Datasheet)