SEMICONDUCTORS

Semi-conductors → Semi-conductors are those materials which have conductivity between Conductors (Cu, Ag) and Insulators (glass, diamond)

* semi-conductors have very much use in electronics and communication because semi-conductors have two basic properties.
  - (i) we can control the number of charge carriers (electrons and holes) i.e conductivity can be controled.
  - (ii) can give current in one direction and zero in other (like in rectifier)

* Temperature coefficient (α) of a semi-conductor is -ve. Hence resistivity and hence resistance of semi-conductor decreases with increase in Temperature.

* Pure semi-conductors (ELEMENTAL) found in nature are Silicon (Si) and Geremanium (Ge)

* Compound semi-conductors → GaAs, InP etc

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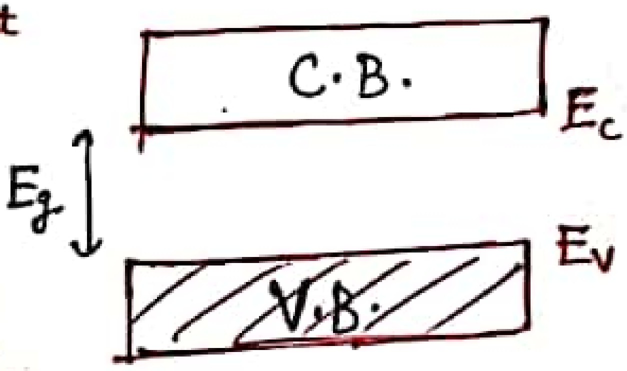
* Valance Band (VB) → Highest energy band filled with valence e^-s.



* VB e^-s do not participate in electrical conductivity.

* Conduction Band (CB) → The energy Band above Valance Band is called C.B.

→ (Lowest unfilled energy band)

* Electrons may or may not exist in CB.
* C.B. e^-s are responsible for conductivity.
* The gap b/w top of VB and bottom of CB is called Energy band gap. (E_g)

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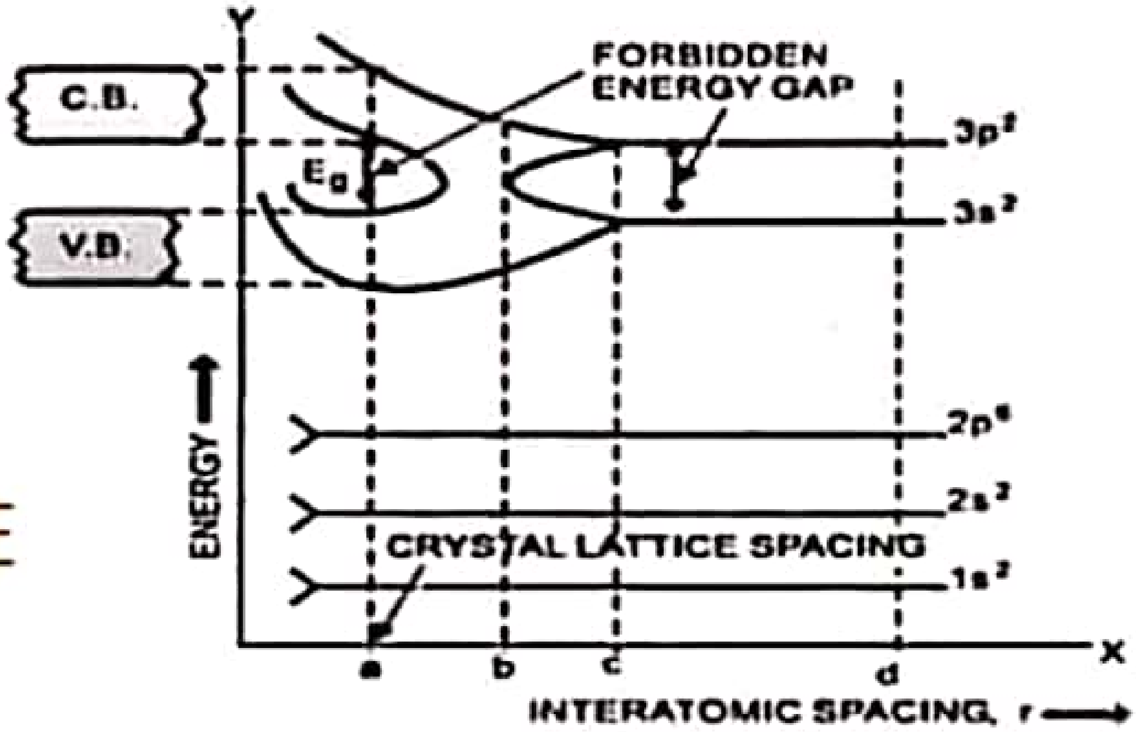
Energy Band Theory of Solids-

According to Bohr's theory there are well defined energy levels of electrons in an atom. If large number of atoms are brought close to one another to form a crystal, they begin to influence each other. Due to this interatomic interaction there is no modification in the energy levels of the electrons in the outer shell but there is a considerable modification in the energy levels of the electrons in the outer shells.



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To understand modification in energy levels of electrons consider a silicon crystal containing N atoms.

Silicon (si) atoms have four valance electrons i.e. number of electrons in the outermost orbit is 4. Therefore the total number of valence electrons in the crystal of si is 4N.

(i) If the interatomic spacing of the si atoms is very Large ($r = d$), then there is no interatomic interaction

(ii) When the interatomic spacing r is less than d but greater than c, then there is no visible spliting of energy levels.

(iii) When the interatomic spacing r is equal to c, the energy of outermost shell electrons of neighbouring silicon atoms start changing i.e the spliting of these energy levels occurs. Whereas there is no change in the energy. levels of electrons in the inner shells.

(iv) When interatomic spacing r lies inbetween b and c ($b < r < c$), instead of a single 3s or 3p level, we get a large number of closely packed levels. Where 2N levels corresponding to a single 3s level and 6N levels for a single 3p level of an isolated atom. This spreading of energy levels reduces the energy gap between 3s and 3p levels of free atom.

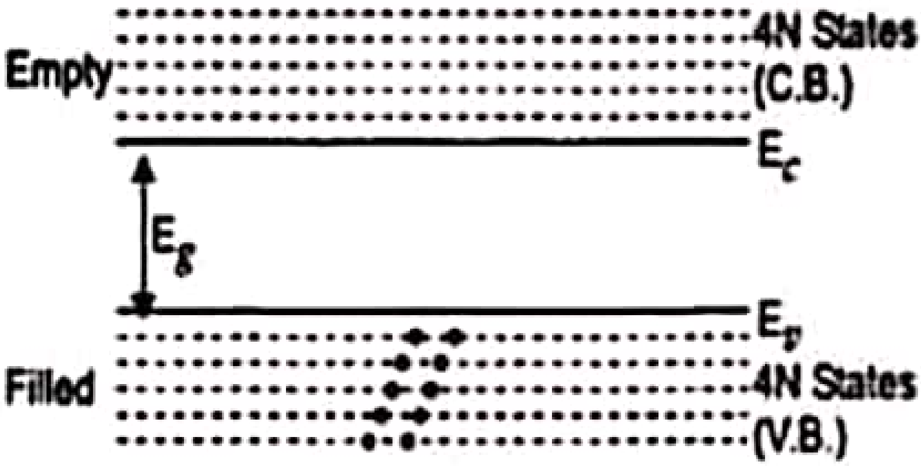
This collection of closely spaced levels is called an energy band.

(v) When the interatomic spacing r becomes equal to b but greater than a ($r = b > a$), the energy gap between 3s and 3p levels completely disappears. In such a situation it is not possible to distinguish between the electrons belonging to 3s and 3p subshells. We can only say that 4N levels are filled and 4N levels are empty.

vi) when the interatomic spacing r becomes equal to a (r = a) then the band of 4N filled energy levels is separated from the band of 4N unfilled energy levels by an energy gap called energy band gap, which is denoted by E_g.

The lower completely filled band is called valance band and the upper unfilled band is called conduction band. The minimum energy required for shifting electrons from valance band to conduction band is equal to energy band gap (E_g).

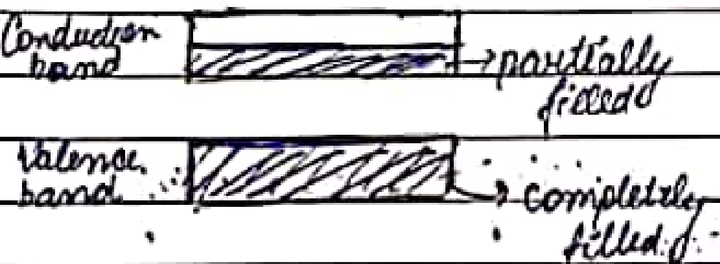
PME

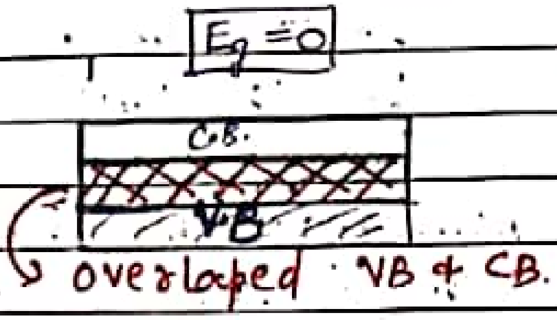


Distinction b/w conductors, insulators & semi-conductors on the basis of band theory

1) Metals/conductors:

In conductors, either there is no energy gap b/w the completely filled valence band & partially filled conduction band or C.B. & V.B. are partly overlapped.

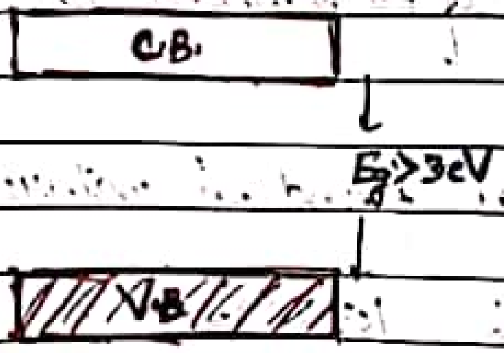




→ From the above, it is clear that, a very small ↑ in energy can make large no. of e⁻s available for the conduction in C.B.

2) Insulators.

In Insulators, V.B. is completely filled while C.B. is completely empty with a large energy gap $\boxed{E_g > 3eV}$ b/w V.B. & C.B.



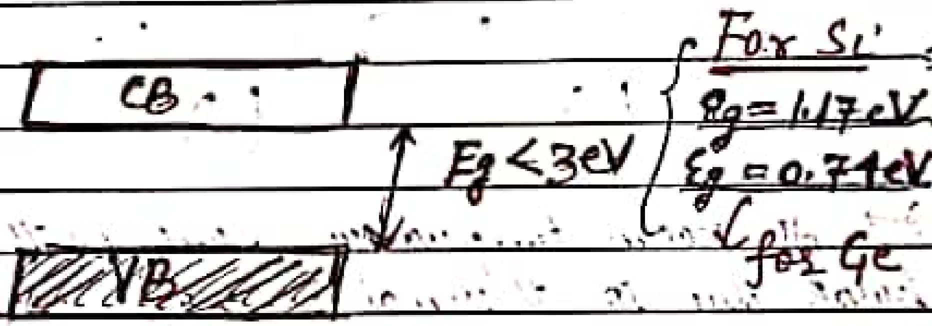
Even a strong E.F. cannot give this amount of energy to an e⁻ to jump from V.B. to C.B.

Hence, due to very small no. of e⁻s in C.B., insulators are poor conductors.

3) Semiconductors :

At 0K, no e⊖ is available for the conduction as each Si atom share its four valence e⊖s with its neighbouring 4 Si atoms.

→ Hence at 0K, C.B. is completely empty and V.B. is completely filled.



⇒ But at room temperature, some of the covalent bonds may break & e⊖s get free and are available for the conduction.

⇒ Hence, semiconductor acquire small conductivity at room temperature.

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INTRINSIC Semiconductors

* A semi-conductor free from any kind of impurity is called an intrinsic semiconductor.

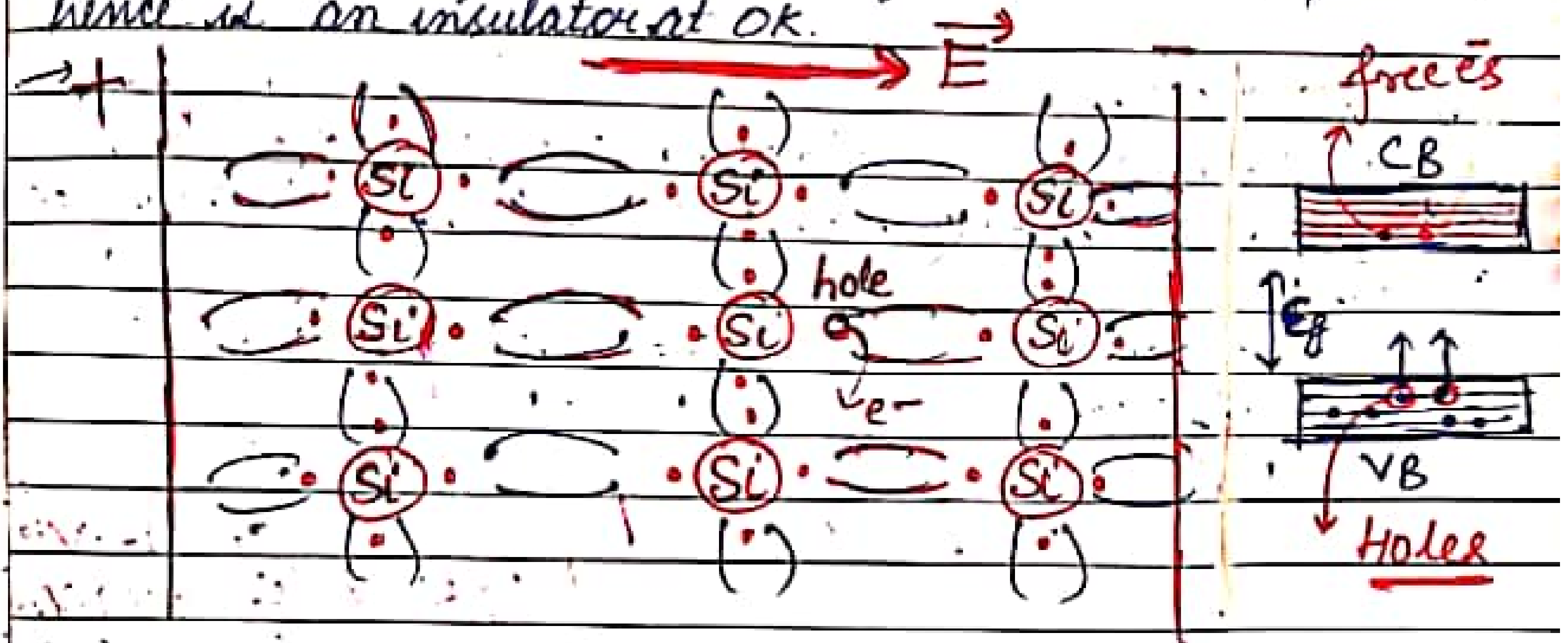
e.g. Si & Ge.

→ Electronic configuration of Si : $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2$

→ Hence there are 4 e⁻s in each Si atom

→ At 0K, each Si-atom shares its valence e⁻s with other Si atoms to make covalent bonds.

Hence, each Si- atom behaves as if its octet is completed & hence is an insulator at 0K.



→ At room temperature, some of the covalent bonds may break due to thermal energy. Hence e^-s may break away from a covalent bond & is available for the conductivity, leaving behind a vacancy with an effective +ve charge called hole.

→ In intrinsic semiconductor, no. density of e^-s & holes are always equal.

i.e. $\boxed{n_e = n_h = n_i = \text{intrinsic charge carrier density}}$

→ The motion of both e^-s & holes constitute current.

i.e. $\boxed{I = I_e + I_h}$

→ Hole is slightly heavier than e^-s.

$$n_e = n_h = n_i$$

$$\boxed{\mu_h = \frac{V_d}{E}}$$

* In a pure semiconductor, $n_e = n_h$ & has small no. density i.e. why a pure semi-conductor has low conductivity.

* When an EF is applied e^-s move in the direction opposite to EF and holes in the dir^n of EF to constitute electric current.

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* Also charge carriers in pure semi-conductor are always thermally generated. Hence flexibility is not available to control their no.

Doping :→
The process of addition of suitable impurity to a pure semi-conductor.
* The impurity atoms added are called Dopants & the semi-conductor formed is called EXTRINSIC semi-conductor.

Essential conditions for doping.

1. Dopant atom should take the position of semi-conductor atom.
2. Size of dopant atom should be same as that of semi-conductor atom.
3. Dopant atoms should not distort the crystal structure/lattice.
4. The concentration of dopant atoms should be small. (about 1ppm)

Methods of Doping
Doping can be achieved by
(1) adding impurity atoms in the melt of semi-conductor or
(2) heating the semiconductors in an atmosphere containing dopant atoms so that these diffuse into the semiconductor or
(3) bombarding the dopant atoms into the semi-conductor.

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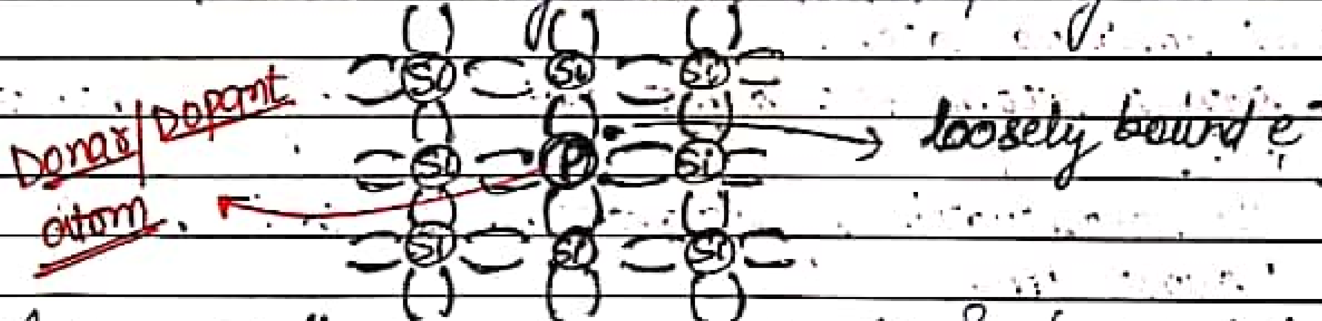
Extrinsic semi-conductor :→
A semi-conductor doped with some suitable impurity atoms so as to ↑ the no. density of charge carriers

Types :→

1. n-type semiconductor
2. p-type semiconductor

1. n-type semiconductor
→ When a pure semiconductor is doped with pentavalent impurity (P, As, Sb, Bi) atoms having 5 valence e⁻s, the resulting semi-conductor is called n-type semiconductor.
→ Out of the five e⁻s, 4 of its valence e⁻s form covalent bonds with the neighbouring Si atoms while 5th e⁻ remains loosely bound to the impurity atoms

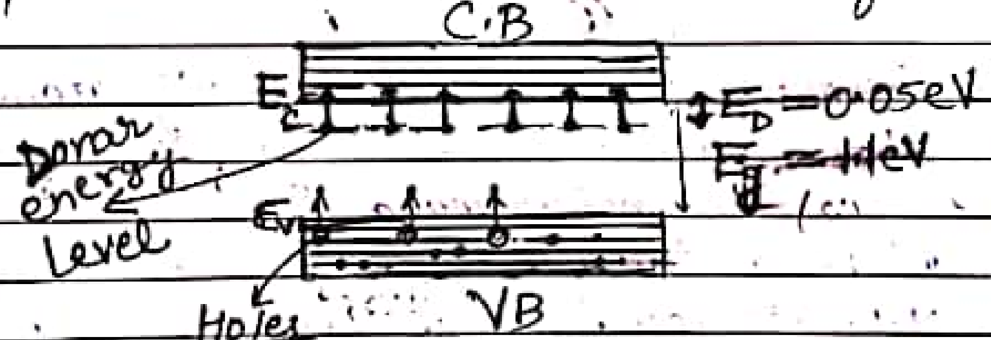


→ A very small energy (0.01 eV) for Ge & (0.05 eV) for Si is required to get this e⁻ free.
→ At room temperature, thermal energy is sufficient to get this e⁻ free.
→ As each pentavalent impurity atom donates one extra e⁻ for the conduction. Hence it is called donor atom.
→ With ↑ in temperature, covalent bonds also break creating equal no. of e⁻s & holes.
But the overall concentration of e⁻s is more, hence, the semiconductor is called n-type

→ In n-type semiconductor, the majority charge carriers are e⊖s & minority charge carriers are holes.
→ For n-type semiconductor, $\boxed{n_e >>> n_h}$

v.v.imp
1. n-type semiconductor from energy band diagram :→

→ In n-type semiconductor, the 5th e⊖ is weakly attracted by the donor impurity atom.
→ A very small energy (0.05eV) for Si is required to free this e⊖.
→ The energies of these e⊖s are slightly less than the energies of free e⊖s in lowest energy level of C.B.
→ Due to this, these e⊖s occupy discrete energy levels just below the C.B. called donor energy levels.
→ At room temperature, this small energy gap is easily filled & hence C.B. has more no. of e⊖s than holes in V.B.



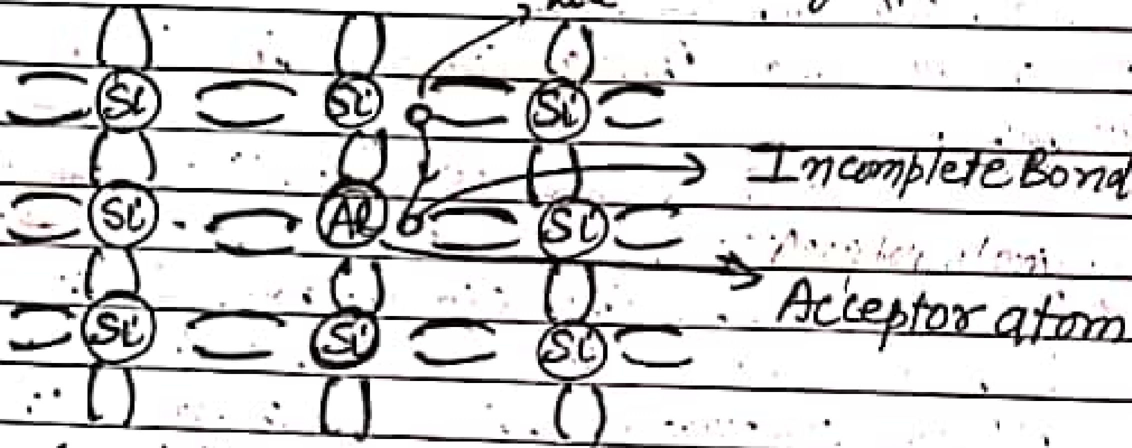
2. p-type semiconductor

→ When a pure semiconductor is doped with trivalent impurity atom (Al, Ga, B, In), the resulting semi-conductor is p-type.
→ The impurity atom uses its third valence e⊖s to form covalent bonds with neighbouring Si atoms, with one bond left incomplete, due to deficiency of e⊖
→ This deficiency is completed by an e⊖ from the neighbouring Si — Si bond creating a vacancy (hole) there.

→ Now, this hole is available for the conduction.

→ As each trivalent impurity atom accepts one $e^{\ominus}$, hence is called acceptor atom.

→ With ↑ in temperature, equal no. of holes & $e^{\ominus}$s are created due to breakage of bond. But the overall concentration of holes is more i.e. $n_h >> n_e$, hence is called p-type semiconductor as majority carriers are holes.



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p-type semiconductor from energy band diagram

→ In a p-type semiconductor, each acceptor impurity atom

→ Each acceptor atom creates a hole which can be easily filled by $e^{\ominus}$s from neighbouring Si – Si bond.

→ i.e. very small energy (0.040-0.05 eV) is required by an $e^{\ominus}$ from V.B. to move into this hole.

→ Hence, these impurity atoms form an energy level just above the V.B called acceptor energy level.

→ At room temperature, large no. of $e^{\ominus}$s get excited to these acceptor levels creating large no. of holes in V.B.

→ These holes conduct electricity when an electric field is applied.

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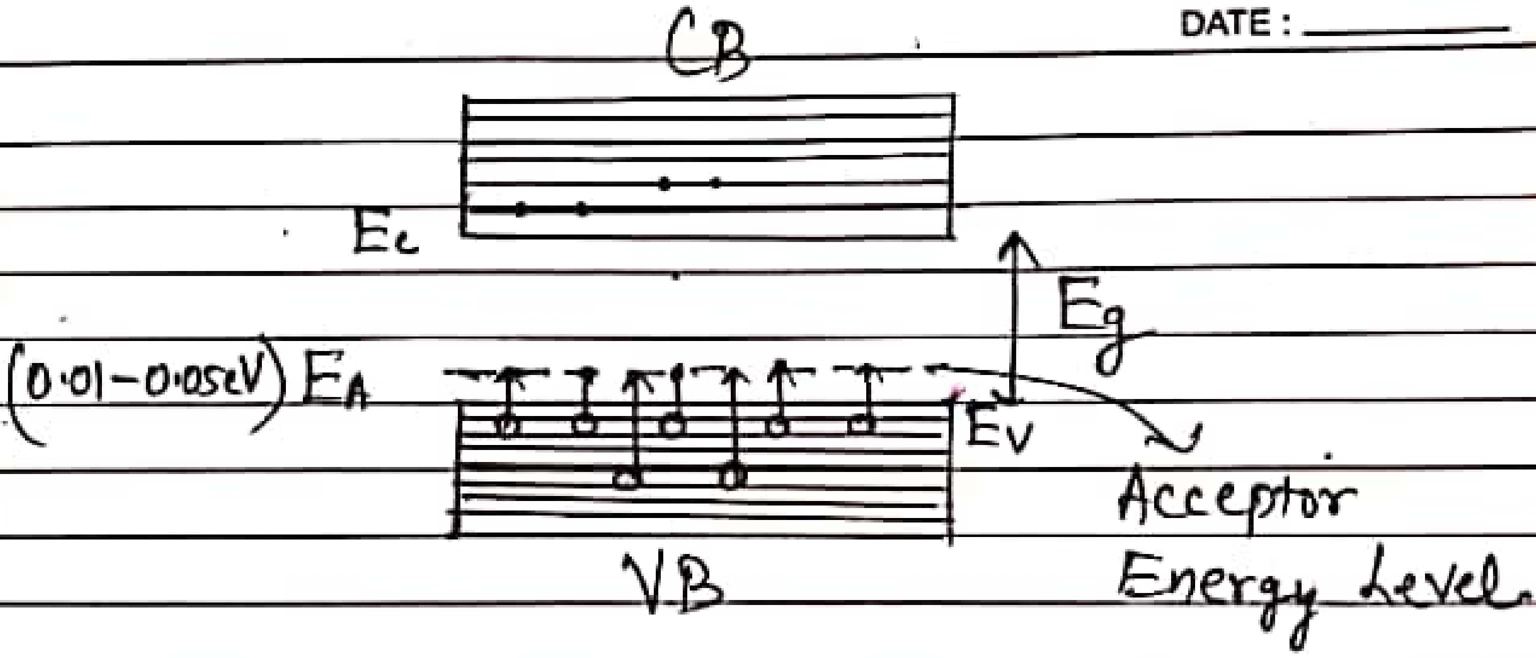

* In an intrinsic semiconductor, $\boxed{n_e = n_h = n_i}$

* In an extrinsic semiconductor, $\boxed{n_e n_h = n_i^2}$
This is also called Mass Action Law

* In n-type semiconductor,
$\boxed{N_D \simeq n_e >>> n_h}$ {N_D = no. density of donor atom

* In p-type semiconductor
$\boxed{N_A \simeq n_h >>> n_e}$ {N_A = no. density of acceptor atom

Q→ Suppose a pure Si crystal has 5×10^{28} atoms per m^3. It is dopped by 1ppm concentration of As. Calculate the no. of e^-s & holes ($n_i = 1.5\times10^{16}/m^3$)

As the impurity is pentavalent, the semiconductor is n-type.

no. of dopants $/m^3$ = $\frac{5\times10^{28}}{10^6} = 5\times10^{22}/m^3$

$N_D \simeq n_e$

$n_e = 5\times10^{22}$ &

$n_e n_h = n_i^2$

$n_h = \frac{n_i^2}{n_e} = \frac{(1.5\times10^{16})^2}{5\times10^{22}}$

$n_h = 4.5\times10^{9}$ holes$/m^3$

Difference b/w Intrinsic & Extrinsic semi-conductors

Intrinsic semiconductors	Extrinsic semiconductors
1. They are pure semi-conducting tetravalent crystals.	1. They are semi-conducting crystals doped with group 13th or 15th elements
2. Their electrical conductivity is low.	2. Their conductivity is high.
3. There is no permitted energy state b/w V.B. & C.B.	3. There is permitted energy state of impurity atom b/w V.B. & C.B.
4. Their electrical conductivity depends on temperature.	4. Their electrical conductivity depends upon temperature as well as on dopant concentration.

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Difference b/w n & p-type semi-conductors

n-type semiconductor	p-type semiconductor
1) These are extrinsic semiconductors obtained by doping with Gp 15 atom.	1) These are extrinsic semiconductors obtained by doping with Gp 13
2) The impurity atoms provide free e^-s & are called donors.	2) The impurity atoms added create vacancies of e^-s called acceptor atom
3) The donor impurity energy level lies just below the C.B.	3) The acceptor impurity band/level lies just above the V.B.
4) e^-s are majority charge carriers while holes are minority charge carriers.	4) The holes are majority charge carriers while e^-s are minority charge carriers.

Effect of Temperature on conductivity of semi-conductors

With ↑ in temperature, the mobility of e^-s & holes (μ_e & μ_h) ↓es due to ↑ in collision frequency.

But due to small energy gap of semi-conductors, more & more e^-s from V.B. reach C.B. The ↑ in charge carrier concentration (n_e, n_h) is so large that ↓ in μ_e & μ_h has no effect.

→ Hence, the conductivity of a semi-conductor ↑es with ↑ in temperature.

* Mobility of charge carrier: $\mu = \frac{v_d}{E}$

We know $\mu_e = \frac{v_e}{E}$ & $\mu_h = \frac{v_h}{E}$ $\quad$ $\left\{ v_d = \frac{eE\tau}{m} \right.$

→ Mobility of an e^- in C.B. is greater than mobility of a hole in V.B.

Reason: The e^-s in C.B. are almost free. Hence, they get easily accelerated by E.F. but e^-s in V.B. are bounded.

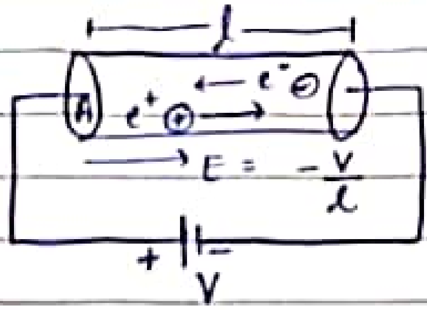
* As the motion of e^- in V.B. is equivalent to motion of hole in V.B. but in opposite direction. Hence, mobility of hole is small

Effect of Temperature on Resistivity and conductivity of Semiconductor:-
For a conductor of length (l) and area (A) the current flowing is given by:-

$$I = I_e + I_h$$

$$\frac{V}{R} = n_e e A v_e + n_h e A v_h$$

$$\frac{V}{\frac{\rho l}{A}} = eA(n_e v_e + n_h v_h)$$



$$\frac{1}{\rho}\left(\frac{V}{l}\right) = e(n_e v_e + n_h v_h)$$

$$\frac{1}{\rho}(E) = e(n_e v_e + n_h v_h)$$

$$\therefore \quad \sigma = \frac{1}{\rho} = e\left(n_e \frac{v_e}{E} + n_h \frac{v_e}{E}\right)$$

$$\boxed{\sigma = \frac{1}{\rho} = e(n_e \mu_e + n_h \mu_h)}$$

With the increase in temperature, number density of electron and hole will increase whereas mobility decreases.
Decrease in mobility is negligible. Hence, with the increase in temperature, conductivity increase and resistivity decreases.

Q.→ What is the charge on n-type semiconductor?
Ans:→ There will be no charge as atom(Si) is replaced by impurity-atom which are electrically neutral.

p-n junction :→

It is a single crystal of Ge or Si doped in such a way that half portion of it act as a p-type & half as n-type semiconductor.
→ A p-n junction cannot be formed by just placing a p-type si close contact with n-type semiconductor ∵ we cannot have a continuous contact b/w the two semiconductors at atomic level.
→ A p-type p-n junction is obtained by growing both acceptor and donor impurities in a single crystal of Si or Ge.

Unbiased p-n junction (without ext. Potential difference)
Or
Formation of Depletion region and potential difference

Two important processes involved in the formation of p-n junction are:
1) Diffusion
2) Drift

* When a p-n junction is formed, the two sides have charge carrier gradient i.e. p-side has higher concentration of holes & n-side has higher concentration of e⁻s.
* Due to the difference in concentration, the holes begin to diffuse p → n & e⁻s begin to diffuse n → p.

Depletion Layer : A layer across the junction which contains immobile ions.

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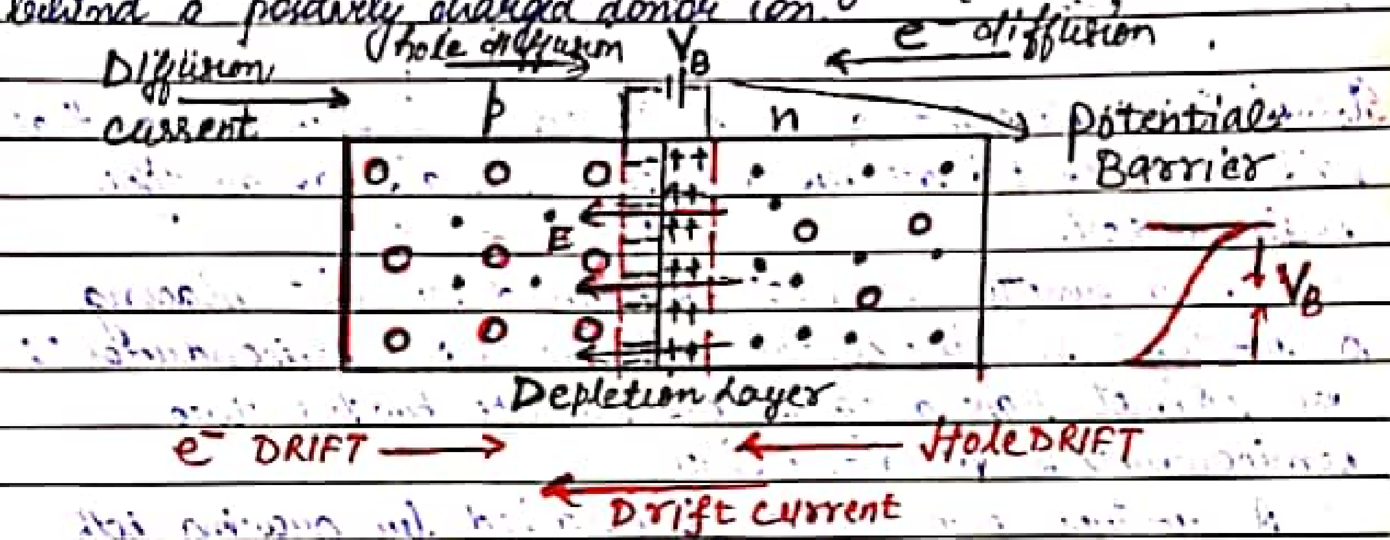
* This sets up a diffusion current across the p-n junction.

→ As a hole diffuses from p → n, it leaves behind negatively charged acceptor ion and the diffusion of e⁻ from n → p leaves behind a positively charged donor ion.



→ This forms a layer of +ve & -ve charged ions across the junction.

→ This small spaced charge region across the junction which is free from free charge carriers is called depletion region or depletion layer.

→ The accumulation of these charged ions across the junction sets up a potential barrier & hence E.F. from n → p.

→ This E.F. oppose the further diffusion of majority carriers across the junction.

→ This E.F. across the junction supports the motion of minority carriers.

→ Due to this E.F., e⁻s drift from p → n & holes from n → p.

→ This sets up a drift current across the junction from n → p.

→ In eqlbᵐ, both diffusion & drift currents become equal i.e. there is no net flow of charge across the junction. Hence, the p-n junction is formed.

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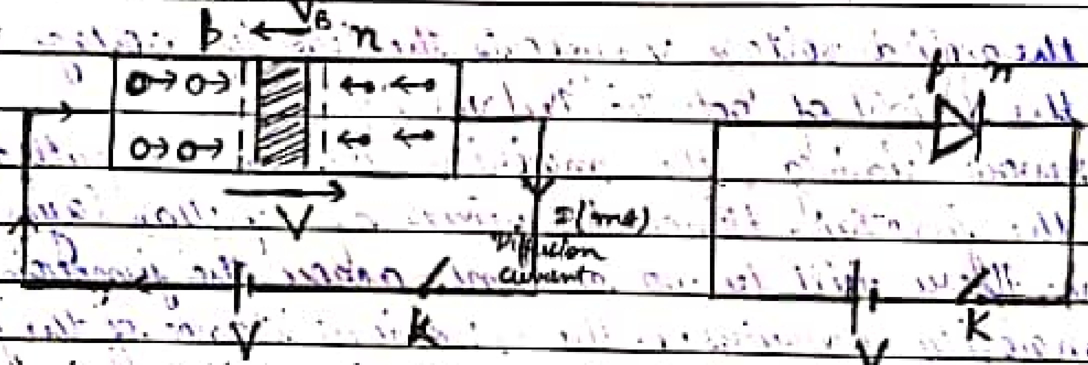
Symbolical Representation of p-n junction

p-n junction diode.

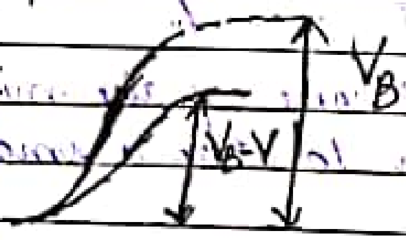
Biasing of a p-n junction :→

(1) **Forward biasing :**

If the +ve terminal of external battery is connected to p-side & -ve to the n-side, the junction is said to be forward biased.



As shown the applied voltage V oppose the barrier voltage V_B. Hence the height of potential barrier ↓es $(V_B - V)$



→ The majority carriers, holes in p-side & e⁻s in n-side are pushed towards the junction by the external battery.

→ Hence, in forward biasing, the width of depletion layer ↓es and hence, the effective resistance across the junction ↓es.

→ When V exceeds V_B, there will be free flow of majority charge carriers across the junction, setting up a forward current (mA). [which ↑es with ↑ in applied voltage].

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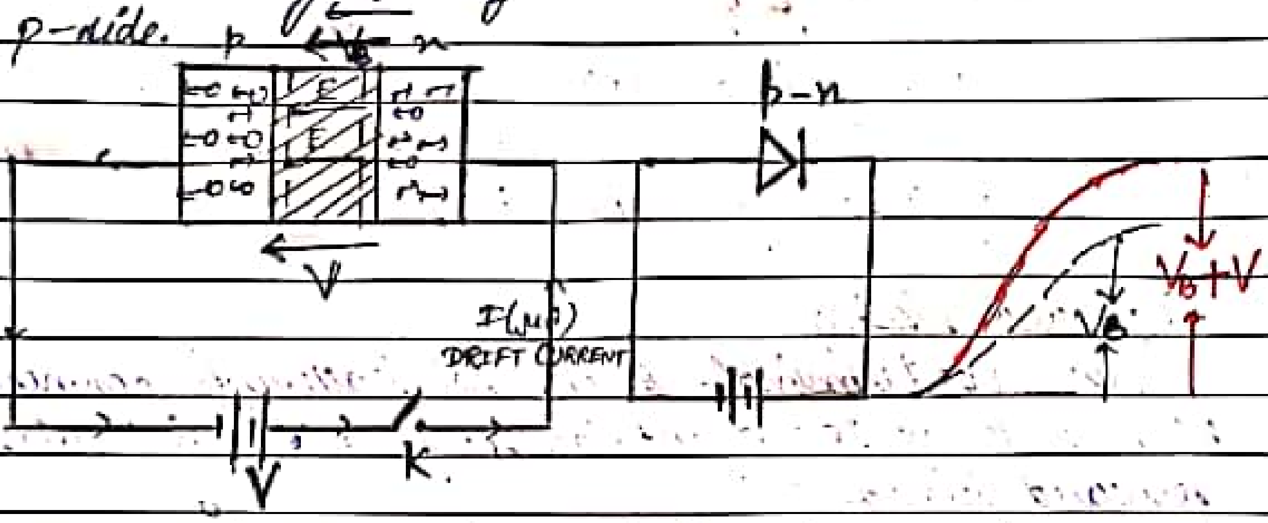
2. Reverse biasing

A p-n junction said to be reverse biased if +ve terminal of external battery is connected to n-side & -ve to the p-side.



→ Here, the applied voltage V supports the barrier voltage V_B. Hence, the height of potential ↑es (V_B+V)

→ In reverse biasing, the majority carriers are pulled away from the junction. Hence, the width of depletion layer ↑es.

→ Hence, there will be no current across the junction due to majority carriers i.e. the effective resistance of the junction in reverse biasing is very high.

→ As the width of depletion layer ↑es, the strength of E.F. also ↑es.

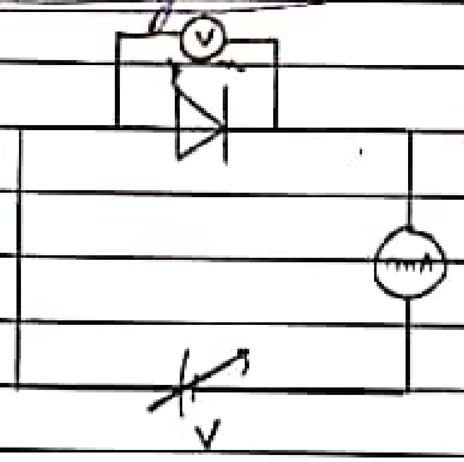
→ This E.F. may pull some of the minority carriers across the junction to set up a small reverse current (μA)

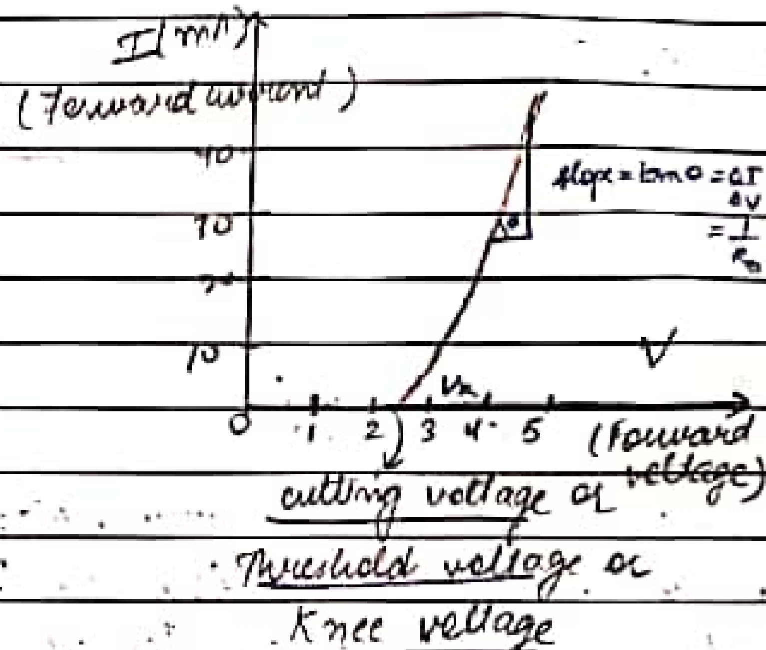
→ The small value of reverse current is due to the small no. of minority carriers.

V-I characteristics of a p-n junction diode

A graph showing the variation of current (forward current or reverse current) with voltage (forward voltage or reverse voltage).

1) Forward characteristics.
Circuit Diagram





* I – V curve is not a straight line i.e. p-n junction diode does not follow ohm's Law.
* Initially, the current is negligible till an applied voltage reaches a value called Knee Voltage above which current varies linearly.
* Before V_k, potential barrier voltage is more or depletion layer dominates.
* As V ↑es, the width of depletion layer ↓es & at $V = V_k$, the depletion layer disappears i.e. there is free movement of charge carriers across the junction.
* Hence, in forward biasing, the resistance offered by the diode is negligible.

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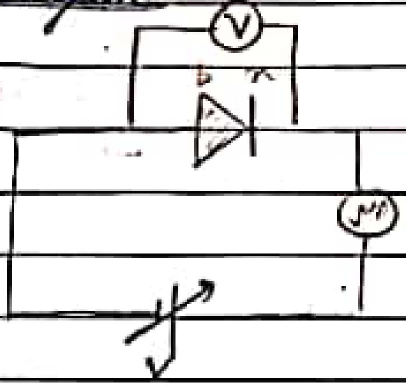
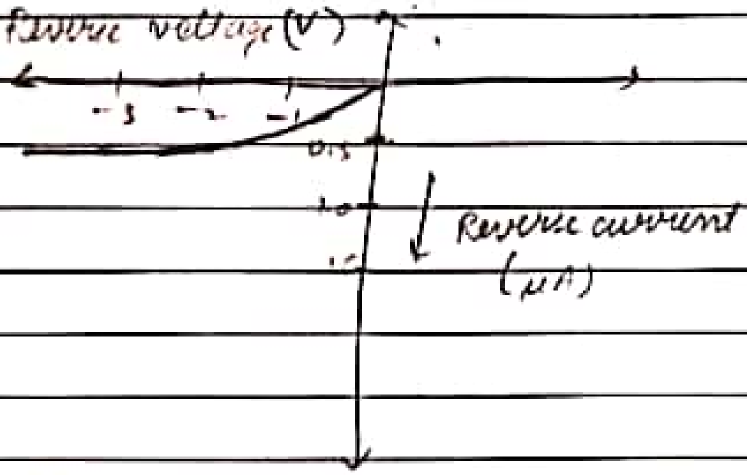
* for Si , $V_k = 0.7V$
for Ge , $V_k = 0.2V$

Reverse Characteristics

Circuit Diagram





* With increase in reverse voltage, the reverse current ↑es
* as minority carriers are pushed towards the junction.

→ As reverse voltage ↑es, the current becomes constant called reverse saturation current.

* Reason for constant reverse current

The reverse current is due to the motion of minority charge carriers across the junction, which are very less in number. As the concentration of minority carriers remain constant for a particular temperature & diode, hence, the magnitude of reverse current remains constant & is independent of the applied voltage.

* As there is very small increase in current with reverse voltage, hence, the resistance offered by the diode is very large.

Dynamic Resistance :→

As I-V curve for a p-n junction diode is not a straight line i.e it doesnot follow Ohm's law.
The resistance of the diode varies with the applied voltage.
Hence, we define a quantity called dynamic resistance

$$\boxed{R_d = \frac{\Delta V}{\Delta I}}$$

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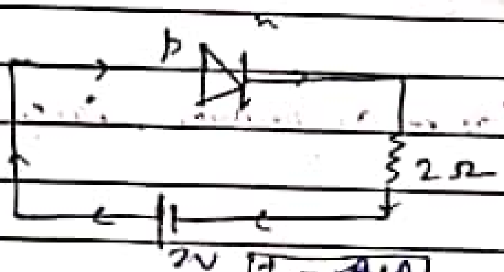
i.e. it is the ratio of small change in applied voltage (ΔV) to the corresponding change in current (ΔI).

* Above knee voltage, R_D is almost independent of V.

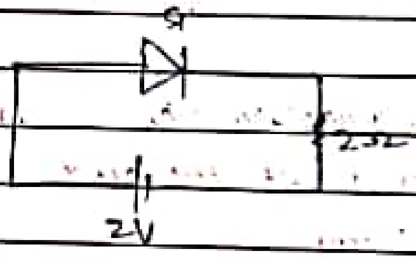
For an Ideal diode, the resistance offered in forward biasing is 0 and in reverse biasing is infinity.
i.e. in forward biasing, the diode fully conducts but in reverse biasing, it doesn't conduct.

* But if the diode is of Si or Ge, then, there will be a potential drop across the diode.

* In case of Si $\boxed{V = 0.7V}$ & in Ge $\boxed{V = 0.2V}$

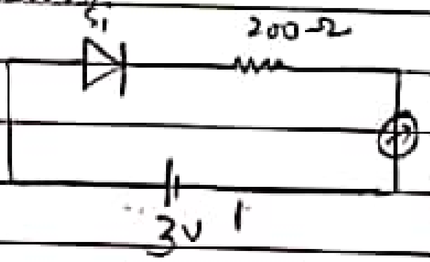


$\boxed{I = 1A}$



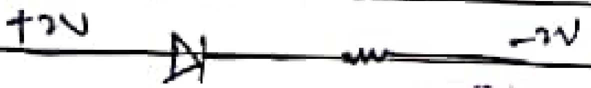
$I = \frac{1.3}{2} = 0.65A$

Q:→1) Find the reading of Ammeter for the Si diode in the circuit shown.



$I = \frac{2.3}{200}$

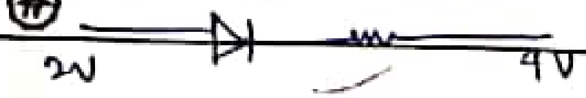
Q:2) Identify the diodes which are connected in forward bias & reverse bias mode.

a) 

Forward

b) 

Reverse

c) 

Reverse

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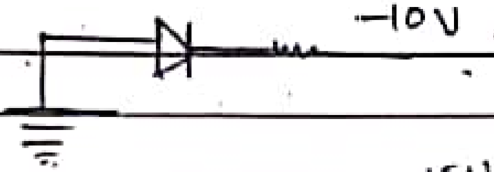
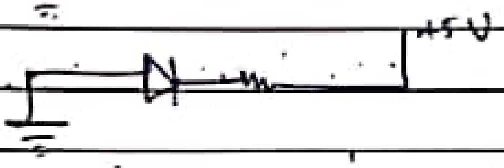
d) 

Forward

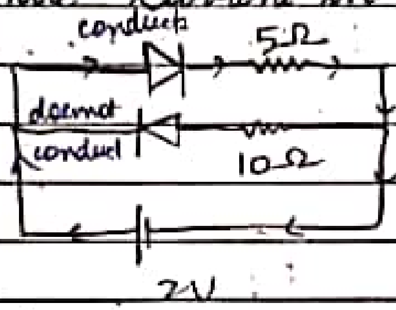
e) 

Reverse

f) 

Forward

Q1.3) Find the current in the circuit.



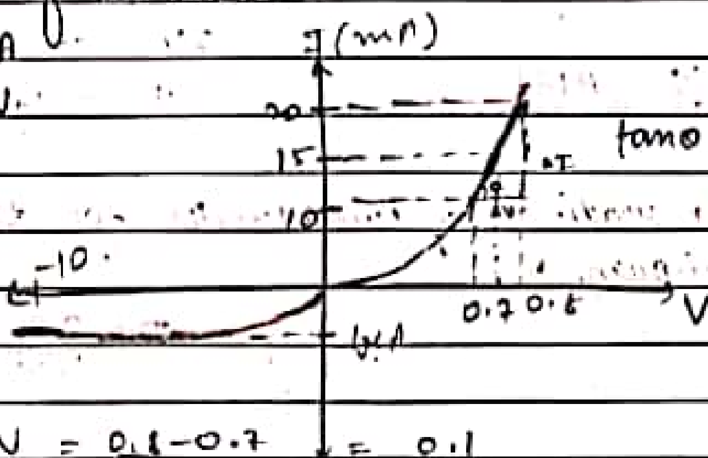
~~$I = \frac{5\Omega}{2V}$~~ $I = \frac{2}{5} = 0.4A$

~~$I = 2\times5$~~

Q1.4) I-V characteristics of a Si diode is as shown. Calculate the resistance of the diode at

(i) $I = 15mA$

(ii) $V = -10V$.



$\tan\theta = \frac{\Delta I}{\Delta V}$

(i) $R_D = \frac{\Delta V}{\Delta I} = \frac{0.8-0.7}{20-10} = \frac{0.1}{10\times10^{-3}}$

$R_D = \frac{10^3}{10^2} = 10\ \Omega$

(ii) at $V = -10V$

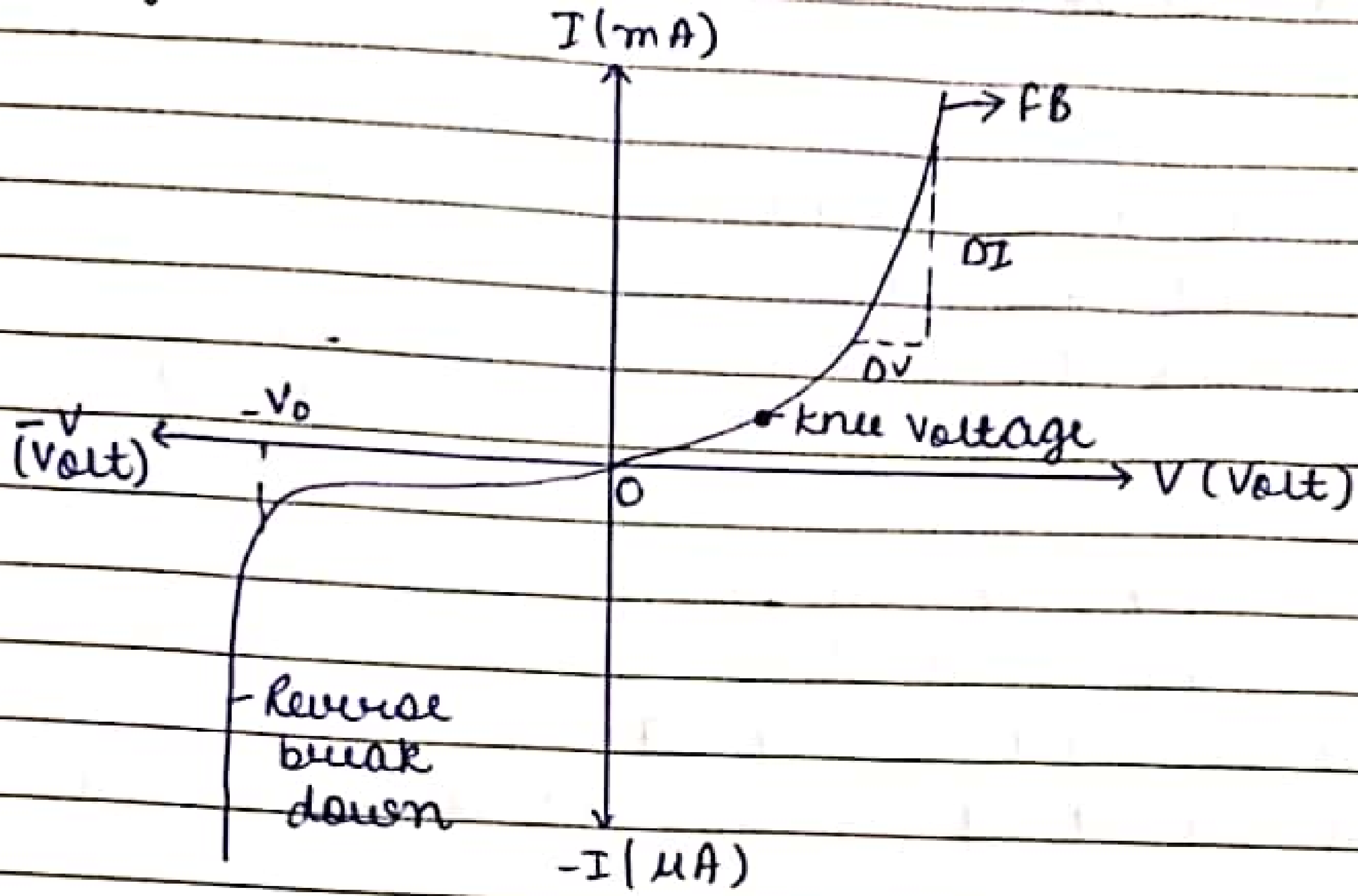
$R_D = \frac{10}{1\times10^{-6}} = 10^7\ \Omega$

(H)

* Reverse breakdown:- If the reverse voltage is increased beyond a certain value ($-V_0$), called reverse break down voltage, then the current suddenly increase to very large value.
This sudden increase in current is due to breakdown of large no. of covalent bond which release large no. of free electrons and the current become very large.

Note:- Due to heating, the diode may burn out.

(I–V) graph:-



I (mA)
FB
ΔI
ΔV
knee voltage
$-V_0$
$-V$ (Volt)
O
V (Volt)
Reverse break down
$-I$ (μA)

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V.V.Imp

* An ideal p-n junction offers negligible resistance when forward biased and very high resistance when reverse biased.

* i.e. a diode can conduct current well only in one direction.

→ This property of p-n junction is used for rectification i.e. to convert AC into DC.

Rectifier :→

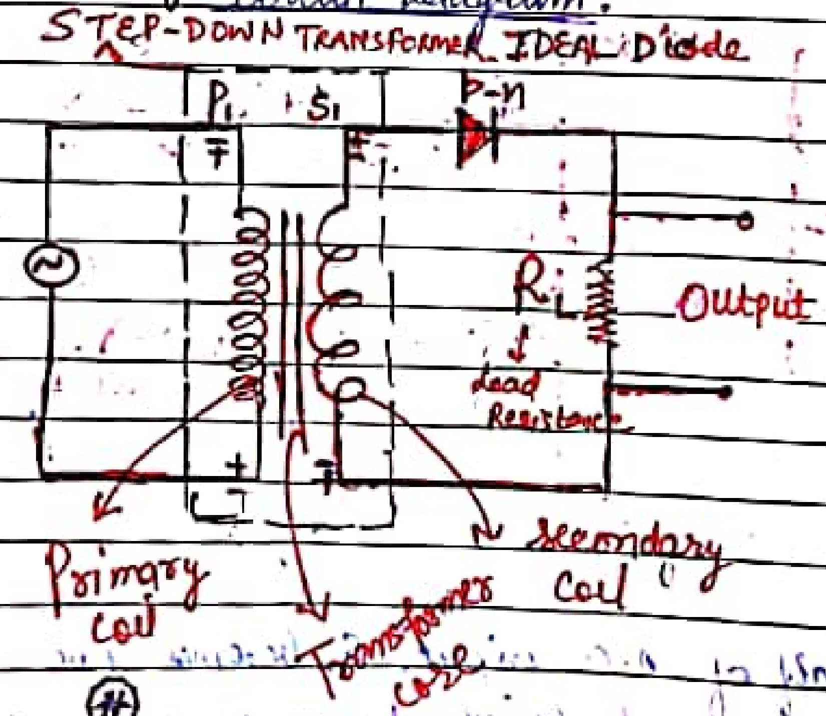
A device which converts A.C. into D.C.

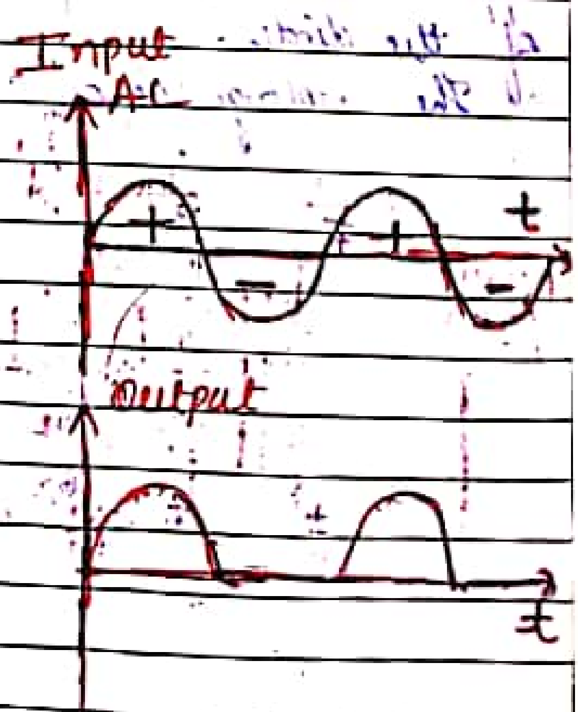
Principle →

Its working is based on the fact that when a p-n junction diode is forward biased, its resistance becomes low & hence conducts and when reverse biased, its resistance becomes high & hence it does not conduct.

1. Half-wave Rectifier

Circuit Diagram:





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Working:→

Let during the first +ve half of AC input, S_1 becomes +ve & S_2 becomes -ve. Hence, the diode gets forward biased & ~~we get~~ conducts ∴ We get output across R_L.

→ During the next negative half of AC input, S_1 becomes -ve & S_2 gets +ve. Now, the diode becomes reverse biased & we donot get any output across R_L.

From the above, it is clear that half-wave rectifier rectifies only half of the A.C. input.

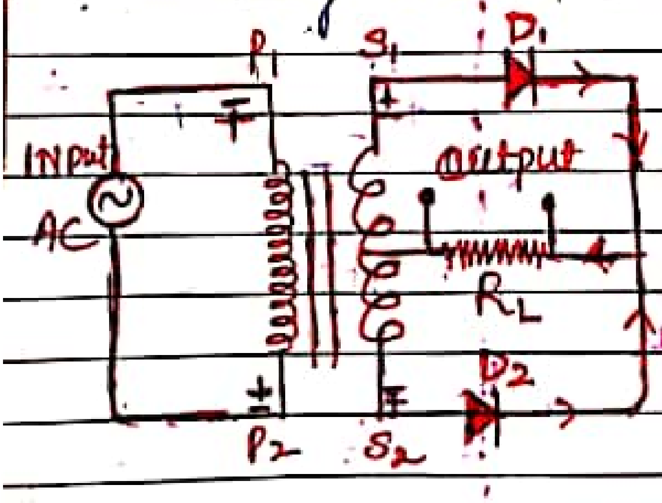
②

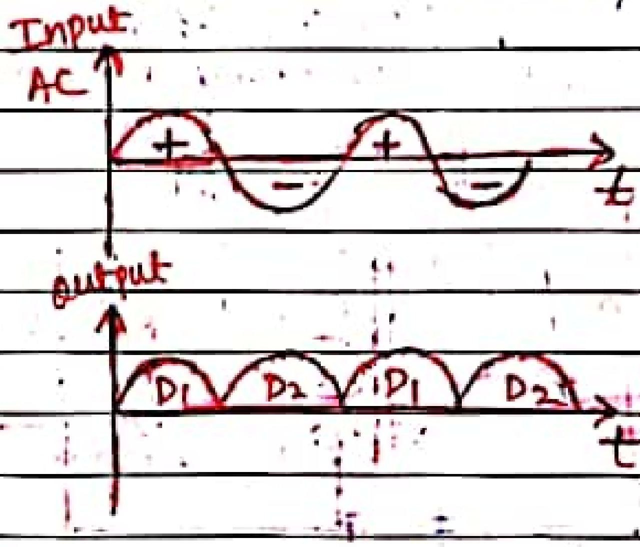
Full Wave Rectifier

Circuit Diagram

→ Here, we use centre-tap transformer i.e. the secondary is tapped at its centre point which is connected to n-side of the diodes.

→ The voltage across S_1 & S_2 is measured w.r.t. centre tap.





Working:→

→ Let during the +ve half of A.C. input, S_1 becomes +ve & S_2 -ve. Diode D_1 is forward biased, hence conducts but

DATE :

diode D_2 is reverse biased & hence does not conduct.
Hence output across R_L will be due to D_1

→ During the next negative half of A.C. input, S_1 will be -ve & S_2 will be +ve. Hence, D_1 gets reverse biased & D_2 get forward biased. Hence, output across R_L will be due to D_2.

* Hence, in full wave rectifier, the output across R_L is taken/obtained for both cycles.

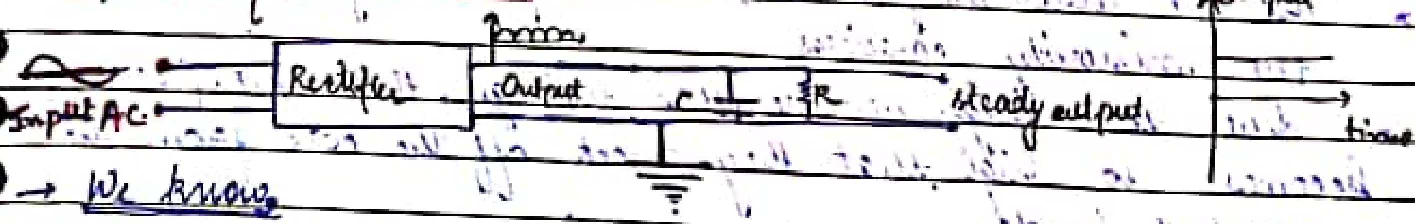
vvImp

* In a half-wave rectifier, the frequency of input A.C. & the output is same but in full wave rectifier, the frequency of output is twice the frequency of input A.C.
for e.g. if 50 Hz input A.C. is applied
$\nu_{input} = 50\ Hz$; $\nu_{output} = 100\ Hz$

* The output obtained from the rectifier is not unidirectional but is also pulsating i.e. contains ripple contents.
b/c the output signal contains both A.C. as well as D.C. components.

* To get steady D.C., we use filter circuits.

Capacitor filter circuit



→ We know

$X_C = \frac{1}{\omega C} = \frac{1}{2\pi\nu C}$

for A.C. X_C less (very low)
for D.C. $\boxed{\nu_{dc} = 0}$ $\boxed{X_C = \infty}$

3/4

i.e capacitor offers low resistance to high frequency DATE : ________

A.C. component & hence bypass it but it offers high resistance to D.C. component, hence blocks it which appears across R

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Imp

DATE :

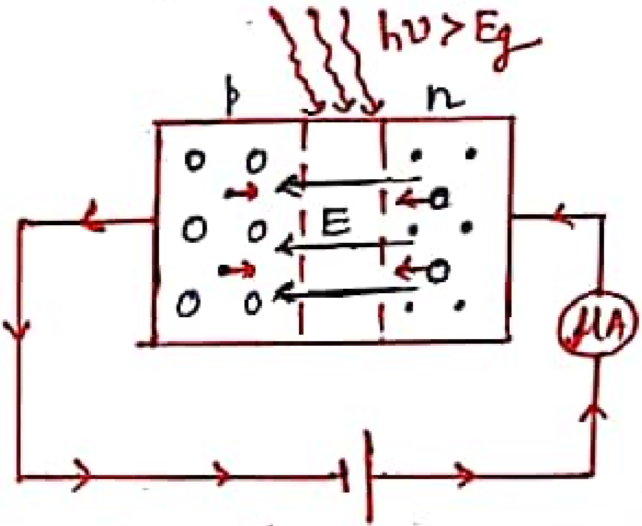
* Photodiode

A photodiode is a p-n junction fabricated from a photosensitive semi-conductor and provided with a transparent window to allow the light to fall on its junction.

→ A photodiode is a device which detects optical signal by converting light energy into electrical energy.

$h\nu > E_g$

OR $\frac{hc}{\lambda} > E_g$



WORKING →

→ A photodiode is always operated in reverse biased mode.

→ When no light is incident on the junction, there will be a small reverse saturation current called dark current.

→ When light photons of energy $(h\nu > E_g)$ is incident on the junction, additional e⁻-hole pairs are generated near the junction due to the breakage of covalent bonds.

→ Due to the junction field, the e⁻s get collected on n-side and holes on p-side.

→ This motion of charges set up an additional current shown by the Ammeter.

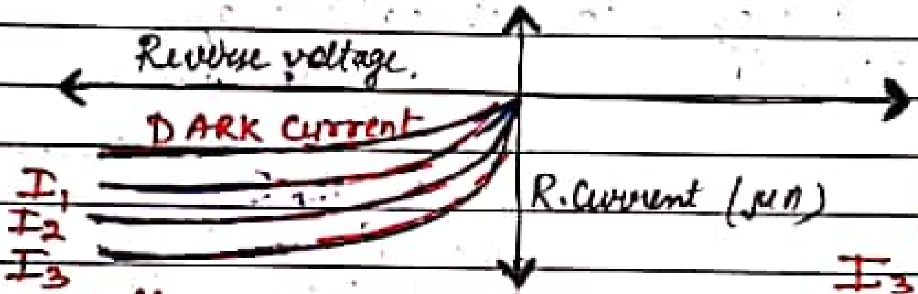
* Why Photodiode is connected in reverse bias mode: →

In reverse bias, the fractional change in minority carriers due to the incident light is much large than

in forward biasing (fractional change in majority carriers).
Hence, we can easily observe the change in photocurrent with the change in intensity of incident light.

→ Hence, the photodiode is used to detect optical signals.

I–V characteristics :→



INTENSTY

$I_3 > I_2 > I_1$

* Photocurrent is proportional to intensity of incident light.

Uses :→

1) In detection of
   (i) optical signals
   (ii) in switching light on/off.
   (iii) in demodulation of optical signals.

Q: A p–n junction photodiode is fabricated with a band gap of 2.8 eV. Can it detect a light of $\lambda = 6000$ Å

$$E = \frac{hc}{\lambda} = \frac{1240\cancel{0}}{600\cancel{0}} = \frac{62}{30} = 2.066\,eV$$

$$\boxed{E = 2.066\,eV}$$

⇒ $E < E_g$ hence can't be detected.

L.E.D :→ (Light emitting diode)

L.E.D. is fabricated by :

(i) heavy doping both p & n side.

(ii) providing transparent cover so that light can come out.

(iii) L.E.D. operates under forward bias.

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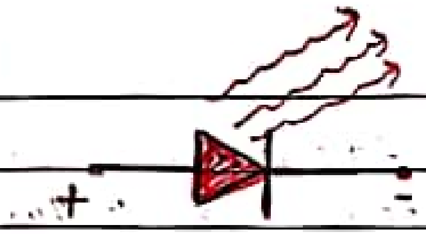
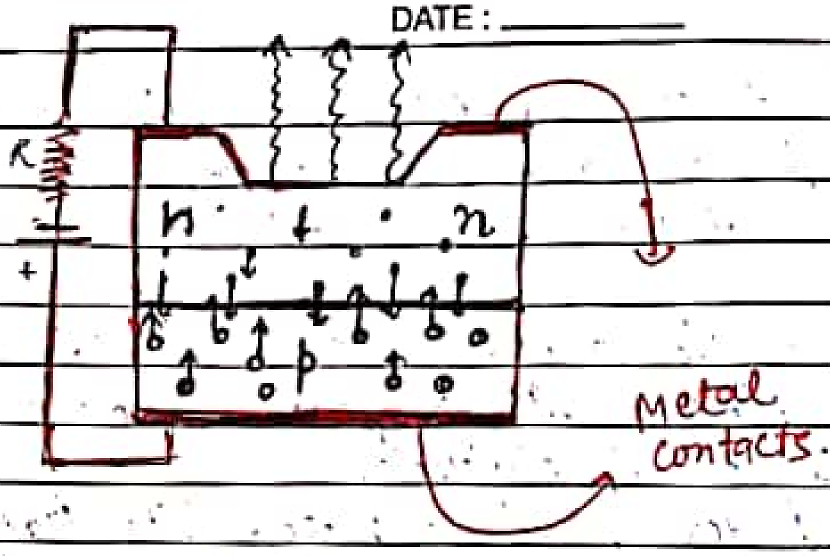




Working :⟶

* When p-n junction is forward biased, the e⁻s are sent from n ⟶ p (where they are minority) & holes are sent from p to n where they are minority.
* Near the junction, the concentration of minority carriers ↑es.
* Then excess of minority carriers combine with the majority carriers.
* On recombination, the energy is released in the form of photons.
* If λ = wavelength of photons emitted
  E_g = band gap energy

$$E_g = \frac{hc}{\lambda}$$

$$\boxed{\lambda_{photon} = \frac{hc}{E_g}}$$

⟶ The wavelength of visible light ranges from 400nm to 700nm.

for $\lambda = 400$ nm

$$E = \frac{hc}{\lambda}$$

$$E = \frac{1240}{400} = 3.1$$

$$\boxed{E \simeq 3.0 eV}$$

$\lambda = 700$ nm

$$E = \frac{hc}{\lambda}$$

$$= \frac{1240}{700}$$

$$\boxed{E = 1.8 eV}$$

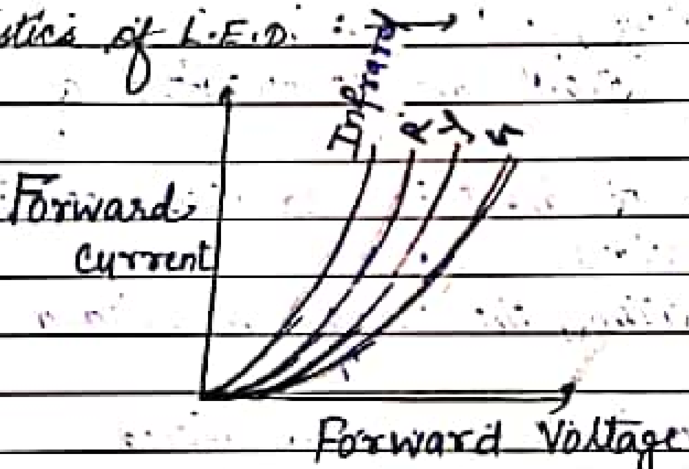
(*)

DATE :

→ Hence, the choice of semi-conductor in fabrication of L.E.D is such that the band gap of semi-conductor should lie b/w 1.8eV – 3eV.

* For a p-n junction of Si & Ge, the larger % of energy released is transferred into thermal energy. Hence, no light is emitted.
* For semi-conductor like GaAs, GaAsP, major part of energy released is in the form of visible light.

I-V Characteristics of L.E.D. :→

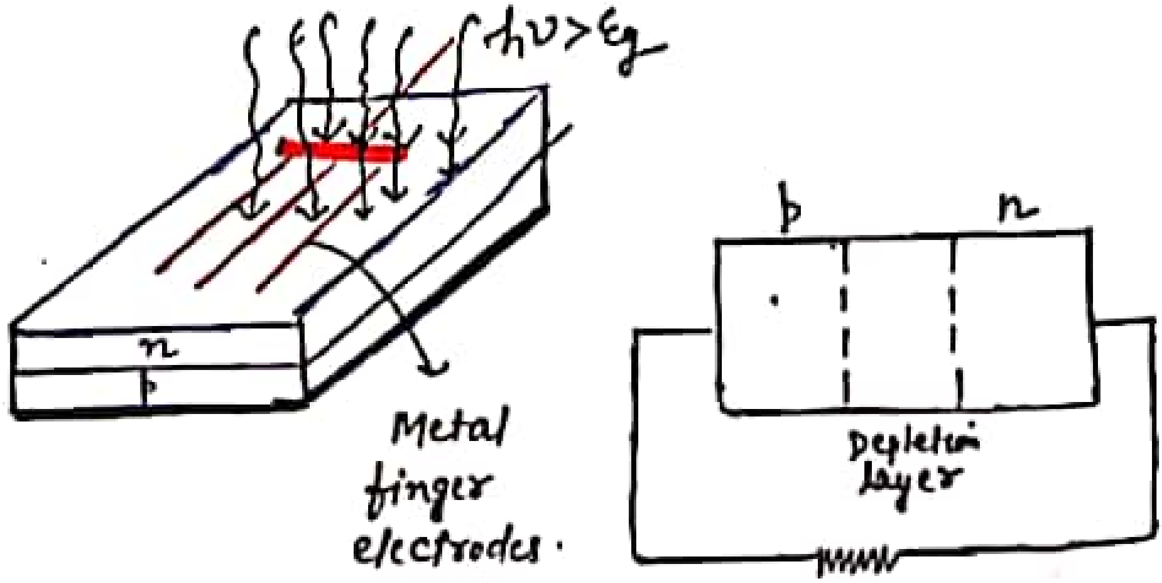


Uses of L.E.D. :⟶

1. In remote control
2. Headlights of car, in TV, mobiles etc.
3. In calculator, digital watches, traffic lights, in burglar alarm.

Advantages of L.E.D. over conventional lamps/ bulbs :⟶
1. Low operational voltage & less power consumption.
2. Fast action & no warm up is required.
3. Long life & ruggedness.
4. Cheap & easy to handle.

SOLAR CELL → A device which converts solar energy into electrical energy.



* On the top of n-side, metal finger electrodes is deposited which acts front contact. Metal electrodes occupies very small area (<15%) so that light can incident on the cell.

Imp

* In solar cell, no external biasing is required. and junction area is kept much larger for solar radiation to incident because more power is required.

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DATE : ________

Working :→

When a solar cell is illuminated with light $(h\nu > E_g)$, it generates E.F. due to three basic processes :→

(i) Generation : Generation of e^--hole pairs due to excitation of e^-s from V.B. to C.B. near the junction by the light of energy $(h\nu > E_g)$

(ii) Separation : e^-s - holes produced get separated due to junction field

(iii) Collection : The e^-s are swept to n-side & holes to p-side and get collected at the metal contacts.

→ Hence p side becomes +ve & n side becomes -ve & a p.d. is created / produced across p-n diode.

→ When a load is connected in external circuit, current (photo-current) flows.

I - V characteristics of solar cells :→

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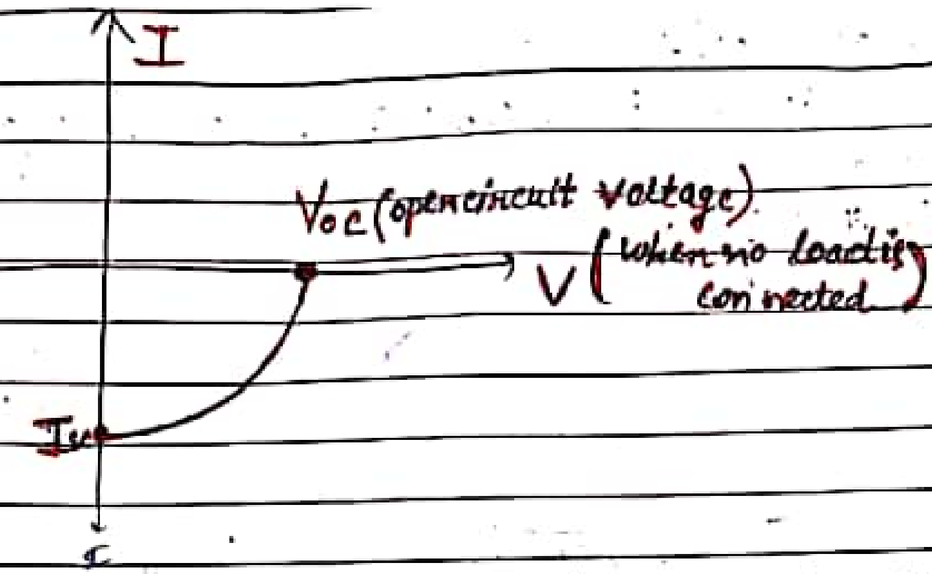

→ The curve is drawn in 4th quadrant because solar cell doesnot draw the current but supplies to the load.

Materials used for fabricating of solar cells :→

(i) The band gap should be from 1eV to 1.8eV

(ii) High optical absorption coefficients.

(iii) Availability of raw material.

(iv) Cost

Uses of solar cells :→

1. In calculators, wrist watches etc.
2. To power traffic signals.
3. Used to power electronic devices in satellites.
4. For generating electrical energy in cooking food & pumping water.

Advantages of solar cell :→

(i) Pollution free.

(ii) long-lasting.

(iii) maintenance free