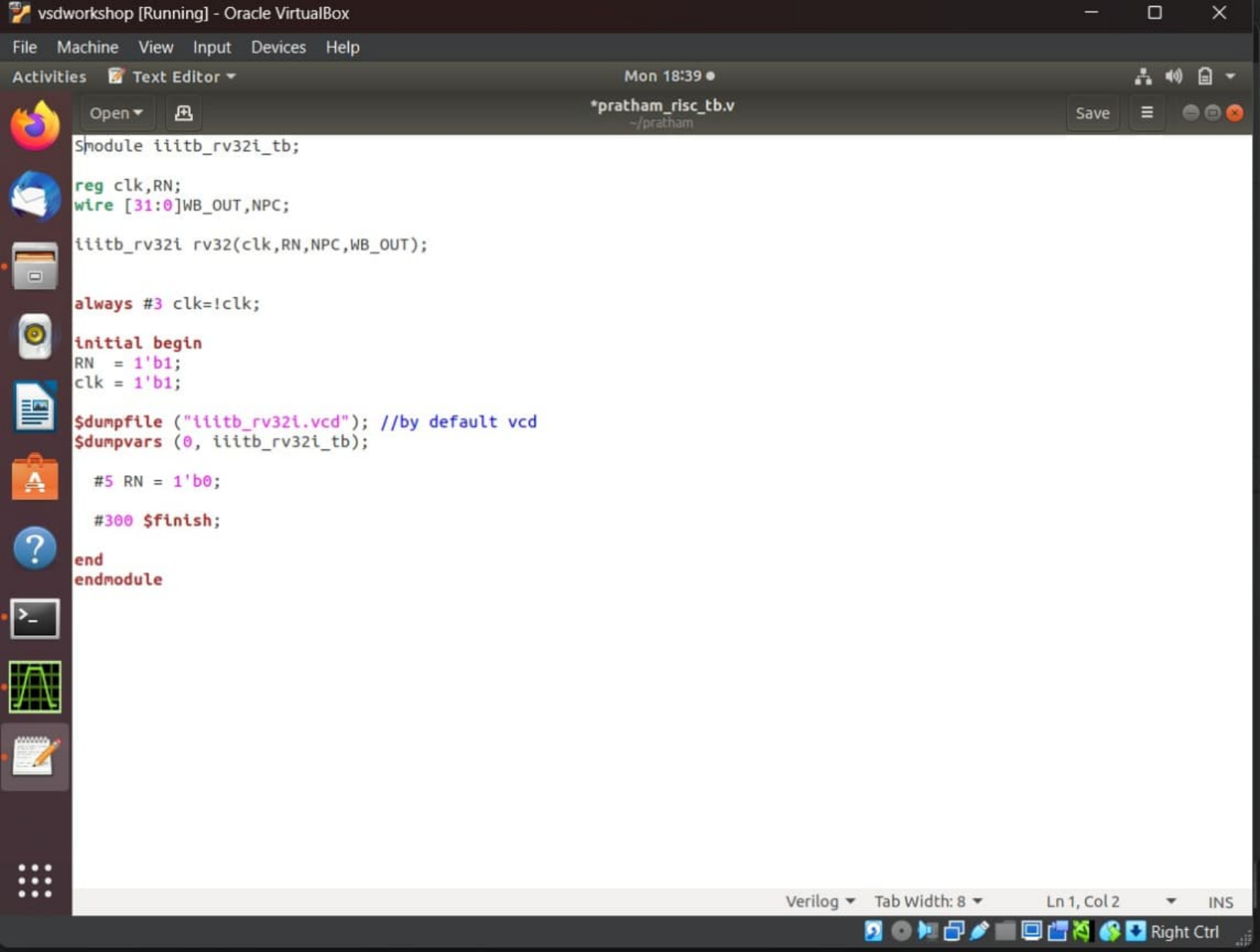
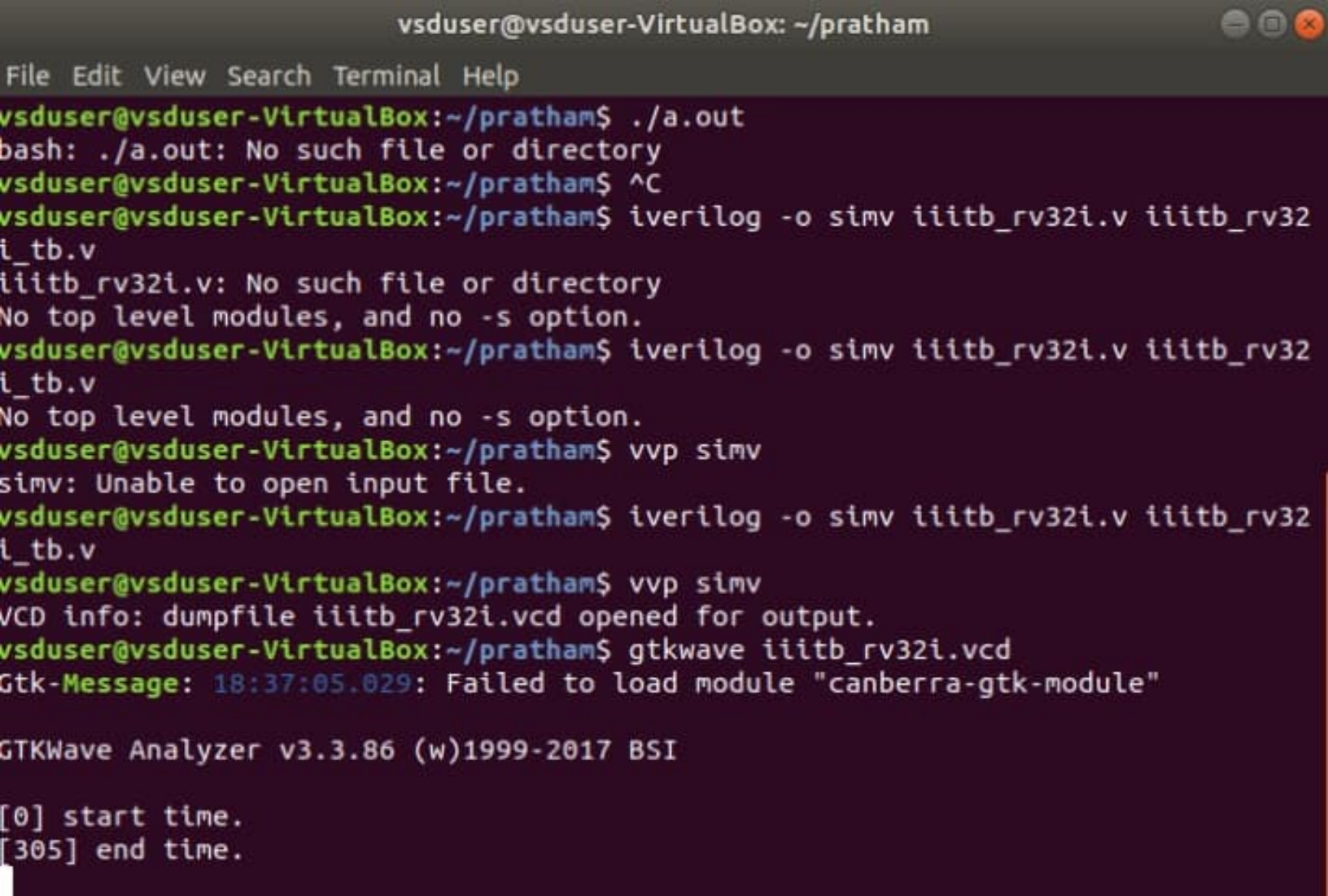
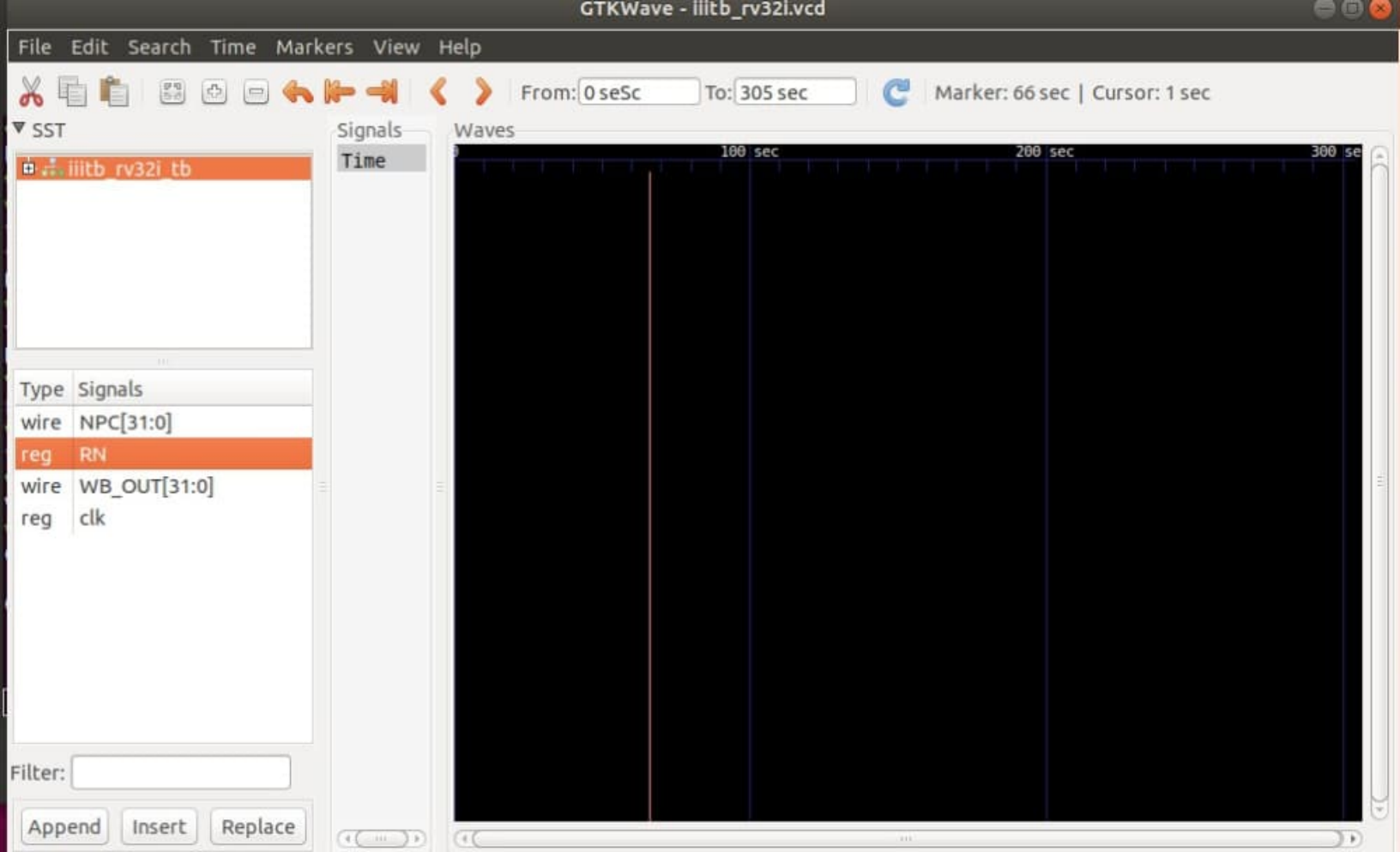
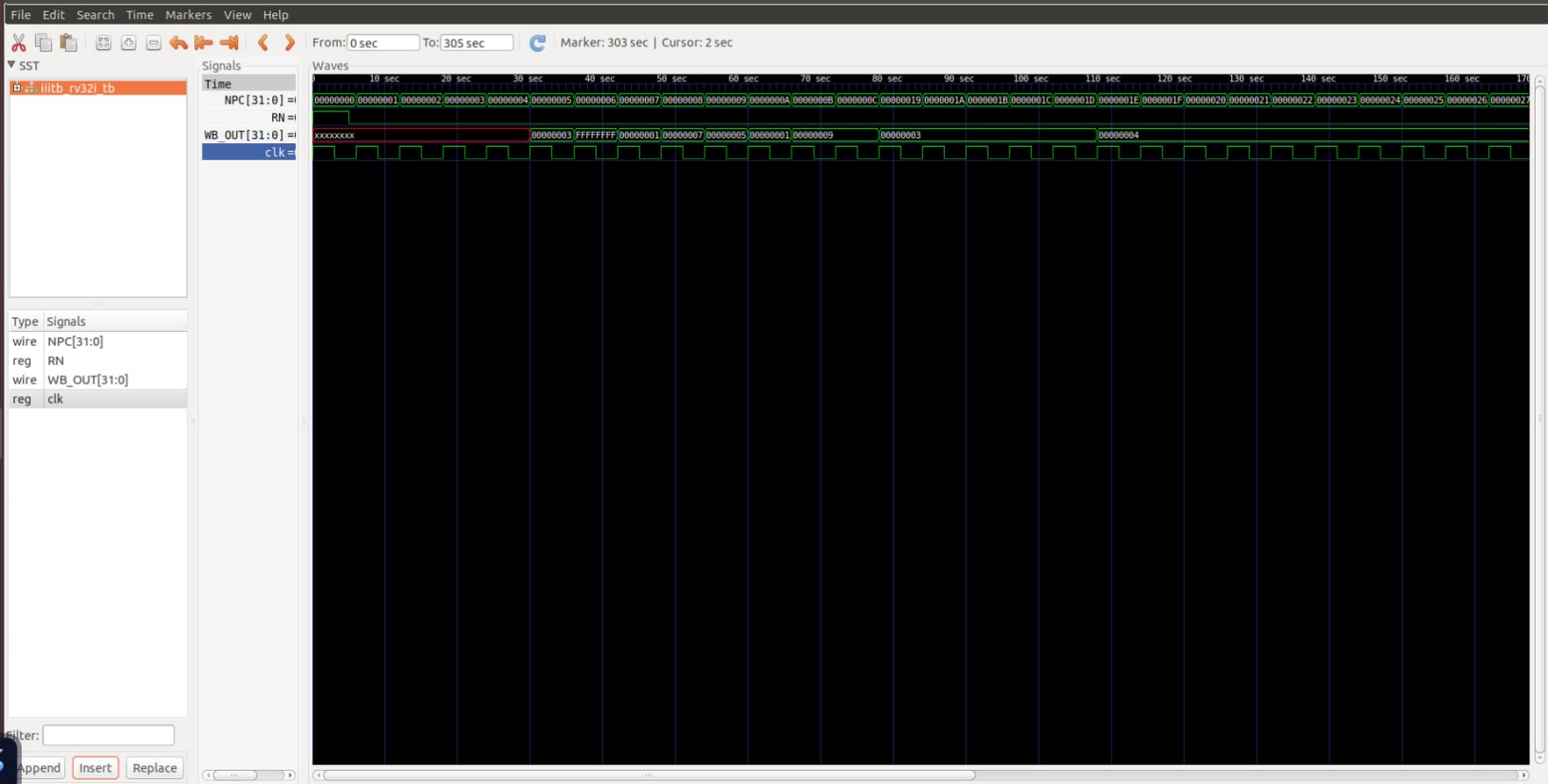
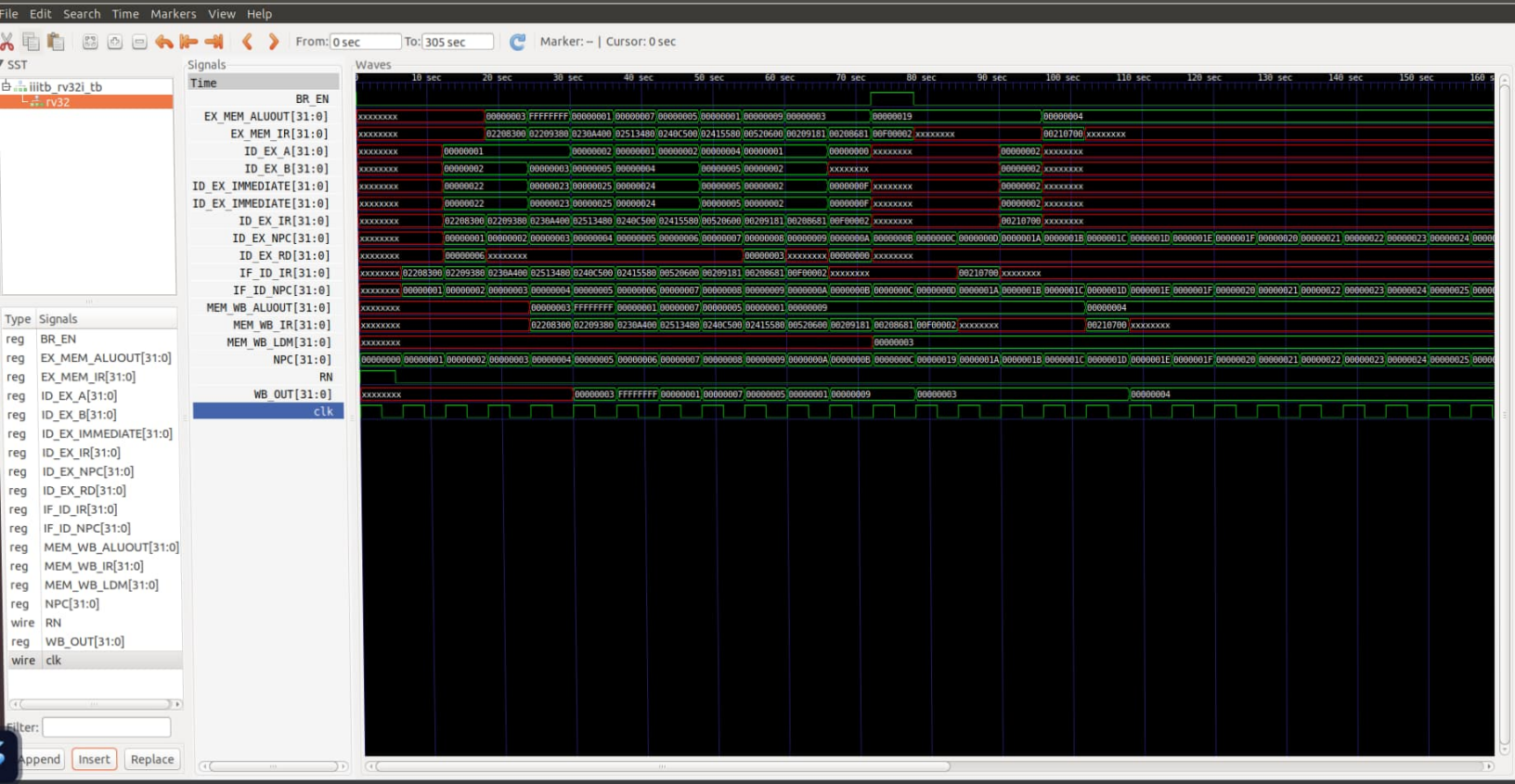
```
module iiitb_rv32i(clk,RN,NPC,WB_OUT);
input clk;
input RN;
//input EN;
integer k;
wire  EX_MEM_COND ;

reg
BR_EN;

//I_FETCH STAGE
reg[31:0]
IF_ID_IR,
IF_ID_NPC;

//I_DECODE STAGE
reg[31:0]
ID_EX_A,
ID_EX_B,
ID_EX_RD,
ID_EX_IMMEDIATE,
ID_EX_IR,ID_EX_NPC;

//EXECUTION STAGE
reg[31:0]
EX_MEM_ALUOUT,
EX_MEM_B,EX_MEM_IR;

parameter
ADD=3'd0,
SUB=3'd1,
AND=3'd2,
OR=3'd3,
XOR=3'd4,
SLT=3'd5,

ADDI=3'd0,
SUBI=3'd1,
```


vsdworkshop [Running] - Oracle VirtualBox
File Machine View Input Devices Help
Activities Text Editor Mon 18:39
Open *pratham_risc_tb.v ~/pratham Save
module iiitb_rv32i_tb;
reg clk,RN;
wire [31:0]WB_OUT,NPC;
iiitb_rv32i rv32(clk,RN,NPC,WB_OUT);
always #3 clk=!clk;
initial begin
RN = 1'b1;
clk = 1'b1;
$dumpfile ("iiitb_rv32i.vcd"); //by default vcd
$dumpvars (0, iiitb_rv32i_tb);
#5 RN = 1'b0;
#300 $finish;
end
endmodule
Verilog Tab Width: 8 Ln 1, Col 2 INS
Right Ctrl


vsduser@vsduser-VirtualBox: ~/pratham
File Edit View Search Terminal Help
vsduser@vsduser-VirtualBox:~/pratham$ ./a.out
bash: ./a.out: No such file or directory
vsduser@vsduser-VirtualBox:~/pratham$ ^C
vsduser@vsduser-VirtualBox:~/pratham$ iverilog -o simv iiitb_rv32i.v iiitb_rv32
i_tb.v
iiitb_rv32i.v: No such file or directory
No top level modules, and no -s option.
vsduser@vsduser-VirtualBox:~/pratham$ iverilog -o simv iiitb_rv32i.v iiitb_rv32
i_tb.v
No top level modules, and no -s option.
vsduser@vsduser-VirtualBox:~/pratham$ vvp simv
simv: Unable to open input file.
vsduser@vsduser-VirtualBox:~/pratham$ iverilog -o simv iiitb_rv32i.v iiitb_rv32
i_tb.v
vsduser@vsduser-VirtualBox:~/pratham$ vvp simv
VCD info: dumpfile iiitb_rv32i.vcd opened for output.
vsduser@vsduser-VirtualBox:~/pratham$ gtkwave iiitb_rv32i.vcd
Gtk-Message: 18:37:05.029: Failed to load module "canberra-gtk-module"
GTKWave Analyzer v3.3.86 (w)1999-2017 BSI
[0] start time.
[305] end time.


GTKWave - iiitb_rv32i.vcd
File Edit Search Time Markers View Help
From: 0 seSc
To: 305 sec
Marker: 66 sec | Cursor: 1 sec
SST
iiitb_rv32i_tb
Signals
Time
Waves
100 sec
200 sec
300 se
Type Signals
wire NPC[31:0]
reg RN
wire WB_OUT[31:0]
reg clk
Filter:
Append
Insert
Replace


File Edit Search Time Markers View Help
From: 0 sec
To: 305 sec
Marker: 303 sec | Cursor: 2 sec
SST
iiitb_rv32i_tb
Signals
Time
NPC[31:0]
RN
WB_OUT[31:0]
clk
Waves
10 sec
20 sec
30 sec
40 sec
50 sec
60 sec
70 sec
80 sec
90 sec
100 sec
110 sec
120 sec
130 sec
140 sec
150 sec
160 sec
00000000 00000001 00000002 00000003 00000004 00000005 00000006 00000007 00000008 00000009 0000000A 0000000B 0000000C 00000019 0000001A 0000001B 0000001C 0000001D 0000001E 0000001F 00000020 00000021 00000022 00000023 00000024 00000025 00000026
xxxxxxxx
00000003 FFFFFFFF 00000001 00000007 00000005 00000001 00000009
00000003
00000004
Type Signals
wire NPC[31:0]
reg RN
wire WB_OUT[31:0]
reg clk
Filter:
Append
Insert
Replace


File Edit Search Time Markers View Help
From: 0 sec
To: 305 sec
Marker: -- | Cursor: 0 sec
SST
iiitb_rv32i_tb
rv32
Signals
Waves
Time
BR_EN
EX_MEM_ALUOUT[31:0]
EX_MEM_IR[31:0]
ID_EX_A[31:0]
ID_EX_B[31:0]
ID_EX_IMMEDIATE[31:0]
ID_EX_IMMEDIATE[31:0]
ID_EX_IR[31:0]
ID_EX_NPC[31:0]
ID_EX_RD[31:0]
IF_ID_IR[31:0]
IF_ID_NPC[31:0]
MEM_WB_ALUOUT[31:0]
MEM_WB_IR[31:0]
MEM_WB_LDM[31:0]
NPC[31:0]
RN
WB_OUT[31:0]
clk
10 sec
20 sec
30 sec
40 sec
50 sec
60 sec
70 sec
80 sec
90 sec
100 sec
110 sec
120 sec
130 sec
140 sec
150 sec
160 s
Type
Signals
reg BR_EN
reg EX_MEM_ALUOUT[31:0]
reg EX_MEM_IR[31:0]
reg ID_EX_A[31:0]
reg ID_EX_B[31:0]
reg ID_EX_IMMEDIATE[31:0]
reg ID_EX_IR[31:0]
reg ID_EX_NPC[31:0]
reg ID_EX_RD[31:0]
reg IF_ID_IR[31:0]
reg IF_ID_NPC[31:0]
reg MEM_WB_ALUOUT[31:0]
reg MEM_WB_IR[31:0]
reg MEM_WB_LDM[31:0]
reg NPC[31:0]
wire RN
reg WB_OUT[31:0]
wire clk
Filter:
Append
Insert
Replace