Current mirror OTA in 45nm and 90nm CMOS technology

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Abstract

This project explores the design and simulation of an Abstract Current Mirror Operational Transconductance Amplifier (OTA) implemented in both 45nm and 90nm CMOS technologies. The study aims to compare the performance of the OTA in terms of key parameters such as transconductance, gain, bandwidth, power consumption, and output impedance across both process nodes. Using advanced simulation tools like LT SPICE, the project evaluates the effects of scaling on the performance, focusing on challenges related to power efficiency, frequency response, and device sizing. Additionally the impact of process variations on the OTA's performance is examined through Monte Carlo simulations. The findings of this project offer insights into the trade-offs between using smaller (45nm) and larger (90nm) process nodes for designing high-performance, low-power analog circuits, providing valuable guidelines for future analog design in modern CMOS technologies.

I. INTRODUCTION:

Operational amplifiers (Op-Amps) are key in analog circuits for tasks like amplification and filtering. A variant, the operational transconductance amplifier (OTA), converts differential voltage inputs to current, making it ideal for low-power designs.

OTAs are widely used in biomedical applications to amplify weak bio-signals like EEG, ECG, and EMG, which have low amplitude, low frequency, and high noise. Modern systems favor portable, battery-powered designs using sub-micron CMOS technology, though short-channel effects can impact performance.

Common OTA topologies include two-stage, telescopic cascode, folded cascode, and current mirror. Each offers trade-offs in power, gain, noise, and frequency response. The current mirror OTA is preferred for biomedical use due to its simplicity and low power, despite some frequency limitations at smaller nodes.

This paper designs and analyzes a current mirror OTA in 45 nm and 90 nm CMOS, evaluating DC gain, CMRR, and power consumption to determine the most suitable node for biomedical applications.

2. LITRATURE SURVEY:

Operational Transconductance Amplifiers (OTAs) are fundamental components in analog design, and the Current Mirror OTA is particularly valued for its compact structure and low-power operation. As CMOS technology scales, OTA performance is affected by factors like short-channel effects, leakage, and reduced intrinsic gain.

Razavi [1] provided a strong foundation in OTA design, outlining performance trade-offs in deep-submicron processes. Gupta et al. [2] analyzed OTA behavior across different nodes and observed that gain and bandwidth improve with reduced channel lengths, though sensitivity to process variation increases.

Kumar and Singh [3] implemented a 90nm OTA that optimized power and linearity, suitable for portable and biomedical devices. Wan Jusoh et al. [4] compared symmetrical OTA performance in 180nm, 130nm, and 90nm technologies, showing benefits of scaling but also noting layout and mismatch challenges

However, existing studies focus either on a single node or general OTA topologies. A direct comparison of the Current Mirror OTA in both 45nm and 90nm CMOS is still lacking. This work aims to fill that gap through detailed design, simulation, and performance evaluation in both technologies.

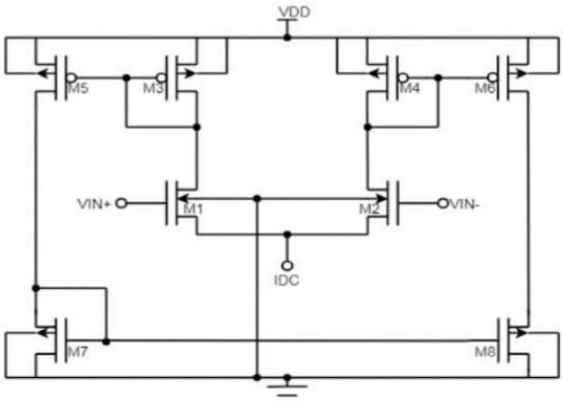
3. RESEARCH METHOD

Current mirror symmetrical OTA:

Both OTA with 45 nm and 90 nm CMOS technology implemented symmetrical current mirror topology. The topology has several advantages; larger transconductance, larger slew rate and larger gain bandwidth produced during amplification operation. The OTA was designed from several current mirrors that acted as active load to each other. The input stage of OTA consisted of two NMOSs in differential pair structure and then three simple current mirrors were constructed to bias the inverters in OTA circuit as shown in Figure The OTA circuit was designed by fixing the dimension of differential input pair and current mirrors. The dimension of differential input pair is given by (1) and dimension of the three current mirrors is given by (2). Initially, the dimensions of each transistor in the OTA were obtained through characterization of PMOS and NMOS in Synopsys tools. The 90 nm OTA was designed using SAED_90nm Process Design Kit (PDK) meanwhile 45 nm OTA is designed using 45nm Process Design Kit. Both OTAs were simulated
in Synopsys LTSpice simulator.S =(W/L) ,$S_{M1}=S_{M2}$
$S_{M3}=S_{M4}$,$S_{M5}=S_{M6}$,$S_{M7}=S_{M8}$

where S is the ratio of width over length of MOSFET in both designs of the OTA.

CIRCUIT DIAGRAM::



WIDTH AND LENGTH RATIO OF MOSFET:

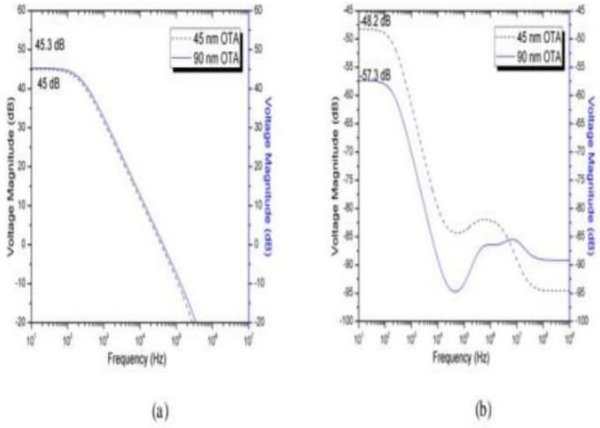
Transistor	Width(um)	Length (um)
M1&M2	2	1
M3&M4	3	1
M5&M6	6	1
M7&M8	0.24	1

OTA SPECIFICATIONS:

Both OTAs were designed in 45 nm and 90 nm CMOS technology, and were meant to be applied in bio-medical application. Therefore, there were several specifications that must be declared and followed during the design process and simulation. The current mirror symmetrical OTA specifications are shown in table

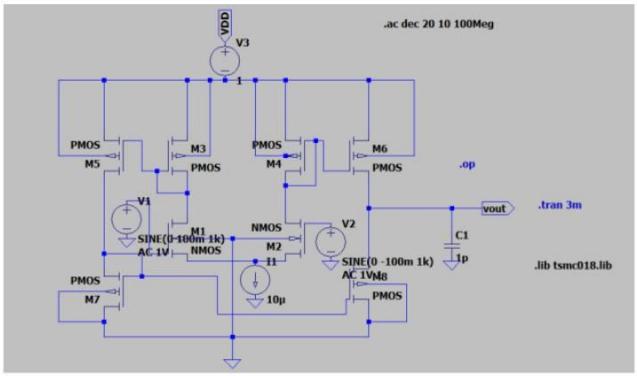
Specification	Value
Voltage supply	1
Open loop gain(dB)	>40
CMRR(dB)	>100
Power consumption(uW)	<10
Slew rate(V/us)	>10
Input referred Noise	<4

EXPECTED WAVE FORM:



4. SIMULATION RESULT AND ANALYSIS IN LT SPICE:

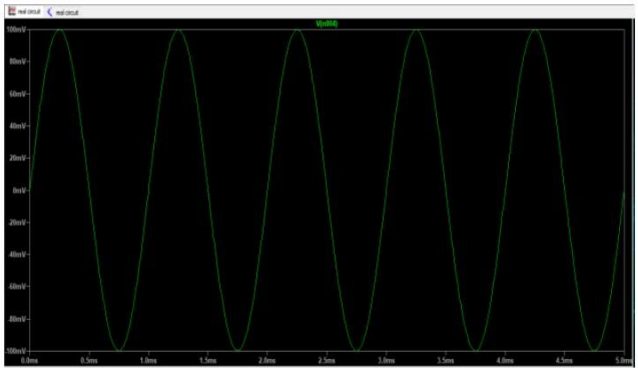
CIRCUIT DIAGRAM:



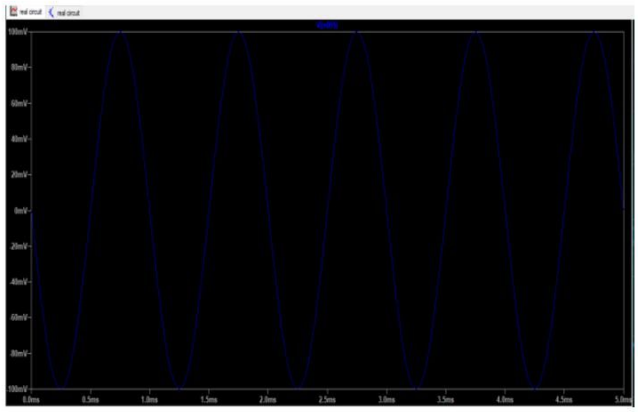
TRANSIENT ANALYSIS:

For transient analysis, both OTAs were simulated in two testbench for common input signals and differential input signals. For common input signal analysis, the sinusoidal voltage with amplitude of 2 mV was fed into both positive and negative input termina ls. The frequency of sinusoidal voltage supply is set at 1K Hz. Both amplitude and frequency were set in the manner of imitating the electrocardiogram (ECG) signals from human body. Then, for differential input signal analysis, the negative input termina l of OTA was fed with a positive 20 mV of sinusoidal voltage and negative terminal was fed with a negative 20mV of sinusoidal voltage. Below image shows the transient result of differential input signals analysis for 90 nm OTA and for 45 nm OTA.

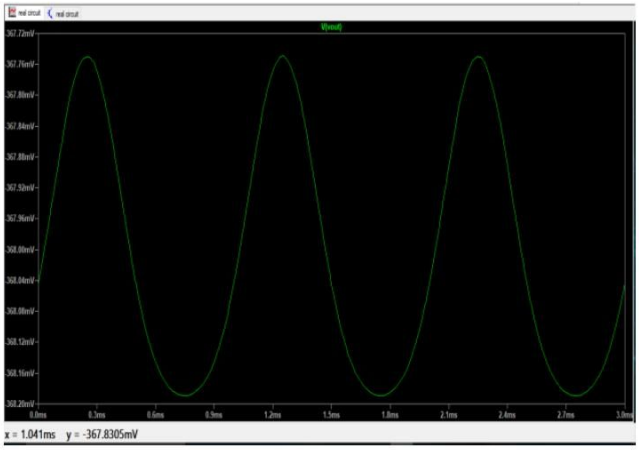
POSITIVE INPUT WAVEFORM:



NEGATIVE INPUT WAVEFORM:

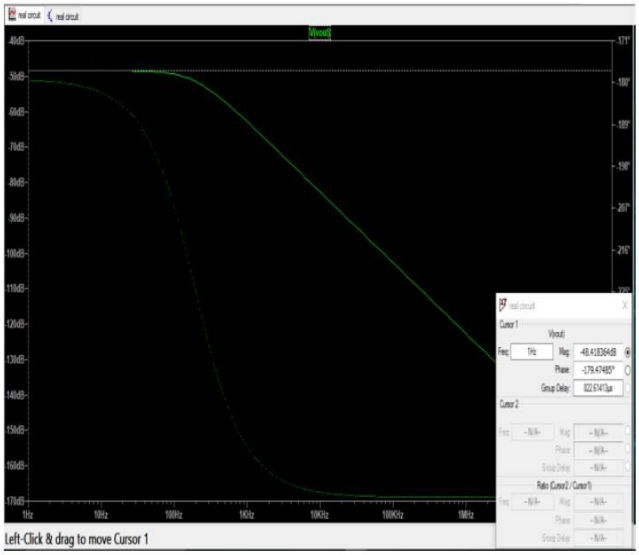


OUTPUT WAVE FORM:



AC ANALYSIS:

Both OTAs were simulated using HSpice simulator to find the open loop gain and the phase margin. According to the design specifications, the OTA must produce a gain more than 40 dB in order to efficiently amplify the bio-potential signals For common mode gain, both input pins of OTA were fed with 1 V of AC supply. The 45 nm OTA produced a common mode gain of -48.4dB while the 90 nm OTA produced -53.3 dB. The results are shown inFigure



1]COMMON MODE REJECTION RATIO(CMRR):

The CMRR for 45 nm OTA was 93.2 dB and for 90 nm OTA was 102.6 dB. According to the design specifications, CMRR of OTA should be more than 100 dB in order to reject common mode signal from input efficiently. In bio-potential signals, there are lots of noises and common mode signals are sourced from external such amplification process to become less accurate.Based on the results, the 90 nm OTA produced higher value of CMRR when compared to 45 nm OTA. Thus, 90 nm OTA reached the CMRR design specifications and can filter out externalnoise together with common mode signals efficiently

POWER CONSUMPTION:

The power consumption can also be calculated manually by analyzing the current flow from source terminal of transistors M5 and M6. Then, the values of both currents at the branches were incorporated in (6) to get the power consumption Value.The 45 nm OTA consumed 28.21 nW from ± 0.5 V of supply whereas the 90 nm OTAconsumed 28.42 nW. This means the 45 nm OTA can do amplification process with overall power consuming less than the 90 nm OTA. The result obtained met the design specifications

RESULT AND DISCUSSION:

PARAMETER	45nm	90nm
Voltage supply	1	1
Gain(dB)	45	45.3
CMRR	93.2	102.6
POWER	28.21nW	28.42nW

DISCUSSION:

Scaling Effect: The 45nm technology generally provides better performance due to shorter channel lengths, resulting in higher speed (bandwidth and slew rate) and lower power consumption.

Gain and Noise: While gain may be slightly lower in deeply scaled nodes due to reduced intrinsic gain of transistors, circuit techniques (like gain boosting) can compensate. 45nm has better noise performance due to lower parasitics.

Power Efficiency: 45nm consumes much less power than 90nm for the same performance, making it preferable for battery-powered and high-density integration systems.

APPLICATION:

1. Analog Signal Processing: Amplifiers, filters, and data converters (ADCs/DACs).
2. Sensor Interfaces: Used in biosensors, pressure sensors, etc., for signal conditioning.
3. Low-Power Systems: Ideal for portable and implantable electronics.
4. Neural Networks & Neuromorphic Computing: Acts as synapse circuits in analog computation.
5. Operational Transconductance Filters (OTFs): Tunable filters in analog circui t s.

CONCLUSION:

In this paper, the current mirror symmetrical OTAs have been designed and simulated using 90 nm and 45 nm CMOS technology. Both OTAs were designed, simulated and analyzed using Synopsys tools. Simulation results from both OTAs also have been comparatively studied and discussed according to the stated design specifications. The stated design specifications are for bio -potential signals detection purpose and based on the discussion, the 45 nm OTA managed to produce 45 dB of open loop gain, 93.2 dB of CMRR and also only consumed 28.21 nW from ±0.5 V of supply. Further more, the input referred noise produced by 45 nm OTA was 1.113 $\mu V\sqrt{Hz}$ which is lesser than 90 nm OTA. Thus, the 45 nm OTA is a suitable choice to be implemented in bio-potential signals detection system. However, there are disadvantages by implementing the current mirror symmetrical topology as the gain bandwidth is too large for bio-potential signals detection purpose, so further research must be done to ensure the OTA design can reach optimal performance according to the design specifications.

ACKNOWLEDGEMENT:

We express our sincere gratitude Dr. Remya Jayachandran for their invaluable guidance, constructive feedback, and encouragement throughout the development of this project. Their expertise and mentorship have been instrumental in shaping the success of our work.

Finally, we extend our appreciation to our institution for providing the necessary resources and facilities for conducting this project.

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