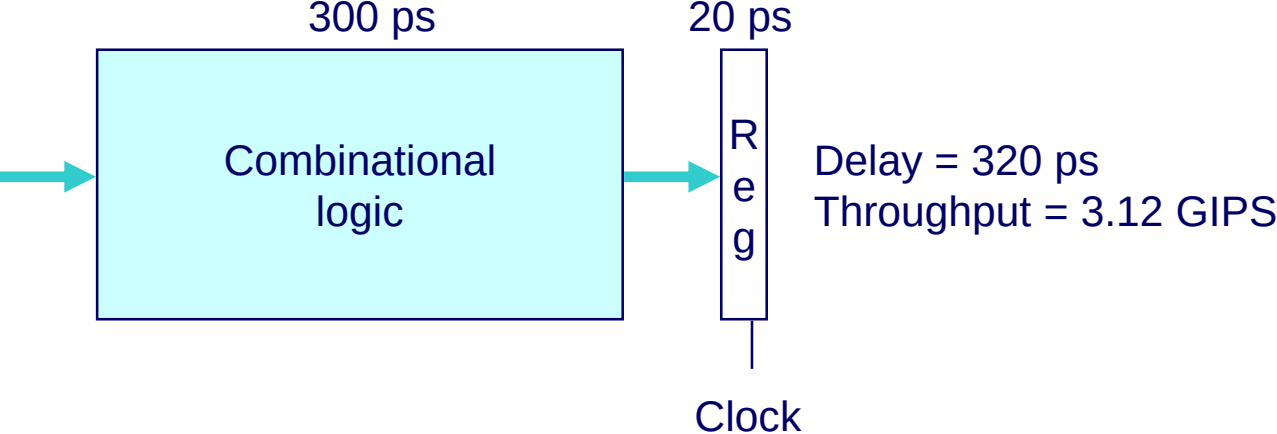
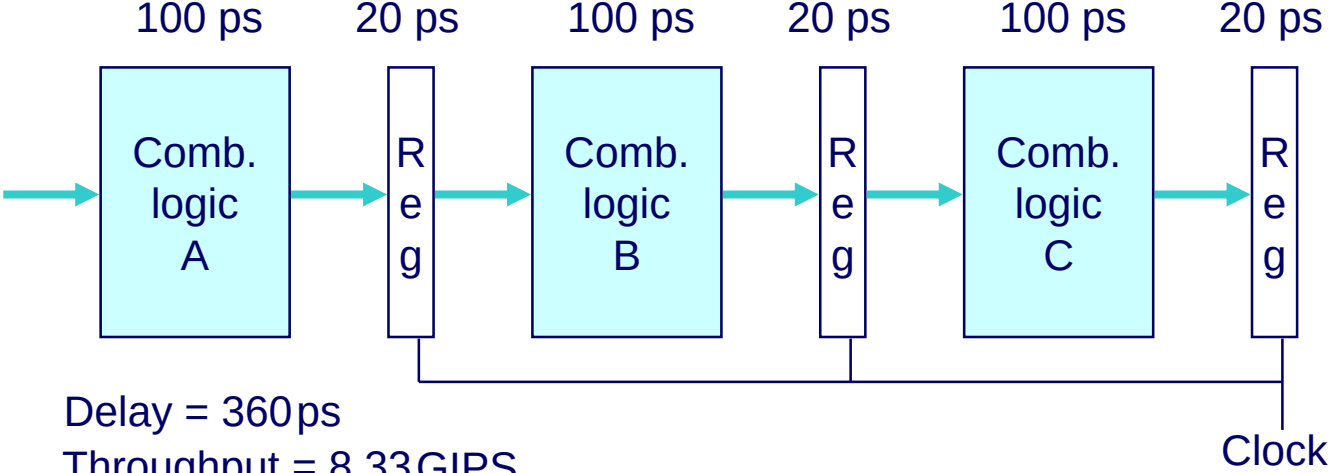
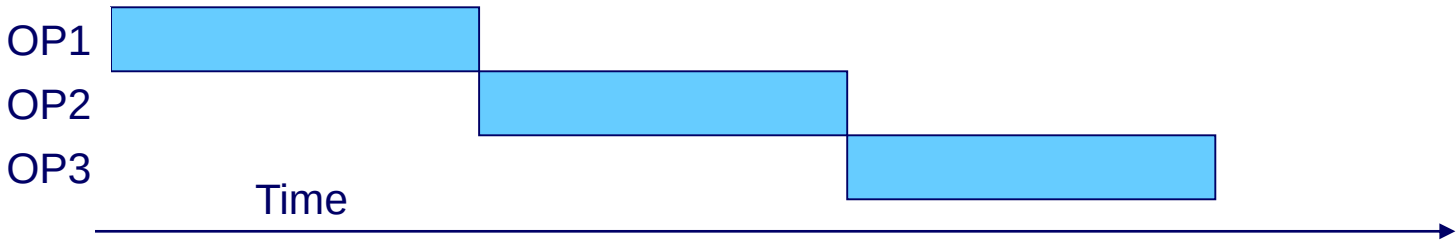

300 ps
20 ps
Combinational logic
Reg
Delay = 320 ps
Throughput = 3.12 GIPS
Clock



Delay = 360 ps

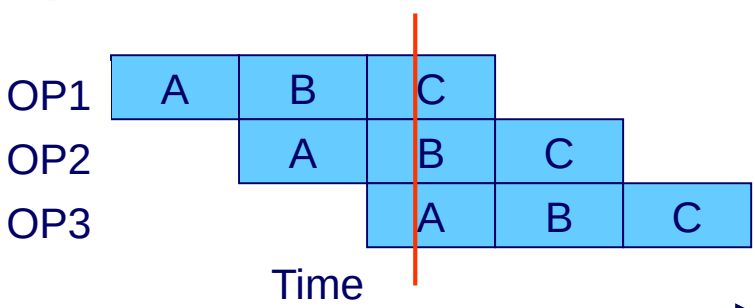
Throughput = 8.33 GIPS

Unpipelined

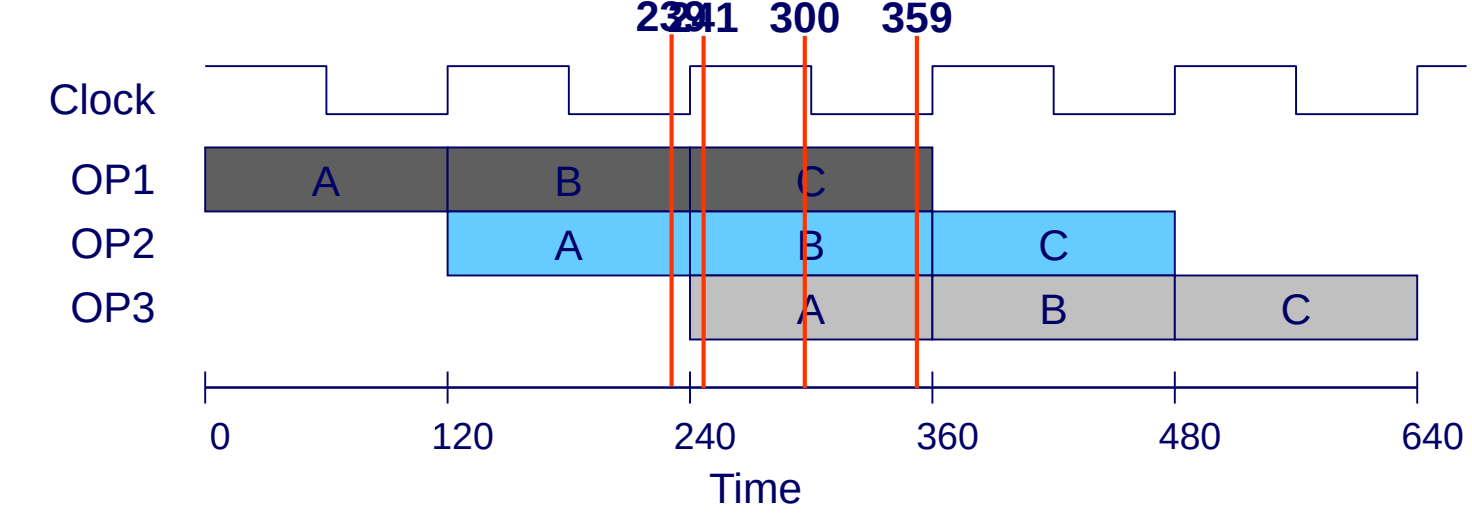


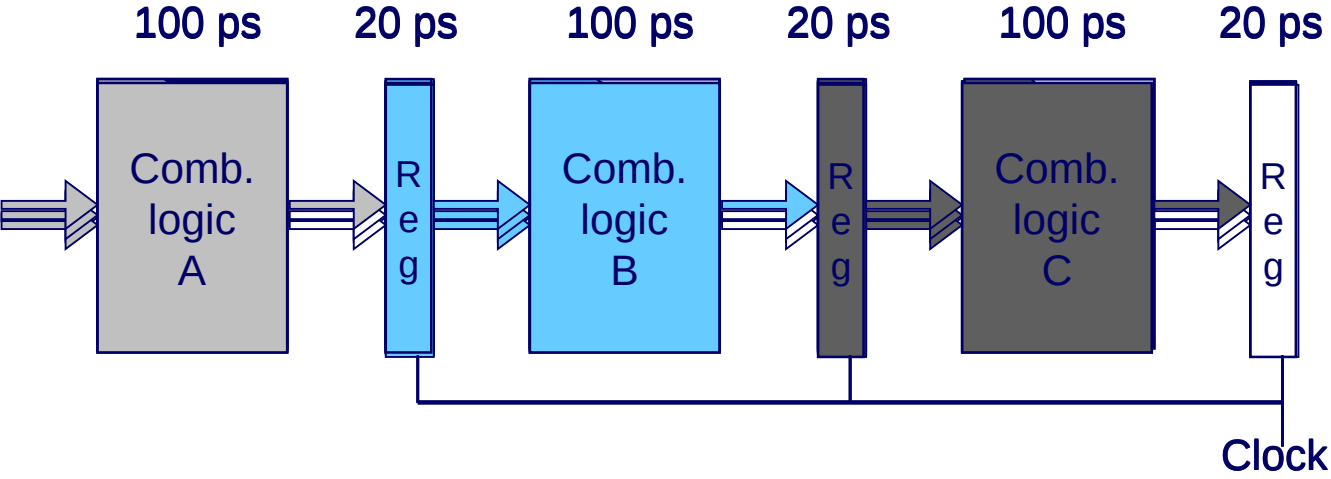
Cannot start new operation until previous one completes

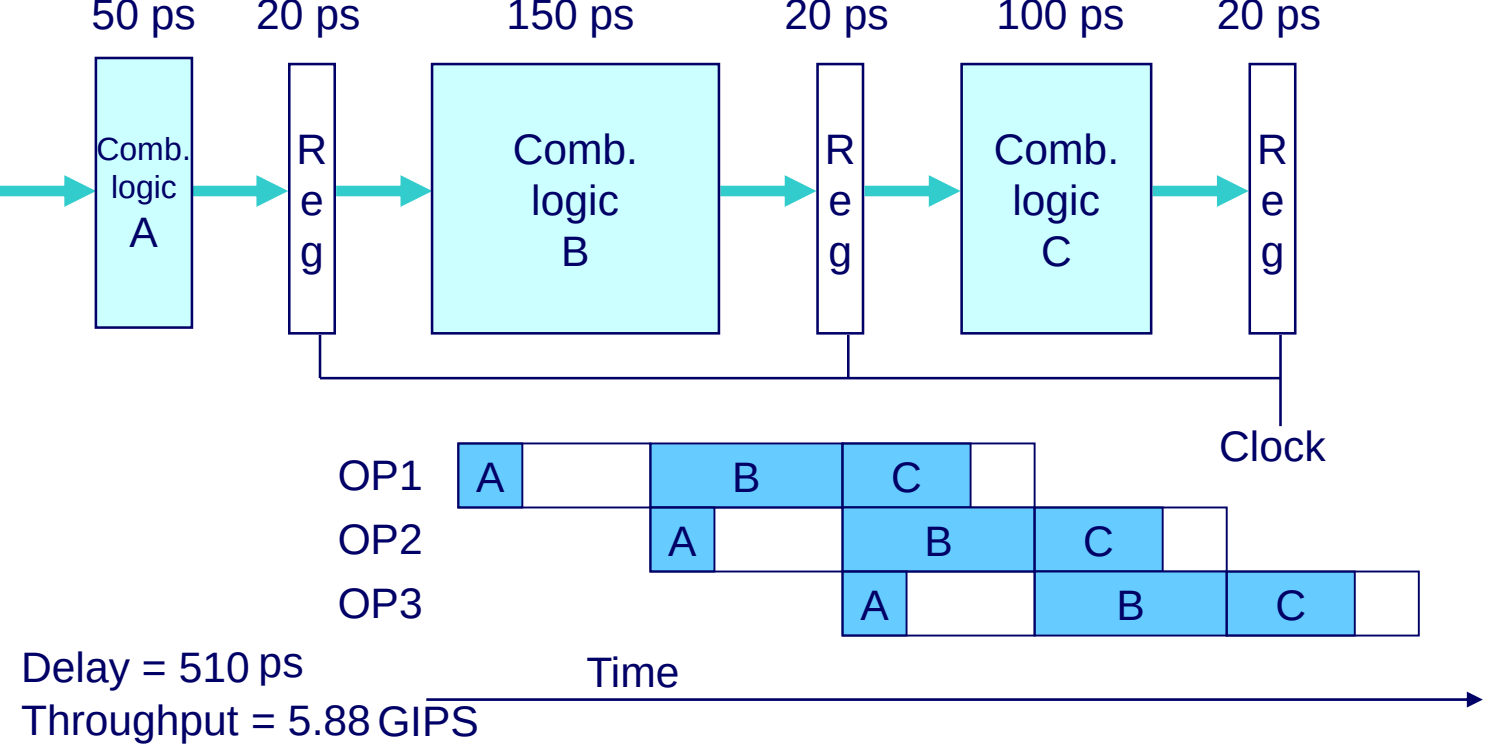
3-Way Pipelined

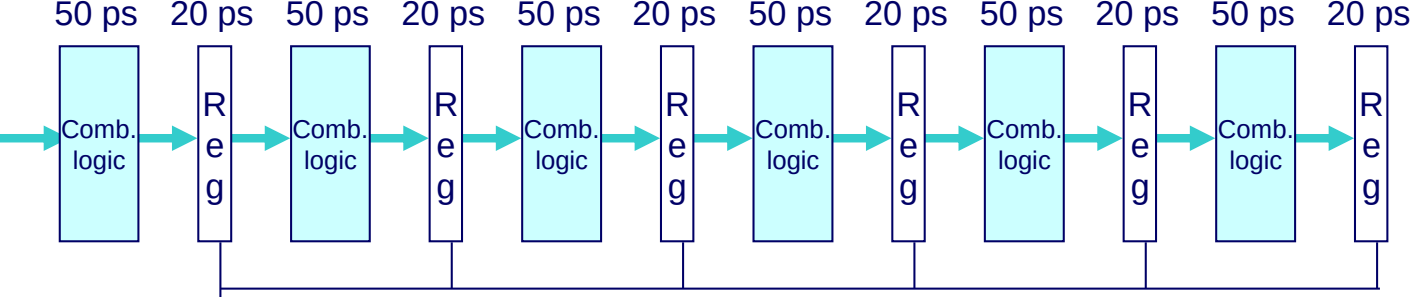


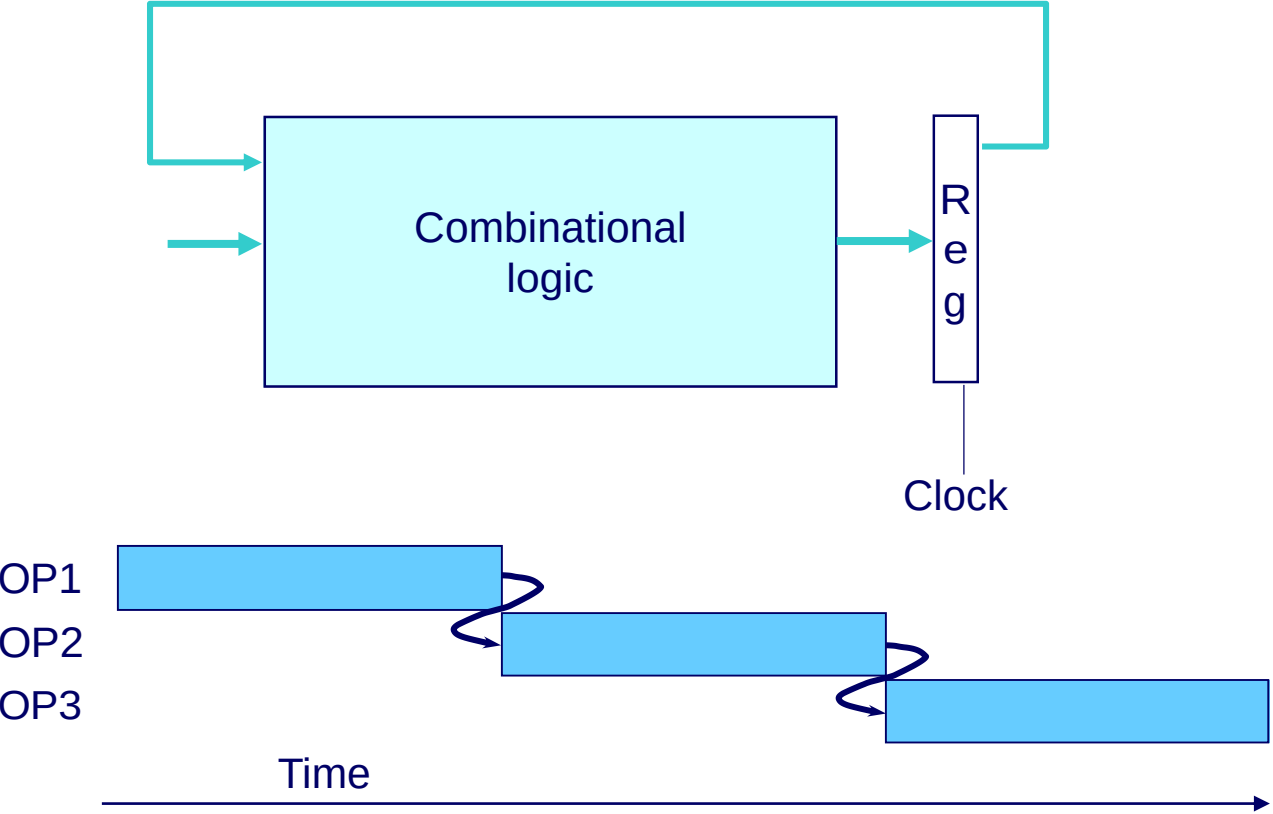
Up to 3 operations in process simultaneously

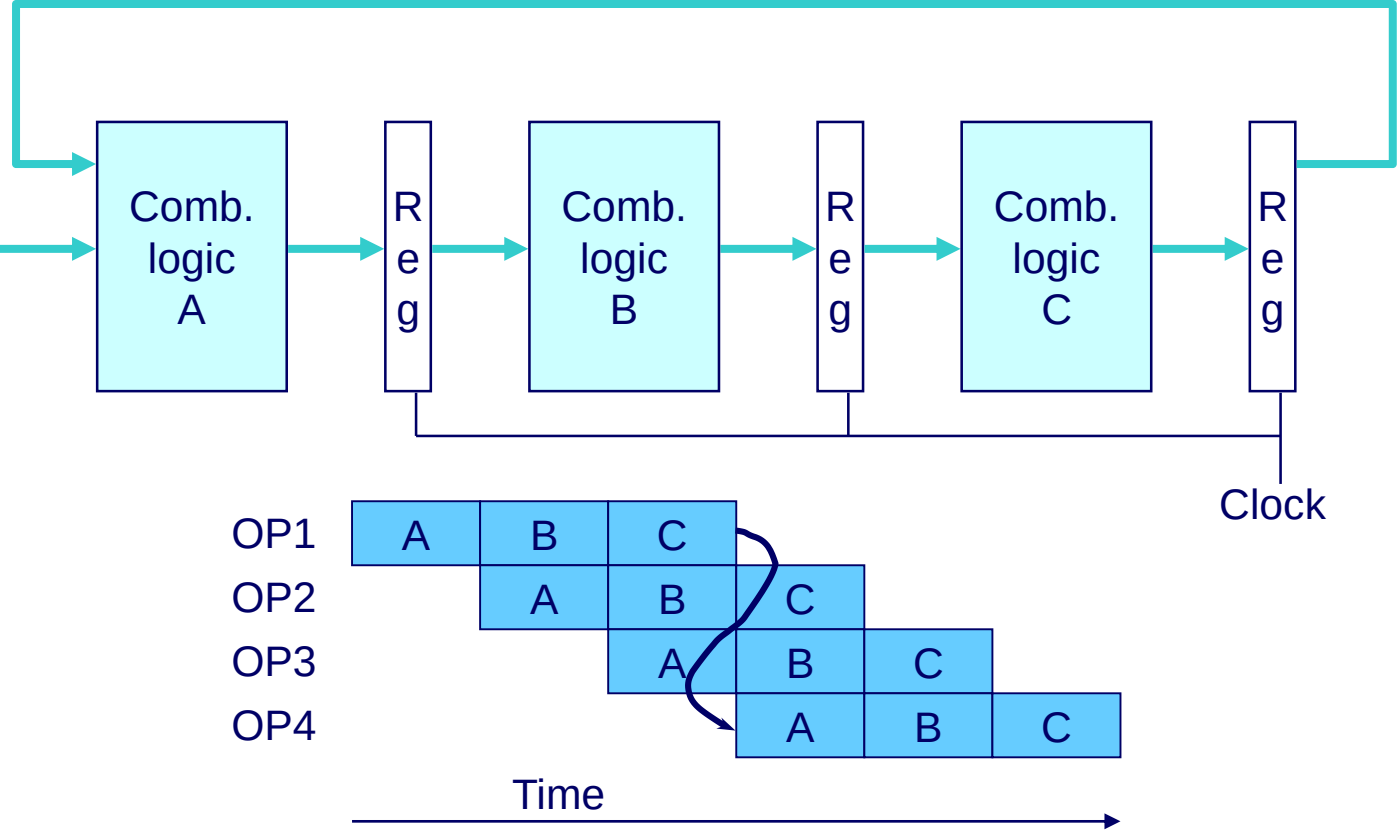

Clock
OP1
OP2
OP3
A
B
C
A
B
C
A
B
C
0
120
240
360
480
640
Time


100 ps
20 ps
100 ps
20 ps
100 ps
20 ps
Comb. logic A
Reg
Comb. logic B
Reg
Comb. logic C
Reg
Clock


50 ps
20 ps
150 ps
20 ps
100 ps
20 ps
Comb. logic A
Reg
Comb. logic B
Reg
Comb. logic C
Reg
Clock
OP1
OP2
OP3
A
B
C
Time
Delay = 510 ps
Throughput = 5.88 GIPS


50 ps
20 ps
50 ps
20 ps
50 ps
20 ps
50 ps
20 ps
50 ps
20 ps
50 ps
20 ps
Comb. logic
Reg
Comb. logic
Reg
Comb. logic
Reg
Comb. logic
Reg
Comb. logic
Reg
Comb. logic
Reg
Clock
Delay = 420 ps, Throughput = 14.29 GIPS


Combinational
logic
Reg
Clock
OP1
OP2
OP3
Time


Comb. logic A
Reg
Comb. logic B
Reg
Comb. logic C
Reg
Clock
OP1
OP2
OP3
OP4
A
B
C
Time