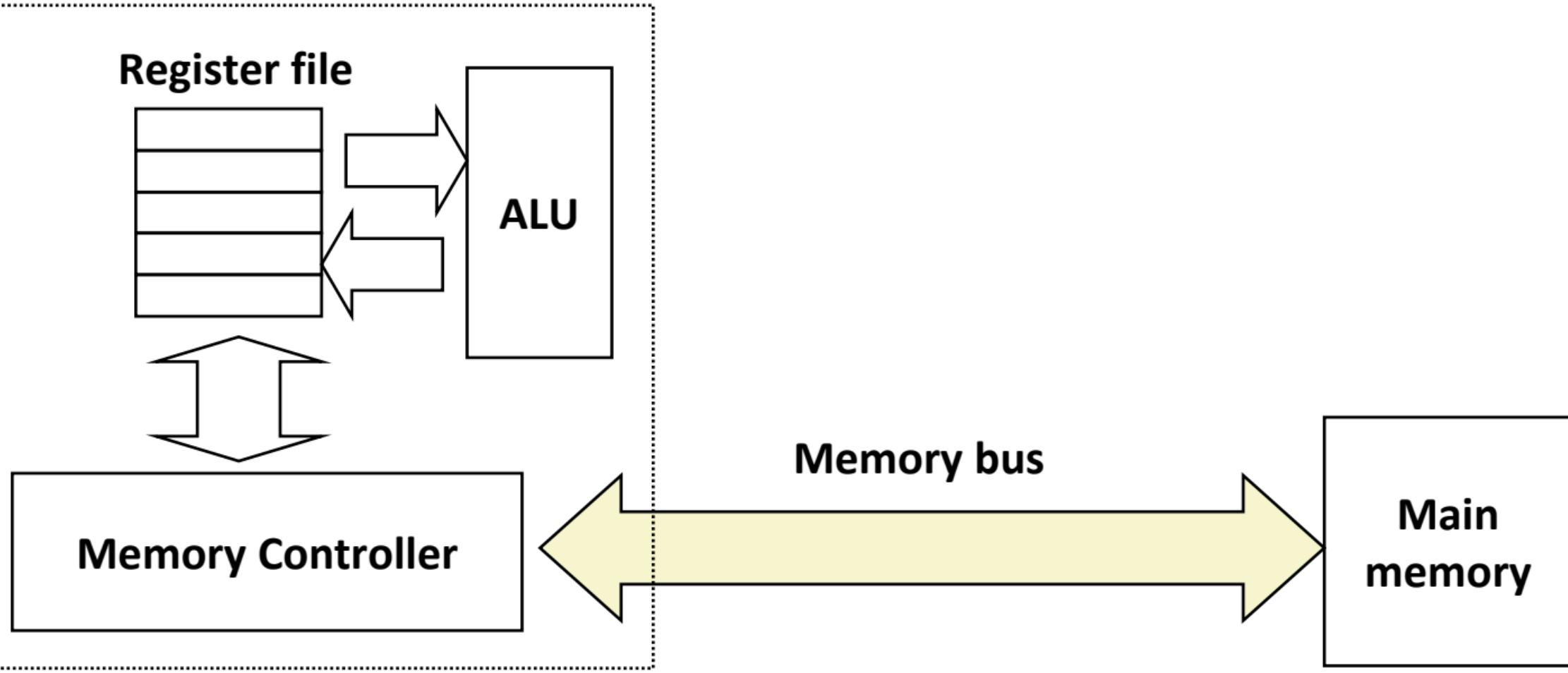
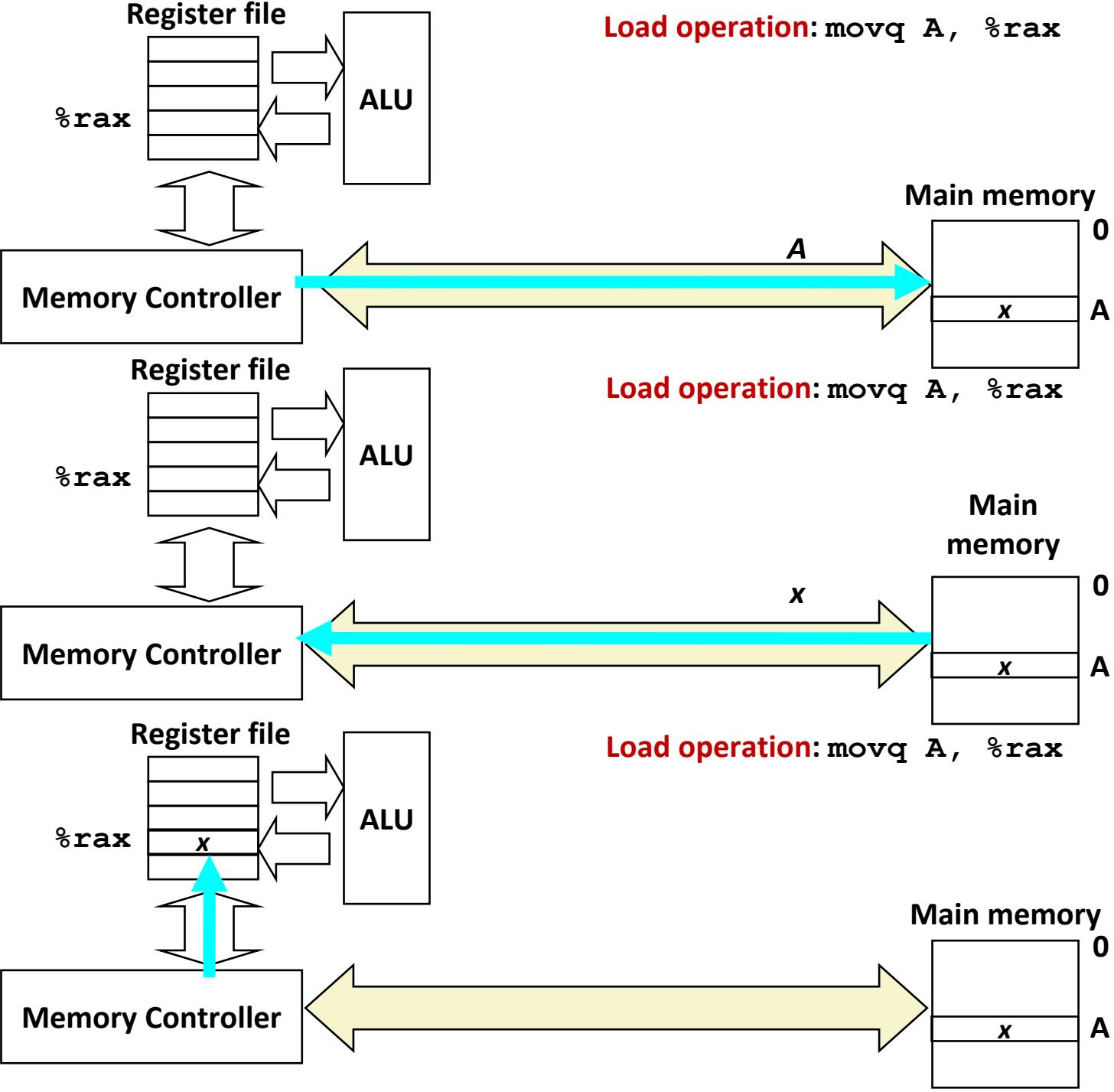
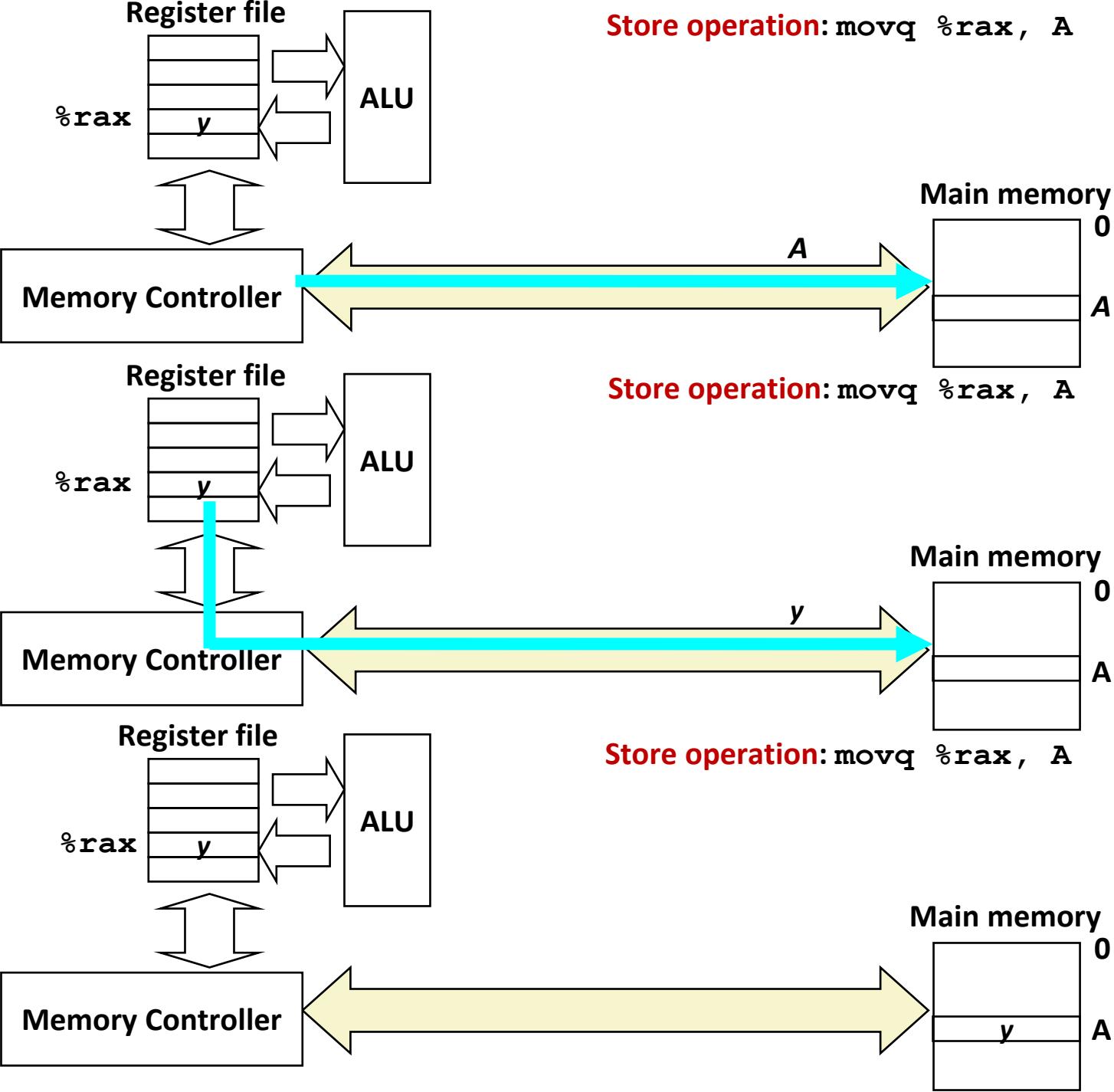
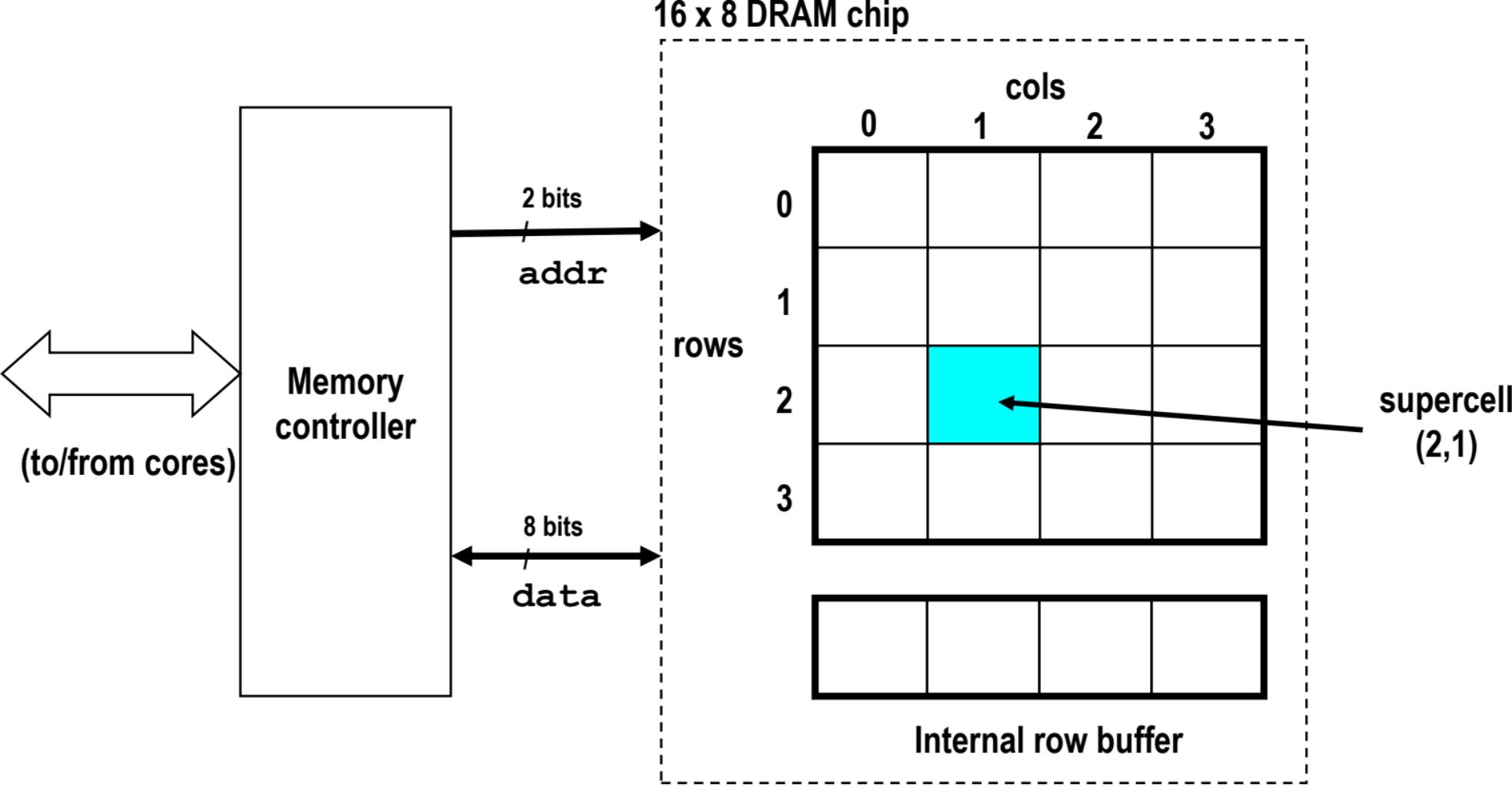


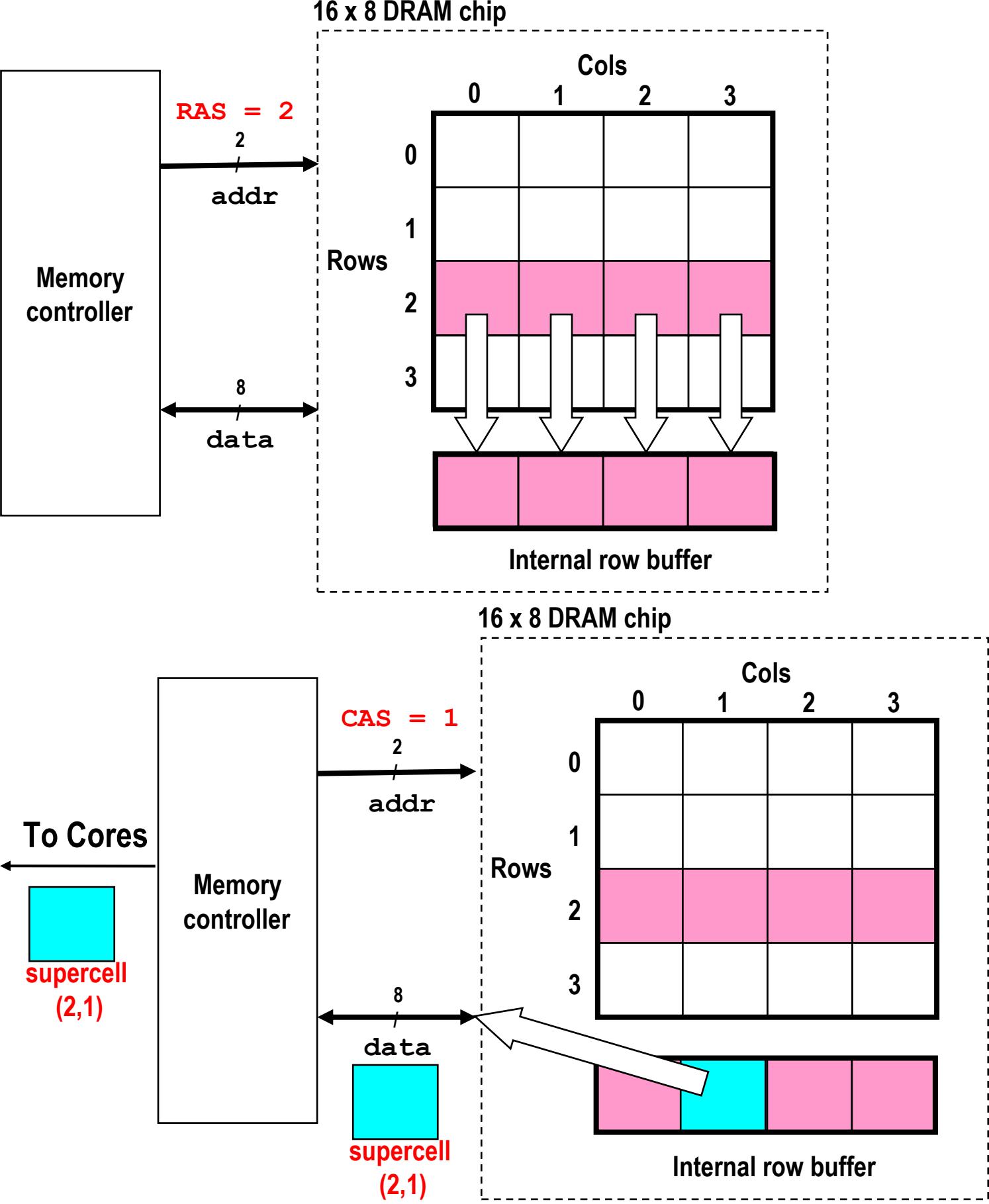
CPU chip

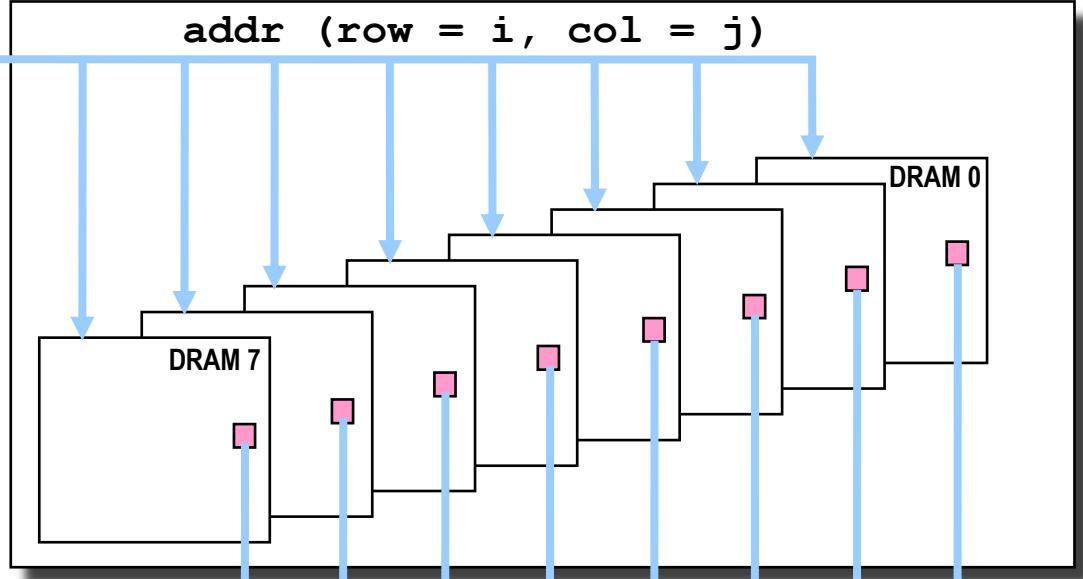






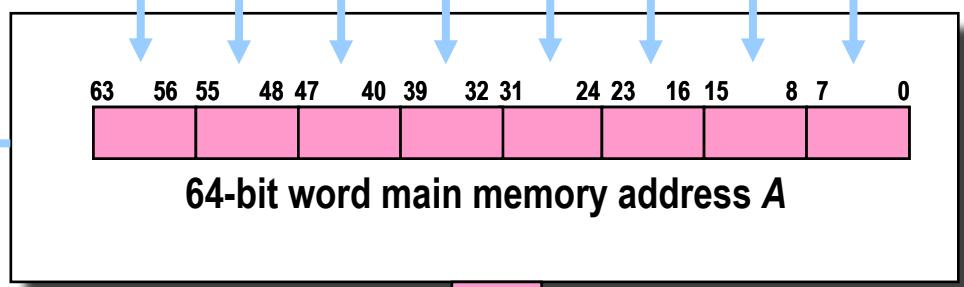




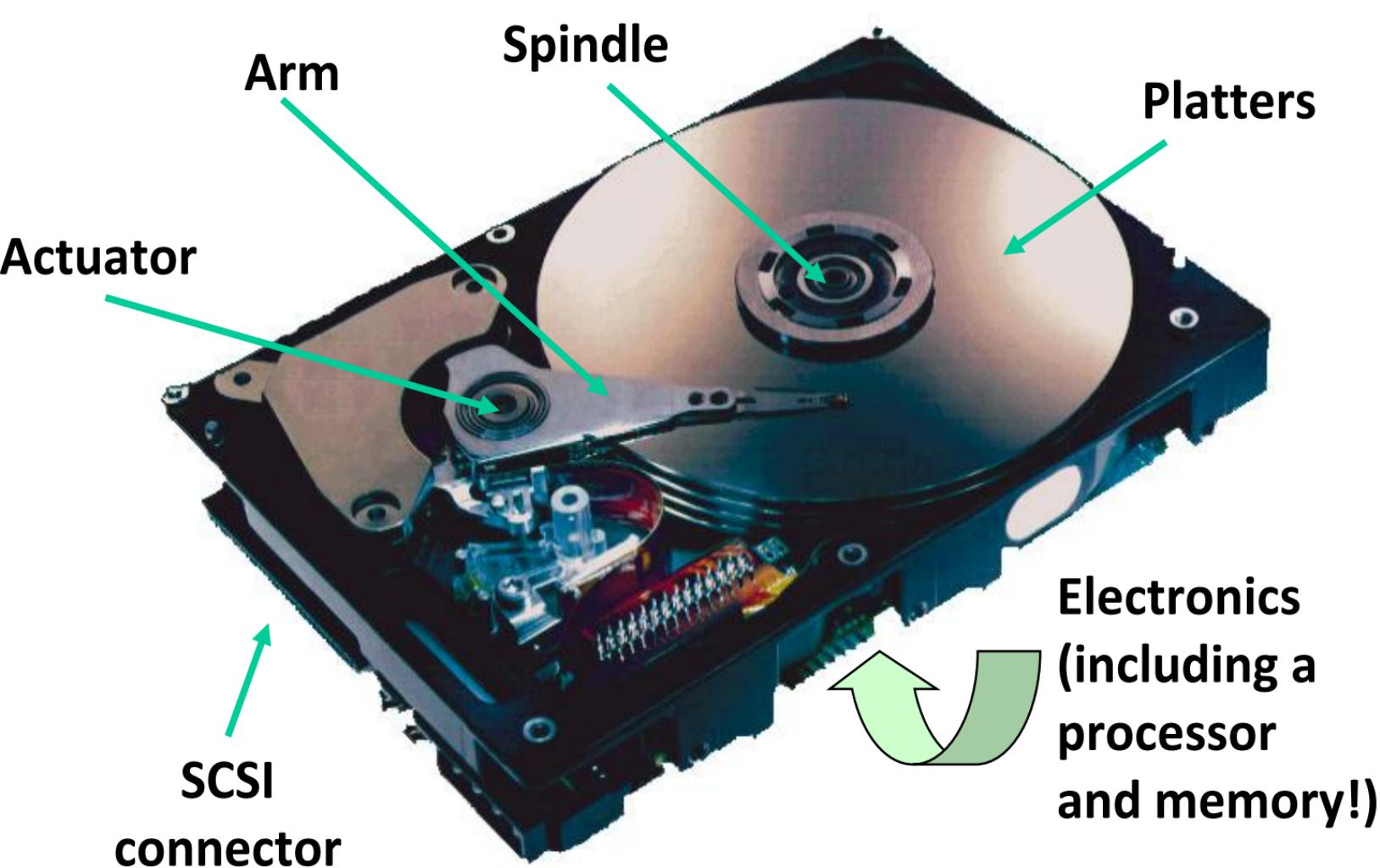


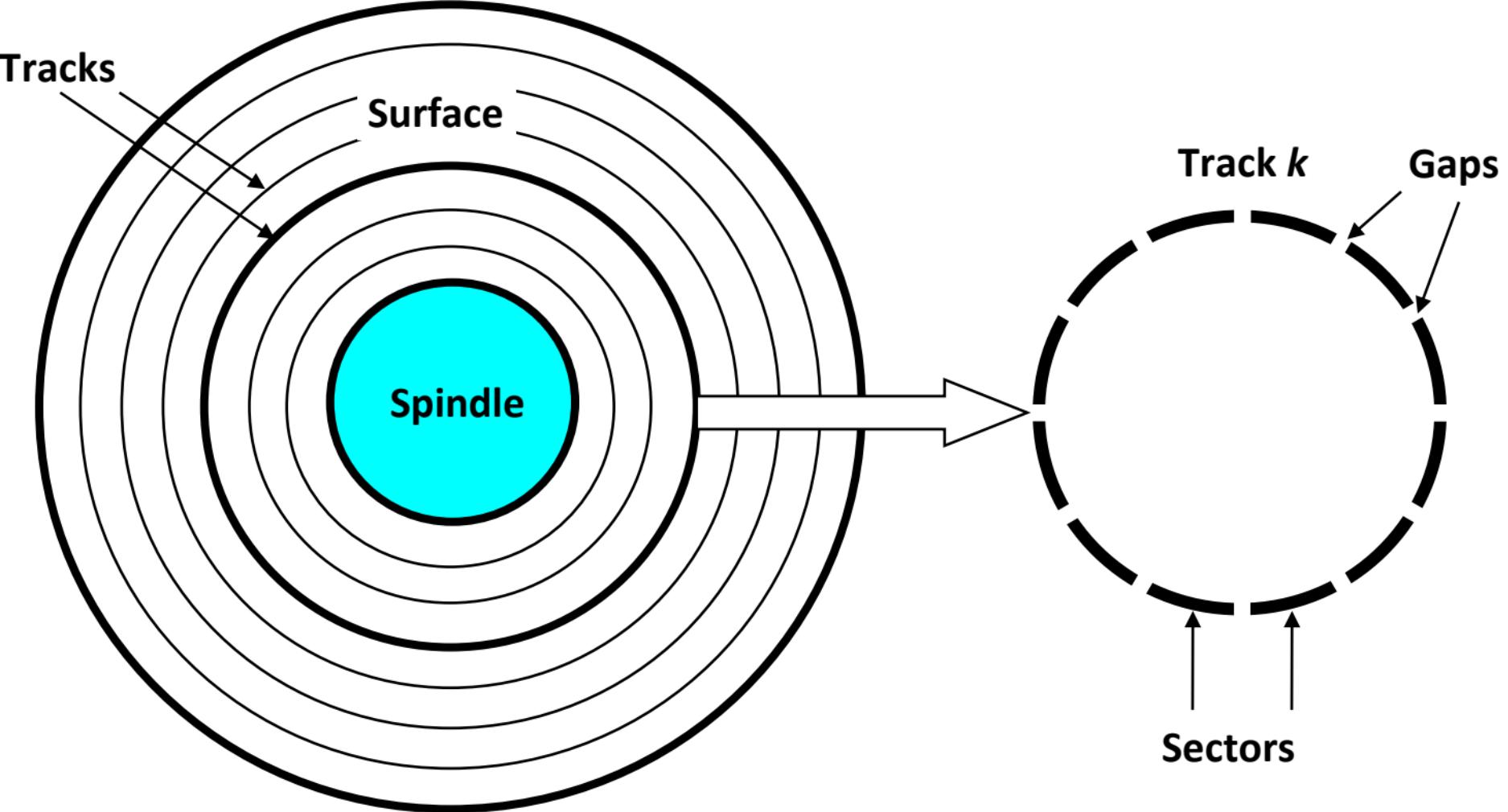
■ : supercell (i,j)

**64 MB
memory module
consisting of
eight 8Mx8 DRAMs**

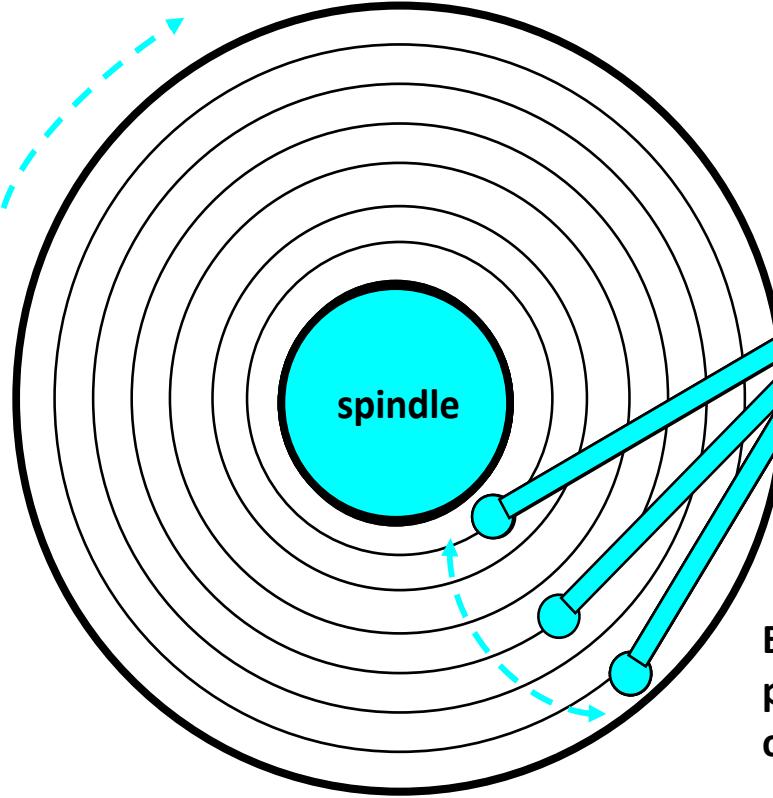


64-bit word





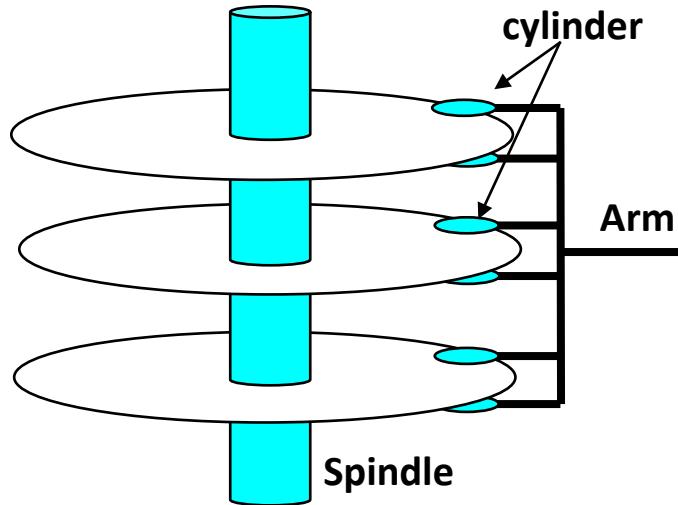
The disk surface
spins at a fixed
rotational rate

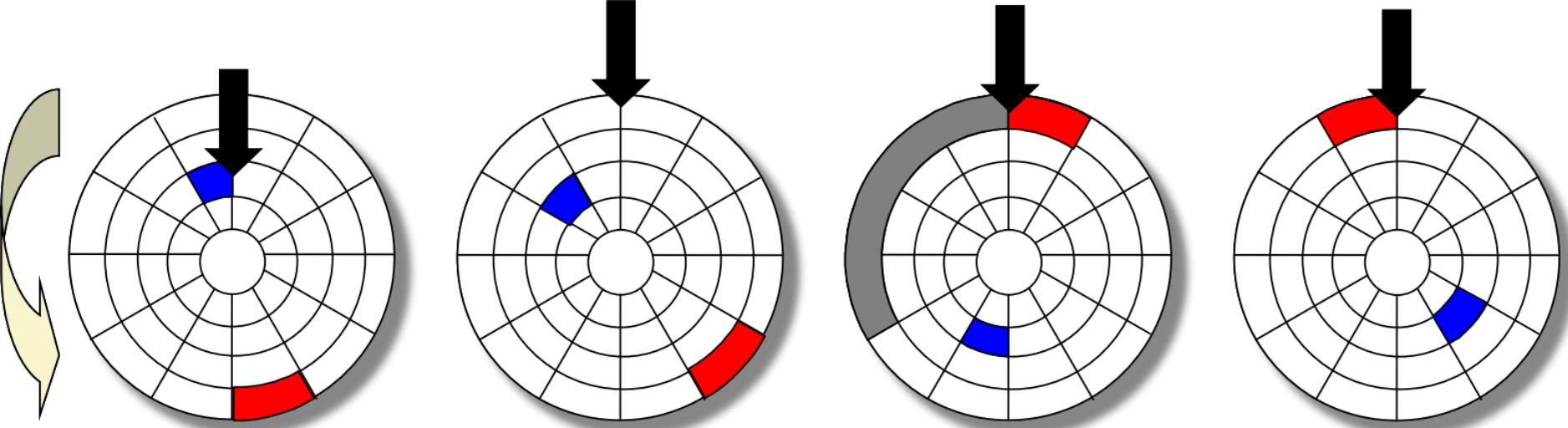


The read/write *head*
is attached to the end
of the *arm* and flies over
the disk surface on
a thin cushion of air.

By moving radially, the arm can
position the read/write head
over any track.

Read/write heads
move in unison
from cylinder to
cylinder





After **BLUE** read

Seek for **RED**

Rotational latency

After **RED** read

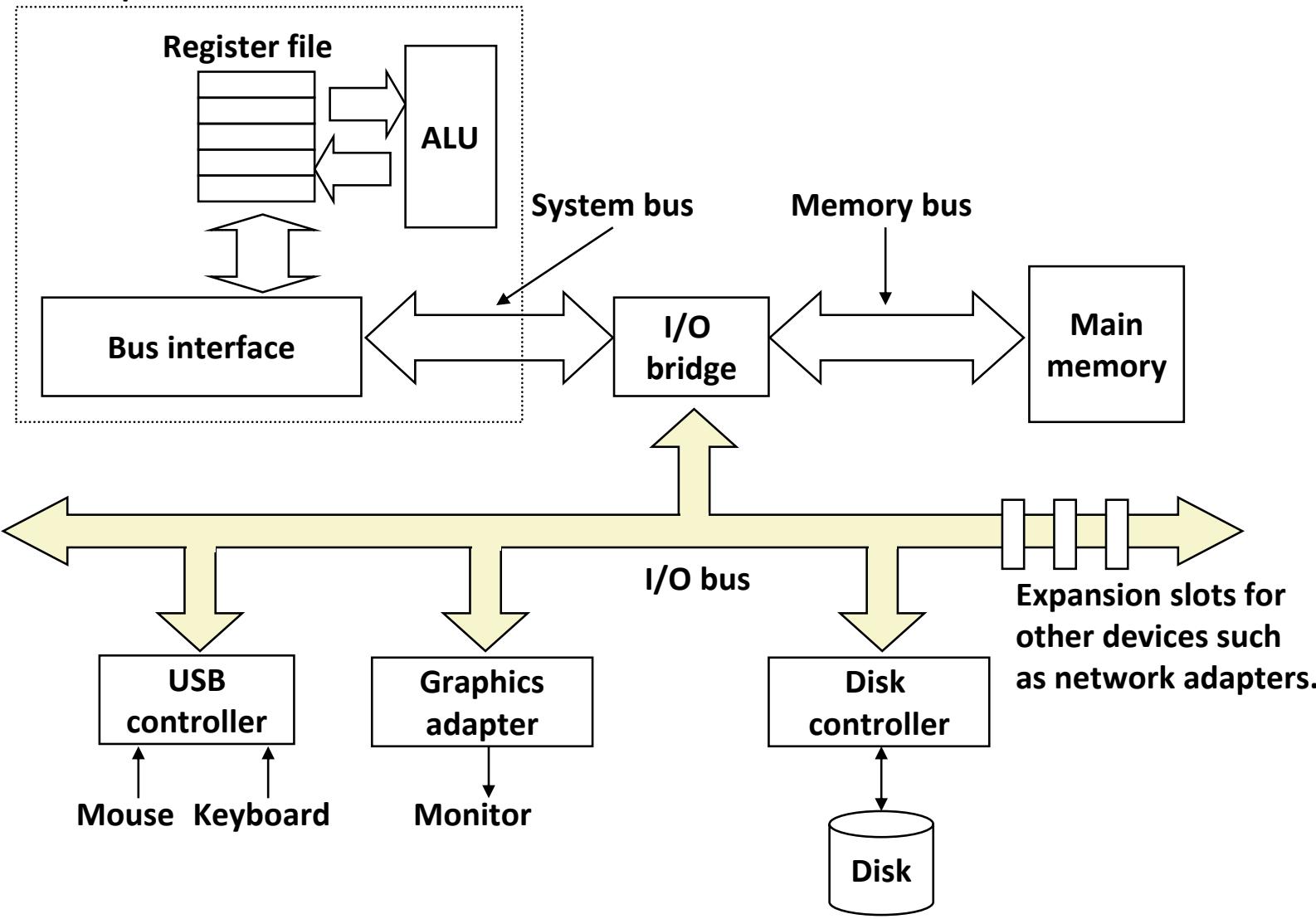
Data transfer

Seek

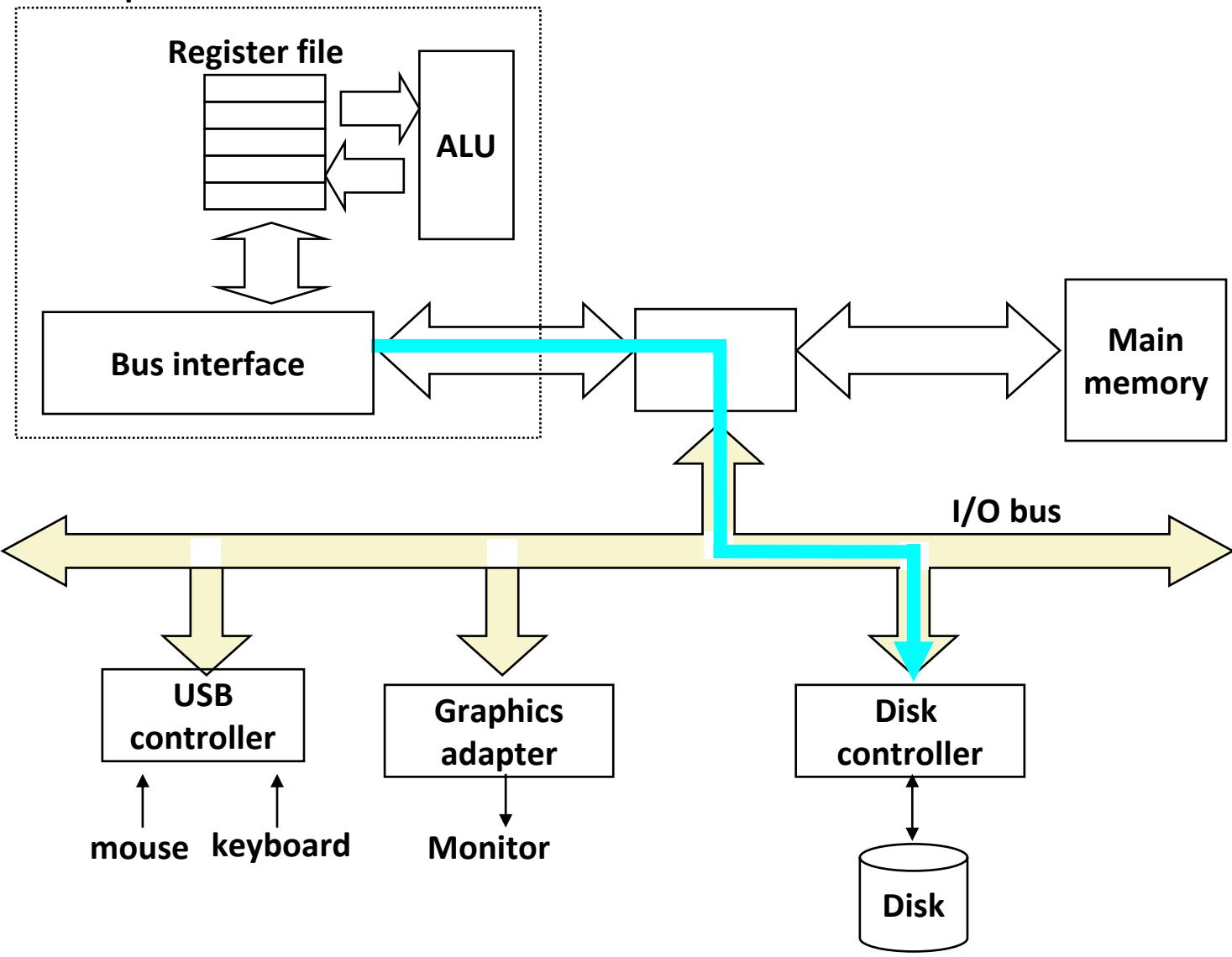
Rotational
latency

Data transfer

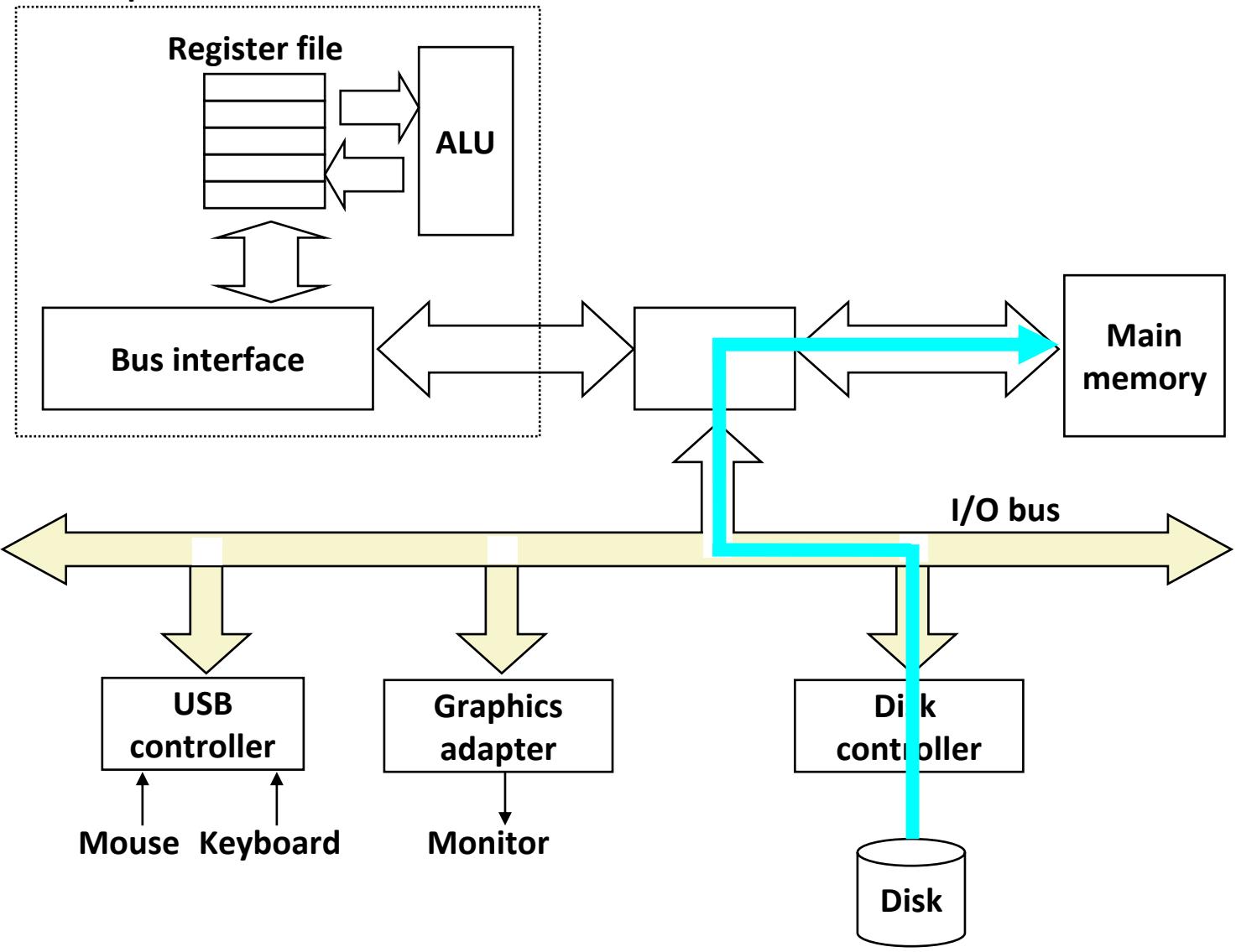
CPU chip



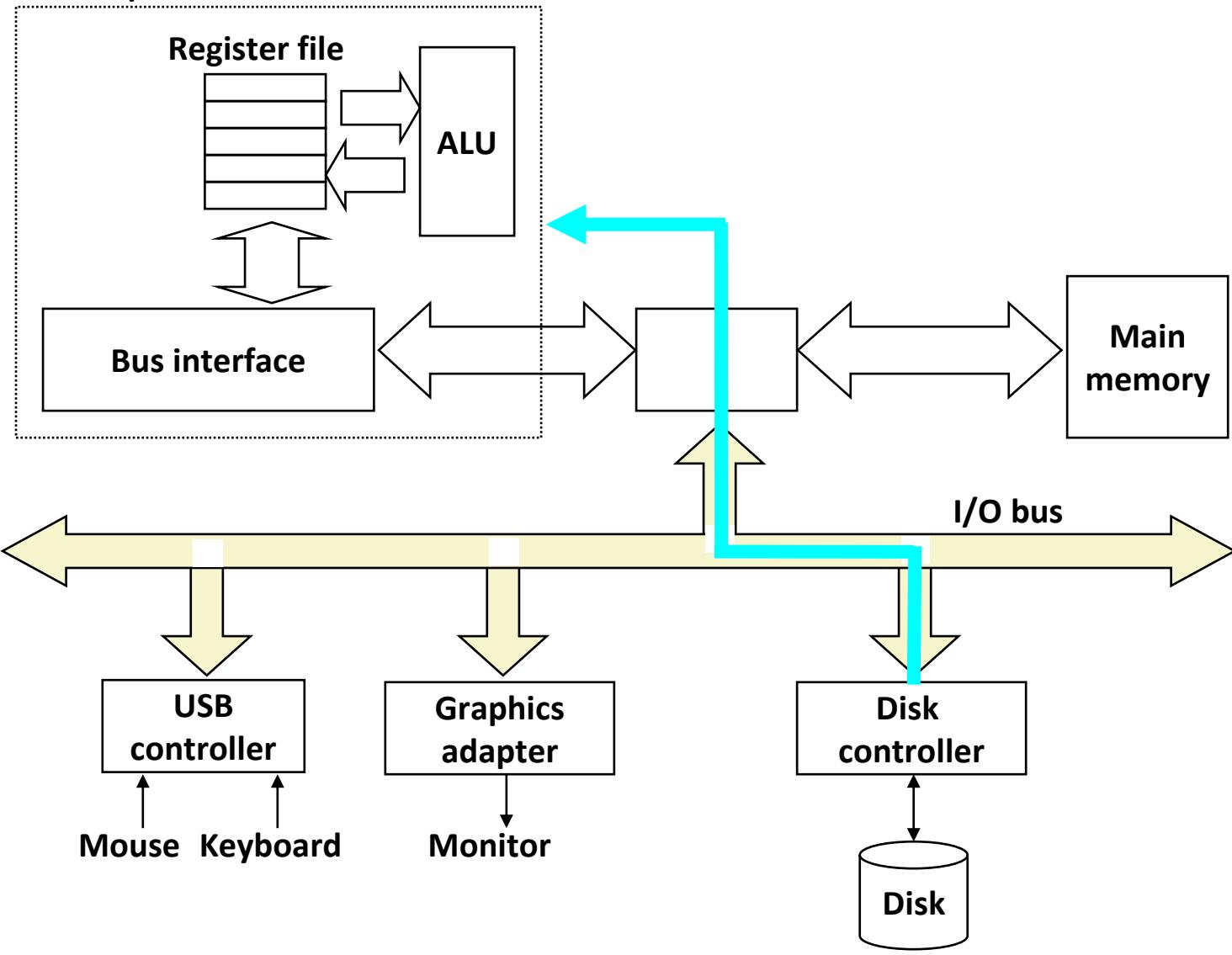
CPU chip

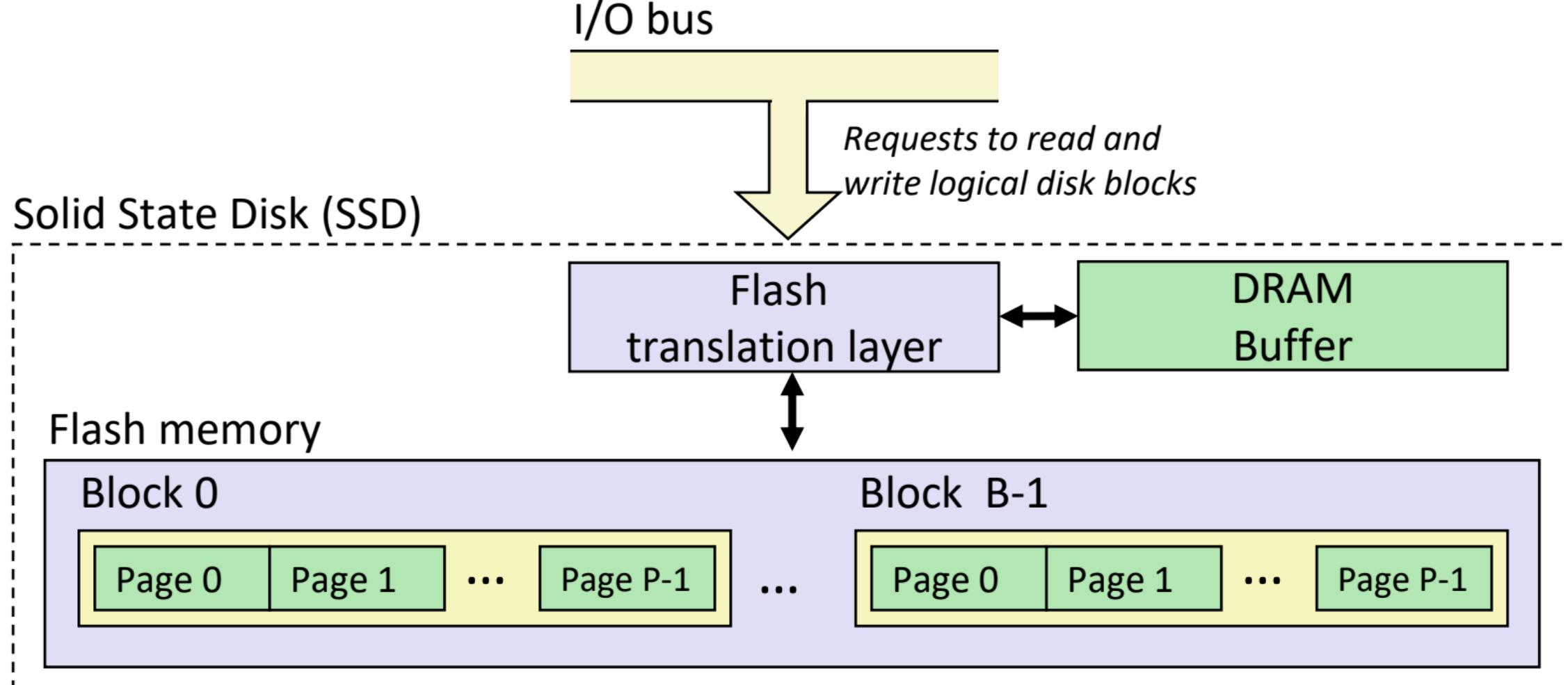


CPU chip

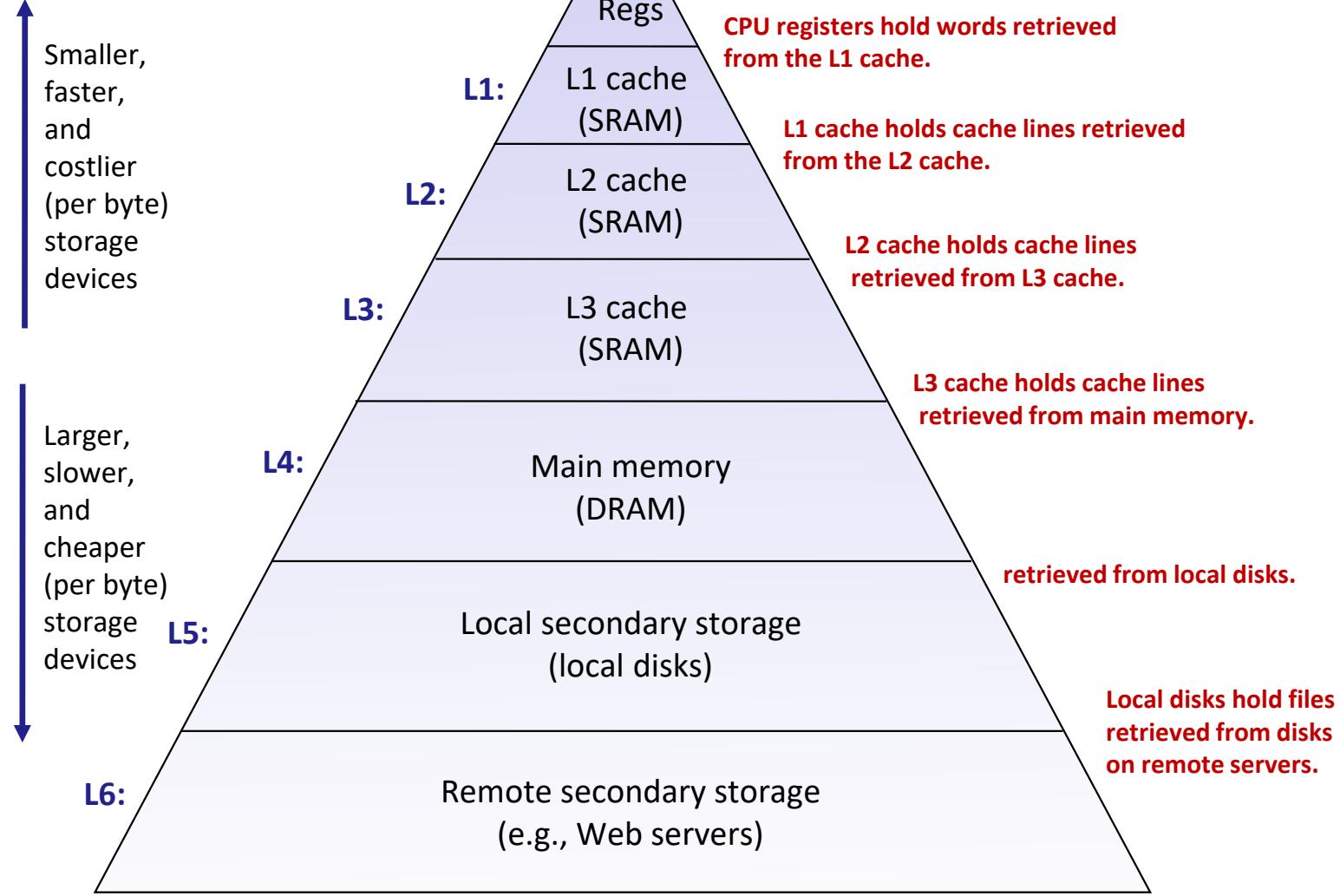


CPU chip

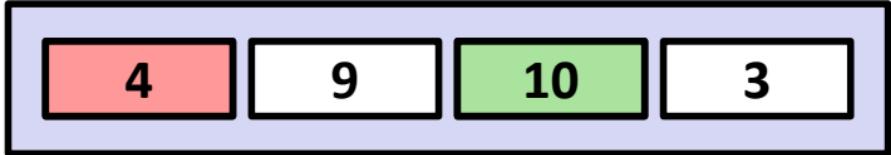




Example Memory Hierarchy



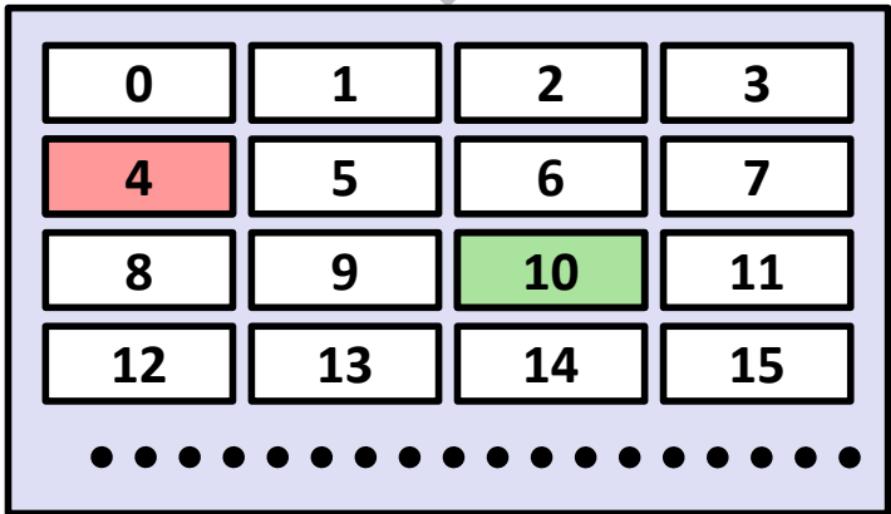
Cache



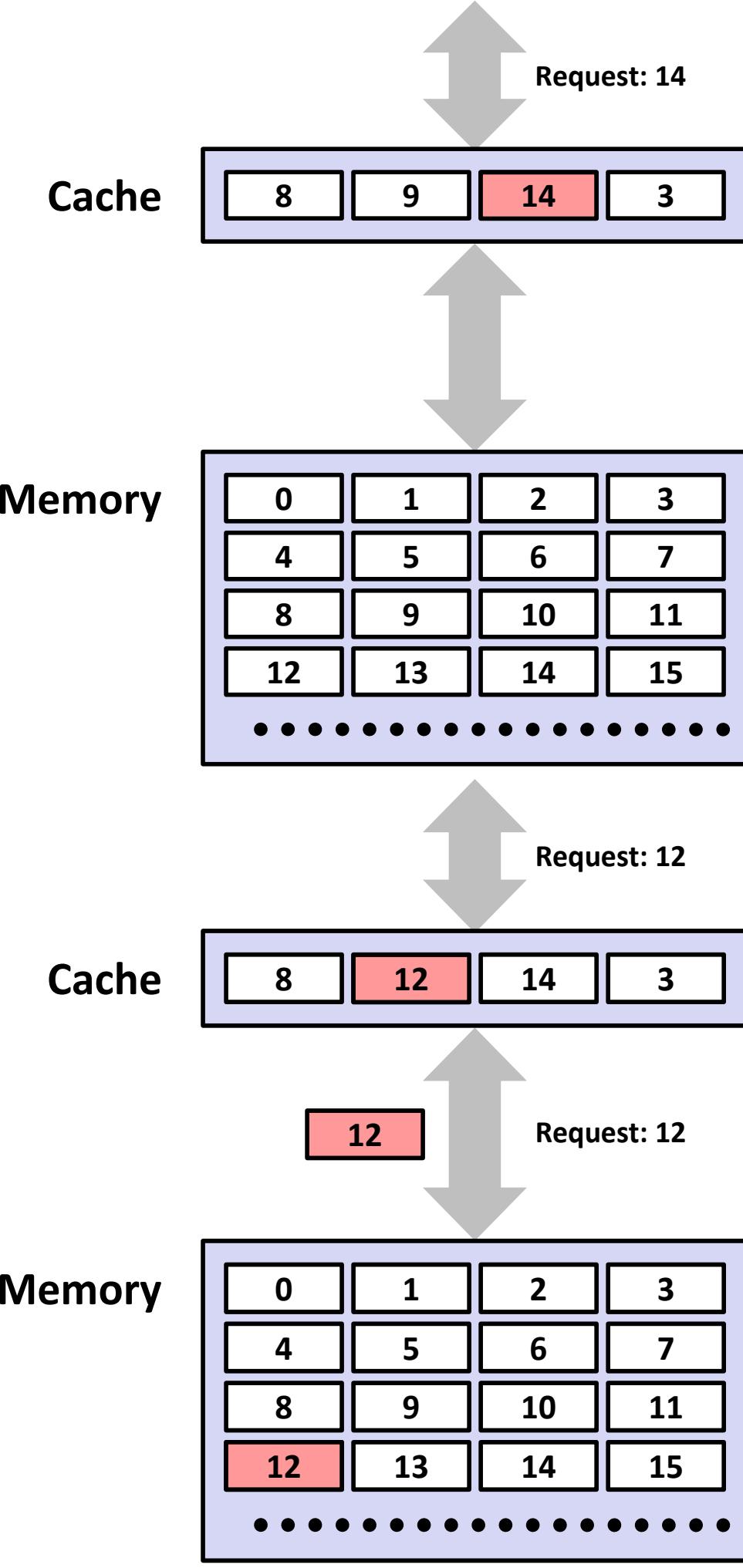
Smaller, faster, more expensive memory caches a subset of the blocks



Memory



Larger, slower, cheaper memory viewed as partitioned into “blocks”



Data in block b is needed

**Block b is in cache:
Hit!**

Data in block b is needed

**Block b is not in cache:
Miss!**

**Block b is fetched from
memory**

Block b is stored in cache

- **Placement policy:** determines where b goes
- **Replacement policy:** determines which block gets evicted (victim)