

# EE-67031-01 Lab 3 Report: Power Amplifier Design

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**Abstract**—A class A-B power amplifier design process is covered in this lab. We aim to design PA operates at 2.4 GHz and achieves 10 W of output power and > 20dB of gain. However, the fabricated PCB board had frequency shifted by 700MHz. The performance of the simulation and fabricated circuit are compared.

## I. INTRODUCTION

The power amplifier (PA) is an important part of the wireless communication system. In the pre-stage circuits of the transmitter, the signal power generated by the modulation circuit is very small, and it needs to go through a series of amplification to obtain sufficient power to transmit a far distance before feeding to the antenna. For wireless transmissions like FM broadcasting, antennas require input signals at thousands of kilowatts of power. In order to obtain sufficient output power, the power amplifier needs to be used in the transmitter. In this lab, we learn about power amplifiers in detail.

The commonly used power amplifiers are classified as A, B, or AB based on their conduction angles. In the class A amplifier, the entire input waveform is used in the amplification process. The electronic component used for amplifying is in use all the time even if there is no input signal. The advantage of this type of amplifier is that it cannot abruptly run out of output current. This generates a lot of heat and reduces the efficiency of class A amplifiers to theoretically 50%. Class B amplifier amplifies half of the waveform so the active device conducts for half ( $180^\circ$ ) of the waveform. The efficiency of class B amplifiers is improved a lot compared with class A amplifiers, theoretically, it can reach about 75% efficiency. The class AB amplifiers' efficiency is between class A and class B. It is a compromise between Class A and Class B configurations. It combines high frequency response like in class A amplifiers and good efficiency as in class B amplifiers.

## II. DESIGN PROCESS

In this lab, we aim to design an amplifier target at 2.4 GHz, narrow bandwidth, and output power larger than 10 watts. Gain is larger than 10 dB, and return loss at 2.4 GHz is smaller than -15 dB. However, the fabricated PCB board has a frequency shift to 1.7GHz. In 1.7GHz the gain is around 14 dB, but at 2.4 GHz the gain is around 7dB. The schematic of the circuit is shown in Fig 1. The PCB picture is shown in Fig 2

### A. Transistor and Bias Point

The transistor we use is CGH40010F, which is a gallium nitride (GaN) high electron mobility transistor (HEMT) that

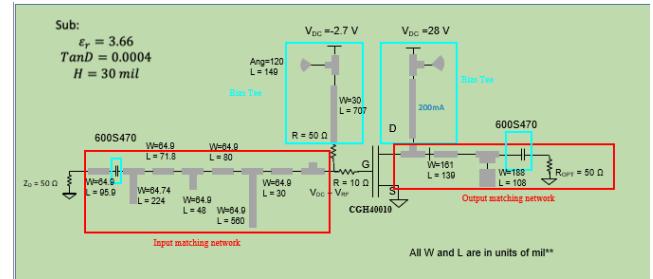


Fig. 1. Schematic of the circuit

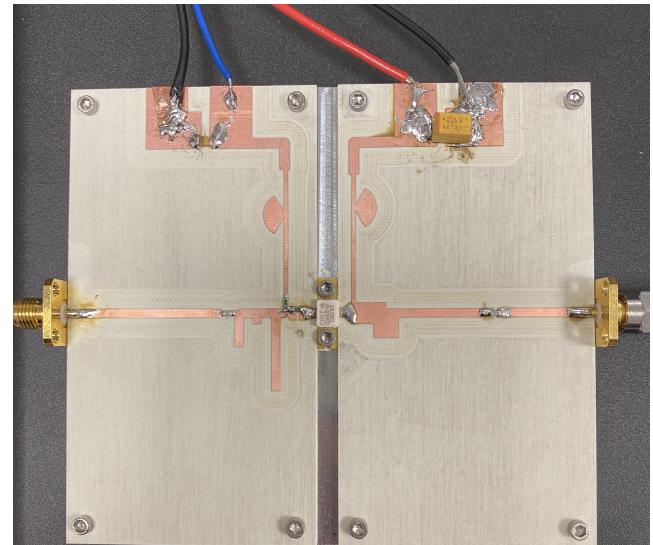


Fig. 2. Circuit picture

can operate from DC to 6 GHz with 10 W output power. We choose the gate quiescent voltage at  $V_{GS} = -2.7V$  and the condition in the data sheet shows the gate voltage  $V_{DS} = 28V$  and the drain current at  $I_{DS} = 200mA$ . The IV curves with load line are shown in Fig 3. The Voltage is chosen based on the load line. The knee voltage is decided by the transistor itself. We want the transistor works at class AB, then we need to choose the points from the middle of the load line (class A) to the bottom of the load line (class B).

$$\text{Efficiency} = \frac{P_{avg}}{P_{avg} + P_{diss}} \quad (1)$$

where the  $P_{avg} = \frac{1}{8}V_{pp}I_{pp}$ . If we keep the same quiescent voltage and move the current lower, the efficiency of the

amplifier increase as the current got rectified. To be more simplified, the less voltage and current overlap, the higher efficiency we can get.

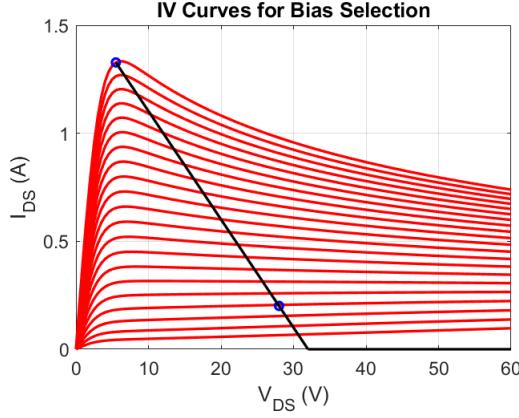


Fig. 3. IV Curves with Load Line

### B. Bias Tee

Bias tees are used to supply DC currents or voltages to bias RF circuits. A Bias tee is a three-port device. The structure of the device can be seen in figure 4. A signal that consists of RF + DC is incident at Port 1 of the Bias Tee. The capacitor blocks all DC signals from getting through to Port 2 and only allows the AC/RF signals to pass through. The inductor in the circuit blocks RF signals from getting through to Port 3 and allows all DC signals to get through. In my design, the bias tee

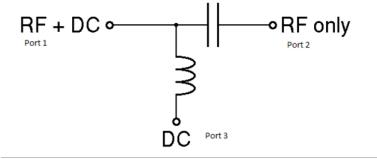


Fig. 4. Bias Tee Structure

schematic is shown in figure 1. The radial stub is used due to its simplicity, more compact than linear stubs, and wider band than linear stubs. The impedance of the radio stub is close to 0, after the quarter transmission line at 2.4GHz, the impedance at 2.4 GHz changed from short to open. The S-parameter of the Bias Tee circuit and harmonic are shown in figure 5. We can see that the  $S_{RF-DC}$  is close to 0 and  $S_{RF-input}$  is extremely low in the individual tuned result and relatively low using the parameters in the tuned overall circuit.

In the fabricated process, we added one  $50\Omega$  resistor in the Bias Tee transmission line to lower the magnitude of the potential input that may cause the oscillation. It will not affect the performance because there is no current at the gate. However, if we drive the transistor into the saturation region, it will start pulling current through the gate which will cause the bias voltage to shift around.

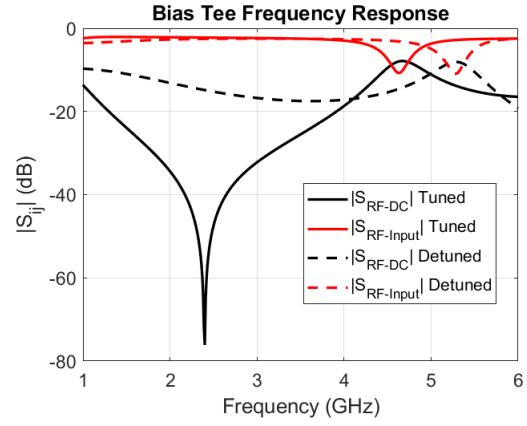


Fig. 5. Bias Tee Result: The dash line is the tuned parameters in the overall circuit, the solid line is Bias Tee individual tuned result

### C. Stability Analysis

To prevent the amplifier from self-oscillation, we need to stabilize the amplifier. A resistor is added around the transistor. Since placing the resistor at the output will suck up the gain we obtained, we will place it at the gate side. It will also weaken the input signal to lower the possibility of oscillation. We choose the transistor as an AB class amplifier, it will amplify the wave at an angle between  $180^\circ$  to  $360^\circ$ . Once the angle of amplification adds the angle of (output-ground-input) equal to  $360^\circ$  in phase shift, and the gain is greater than 1, it will trigger the oscillation. In ADS, it has the S-parameter network analyzer where each port has a separate ideal bias tee.

The  $\mu$  factor is

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta|} > 1 \quad (2)$$

where  $\Delta = S_{11}S_{22} - S_{12}S_{21}$ . The  $\mu$  factor means the distance from the center of the smith chart to the nearest output stability circle, if  $\mu > 1$ , then circuit is unconditionally stable, which means the circuit will remain stable for all passive loads.

After we added the resistor, we also need to pay attention of the circuit gain, to be more specific, how much gain has dropped due to the resistor. According to the simulation, the maximum gain it can achieve at 2.4 GHz is 13.6 dB.

In the Fig 6, we can see that  $\mu > 1$  from 1 GHz to 6 GHz, and the stability factor is greater than 1 too. From the figure, we can see that the  $S_{21}$  (gain) decrease as the stability factor increase till 5 GHz.

If we match the circuit perfectly, according to Fig 7 the  $S_{11}$  we can get is low enough at 2.4 GHz and the gain is around 13 dB.

In the lab, we measured the oscillation that happened at 750MHz as shown in Fig 8. It matched our theory because, in the low frequency, it has a longer wavelength, which may more easily reach  $360^\circ$  in phase shift. If we have more time, we can add a capacitor in front of the gate, and it will further help with the stability.

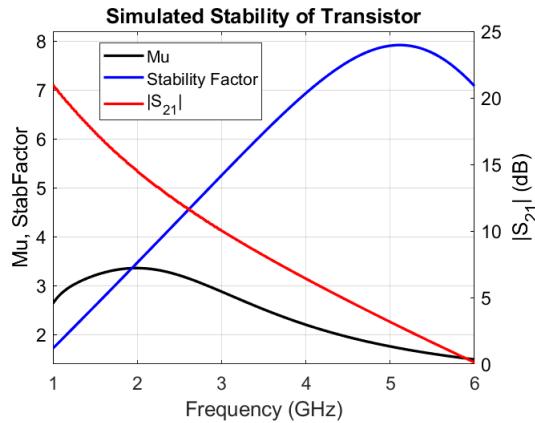


Fig. 6. Simulated Stability

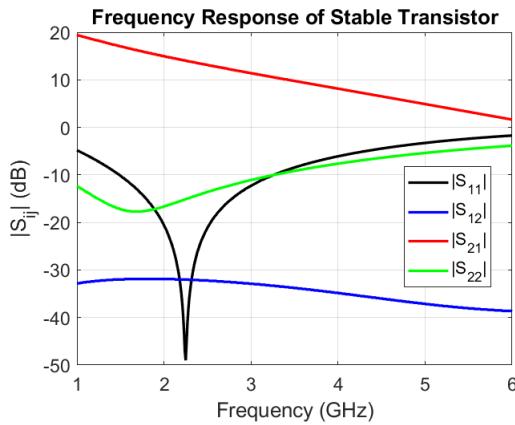


Fig. 7. Stability S Parameter

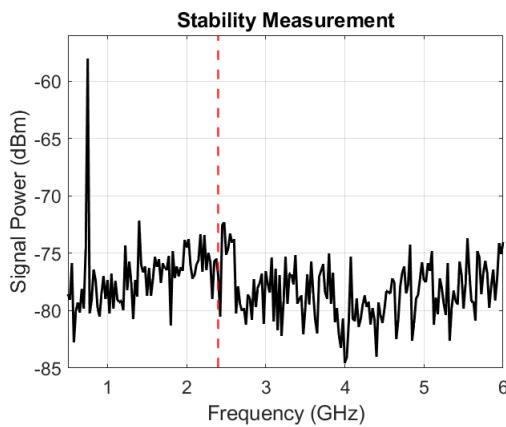


Fig. 8. Oscillation happened at 750MHz

#### D. Load Pull Analysis

Before we move to the matching analysis, we need to know the input impedance and output impedance of the transistor. In the datasheet, it says at 2.5GHz, the input impedance is  $3.19 - j4.76$  and the output impedance is  $19 + j9.2$ . To find a more accurate value, we use the load pull instrument in the ADS to get the input and output simulation impedance. With the stability resistor in the circuit, the simulated input impedance is around  $11.2 + j4.8$  and the output impedance is around  $19.2 + j18.2$ , where the circuit can achieve the highest power added efficiency (PAE).

PAE of an amplifier is the ratio of the effective output power and the DC input power. The effective output power is measured by calculating the difference between the output power and input power, which take into account the gain of the amplifier.

#### E. Matching Network

Based on the load pull analysis we did in the last part, we did the matching network according to the input/ output impedance. We used the conjugate match in the input matching network, because by using conjugate matching, it is possible to achieve maximum power transfer. The input and output matching network is shown in 1. The transmission lines are used in the matching network for it's easy fabrication. However, the transmission line matching network has the disadvantage of narrow bandwidth. To solve that problem, I used multi-stages transmission line with  $Q = 1$  arc to get a relatively wide bandwidth. The input matching network S-parameters is shown in the Fig 9. In order to have a better overall performance, we detuned it afterward. However, the detuned parameters of input matching network performance suit for the overall performance instead of the individual input matching network.

In the output matching network is simple impedance match from the output resistance to  $50\Omega$  and it has relatively small influence on the overall connected circuit compared with the input matching network.

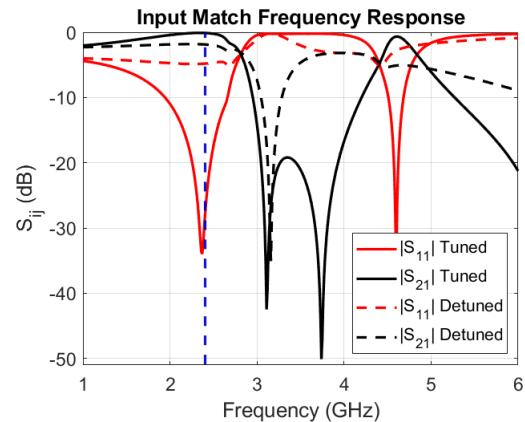


Fig. 9. Input Match Frequency Response

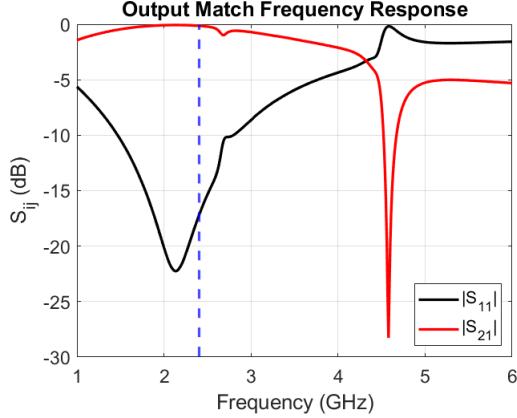


Fig. 10. Output Match Frequency Response

#### F. Overall Performance-Linear S-parameter

Combine the input matching network and output matching network together and tuned again, we have our overall performance analysis.

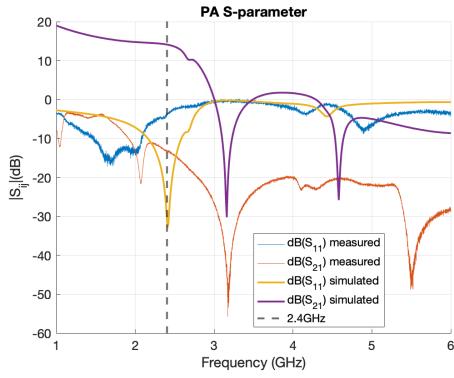


Fig. 11. Overall Performance- Linear S-parameter

In the simulation, we noticed that the simulated  $S_{21}$  remain in the high gain even the  $S_{11}$  is relatively high. That is reasonable because the amplifier's DC power gain is sufficient enough to overcome the loss.

The simulated and measured  $S_{21}$  are similar. When we add the 20 dB on the  $S_{21}$  due to the attenuator, we get the  $S_{21}$  in the same trend.

But there is a large discrepancy between the simulated and measured  $S_{11}$  parameter. There are several reasons that might cause such change. The substrate around transmission line on the PCB board is over milled to make sure there is no copper connected, which will cost the effective dielectric constant going down. After the simulation in the ADC, when we turned down the effective dielectric constant, the  $S_{11}$  parameter moved to lower frequency, which explain the frequency shift. In my opinion, the change of effective dielectric constant will not cause the  $S_{11}$  shifted from 2.4GHz to 1.7GHz. Another reason might be the simulated transistor package is not accurate enough so there is a mismatch between

the input matching network and the input impedance of the transistor. Also the transmission lines have fringing fields that can alter the electrical length of the lines, which will cause the frequency shift of the matching network. The parasitic effect from soldering and lumped components package are also part of the source that cause such frequency shift.

In the measurement, we can achieve 14 dB gain at 1.7GHz.

#### G. Nonlinear Analysis

In the nonlinear measurement, according to our simulation, the IP1dB is around 30 dBm shown in Fig 13. However, the signal generator cannot reach that high power, so we need another driver amplifier to help us reach the high power input. In this case, we also need to know the drive amplifier's Pin-Pout curve so we know the power output of the drive amplifier. As shown in Fig 12, the IP1dB is at 2dB and OP1dB is 26 dB. The driver amplifier provides 24.6 dB gain at 2.4 GHz.

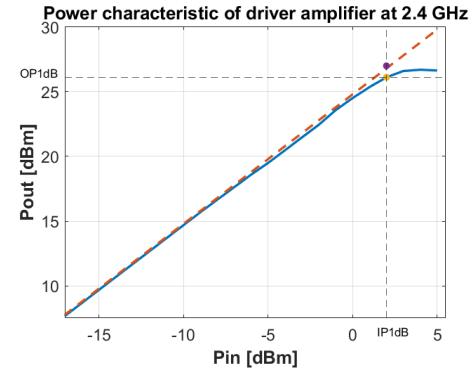


Fig. 12. Drive amplifier Pin-Pout Curve

To protect depletion transistor, gate voltage should be less than the minimum of gate threshold voltage in the datasheet which is  $-3.8V$ .

In the measurement, we didn't get IP1dB around 30 dBm instead at 23.6 dBm and OP1dB is at 26.5dB. One of the reason is because we have oscillation happened at 750 MHz, and the measurement is measured the signal peak at 2.4 GHz, so the power input is not actually power input. The total power input should combine the oscillation input power. The gain of the amplifier is 5.4 dB after taking out the cable loss, drive amplifier's gain, and adding back attenuation, which is lower than the  $S_{21}$  value (7 dB) at 2.4 GHz. The differences might caused by the extra loss of connectors or wires. The IP3 value is calculated by conducting two tone test. In the two tone test, we set the bandwidth to be 100 MHz. The result is shown in Fig 15. The  $IP3 = 35.5dB$ , and  $OIP3 = 33.19dB$ .

### III. CONCLUSION

In this lab, we want to design an amplifier works at 2.4GHz and achieve gain higher than 10 dB. We did the whole PA design simulation. The simulation result is perfect at 2.4 GHz. But the milled PCB circuit frequency shifted to 1.7GHz. I did realize that there are a lot of detail we need to pay attention in the fabrication process. Even though we put two big capacitor

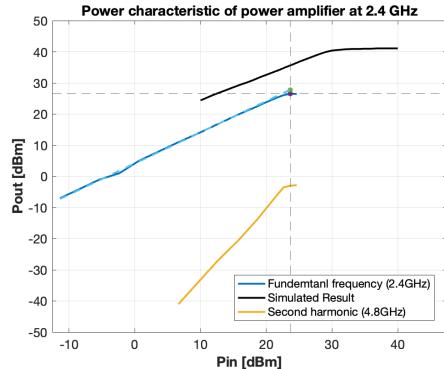


Fig. 13. P1dB

between ground and the circuit, the oscillation still happened. For the next stage, to solve the oscillation problem, putting an capacitor parallel with the stability resistor maybe helpful, due to the DC signal cannot pass the capacitor and RF can pass. To solve the frequency shift problem, we need to do a more accurate EM simulation. Extracting the s2p file of the transistor if we can, for us to get a more accurate load pull file. In another way, we can design the circuit in a higher frequency.

In the Gain measurement step, we should conduct our experiment at 1.7 GHz instead of 2.4 GHz because we have about 14dB gain at 1.7GHz.

As for safety using instruments, I need to slow down in the lab. In the PA measuring process, to protect the sensitive transistor, the current should be limited and no sudden change. In that case, the safety precaution, setting power supply, is important.

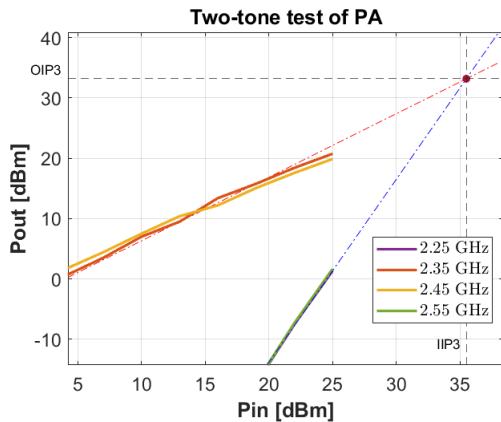


Fig. 14. Harmonic output power and nonlinear intercept points

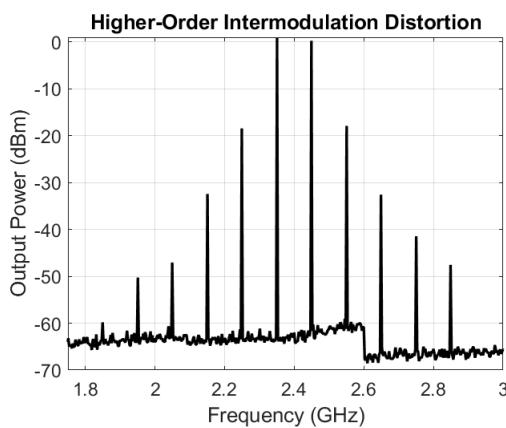


Fig. 15. Intermodulation products resulting from a two-tone input at 2.35GHz and 2.45GHz