			_																							
Audio	Prop	lative	SPIO	vudio	exIO	XDar 12C	CAN	SPI	Serial	Analog	PWM	Digital		Digital	PWM	nalog	Serial	SPI	CAN	o ar	lexiO	oibn	SPIO	Native	Prop	Audio
G	GND	Ž	<u>O</u>	₹	<u> </u>	< □	Ú	<u> </u>	σ	₹	Ē	GND	O 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Ē	₹	Й	<u></u>	O S	Y X	<u>II.</u>	₹	<u>o</u>	Z	5V	
<u> </u>		AD B0 03	1.3		1	17	RX2	CS1	RX1		1X1	0	- m	GNE)										G	G
		AD_B0_02			1	16		MISO1			1X0	1	0=0 3v		250mA m	ax									3V	3.3
	S	EMC_04	4.4	O2 1	1:4	6					4A2	2	5V = 5	23	4A1	A9			RX1		3:9	MCL1	1.25	AD_B1_09	CSI_D8	Α
М		EMC_05	4.5	LR2	1:5	7					4B2	3		22	4A0	A8			TX1		3:08		1.24	AD_B1_08	CSI_D9	-
Α		EMC_06	4.6	BCL2 1	1:6	8					2A0	4		21		A7	RX5				3:11	BCL1	1.27	AD_B1_11	CSI_D6	Α
Α	A-EN	EMC_08	4.8	IN2	1:8 1	17					2A1	5	2 W 111 0 0 0 0	20		A6	TX5				3:10	LRC1	1.26	AD_B1_10	CSI_D7	Α
	M-CS	B0_10	2.10	O1D 2	<u>!:10</u>						2A2, Q41	6	6 m : 11 F " " 6	19	Q30	A5	CTS3		SC	CLO	3:00		1.16	AD_B1_00	S	С
	L-EN	B1_01	2.17	O1A 2:17	7, 3:17 1	15			RX2		1B3	7	~ [] *	18	Q31	A4			SE	A0	3:01		1.17	AD_B1_01	S	С
		B1_00	2.16	IN1 2:16	6, 3:16	sda0)		TX2		1A3	8		17		A3	TX4		SE	A1	3:06		1.22	AD_B1_06	CSI_VSYNC	
		B0_11	2.11	O1C 2	1:11						2B2,Q42	9	O' >	16		A2	RX4		SC	L1	3:07		1.23	AD_B1_07	CSI_HSYNC	
S		B0_00	2.0	MQR 2:0	0			CS0			Q10	10	MIMXRT1052 DVJ6A	15	Q33	A1	RX3				3:03	SPDI		AD_B1_03		V
SM	M/L	B0_02	2.2		2:2		TX1	MOSI0			Q12	11	0N00X CTAB1912J	14	Q32	A0	TX3				3:02	SPDO	1.18	AD_B1_02		
SM	М	B0_01	2.1	MQL 2:	1			MISO0			Q11	12		13	Q20	LED		SCK0	rx1		2:03		2.3	B0_03	М	SM
												3.3V		GNE								_				
		AD_B0_12				SCL2				A10-1	1X2	24			GPT2-1	A17					3:5			AD_B1_05	CSI_MCLK	
		AD_B0_13				SDA2	2		RX6	A11-1	1X3	25		40	GPT2-2	A16					3:4			AD_B1_04	CSI_PIXCLK	
	CSI_D3	AD_B1_14			:14			MOSI1		A12-2		26		39		A15-2		MISO1			3:13			AD_B1_13	CSI_D4	
	CSI_D2	AD_B1_15		3	:15			SCK1		A13-2		27		38		A14-2		CS1-0			3:12			AD_B1_12	CSI_D5	
		EMC_32							RX7		3B1	28	Prog Prog Bat	37	2B3			CS0-1		17	2:19,3:19		2.19	B1_03		
		EMC_31 EMC_37	4.31 3.23			20	DVO		TX7		3A1	29		36 35	2A3		TVO	CS0-2		16	2:18,3:18		2.18	B1_02	CSI PIXCLK	
					2	23	RX3				G13	30					TX8		DV4		2:28,3:28		2.28	B1_12		_
		EMC_36 B0 12	3.22	O1B 2	2:12 1	22	TX3				G12	31		34	2B0		RX8		TX1	0	2:29,3:29	MCL2	2.29 4.7	B1_13 EMC_07	CSI_VSYNC	
		BU_12	2.12	OIB 2	.12	10						32		<u>J</u> 33	200				IAI	9	1.7	IVICL2	4.7	EIVIC_07		
													SDIO Pins													
		SD_B0_03		DATA		7		MISO2			1B1	42			1A2		TX5			8	DATA2			SD_B0_04		
		SD_B0_02	3.14	DATA	A0	6		MOSI2	CTS5		1A1	43 GND			1B2 1A0		RX5	SCK2	SC	L1 4	DATA3			SD_B0_05 SD_B0_00		
_		SD_B0_01	3.13	CLK		5 SDA1	1	CS2			1B0	44		10	1710	3.3V		JUNE			CINID		J.IL	05_50_00		
													Back Memory Chips													
F														GNE												
	2A_D0	EMC_26	4.26		1:12				RX1		1B1	52		GINL							_	_				
_	2A_SCLK	EMC_25	4.25						RX1 TX1		1A1	52 53		50	1B2		CTS8				1:14	_			F2A_D2	
					1:12							53 54	≡. ≡	50	1B2 1A2		CTS8	MOSI2 SCK2			1:14 1:13	,	4.27	EMC_27	F2A_D1	
_	2A_SCLK	EMC_25	4.25								1A1	53	<u>اليا</u>	50	1B2		CTS8		SC	L1		,	4.27	EMC_27		
F	2A_SCLK 2A_D3	EMC_25 EMC_29	4.25 4.29		1:15			MISO2	TX1		1A1 3A0	53 54 3.3V		50	1B2 1A2 3B3,Q23		CTS8		SC	L1		,	4.27	EMC_27	F2A_D1	
F	2A_SCLK 2A_D3 2A_D0	EMC_25 EMC_29	4.25 4.29 4.26					MISO2	TX1		1A1	53 54 3.3V		50 49 51 GNI	1B2 1A2 3B3,Q23			SCK2	SC	L1	1:13		4.27 4.22	EMC_27 EMC_22	F2A_D1 F2A_SS1_B	E
F	2A_SCLK 2A_D3	EMC_25 EMC_29	4.25 4.29		1:15			MISO2	TX1		1A1 3A0 1B1	53 54 3.3V		50 49 51	1B2 1A2 3B3,Q23		CTS8		SC	L1			4.27 4.22 4.28	EMC_27 EMC_22 EMC_22	F2A_D1	E