Reverberation Module Test Report

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1 Bugs Found

— The **err_** signal was found to be incorrectly implemented. It does not assert (**1'b0**) when **prgrm_go** prematurely deasserts in the middle of programming. This was caught by a directed test in the *Testing err_ signal* section of the testbench. During programming of delay line 0, **prgrm_go_** was deasserted, which should have triggered the error signal, but it did not and the assertion caught it.

— The **err_** also does not trigger when the control block is programmed with Read Mode (**prgrm_in[0] == 1'b1**). This was caught by another assertion.
FIX : In line **68** of **/DAR/design/delay_prgrm.v**, assign **nxt_err** to the **err_** flop :
`always @(posedge clk) err_ <= (!rst)? 1'b1: nxt_err_;`

2 Assumptions

— Programming the tap for a single delay line takes 7 cycles - 6 for programming and 1 more cycle for the tap register to acquire its new value.

3 Execution Instructions

No additional files were created for the testbench. All of the tests and assertions are written in the **audio_app.test_top.sv** file. To compile the design and the testbench, **>cd** into the DAR directory and then execute the command **>make all**. To run the simulation use either **>make run** or **>./simv**. In order to pull up the VPD, please use **>make dve**