Reverberation Module Testplan

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1. Reset Functionality
   (a) Need to exercise reset signal and check whether the expected outcome is what actually occurs
      - Shift in same 16-bit value into all 4 Delay Lines for 8-cycles. This will ensure all 8 registers within each queue have a non-zero value. Then, assert **`rst_`**. The outputs from all delay lines should be zero.
      - Visually inspect in DVE that all 8 registers have been reset to zero.
2. Delay Line and Delay amount
   (a) The Delay Line selection must function correctly (correct delay line must be selected during programming):

   prgrm_in[3:2] = 2'b10 $\Rightarrow$ Delay Line 2 selected

   (b) Need to ensure that the actual delay in each line at the output matches the programmed delay
      - Program different delay values into each delay line and make sure that the outputs from each line match their corresponding delays
      - Program each line with random delays and check to make sure the output appears after the correct number of cycles
3. Reprogramming Delay Tap
   (a) Ensure reprogramming of the tap is executed correctly (tap switch from initial position to new position at the end of programming)
   (b) Ensure no more than a maximum of 7 words of data are lost due to reprogramming tap from 7 units of delay to 0 units of delay
   (c) Ensure no more than 7 words of data are repeated when reprogramming tap from 0 units of delay to 7 units of delay
   (d) Reprogram tap to some intermediate value and check the output to make sure it is delayed by the correct amount
   (e) Reprogram the tap, but maintain the same delay value to make sure it doesn't move
4. Error Signal Testing
   (a) Ensure correct functionality of error signal using assertions:
      - **`err_`** must be asserted if **`prgrm_go_`** de-asserts before **`prgrm_in`** completes programming the Host
      - **`err_`** must be asserted if **`prgrm_in[0] == 1'b1`** since read mode is not supported by module
      - **`err_`** should only be asserted for one cycle