Question #1

Problems

아래 링크된 데이터시트와 오른쪽 그래프를 참고하여 25℃ & *TYP* 조건에서 다음 빈칸(?)을 채우시오

Datasheet download : alldatasheet.com → RURG3020CC search
https://pdf1.alldatasheet.com/datasheet-pdf/view/54465/FAIRCHILD/RURG3020CC.html

Forward Voltage at	?
Resistance at	?
Parasitic Inductance	20[nH](Package)
Parallel Capacitance	0
Forward Current	?
Peak Reverse Current	?
Current Slope	100e6
Reverse Recovery Time	?

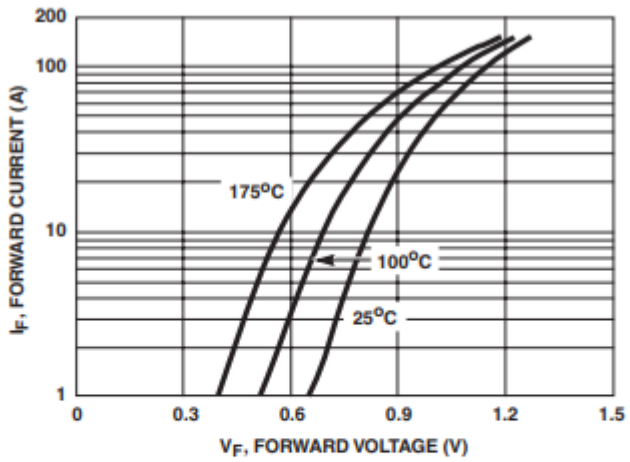
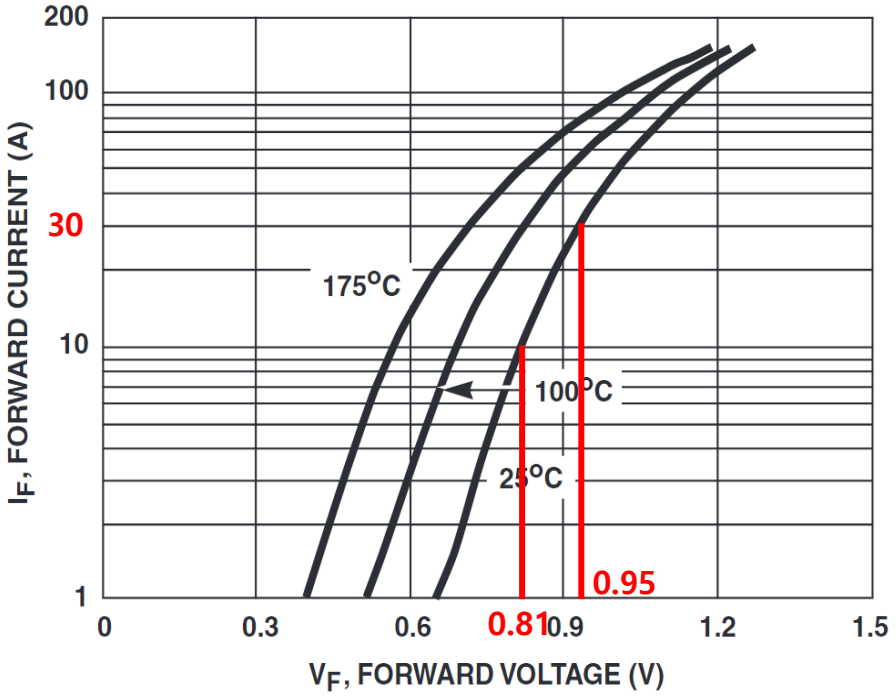


FIGURE 1. FORWARD CURRENT vs FORWARD VOLTAGE



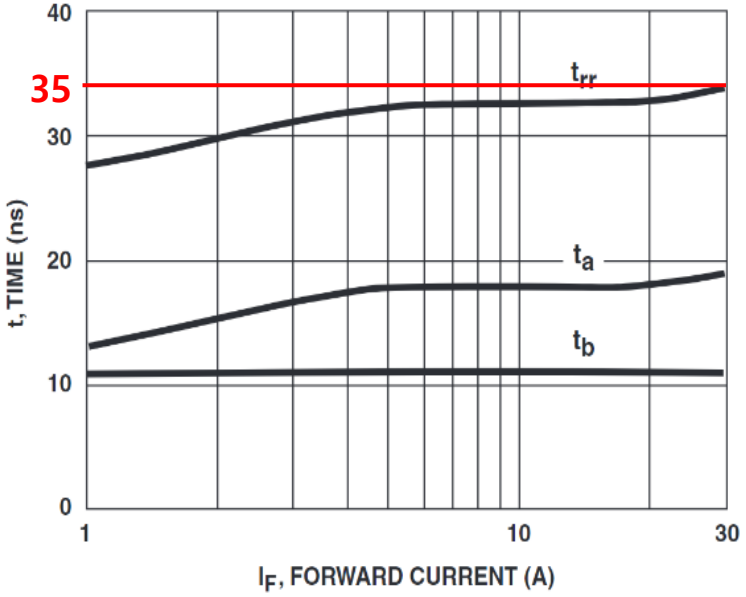


FIGURE 3. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

$$R = \frac{\Delta V}{\Delta I} = \frac{0.95 - 0.81}{30 - 10} = 0.007$$

$$t_a * Current\ Slope$$
$$= Peak\ Reverse\ Current$$
$$= 20 * 10^{-9} * 100 * 10^{6}$$

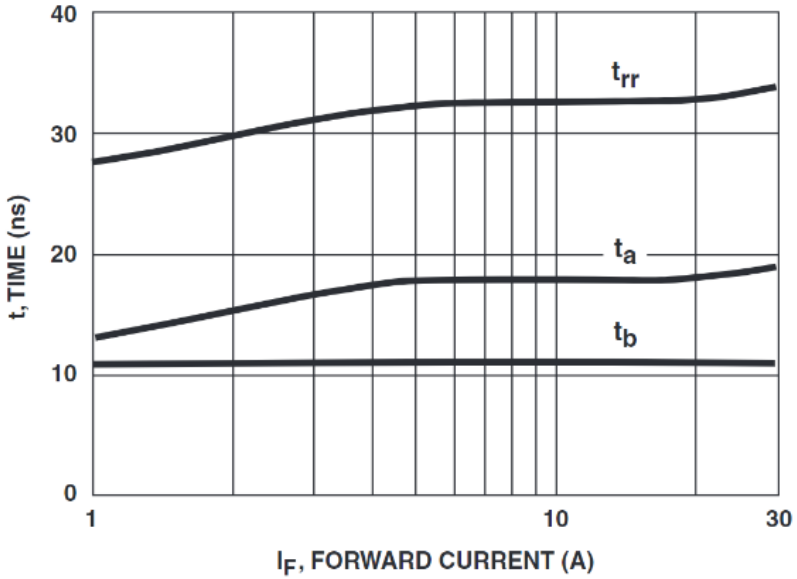


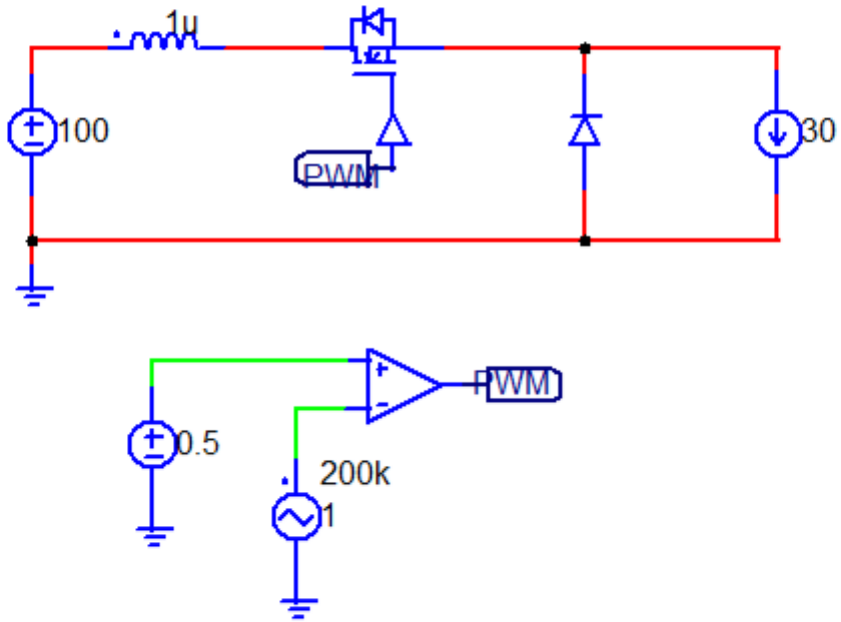
FIGURE 3. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

Forward Voltage at	$0.95\ [V]$
Resistance at	$0.007\ \Omega$
Parasitic Inductance	$20[nH](package)$
Parallel Capacitance	0
Forward Current	$30\ [A]$
Peak Reverse Current	2
Current Slope	$100 * 10^{6}$
Reverse Recovery Time	$35[ns]$

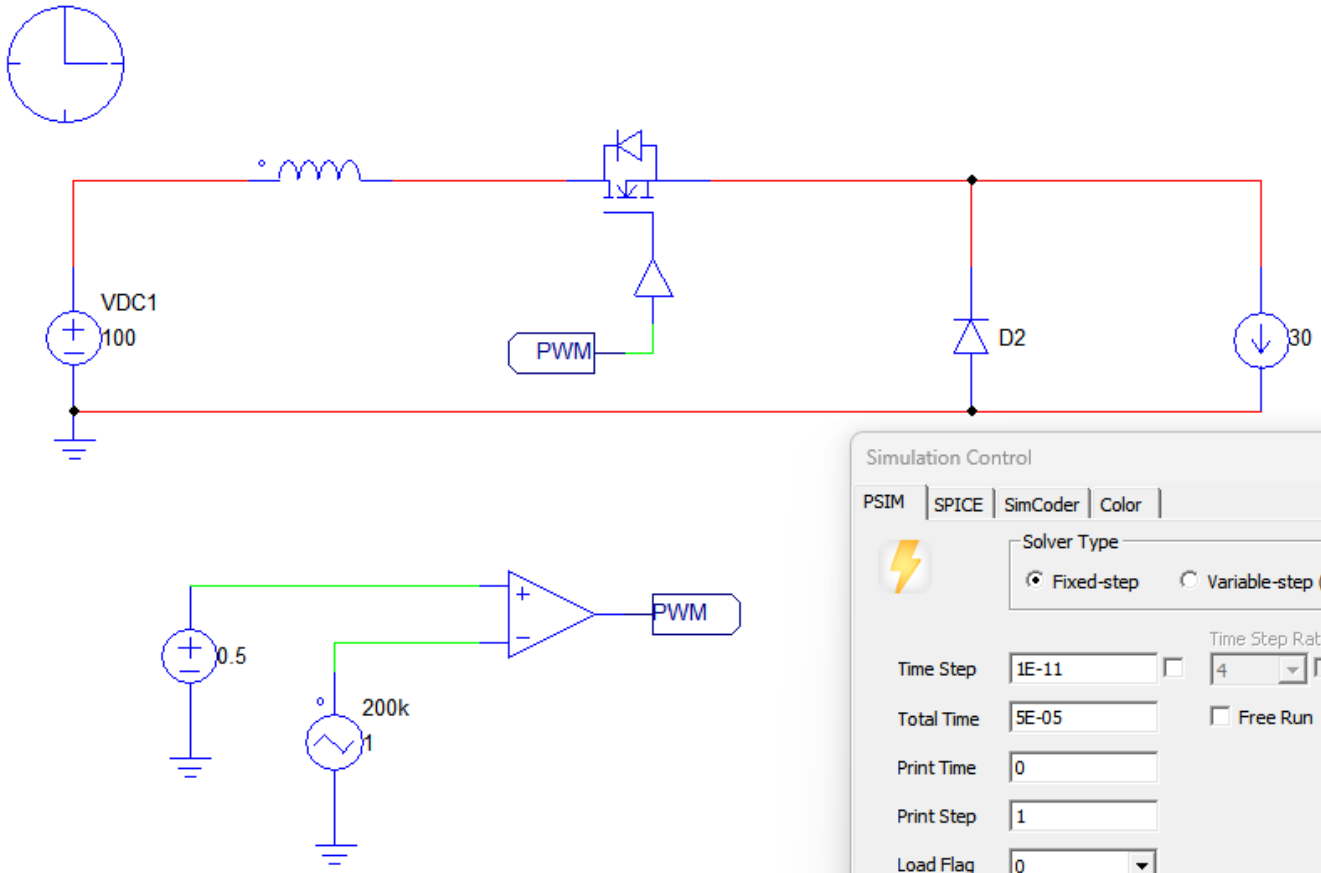
Question #2

Problems

Question #1에서 작성된 표와 PSIM Simulation을 통해 Reverse Recovery Time (t_{rr}) 확인하기!



Question#2 PSIM Simulation



Simulation Control

PSIM | SPICE | SimCoder | Color

Solver Type: Fixed-step / Variable-step (dual) — Help

		Time Step Ratio	Smaller Time Step
Time Step	1E-11	4	2.5e-12
Total Time	5E-05	Free Run	
Print Time	0		
Print Step	1		
Load Flag	0		
Save Flag	0		

Engine Default Values

R_switch_on	1E-05
R_switch_off	1E+007

Triangular : VTRI1

Parameters | Color

Triangular-wave voltage source — Help

		Display
Name	VTRI1	
V_peak_to_peak	1	✓
Frequency	200k	✓
Duty Cycle	1	
DC Offset	0	
Tstart	0	
Phase Delay	0	

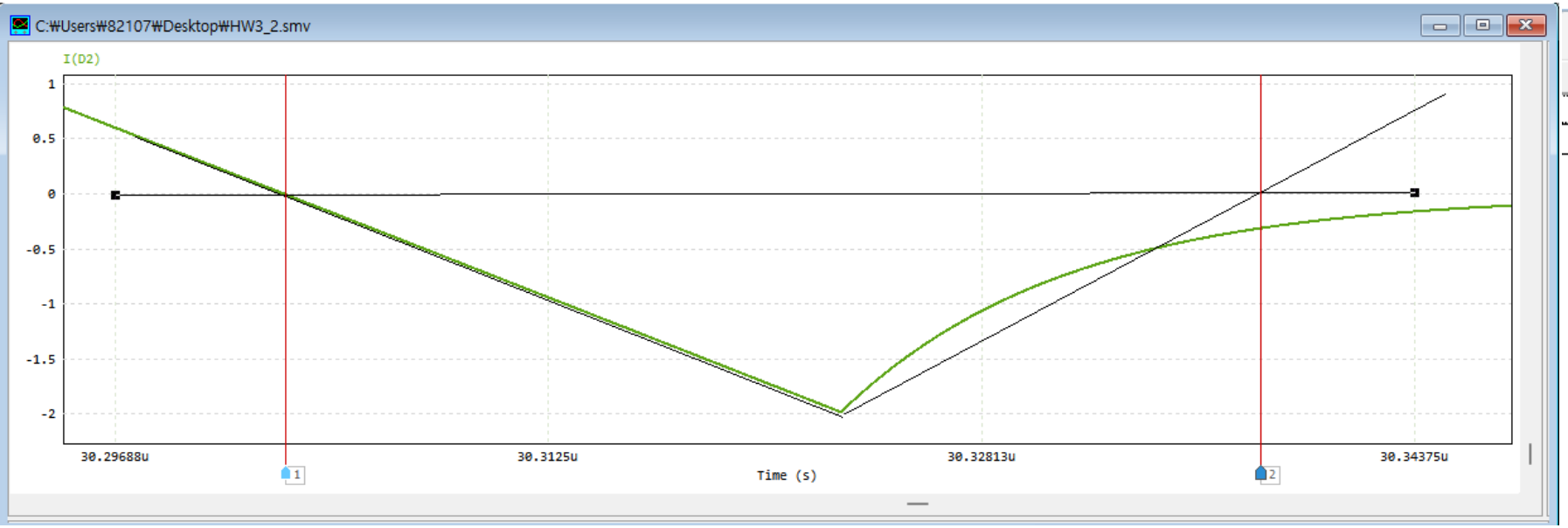
30[uSec] 부분에서의 t_{rr}측정

Measure

	X1	X2	Δ
Time	3.03230e-05	3.03343e-05	1.12600e-08
I(D2)	-1.97734e+00	-4.93506e-01	1.48384e+00

$$0.25 * I_{rm} = 0.25 * -1.97734 = -0.494335[A]$$

0.25xI_{rm}과 I_{rm}을 이으면 그래프는 다음과 같다.



Measure

	X1	X2	Δ
Time	3.03030e-05	3.03382e-05	3.51639e-08
I(D2)	2.33862e-03	-3.06551e-01	-3.08890e-01

t_{rr}은 다음과 같이 35.16[ns]으로

35[ns]와 비슷한 값이 나온다는 것을 알 수 있다.

Question #3

Problems

아래 링크된 데이터시트를 참고하여 다음 빈칸을 채우시오

Datasheet download : alldatasheet.com → IRF830 search
https://pdf1.alldatasheet.com/datasheet-pdf/view/17803/PHILIPS/IRF830.html

Vbreakdown(drain-source)_MAX.	?
On Resistance_TYP.	?
Threshold Voltage VGS(th)_TYP.	?
Transconductance_TYP.	?
Capacitance Cgs_TYP.	?
Capacitance Cgd_TYP.	?
Capacitance Cds_TYP.	?
Diode Forward Voltage_MAX.	?
Diode Resistance	$1[\mathrm{m}\Omega]$
Parasitic Inductance Ls	0
Internal Gate Resistance	$5[\Omega]$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 3 A	-	1.2	1.5	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 3 A	2	3.6	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	∝A
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	30	250	∝A
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	610	-	pF
C_{oss}	Output capacitance		-	96	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF
V_{SD}	Diode forward voltage	I_S = 6 A; V_{GS} = 0 V	-	-	1.2	V

$$C_{iss} = C_{gd} + C_{gs} = 610[pF]$$

$$C_{oss} = C_{ds} + C_{gd} = 96[pF]$$

$$C_{rss} = C_{gd} = 54[pF]$$

Vbreakdown(drain-source)_Max.	**500**
On Resistance_TYP	$1.2[\Omega]$
Threshold Voltage VGS(th)_TYP	$3[V]$
Transconductance_TYP	3.6
Capacitance Cgs_TYP.	$556[pF]$
Capacitance Cgd_TYP.	$54[pF]$
Capacitance Cds_TYP.	$42[pF]$
Diode Forward Voltage_MAX.	$1.2[V]$
Diode Resistance	$1[\mathrm{m}\Omega]$
Parasitic Inductance Ls	0
Internal Gate Resistance	$5[m\Omega]$

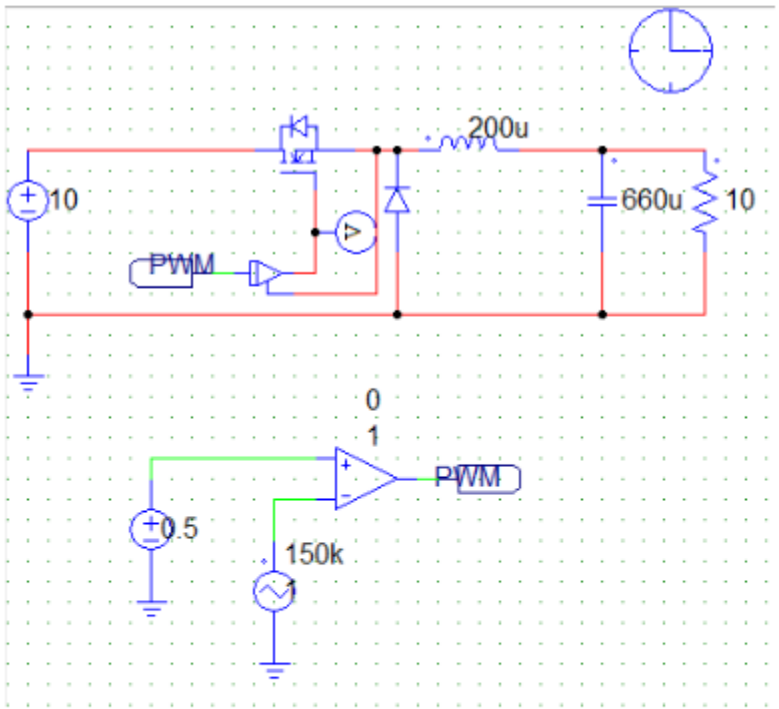
Question #4

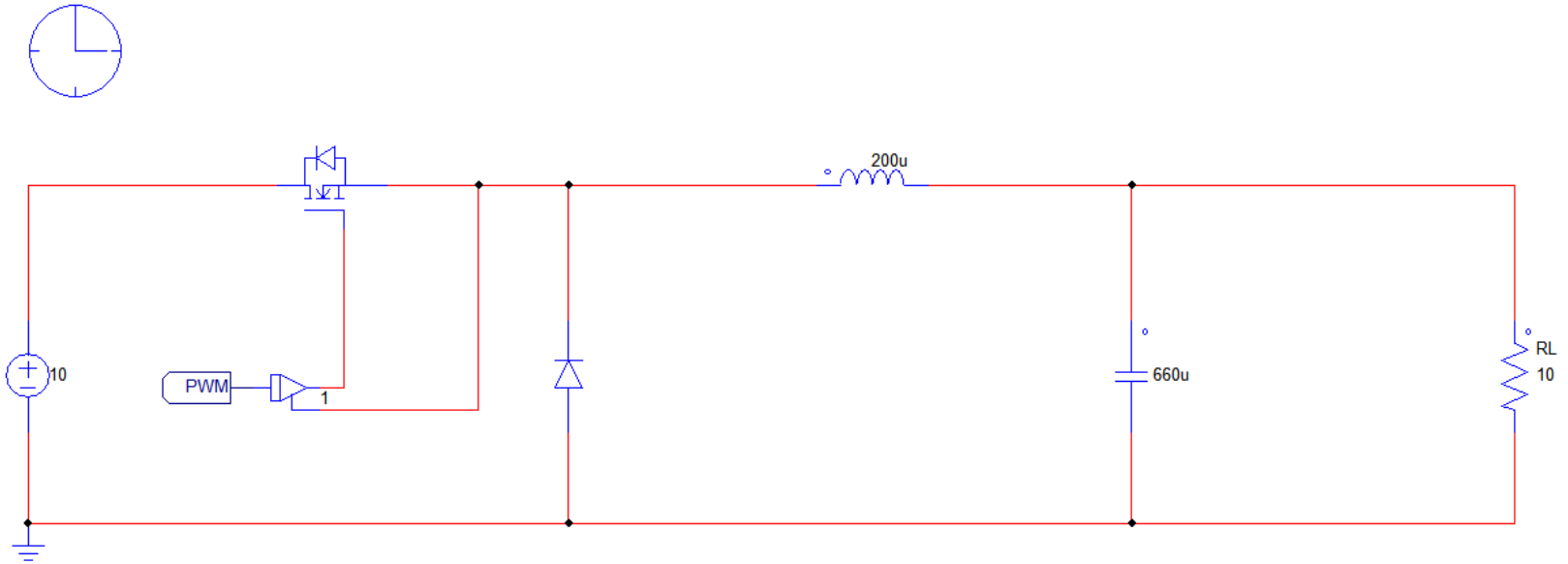
Problems

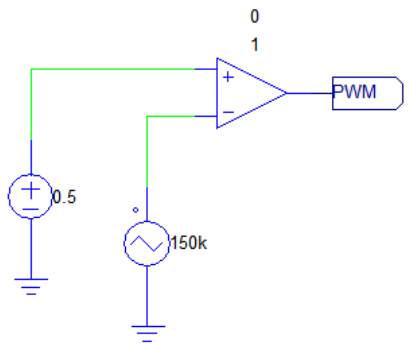
Question #3에서 작성된 표와 PSIM Simulation을 통해

출력 전압(V_o), 출력 리플 전압(Δv_o), 인덕터 전류(I_L), 그리고 인덕터 리플 전류(Δi_L) 확인!

(Level 2 MOSFET은 on-off controlle를 사용할 수 없어 on-off controller(multi level)로 변경 후 I/O signal type을 control to model로 설정. gate resistance는 1[Ω]으로 설정)







Simulation Control

PSIM | SPICE | SimCoder | Color

Solver Type: Fixed-step / Variable-step (dual) — Help

		Time Step Ratio	Smaller Time Step
Time Step	1E-07	4	2.5e-08
Total Time	0.1	Free Run	
Print Time	0		
Print Step	1		
Load Flag	0		
Save Flag	0		

Engine Default Values

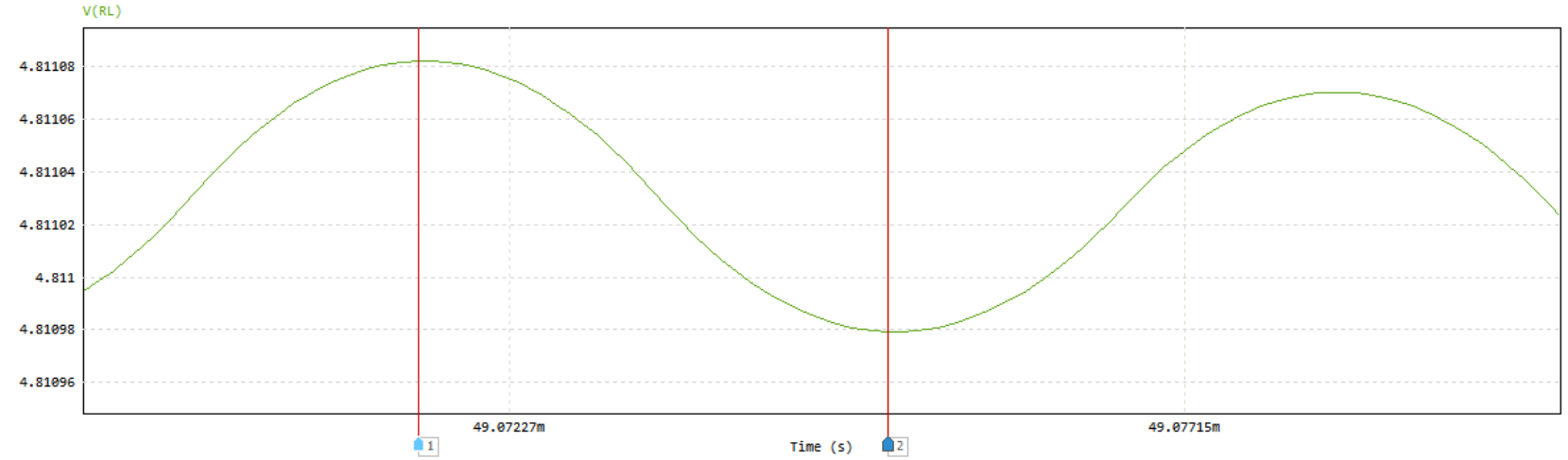
R_switch_on	1E-05
R_switch_off	1E+007

MOSFET : Q1

Parameters | Color | Simulation Models

MOSFET (3-state) (Level 2) — Help

		Display
Name	Q1	
Model Level	Level 2	
Vbreakdown (drain-source)	500	
On Resistance	1.2	
Threshold Voltage VGS(th)	3	
Internal Gate Resistance	5	
Transconductance	3.6	
Capacitance Cgs	556p	
Capacitance Cgd	54p	
Capacitance Cds	43p	
Diode Forward Voltage	1.2	
Diode Resistance	1m	
Parasitic Inductance Ls	0	
Current Flag	1	
Voltage Flag	1	

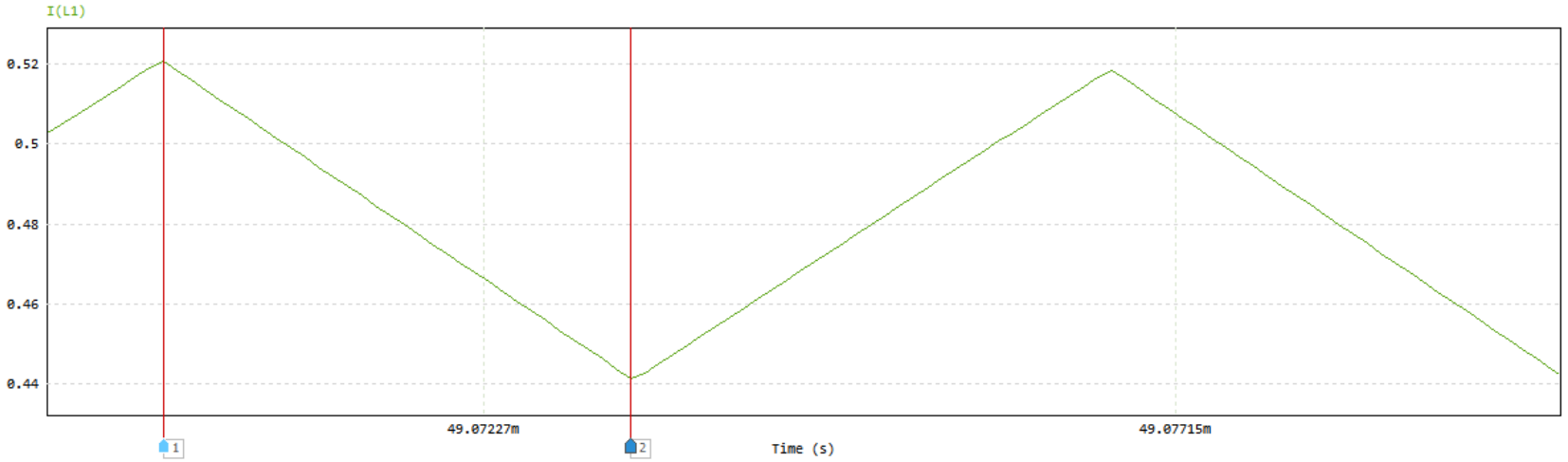


Measure

	X1	X2	Δ	Average
Time	4.90716e-02	4.90750e-02	3.40000e-06	
V(RL)	4.81108e+00	4.81098e+00	-1.03093e-04	4.81103e+00

$$V_o = 4.811[V]$$

$$\Delta V_o = 5.15465 * 10^{-5}[V]$$



Measure

	X1	X2	Δ	Average
Time	4.90700e-02	4.90733e-02	3.30000e-06	
I(L1)	5.20779e-01	4.41397e-01	-7.93827e-02	4.81088e-01

$$I_L = 0.481088\ [A]$$

$$\Delta I_L = 0.03969[A]$$

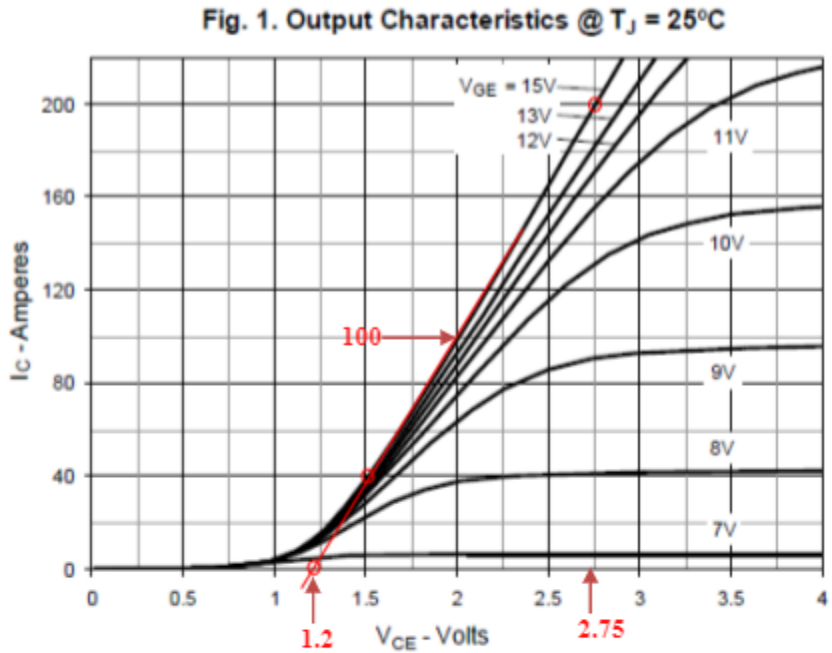
Question #5

Problems

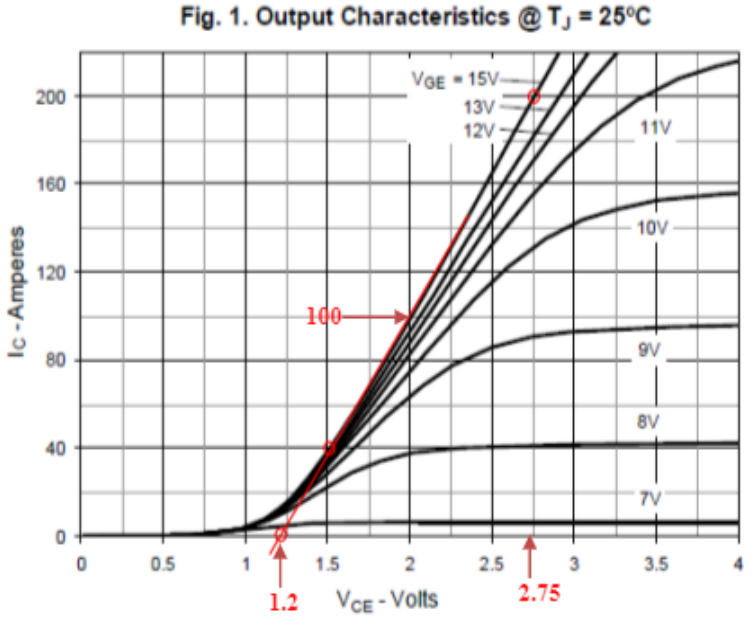
아래 링크된 데이터시트와 오른쪽 그래프를 참고하여 25℃ 조건에서 다음 빈칸(?)을 채우시오

Datasheet download : alldatasheet.com → IXXH110N65C4 search
https://pdf1.alldatasheet.com/datasheet-pdf/view/837725/IXYS/IXXH110N65C4.html

Vce_MAX.	?
Vec_MAX.	15[V]
Gate Threshold Voltage_MAX.	?
Transconductance_TYP.	?
Fall Time @ 25℃	?
Capacitance Cies_TYP.	?
Capacitance Coes_TYP.	?
Capacitance Cres_TYP.	?
Rce_on @ 25℃	?
Vce_threshold	?
Internal Gate Resistance	5[Ω]
Parasitic Inductance Ls	0



$R_{ce}(on)$은 V_{ce}와 I_c그래프의 기울기를 나타냄



$R_{ce}(on)$은 V_{ce}와 I_c그래프의 기울기를 나타냄

$$R_{ce}(on) = \frac{V_{ce1}-V_{ce2}}{I_{ce1}-I_{ce2}} = \frac{2.75-2}{200-100} = 7.5[m\Omega]$$

Symbol	Test Conditions	Maximum Ratings
V_{CES}	T_J = 25°C to 175°C	650 V
V_{CGR}	T_J = 25°C to 175°C, R_{GE} = 1MΩ	650 V
V_{GES}	Continuous	±20 V
V_{GEM}	Transient	±30 V

BV_{CES}	I_C = 250μA, V_{GE} = 0V	650			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	4.0		6.5	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			25	μA
	T_J = 150°C			2	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±100	nA
$V_{CE(sat)}$	I_C = 110A, V_{GE} = 15V, Note 1		1.98	2.35	V
	T_J = 150°C		2.34		V
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	24	40		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		3690		pF
C_{oes}			240		pF
C_{res}			140		pF

$$V_{CES} = 650V$$
$$I_{C110} = 110A$$
$$V_{CE(sat)} \leq 2.35V$$
$$t_{fi(typ)} = 30ns$$

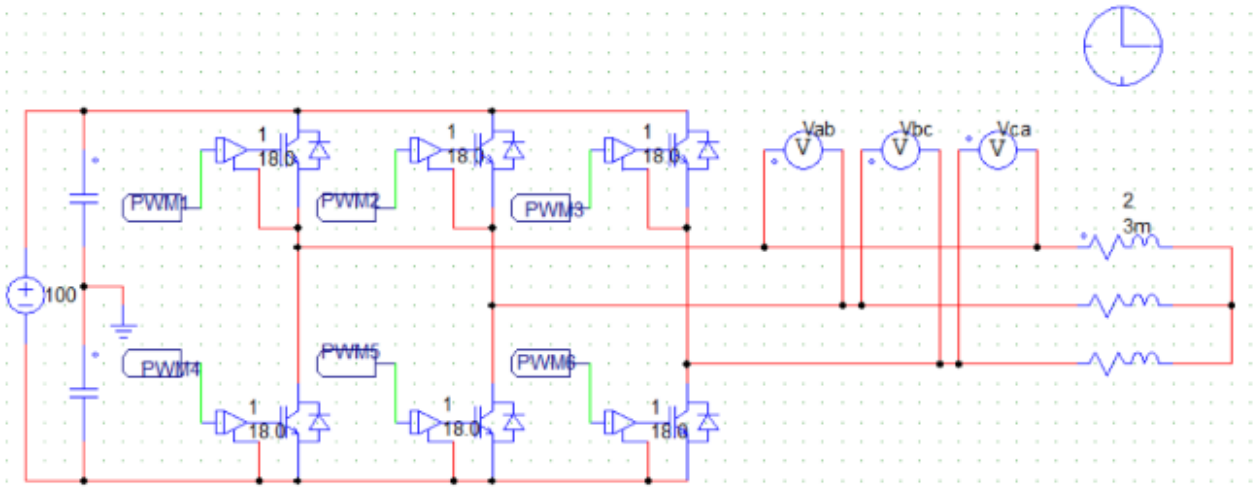
V_{ce_max}	$650[V]$
V_{ec_max}	$15[V]$
Gate Threshold Voltage_max	$6.5[V]$
Transconductance_TYP	$g_{fs} = 40[S]$
Fall Time	$35[\text{sec}]$
Capacitance C_{ies_TYP}.	$3690[pF]$
Capacitance C_{oes_TYP}.	$240[pF]$
Capacitance C_{res_TYP}.	$140[pF]$
R_{ce_on}	$7.5[m\Omega]$
$V_{ce\_threshold}$	$1.2[V]$
Internal Gate Resistance	$5[\Omega]$
Parasitic Inductance Ls	0

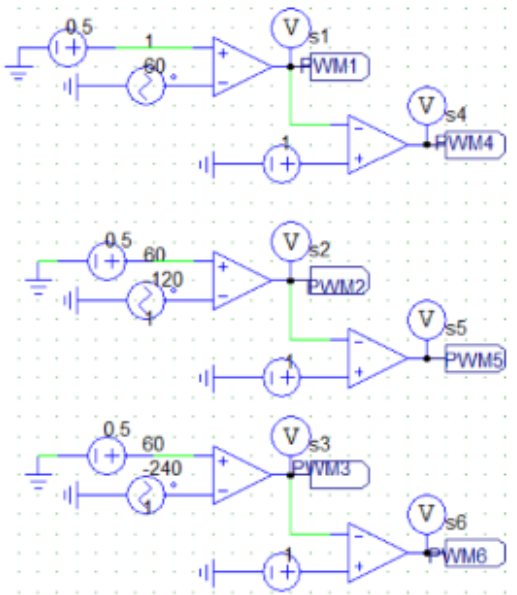
Question #6

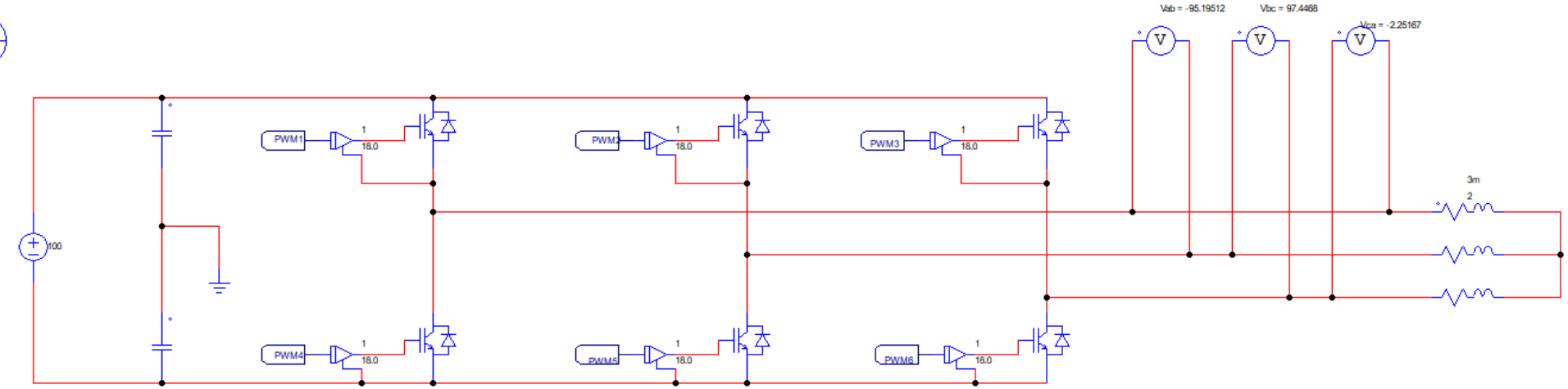
Problems

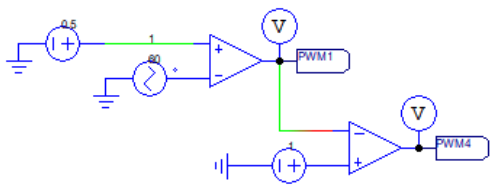
Question #5에서 작성된 표와 아래 회로를 통해 PSIM Simulation 후 3-ph inverter의 선간전압 V_{ab}, V_{bc}, V_{ca} & 상전류 I_a, I_b, I_c 확인!

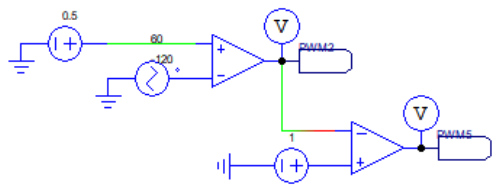
(Level 2 IGBT → on-off controller(multi level) & control to model mode 사용. 이 때 gate voltage high 는 $18[V]$, gate voltage low는 $0[V]$, gate resistance는 $1[\Omega]$로 설정한다.)

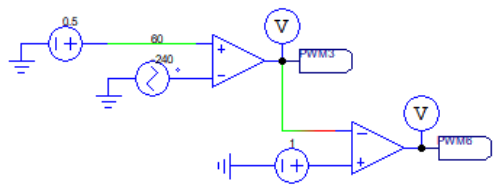












Simulation Control

PSIM | SPICE | SimCoder | Color

Solver Type: Fixed-step / Variable-step (dual) — Help

Time Step	1E-06	Time Step Ratio: 4	Smaller Time Step: 2.5e-07
Total Time	0.1	Free Run	
Print Time	0		
Print Step	1		
Load Flag	0		
Save Flag	0		

Engine Default Values

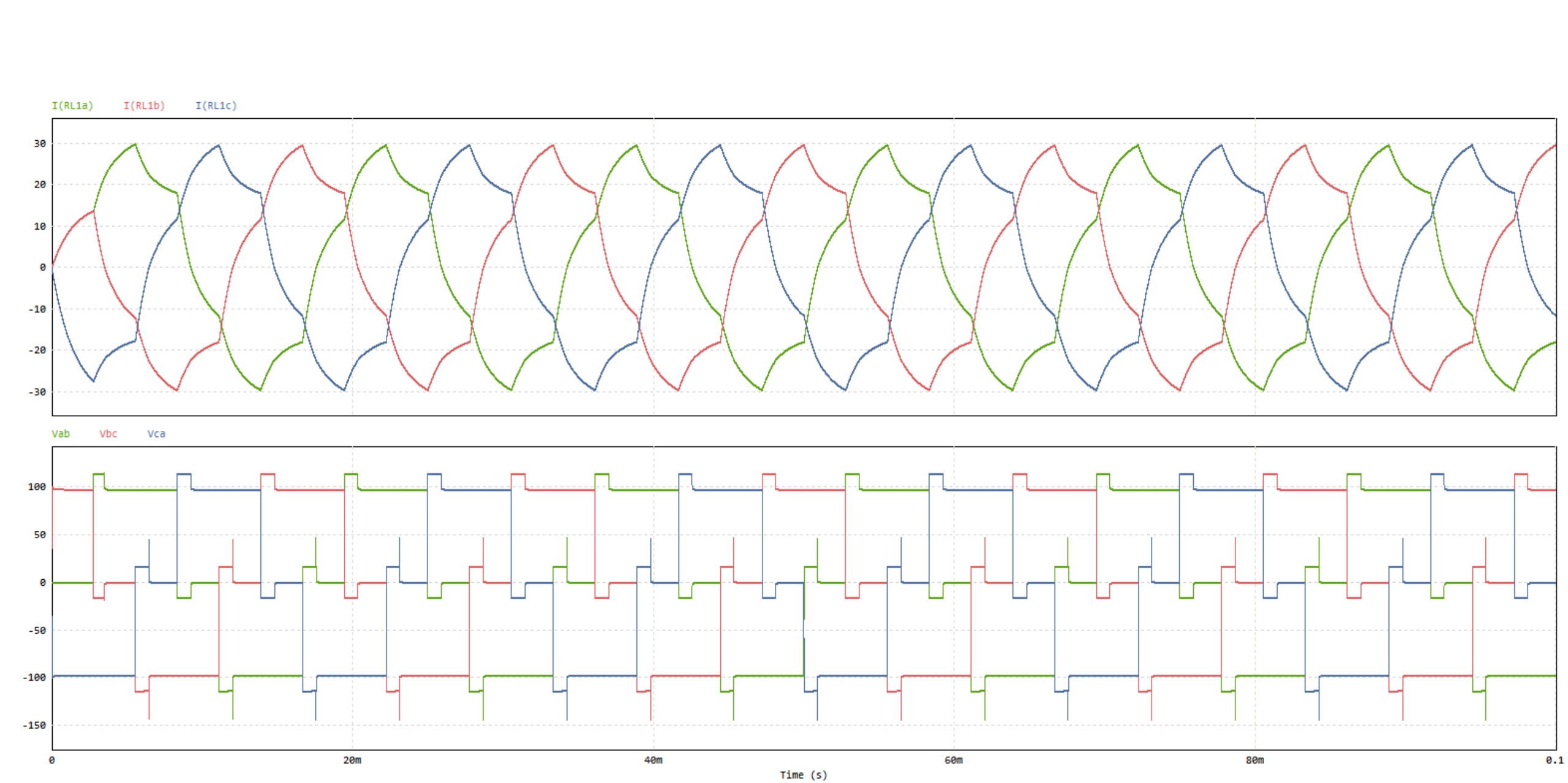
R_switch_on	1E-05
R_switch_off	1E+007

IGBT : Q7

Parameters | Color | Simulation Models

IGBT Model (Level 2) — Help

	Display
Name	Q7
Model Level	Level 2
Maximum Vce	650
Maximum Vec	15
Gate Threshold Voltage	6.5
Transconductance	40
Fall Time	35n
Capacitance Cies	3690p
Capacitance Coes	240p
Capacitance Cres	140p
Rce_on	7.5m
Vce_threshold	1.2
Internal Gate Resistance	5
Parasitic Inductance Ls	0
Current Flag	0
Voltage Flag	0


I(RL1a)
I(RL1b)
I(RL1c)
30
20
10
0
-10
-20
-30
Vab
Vbc
Vca
100
50
0
-50
-100
-150
0
20m
40m
60m
80m
0.1
Time (s)