

# Digital Logic Circuit Design Lab

## Combinational Logic Circuit Lab

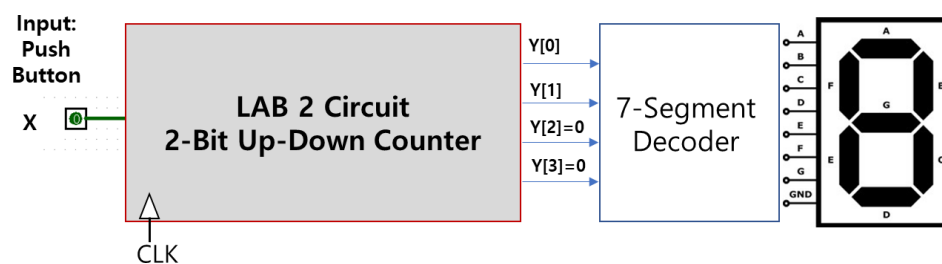
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Date: 2023-05-29

## Problem 1

Design and make a circuit for 2-bit up-down counter and display the output with a 7-segment display.

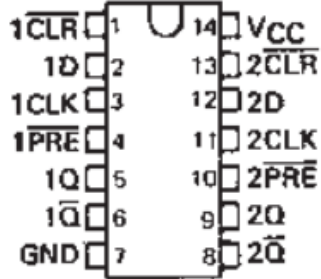
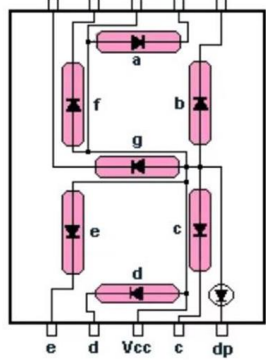
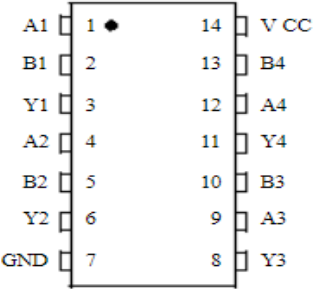


- The clock period is 1 second. Use Arduino to generate the clock.
- There are 2 modes for the counter:
  - Up-counting mode, Down-counting mode
- Use one push button to control the counter mode. See Table 1
- Display the output decimal number '0'~'3' with a 7-Segment Display
- Use 7-segment decoder chip(SN74LS47N) to control 7-Segment Display
- Design the circuit and check the results in the simulation program.
- Implement the circuit on a breadboard and demonstrate the result.

Input X	Counter mode
X = 0	UP_Counting
X=1	DOWN_Counting

Design Process

Table 1. Electrical Components

<p>(TOP VIEW)</p> 	<p>Common Anode</p> 
D-FFs (74LS74)	7-segment decoder (SN74LS47N)
<p>PIN ASSIGNMENT</p> 	
XOR gate (74HC86)	

- State Table & State Graph (Mealy)

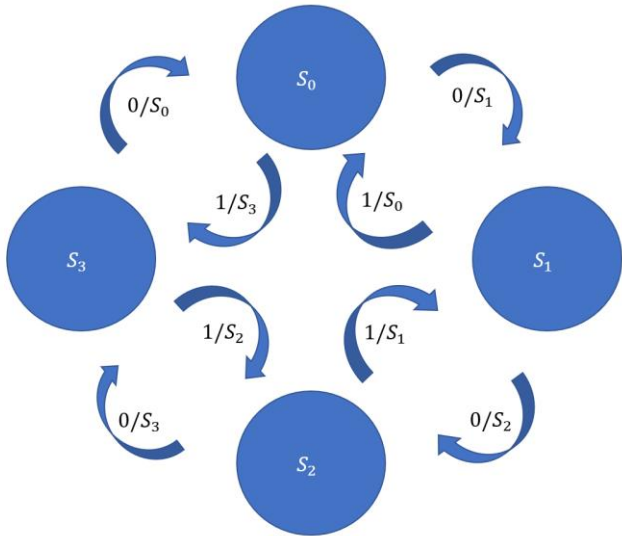


Fig 1. State Graph

## State Definition

$S_0$ : Normal State

$S_1$ : Shifted State #1

$S_2$ : Shifted State #2

$S_3$ : Shifted State #3

**Table 2. State Table**

Present State	U=0	U=1	Output(Z)	
$S_0$	$S_1$	$S_3$	$S_1(01)$	$S_3(11)$
$S_1$	$S_2$	$S_0$	$S_2(10)$	$S_0(00)$
$S_2$	$S_3$	$S_2$	$S_3(11)$	$S_2(01)$
$S_3$	$S_0$	$S_2$	$S_0(00)$	$S_2(10)$

- Truth table & Boolean expression

**Table 3. Truth Table**

Input		Next State ( $B^+$ , $A^+$ )			
B	A	U=0		U=1	
0	0	0	1	1	1
0	1	1	0	1	0
1	0	1	1	0	1
1	1	0	0	0	0

**Table 4. D-FF Truth Table**

FF Inputs ( $D_B$ , $D_A$ )			
U=0		U=1	
0	1	1	1
1	0	1	0
1	1	0	1
0	0	0	0
0	0	0	0

**Table 5. K - Map**

U \ BA	0	1
00	1	0
01	0	1
11	1	0
10	0	1

 $B^+$ 

U \ BA	0	1
00	1	1
01	0	0
11	0	0
10	1	1

 $A^+$ **SOPs:**

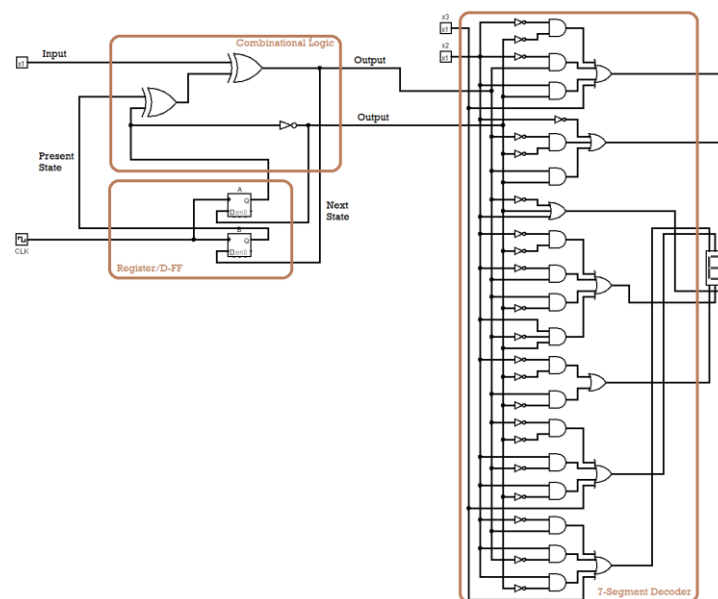
$$B^+ = \bar{U}(B \oplus A) + U\overline{(B \oplus A)}$$

$$A^+ = \bar{A}$$

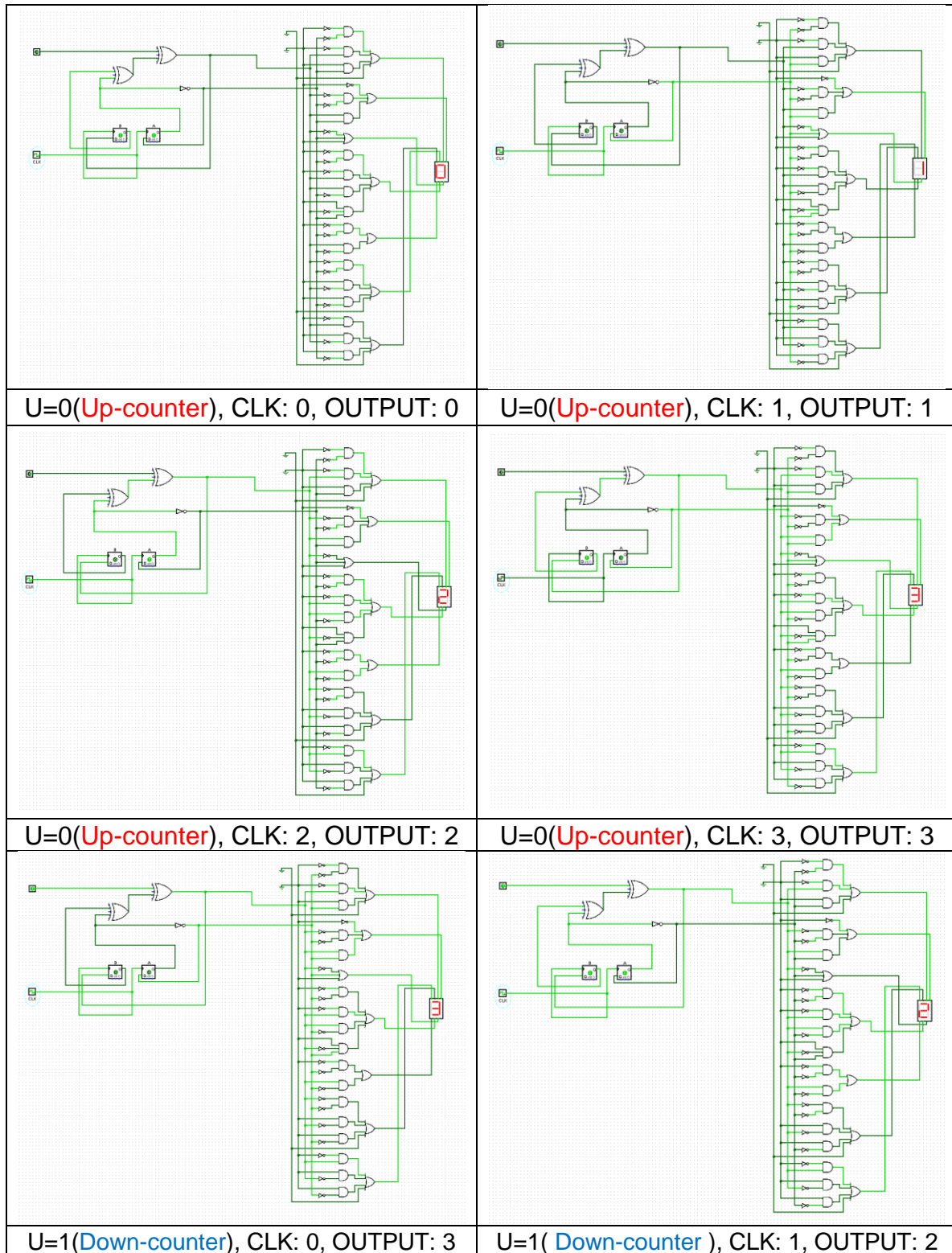
$$D_B = B^+$$

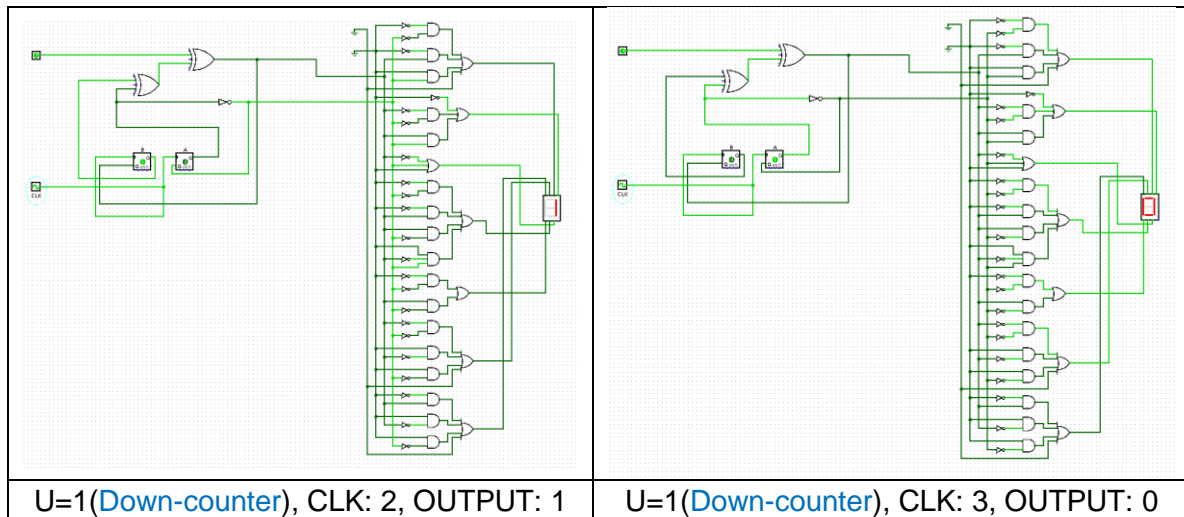
$$D_A = A^+$$

- Draw the circuit

**Fig 2. Design Circuit**

- Simulation Circuit Design





**Figure 3.Circuit Output**

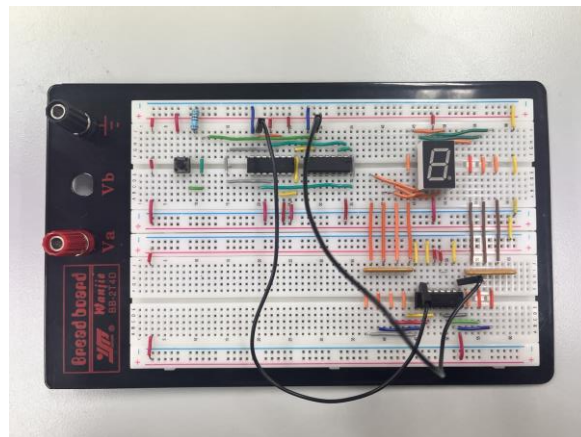
Logisim을 이용해서 다음과 같은 Up-Down Counter 7-Segment를 구현하였다. 위의 Circuit은 0부터 3까지 출력되는 2-bit 7-Segment이다. Input (U)에 0을 주면 Up-Counter를, Input (U)에 1을 주면 Down-Counter의 역할을 한다. 이후 CLK에 신호가 들어오고 나갈 때마다 Counting이 진행된다. XOR gate 2개와 D-FF 2개를 이용하였으며 7-Segment는 LAB#1에서 구현한 것을 활용하였다.

## Results and Discussion

### Demo Video

<https://youtu.be/rsQgcMQciZw>

### Results



**Fig 4. Actual Circuit**



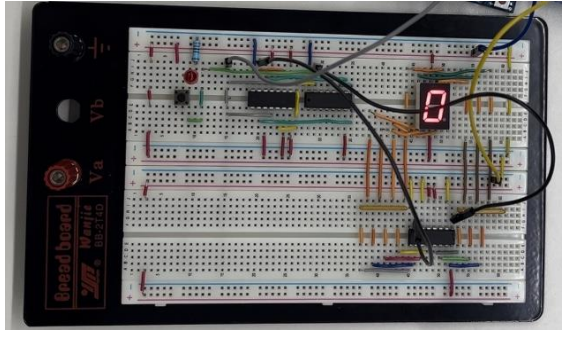
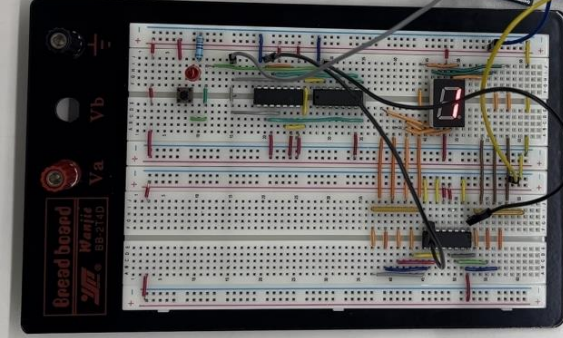
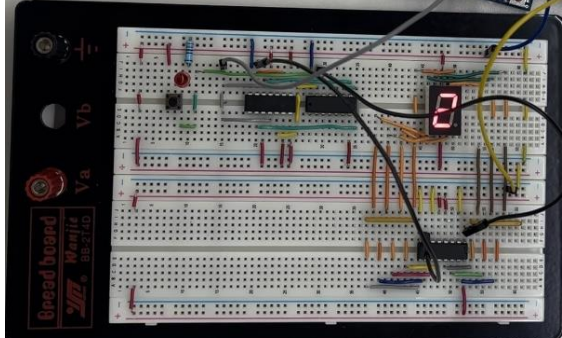
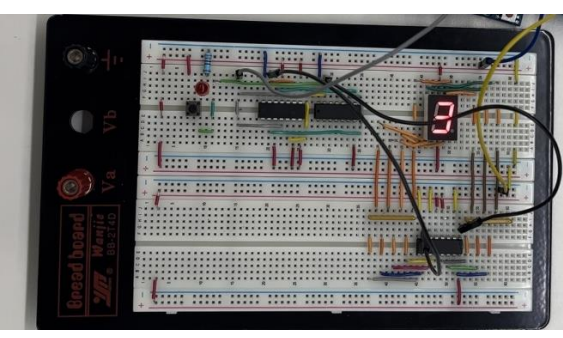
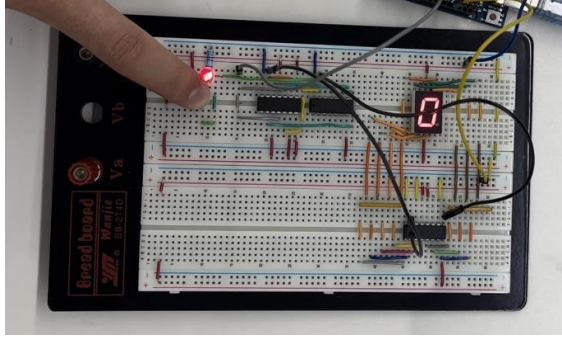
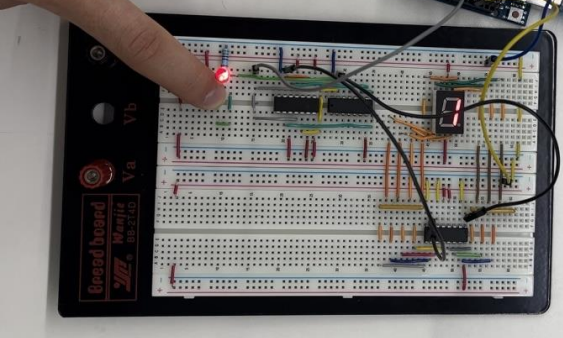
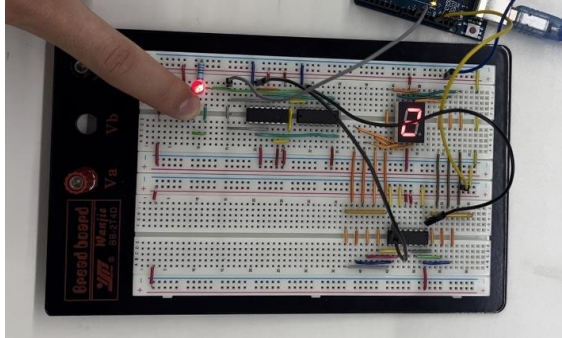
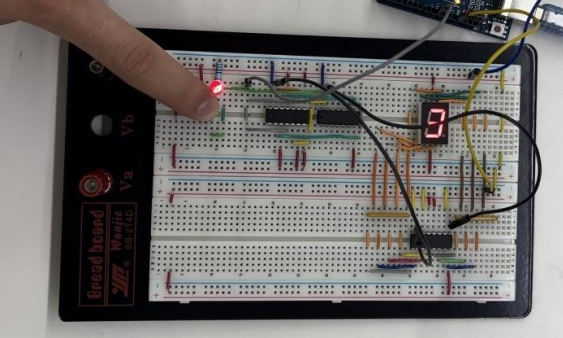
	
U=0( <b>Up-counter</b> ), CLK: 0, OUTPUT: 0	U=0( <b>Up-counter</b> ), CLK: 1, OUTPUT: 1
	
U=0( <b>Up-counter</b> ), CLK: 2, OUTPUT: 2	U=0( <b>Up-counter</b> ), CLK: 3, OUTPUT: 3
	
U=1( <b>Down-counter</b> ), CLK: 0, OUTPUT: 3	U=1( <b>Down-counter</b> ), CLK: 1, OUTPUT: 2
	
U=1( <b>Down-counter</b> ), CLK: 2, OUTPUT: 1	U=1( <b>Down-counter</b> ), CLK: 3, OUTPUT: 0

Fig 5. Circuit Result

## Discussion

Logisim 에서 구현한 Simulation 을 기반으로 BreadBoard 와 아두이노를 사용하여 위와 같은 Up-Down Counter 7-Segment 회로를 구현하였다. LAB#2 Design Problem 에 적힌 Counter Mode Condition 을 고려하여 U 에 0 이 입력되었을 때 Up-Counting 을, 1 이 입력되었을 때 Down-Counting 이 진행되도록 Circuit 을 구현하였다. XOR Gate 구현을 위한 소자는 74HC86 로 4 개의 XOR Gate가 내장되어 있다. D-FF은 74LS74 을 사용하였으며 이는 2개의 D-FF 이 내장되어 있다. 1 번 핀에는  $A^+$ 가, 2 번 핀에는  $B^+$ 가 입력된다. 그리고 CLK 신호는 D-FF 소자에 입력하였다. CLK 신호는 아두이노를 사용하여 입력하였으며 사용한 코드는 Appendix 에 기재하였다.  $A^+$  신호와  $B^+$ 신호는 Decoder 로 입력되며  $C^+$ 와  $D^+$  신호는 2-bit Display 를 위해 Ground 로 입력하였다.

## Appendix

```

1  void setup() {
2      Serial.begin(9600);
3      pinMode(10, OUTPUT);
4
5  }
6
7  void loop() {
8      // put your main code here, to run repeatedly:
9      digitalWrite(10,HIGH);
10     Serial.println("H");
11     delay(500);
12     digitalWrite(10,LOW);
13     Serial.println("L");
14     delay(500);
15
16 }

```

Source Code