## REVISION HISTORY

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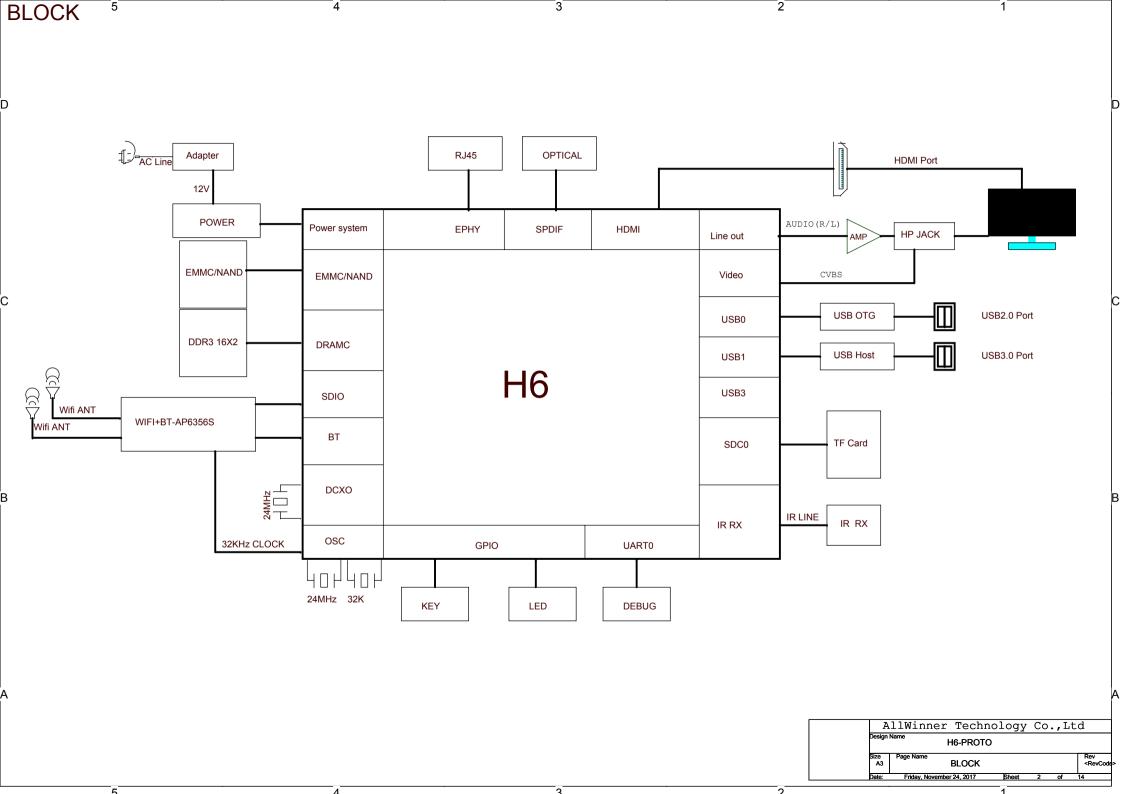
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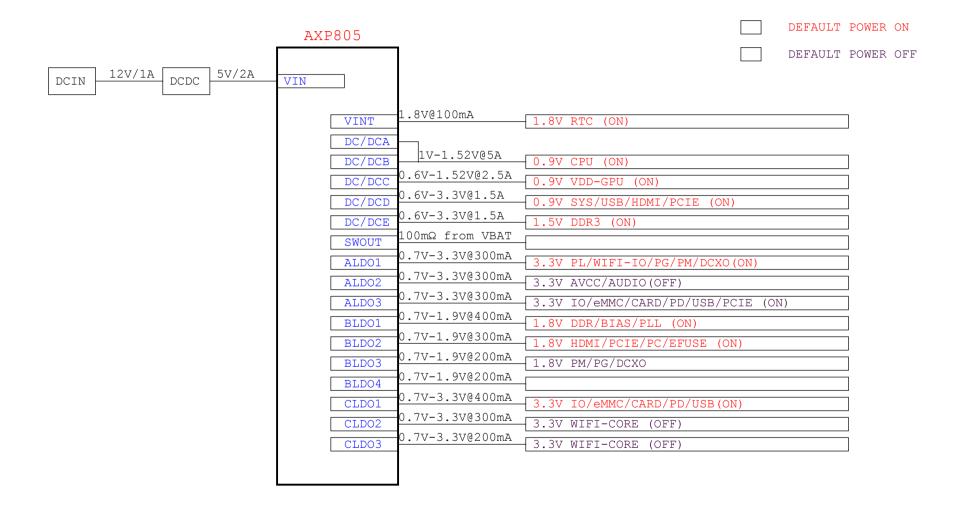
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Revision Description Checked Date Drawn Ver 0.5 Initial Version 2016-12-26 НJ Ver 0.8 2017-04-10 НJ

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**POWER TREE** 



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**GPIO ASSIGNMENT** 

PIN Define CFG Function PCO NAND WE PC1 NAND ALE/SDC2 DS 2/3 PC2 NAND CLE PC3 NAND CE0 PC4 NAND RE/SDC2 CLK 2/3 PC5 NAND RB0/SDC2 CMD 2/3 PC6 NAND DQ0/SDC2 D0 2/3 PC7 NAND DQ1/SDC2 D1 2/3 NAND/eMMC PC8 NAND DQ2/SDC2\_D2 2/3 PC9 NAND DQ3/SDC2 D3 2/3 PC10NAND DQ4/SDC2 D4 2/3 PC11NAND DQ5/SDC2 D5 2/3 PC12NAND DQ6/SDC2 D6 2/3 PC13NAND DQ7/SDC2 D7 2/3 PC14NAND DQS/SDC2 RST 2/3 PC15NAND CE1 PC16NAND RB1

PIN	Define	CFG	Function
PD0			
PD1			
PD2			
PD3			
PD4			
PD5			
PD6			
PD7			
PD8			
PD9			
PD10			
PD11			
PD12			
PD13			
PD14			

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			]
PD22			
PD23			1
PD24			]
PD25			1
PD26			1

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	WTFT+BT
PG7	UART1_RX	2	WIFIIDI
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	
PG13	PCM2_DIN	2	
PG14			

PIN	Define	CFG	Function
PF0	SDC0_D1	2	
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	CARD0
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2			
PH3			
PH4			
PH5			
PH6			
PH7	SPDIF_OUT	3	
PH8	HSCL	2	
PH9	HSDA	2	HDMI
PH10	HCEC	2	

PIN	Define	CFG	Function
PL0	PMU-SCK	3	
PL1	PMU-SDA	3	
PL2	RECOVERY	2	
PL3	LINK-LED	1	
PL4	PWR-LED	1	
PL5	USB0-DRVVBUS	1	
PL6	MUTE	1	
PL7	STATUS-LED	1	
PL8			
PL9	IR-RX	2	
PL10	BT-WIFI-ON	1	
PM0	WL-WAKE-AP	0	
PM1	BT-WAKE-AP	0	
PM2	AP-WAKE-BT	1	WIFI+BT
РМ3	WL-REG-ON	1	WILLIDI
PM4	BT-REG-ON	1	

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PC,PD, 部分IO口不具备中断功能 PF,PG,PH,PL,PM, 部分IO口有中断功能 SPIO\_CLK << PC0/NAND-WE/SPI0-CLK PE0/SDC0-D1/JTAG-MS1 PC1/NAND-ALE/SDC2-DS PF1/SDC0-D0/JTAG-DI1 RC1 33R R0402 SDC0-D0 PC2/NAND-CLE/SPI0-MOSI PE2/SDC0-CLK/LIART0-TX SPIO MISO ( PC3/NAND-CE0/SPI0-MISO PF3/SDC0-CMD/JTAG-DO1 SDC0\_CMD PC5/NANN\_PRO/SDC2-CLK
N22 PC5/NANN\_PRO/SDC2-D0/SPI0-HOLD
R22 PC5/NANN\_PD0/SDC2-D0/SPI0-HOLD
R23 PC5/NANN\_PD0/SDC2-D1/SPI0-WP
R23 PC5/NANN\_PD0/SDC2-D1/SPI0-WP
R24 PC5/NANN\_PD0/SDC2-D2
PC5/NANN\_PD0/SDC2-D2
PC5/NANN\_PD0/SDC2-D2 PE4/SDC0-D3/LIARTO-RX PF5/SDC0-D2/JTAG-CK1 10 10 -TDDE1 SDC0-DET PF6 PC7 PC8 RC3 33R R0402 >> WL-SDIO-CLK PG0/SDC1-CLK PG1/SDC1-CMD | 122 | PCUMAND-DQ3/SDC2-D3 | | PC10/NAND-DQ4/SDC2-D4 | | PC10/NAND-DQ5/SDC2-D5 | PC12/NAND-DQ6/SDC2-D5 | PC12/NAND-DQ6/SDC2-D WL-SDIO-CMD WI-SDIO-D0 13.14 13.14 PG2/SDC1-D0 5pF C0402 13,14 13,14 13,14 13,14 PG3/SDC1-D1 PG4/SDC1-D2 WL-SDIO-D2 WL-SDIO-D3 R19 PC13/NAND-DO7/SDC2-D7 PG5/SDC1-D3 13.14 PC14/NAND-DQS/SDC2-RST PG6/UART1-TX S BT-UART-RX P19 PC14/NAND-DQS P21 PC15/NAND-CE1 N19 PC16/NAND-RB1 13,14 13,14 PG7/HAPT1-PY BT-UART-CTS PG8/UART1-RTS/PLL-STA-DB/SIM0-VPPEN BT-UART-RTS 13,14 VCC-PC PG9/UART1-CTS/PLI-TEST-GPIO/SIM0-VPPPE PG10/PCM2-SYNC/H-PCM2-SYNC/SIM0-PWREN RT-PCM-SYNC 10 BT-PCM-CLK PG11/PCM2-CLK/H-PCM2-CLK/SIM0-CLK/BIST-RESULT( CSI-PCLK <-PG12/PCM2-DOUT/H-PCM2-DOUT/SIM0-DATA/BIST-RESULT1 S BT-PCM-DIN PD0/LCD0-D2/TS0-CLK/CSI-PCLK/RGMII-RXD3/RMII-NULL -S BT-PCM-DOUT PD1/LCD0-D3/T50-ERR/CSI-MCLK/RGMII-RXD2/RMII-NULL PG1/3/PCM2-DIN/H-PCM2-DIN/SIM0-RST/BIST-RESULT2
PD2/LCD0-D4/T50-SYNC/CSI-HSYNC/RGMII-RXD1/RMII-RXD1 PG14/PCM2-MCLK/H-PCM2-MCLK/SIM0-DET/BIST-RESULT3 10 × vcc-pg CSI-VSYNC -PD3/LCD0-D5/TS0-DVLD/CSI-VSYNC/RGMII-RXD0/RMII-RXD0 PD4/LCD0-D6/TS0-D0/CSI-D0/RGMII-RXCK/RMII-NULL CSI-D1 ->> CPUX-UTX 11 PD5/LCD0-D7/TS0-D1/CSI-D1/RGMII-RXCTL/RMII-CRS-DV PD6/LCD0-D10/TS0-D2/CSI-D2/RGMII-RXCTL/RMII-RXER PH0/UART0-TX/PCM0-SYNC/H-PCM0-SYNC/SIM1-VPPEN PH1/UART0-RX/PCM0-CLK/H-PCM0-CLK/SIM1-VPPPE CPUX-URX CSI-D2 C-D2
CSI-D3 C-D4
CSI-D4 C-D6
CSI-D6 C-D6
CSI-D7 C-D7
CSI-SCK CAM-12 PD7/LCD0-D11/TS0-D3/CSI-D3/RGMII-TXD3/RMII-NULL PH2/IR-TX/PCM0-DOUT/H-PCM0-DOUT/SIM1-PWREN PD8/LCD0-D12/TS0-D4/CSI-D4/RGMII-TXD2/RMII-NULL S PH3 PH3/SPI1-CS/PCM0-DIN/H-PCM0-DIN/SIM1-CLK PD9/LCD0-D13/TS0-D5/CSI-D5/RGMII-TXD1/RMII-TXD1 PH4/SPI1-CLK/PCM0-MCLK/H-PCM0-MCLK/SIM1-DATA PWM1 PD10/LCD0-D14/TS0-D6/CSI-D6/RGMII-TXD0/RMII-TXD0
PD11/LCD0-D15/TS0-D7/CSI-D7/RGMII-TXCK/RMII-TXCK PH5/SPI1-MOSI/SPDIE-MCLK/TWI1-SCK/SIM1-RST PH6/SPI1-MISO/SPDIF-IN/TWI1-SDA/SIM1-DET PD12/LCD0-D18/TS1-CLK/CSI-SCK/RGMII-TXCTL/RMII-TXEN PD13/LCD0-D19/TS1-ERR/CSI-SDA/RGMII-CLKIN/RMII-NULL PH7/SPDIF-OUT CSI-SDA CSI-RESET# ->> HSCL ->> HSDA 12 12 PH8/HSCI PD14/LCD0-D20/TS1-SYNC/DMIC-CLK/CSI-D8 PD15/LCD0-D21/TS1-DVLD/DMIC-DATA0/CSI-D9 DHU/HCD/ CSI-STBY-EN CSI-PWR-EN S HCEC PH10/HCEC R2 T2 P4 PD16/LCD0-D22/TS1-D0/DMIC-DATA1 PD17/LCD0-D23/TS2-CLK/DMIC-DATA2 PMU-SCK PL0/S-RSB-SCK/S-TWI-SCK S-UART-TX PD18/LCD0-CLK/TS2-ERR/DMIC-DATA3 PL1/S-RSB-SDA/S-TWI-SDA P3 V3 RECOVERY PD19/LCD0-DE/TS2-SYNC/UART2-TX/MDC PI 2/S-UART-TX TP12 TP PAD PD20/LCD0-HSYNC/TS2-DVLD/UART2-RX/MDIO PL3/S-UART-RX S-UART-RX PD21 PD22 UART3\_TX PD21/LCD0-VSYNC/TS2-D0/UART2-RTS PL4/S-JTAG-MS USB0-DRVVBUS PD22/PWM0/TS3-CLK/UART2-CTS PL5/S-JTAG-CK TP11 TP PAD PD23/TWI2-SCK/TS3-FRR/UART3-TX/JTAG-MS PL6/S-JTAG-DO UART3\_RX UART3\_RTS PD24/TWI2-SDA/TS3-SYNC/UART3-RX/JTAG-CK PL7/S-JTAG-DI STATUS-LED 11 PD25/TWI0-SCK/TS3-DVLD/UART3-RTS/JTAG-DO PD26/TWI0-SDA/TS3-D0/UART3-CTS/JTAG-DI PL8/S-PWM0 PL9/S-IR-RX ->> IR-RX 10 VCC-PD VCC-PD PL10/S-OWC/S-PWM1 VCC-PL PM0 S RT-WAKE-AP 13.14 PM2 S WL-REG-ON PM4 M19 H6-BGA-1219 VCC-PC VCC-PG VCC-PL VCC-PM CC3 CC4 CC5 CC6 H2 H3 H4 C0402 C0402 C0402 C0402 Н1 H1 H1 H1 GND GND GND GND GND AllWinner Technology Co., Ltd esign Name H6-PROTO Rev <RevCode Ã3 SOC1 Friday, November 24, 2017 Sheet

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