		T4 (prev)	T1	T2	T3	Tw	T4
AD_0-AD_{15}	Time MUXed addr-data lines		Address	Data			
	Time MUXed addr-status lines		Most sig. addr lines for m/m ops	Status info available during m/m or I/O ops			
AD_{16}/S_3 - A_{19}/S_6	Low during I/O ops S6 - always low S5 - status of IF S4, S3 - indicate which seg reg is presently being used for m/m access						
BHE/S_7			0 for R/W/INTA cycles whenever byte to be transferred from higher -> lower byte	Status info available			Status info available
RD	0 => processor performing m/m or I/O read op			State during read cycle			
READY	ACK from slow devices or m/m - completed data transfer						
INTR	Level triggered Sampled during last cycle of each instruction						
TEST	Examined by a WAIT instruction 0 => continue; 1 => idle						
NMI	Edge triggered Causes a Type 2 interrupt						
RESET	Terminate cur act., start from FFFF0H Restarts execn when it returns to low						
CLK **Vcc** **GND** **MN/MX**							

M/IO	0 => IO op; 1 => m/m op Logically equivalent to S2	

Min Mode	**INTA**	0 => interrupt accepted		Active low in each interrupt cycle		
	ALE	Availability of valid addr on AD lines				
	DT/R	Dir of data flow thru transreceivers 1 => send out; 0 => receive Logically equivalent to S1	Active			
	DEN	Availability of valid data on AD lines Enable bidir buffers to separate D from AD				
	HOLD **HLDA**					

Max Mode	**S2, S1, S0**	Status lines - type of op by processor Change in T3 => start of new cycle	Active	Passive		Active for next bus cycle
	LOCK	0 => other bus masters prevented from gaining the system bus				
	QS_1, QS_0	Queue Status				
	RQ_0/GT_0, RQ_1/GT_1					

Active High	Tristate during INTA & local bus ACK cycles
	Tristate off during local bus ACK cycles
Active Low	Status - Tristated during HOLD
Active Low	Tristated during HLDA
Active High	Synchronized by 8284A
Active High	Internally synchronized
	Internally synchronized
	Internally synchronized
Active High for >=4 CLK cycles	Internally synchronized

	Tristated during local bus HLDA Active from prev T4 to current cycle T4

S4	S3	Segment
0	0	ES
0	1	SS
1	0	CS/none
1	1	DS

BHE	A0	Indication	
0	0	Whole Word (2B)	D0-D15
0	1	Upper byte from/to odd addr	D8-D15
1	0	Lower byte from/to odd addr	D0-D7
1	1	None	

S2	S1	S0	Indication
0	0	0	INTA

Active High	Never Tristated
	Tristated during HLDA Active from prev T4 to current cycle T4
	Active from middle of T2 to middle of T4 Tristated during HLDA

	Tristate off during HLDA

0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Code access
1	0	1	Read m/m
1	1	0	Write m/m
1	1	1	Passive

QS1	QS0	Indication
0	0	No operation
0	1	1st byte of opcode from queue
1	0	Empty queue
1	1	Subsequent byte from queue