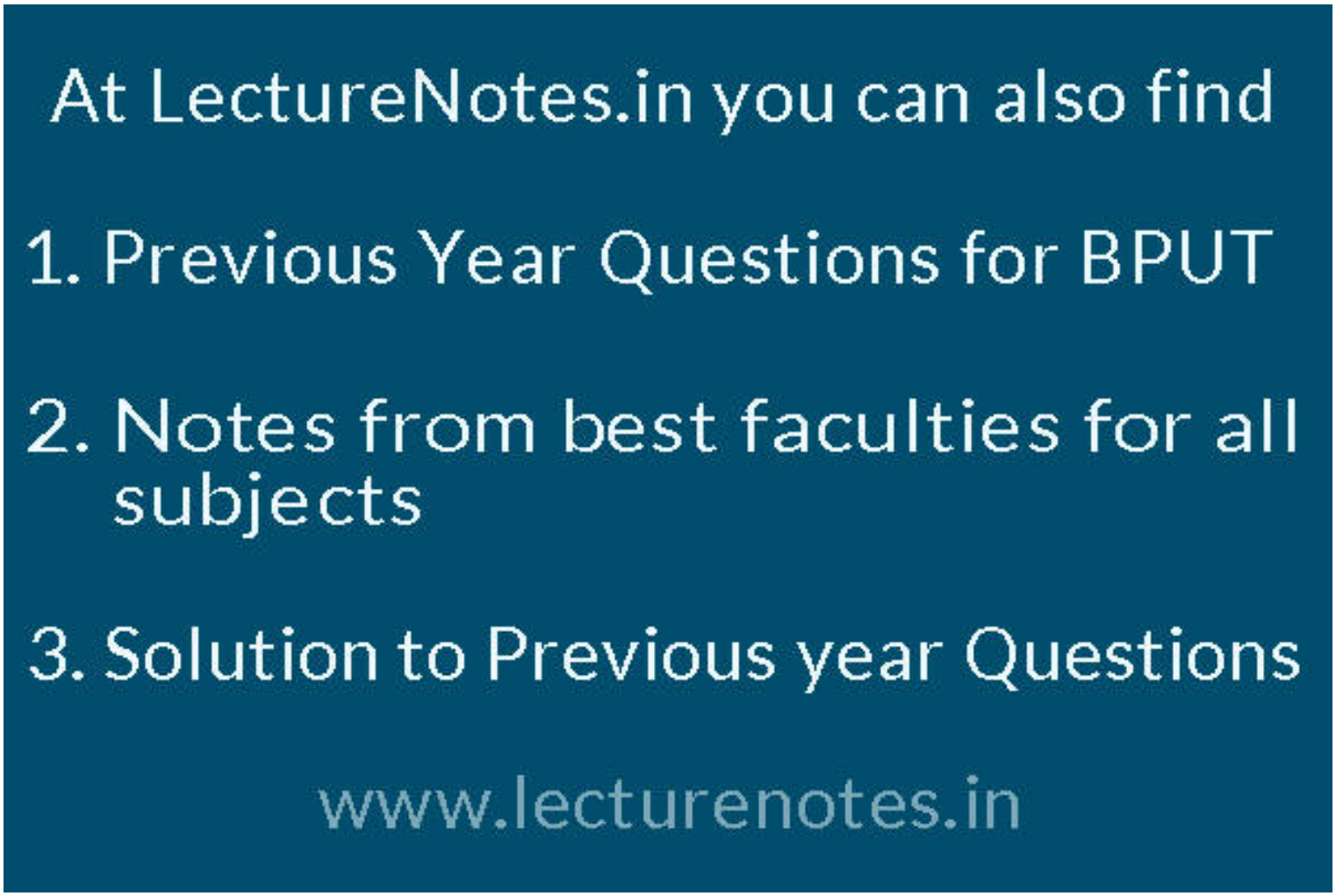
Microprocessor And Microcontroller

Contributed By:
Annapurna Mishra
Silicon Institute Of Technology SIT

Disclaimer



Microprocessor And Microcontroller

Topic:

Intel 8086 Microprocessor

Contributed By:

Annapurna Mishra

Silicon Institute Of Technology SIT

INTEL - 8086 - MICROPROCESSOR

Introduction / Features of 8086 microprocessor :—

→ 8086 is a 16-bit, N-channel, HMOS microprocessor (HMOS - High speed MOS)

→ It is a 40 pin IC package or DIP.

→ It has 16-bit databus and 20-bit wide address bus. It requires +5V. dc for its operation.

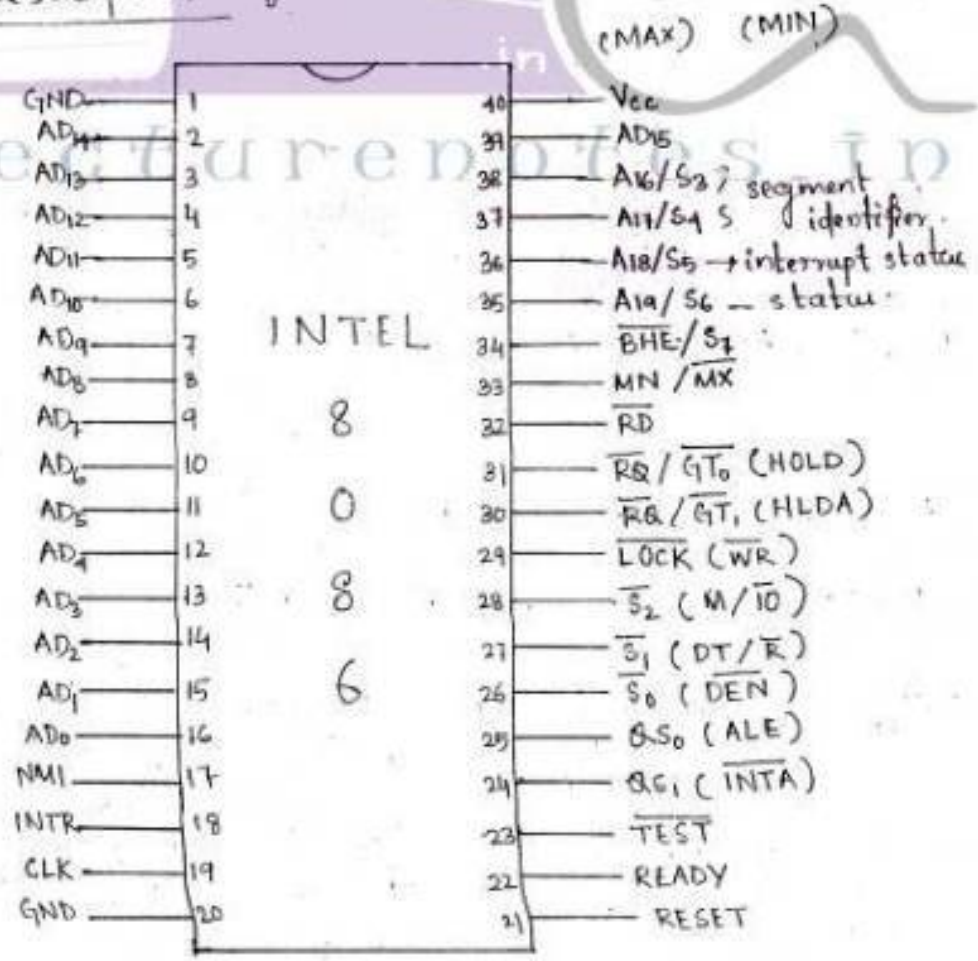
→ Using 20-bit address lines its memory addressing capacity is 2^{20} = 1 MB of memory

→ It can operate on 5, 8 and 10 MHz frequency.

→ It has introduced the pipelining operation technology

→ Memory segmentation is first introduced in this microprocessor.

* Pin Description :—



→ 8086 microprocessor can be operated in two modes.

1. Minimum mode
2. Maximum mode.

→ When only one 8086 CPU is to be used in a microcomputer system, 8086 up is used in the minimum mode of operation. In this mode the CPU issues the control signal required by memory and I/O devices.

→ In multiprocessor system it operates in the maximum mode. In this mode the control signals are issued by '8288 bus controller which is used with 8086 for this purpose.

→ The MN/$\overline{MX}$ decides the operating modes of 8086.

→ 8086 up pin description is as follows.

→ $AD_0 - AD_{15}$: Address/Data lines. These are low-order address bus. They are multiplexed with data lines.

→ $A_{16} - A_{19}$: Higher order address lines. These are multiplexed with status signals.

→ A_{16}/S_3, A_{17}/S_4 : A_{16} and A_{17} are multiplexed with segment identifier signal S_3 and S_4.

→ A_{18}/S_5 : A_{18} is multiplexed with interrupt status S_5.

→ A_{19}/S_6 : A_{19} is multiplexed with status signal S_6.

→ $\overline{BHE}/S_7$: Bus high enable / status. It is used to enable data onto the most significant bits of data bus $D_8 - D_{15}$. The 8-bit interfacing devices connected to the upper half of the data bus use $\overline{BHE}$ signal.

- (Read) : This signal is used for read operation. It is active low.

→ READY : This signal indicates that the peripheral is ready to transfer data. The I/O or memory sends acknowledgement through this pin. This pin is active high.

→ RESET : This signal resets the system. This signal is active high.

→ CLK : It requires clock frequency of 5, 8 or 10 MHz.

→ INTR : Interrupt request.

→ NMI : Non-maskable interrupt pin.

→ $\overline{TEST}$: When this signal is active the microprocessor continues execution or else it waits. It includes an additional test control during wait states.

→ Vcc : Power supply of +5v dc is used.

→ GND : Ground connection (0v).

Pin Description for Minimum mode :-

* For minimum mode operation MN/$\overline{MX}$ pin is made HIGH (1) or +5v power supply.

→ $\overline{INTA}$: Interrupt acknowledgement signal. It is active Low. On receiving interrupt signal the processor issues an interrupt acknowledge signal.

→ ALE : Address latch enable. The up sends this signal to latch the address.

→ $\overline{DEN}$: Data Enable :
→ This signal activates the external data bus buffers.
→ It acts as an output enable signal, when the 8286 octal bus transceiver is used.

→ DT/$\overline{R}$: — Data Transmit / Receive —
→ This signal controls the direction of dataflow through the transceiver i.e Intel 8286/8287.
→ When it is HIGH, data are sent out;
when it is LOW, data are received.

→ M/$\overline{IO}$: — Memory / Input output
→ When it is HIGH, CPU wants to access memory and when it is LOW, CPU wants to access input/output device

→ $\overline{WR}$: — Write control signal.
→ When this signal is LOW, the processor performs write operation.

→ HLDA : — Hold acknowledge signal
→ It is issued by the processor, when the external device passes a hold request.

→ HOLD : —
→ When any external device wants to use the address and databus, it sends a HOLD request to the processor through this pin.

Pin Description for Maximum Mode :-

→ In this mode MN/$\overline{MX}$ is LOW.

→ **QS_1, QS_0 :-** Queue status

→ These signals show the instruction queue status.

QS_1	QS_0	
0	0	→ No operation
0	1	→ 1st byte of opcode from queue
1	0	→ Empty the queue
1	1	→ Next byte from the queue.

→ **$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$:-** status signals

→ These signals are connected to the bus controller i.e Intel 8288.

→ The bus controller generates memory and I/O access control signals.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	
0	0	0	→ Interrupt acknowledge
0	0	1	→ Read data from I/O port
0	1	0	→ write data into I/O port
0	1	1	→ Halt
1	0	0	→ Opcode fetch
1	0	1	→ Memory Read
1	1	0	→ Memory write
1	1	1	→ Passive state.

→ **$\overline{LOCK}$:-**

→ This signal is used to lock peripherals from the system.

→ $\overline{RQ}/\overline{GT_1}$, $\overline{RQ}/\overline{GT_0}$ — Request / Grant.

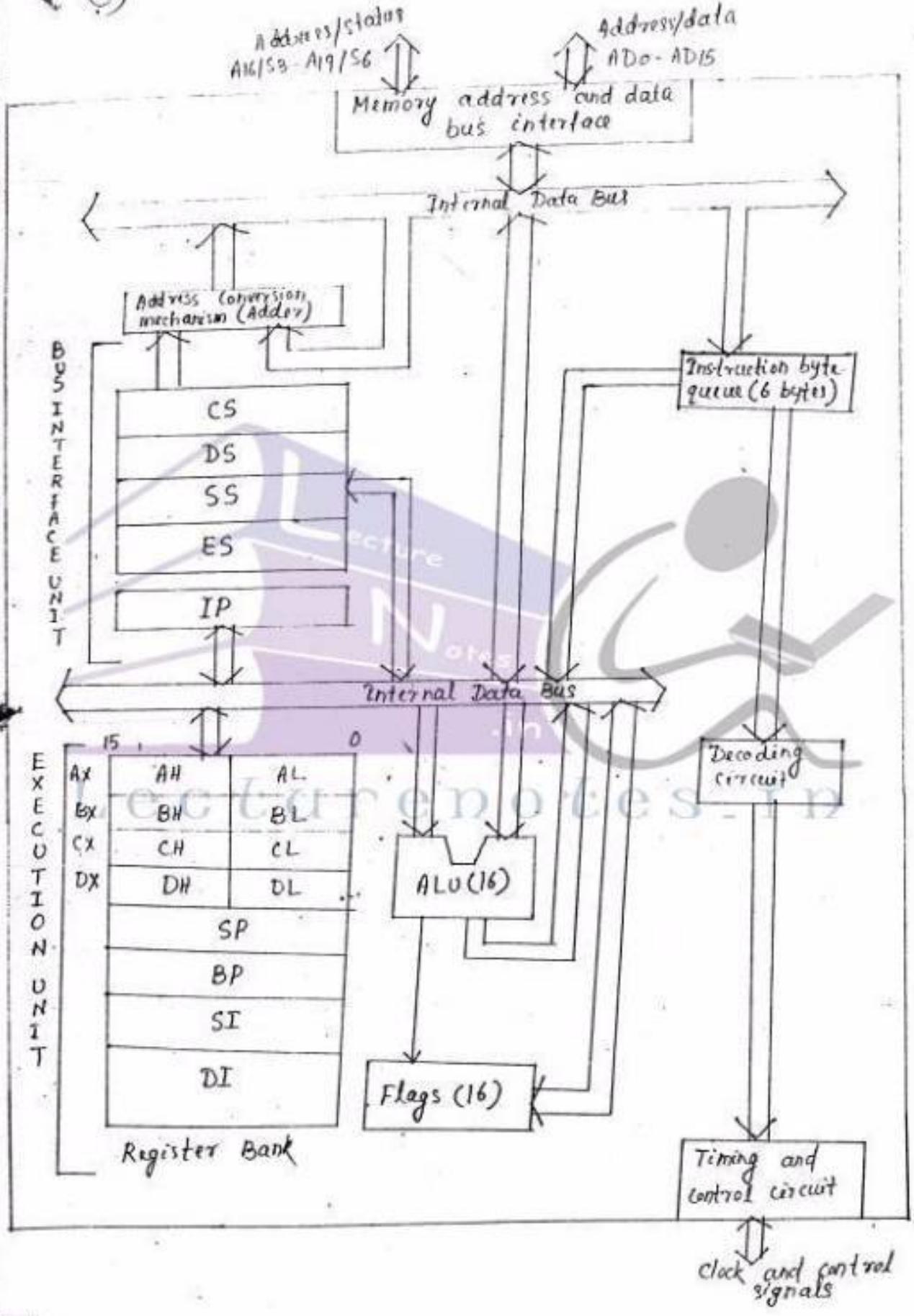
→ These signals are used for local bus priority control.

→ Other processors ask the CPU through these lines to release the local bus.

→ $\overline{RQ}/GT_0$ has higher priority than $\overline{RQ}/GT_1$.

8086 ARCHITECTURE

(3)



8086 Microprocessor Architecture :—

→ The 8086 Microprocessor Architecture is divided into two parts.

1. Bus Interface unit (BIU)
2. Execution unit (EU)

Bus Interface Unit :—

→ The BIU consists of the following units, like Instruction Queue, Segment Registers, Instruction Pointer etc.

→ It interfaces the processor to the outside i.e it is responsible for performing all external bus operations like fetch, read, write, input and output of data.

→ The BIU uses instruction queue for pipelined operation. The instruction queue is a 6-byte first-in-first-out register which can be understood as a cache memory. The queue permits the prefetch of upto 6 bytes of instruction code.

Execution Unit :—

→ The EU consists of the following units, like, ALU, Flag register, General purpose registers, Pointer and Index registers etc.

→ The EU decodes and executes the instructions prefetched by the BIU.

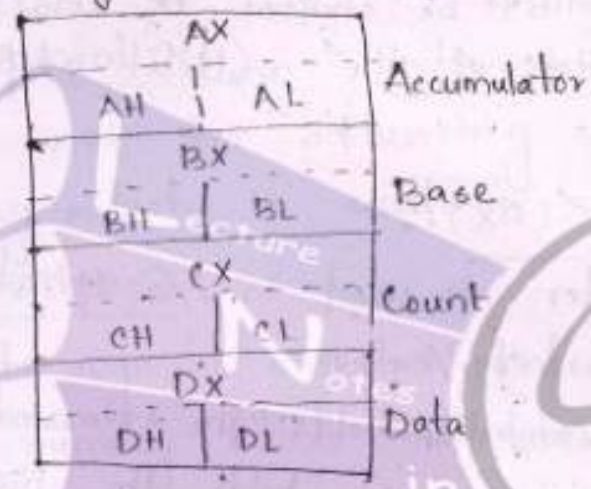
→ It also tests the status and control flags and updates these flags based on the results of the instruction.

Register Organisation :-

→ 8086 microprocessor has a powerful set of registe of 16-bit each. The registers are categorized into four groups.

1. General Data Registers
2. Segment Registers
3. Pointers and Index Registers
4. Flag Register.

General Data Registers —



→ 8086 up contains 4 general data registers like AX, BX, CX and DX.

→ They are used to hold data, variables, results etc temporarily for faster operation.

Accumulator (AX) :-

→ AX is used as 16-bit accumulator, with the lower 8-bits designated as AL and higher 8-bits as AH for 8-bit operations.

→ It performs all the arithmetic and logic operations and the result is also stored in accumulator.

Mindfire is a software service provider,
with unrelenting focus on optimal software development
and delivery.

ase Register (BX) :—

→ BX register is used as a general purpose register as well as to store the offset for forming physical address in certain addressing modes.

Count Register (CX) :—

→ CX register is used as a default counter in case of string and loop instructions.

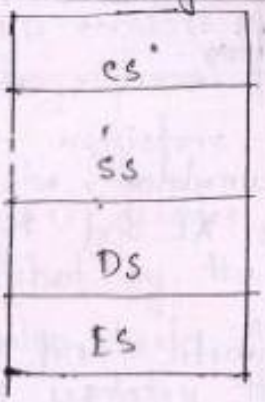
→ CX register is also used for the count of the no. of bits by which the contents of an operand must be shifted or rotated during the execution of the multibit shift or rotate instructions.

Data Register (DX) :—

→ DX register is used in I/O operations to hold the address of I/O port.

→ DX register also holds the remainder after a word division and holds the high-order bits (MSB) of the result after a word multiplication (32-bit).

Segment Registers —



→ There are 4 segment registers in 8086 up. They are code segment (CS), Data segment (DS) stack segment (SS) and Extra segment register (ES).

→ Each of them contains a 16-bit base address that points to the corresponding segment in memory.

→ **Code segment (CS):** —

→ It is used for addressing a memory location in the code segment of memory where the executable program or instructions are stored.

stack segment (SS): —

→ It is used for addressing stack segment of memory which is used to store stack data.

Data segment (DS): —

→ The data segment register points to the data segment of the memory where the data is stored.

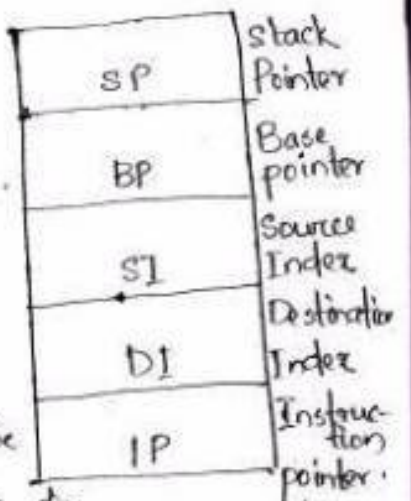
Extra segment (ES): —

→ This register points to the extra segment of the memory. The ES is used as another data segment of memory, which contains data.

Pointers and Index Registers: —

→ There are 3 pointers in 8086 up. They are,

Instruction pointer (IP)
Base pointer (BP)
Stack Pointer (SP)



→ The pointers and index registers contain the offset addresses of memory locations relative to

the segment registers.

→ Instruction Pointer (IP) –

→ The function of IP is similar to a program counter, but it contains the offset address instead of the actual address of the next instruction.

→ IP contains the offset address within the codesegment.

→ IP is combined with the cs to generate the address of the next instruction to be executed.

→ Stack Pointer (SP) —

→ The contents of SP are used as offset from the current value of stack segment (ss) during the execution of instructions that involve the stacksegment.

Base Pointer (BP) —

→ BP also contains the offset within the stack segment (ss). BP contains the offset in the based addressing mode.

→ There are two index registers in 8086 microprocessor. They are:- Source Index register (SI)
Destination Index register (DI)

→ The index registers are used as general purpose registers as well as for offset storage purpose.

→ The SI register is used to store the offset of source data in data segment and DI register is used to store the offset of destination data in data or extra segment.

→ Default segment and offset registers :-

Segment	Offset
CS	IP
SS	SP or BP
DS	BX, SI or DI
ES	DI

Flag Register :-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V	X	X	X	O	D	I	T	S	Z	X	AC	X	P	X	CY

→ 8086 microprocessor has a 16-bit flag register which contains 9 active flags. The flag register can be divided into two parts.

1. Conditional flags
2. Machine control flags.

→ The conditional or status flags are set or reset on the basis of the result generated from the ALU.

→ The lowerbyte of the flag register along with the overflow flag (O) contains the conditional flags.

→ The control flags contain 3 flags like direction flag (D), Interrupt flag (I) and trap flag (T).

→ These flags are used to control the program flow and for controlling the microprocessor.

CY - Flag —

→ This flag is set when there is a carry from the MSB in case of addition or a borrow in case of subtraction.

i.e carry from D_{15} bit for 16-bit operation.
" D_7 bit for 8-bit operation.

P - Flag

→ Parity flag is set when the ALU output has even parity and is reset when the ALU output has odd parity.

→ Parity is the count of 1's in a number.

AC - Flag

→ The AC flag is set when there is a carry after addition and borrow after subtraction between D_3 and D_4 bit positions (for 8-bit data) and carry from D_7 - D_8 (for 16-bit data)

Zero (Z) - Flag

→ The Z flag shows that the result of an ALU operation is zero or ~~any other~~ non zero.

→ If Z = 1, the result is zero.
Z = 0, the result is nonzero.

S - Flag

→ This flag is set, when the result of any ALU operation is positive or negative.

→ The MSB of the result shows the sign bit.

→ If the sign bit = 0, the no. is positive
= 1, the no. is negative.

for 8-bit operation, D_7 bit represents the sign bit
16-bit operation, D_{15} bit " "

Overflow Flag –

→ It is based on the (n-1) bit carry of the result.
→ Over flow occurs when signed nos. are added or subtracted.
→ If the result of a signed operation is large enough to be accomodated in a destination register, then overflow occurs.
→ i.e for 8-bit signed operation,

if there is a carry from D_6 – D_7 bit
OF is set (1).

for 16-bit signed operation,

if there is a carry from D_{14} – D_{15} bit of the result
OF is set (1).

e.g. +127 = 7F = 0111 1111
+01 +01 = 0000 0001
1000 0000 (80H)
OF = 1 (set)
(as there is a carry from D_6 – D_7 bit).

Trap Flag :–

→ The TF = 1 (set), when the 8086 processor enters into the single step mode.
or else it is reset.
→ In single step mode the processor executes one instruction at a time and it is useful for debugging the programs.

Interrupt Flag :- (IF)

→ This flag (IF) is set (1), when the maskable interrupt or INTR is received by the processor.

→ IF = 1 (set), if the INTR pin is enabled.
= 0 (Reset), if the INTR pin is disabled.

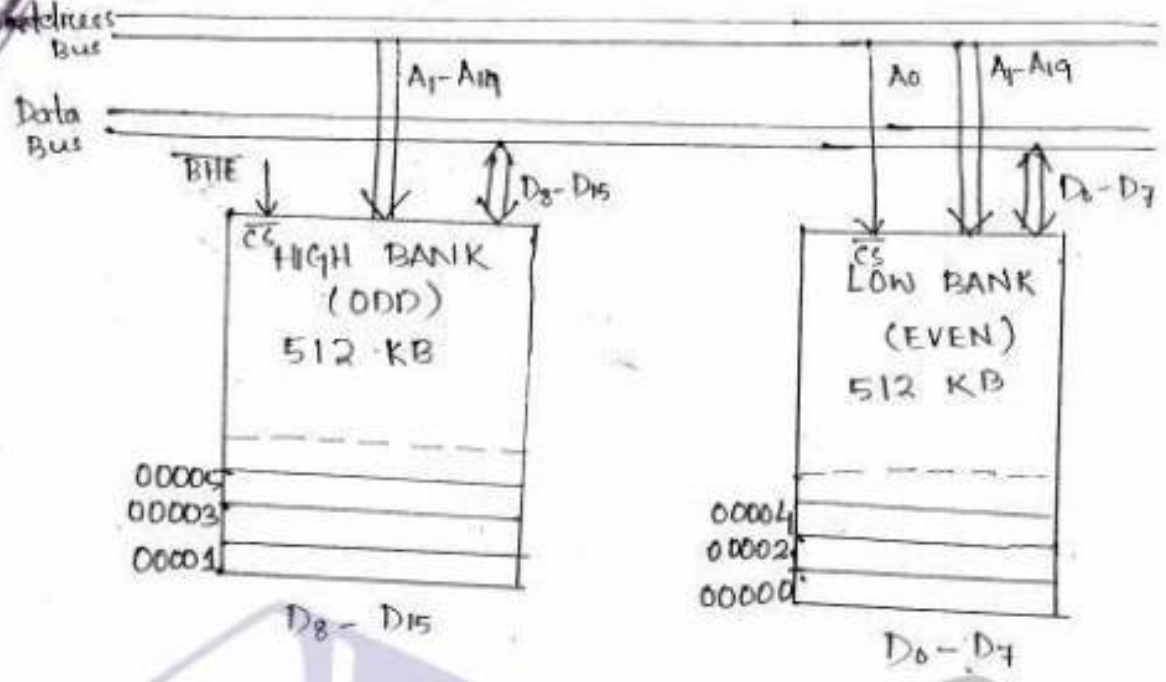
Direction Flag :- (DF)

→ DF is used for string manipulation instructions. i.e the direction flag selects the increment or decrement mode for DI and SI registers in string instructions.

→ If, DF = 1 (set), the registers are automatically decremented.

= 0 (Reset), the registers are automatically incremented.

Physical Memory Organisation :-



→ In 8086 based system, the 1M bytes memory is physically organised as odd bank and even bank each of 512 kbytes, addressed in parallel by the processor.

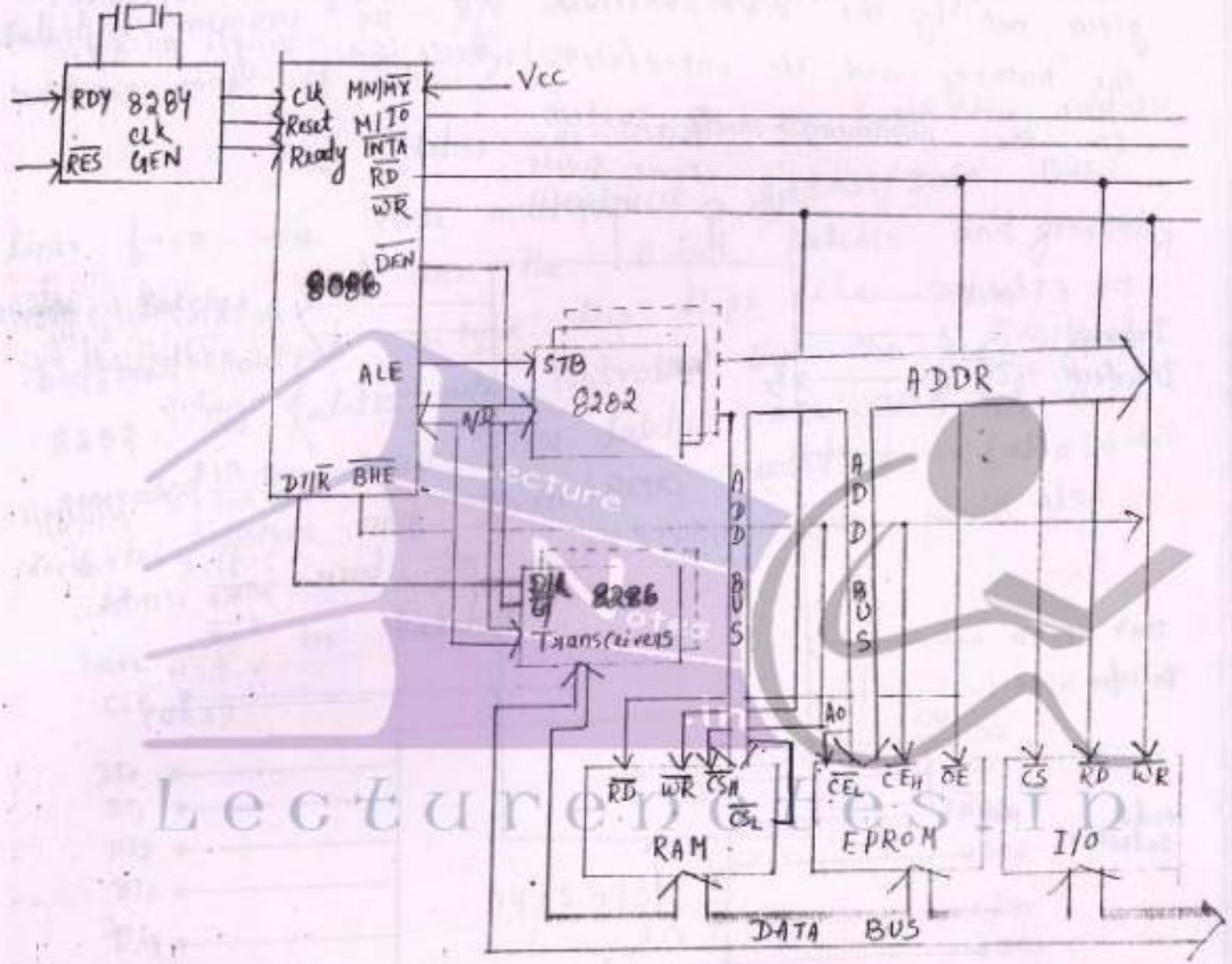
→ The lower bank (even bank) contains bytes with only even addresses like 0, 2, 4 etc. whereas the higher bank (odd bank) contains bytes with only odd addresses like 1, 3, 5 etc. i.e location 0 will have the address 1, location 1 will have the address 3, location 2 will have the address 5 etc.

→ The data lines of the lower bank is connected to D0-D7 of 8086 whereas the data lines of upper bank is connected to D8-D15 of 8086.

⇒ The lowerbank is selected by A0, where as the upper bank is selected by $\overline{BHE}$.

11 D

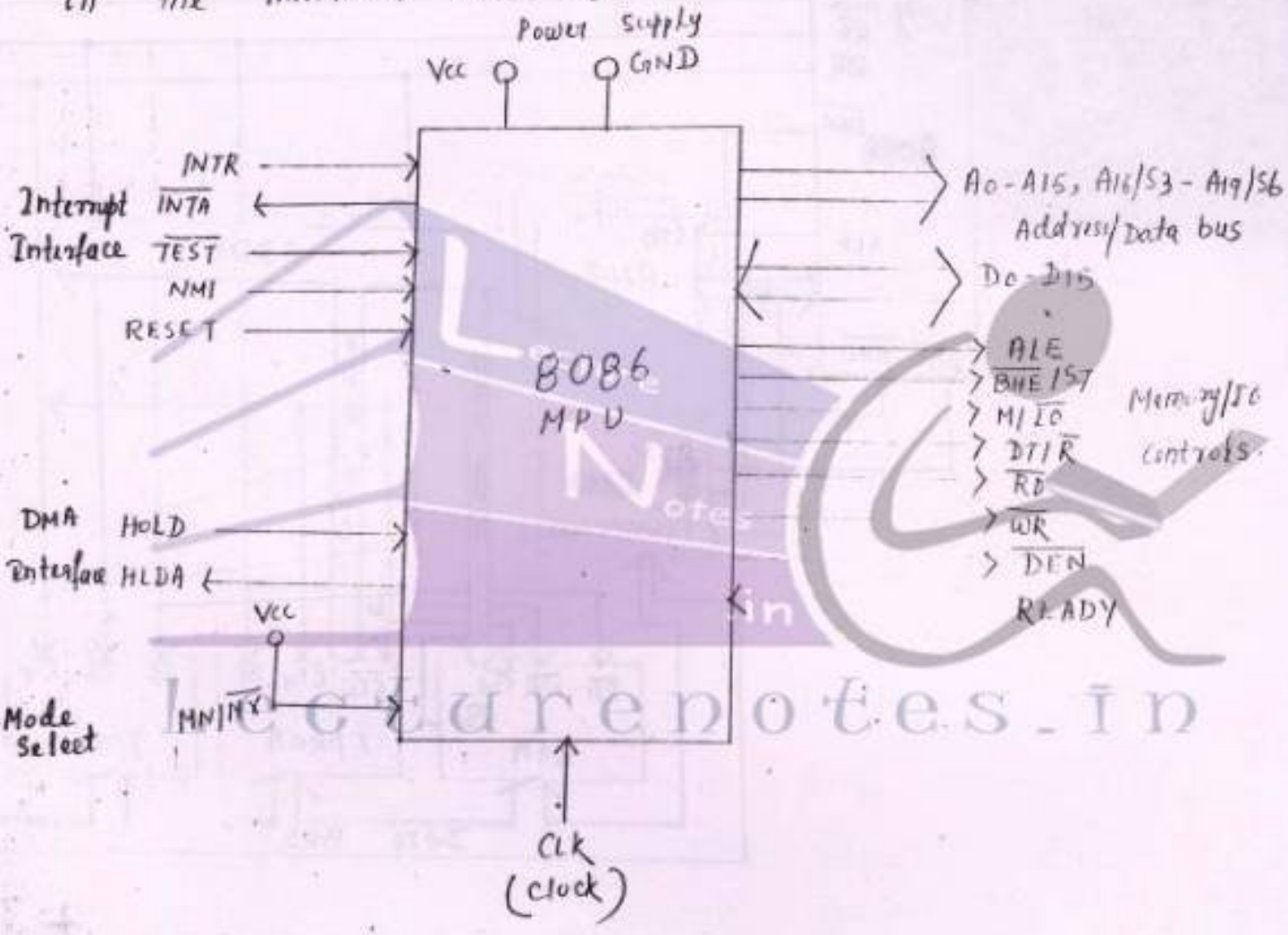
(6)



Minimum Mode 8086 System

MINIMUM MODE 8086 SYSTEM

In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its $MN/\overline{MX}$ pin to logic 1. In this mode, all the control signals are given out by the microprocessor chip itself, to implement the memory and I/O interfaces. There is a single microprocessor in the minimum mode system.



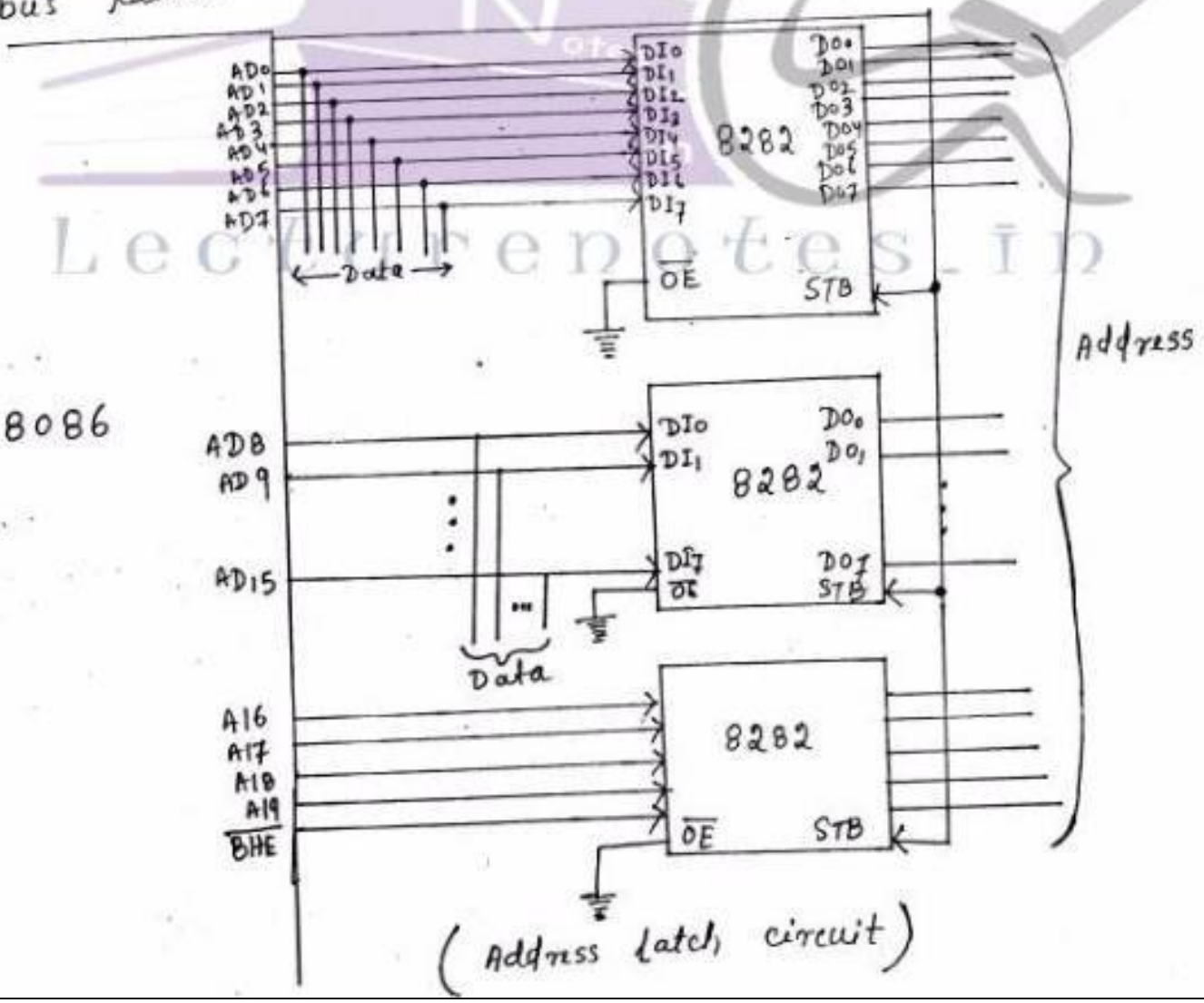
Block diagram of Minimum-mode 8086 MPU.

Mindfire is a software service provider,
with unrelenting focus on optimal software development
and delivery.

There is a single Microprocessor in the minimum mode system. The remaining components in the system are latches, transceivers, clock generator, memory and I/O devices. Chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.

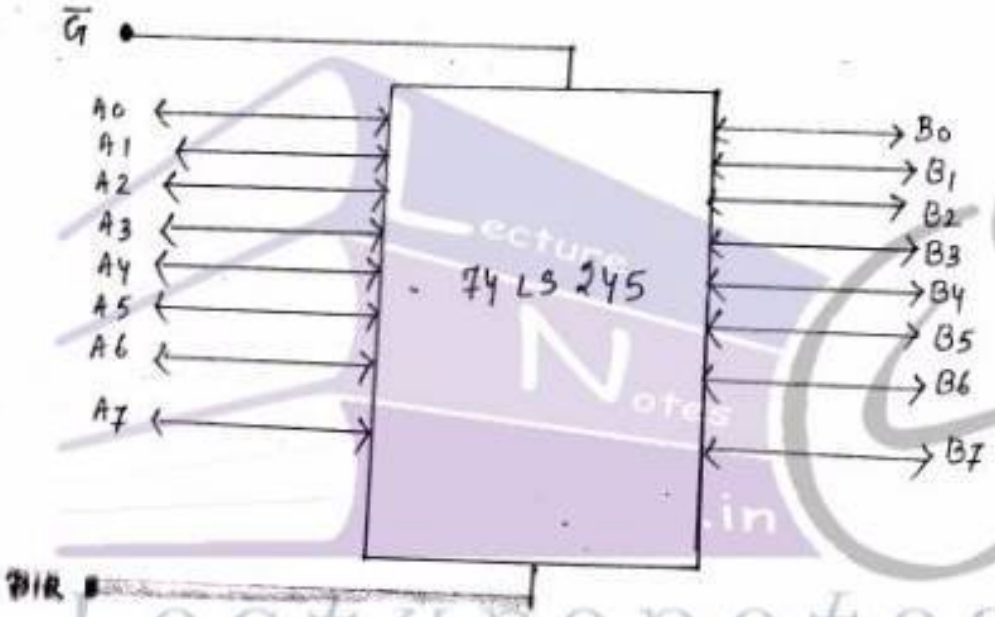
The latches are used to latch the address lines from the time multiplexed Address/Data Bus. The latches used are the 8-bit latches and generally buffered output D-type flip flops like 74LS373 or 8282. The latches are controlled by the ALE signal generated by 8086. Two latches are needed if a full 20-bit address is used. In 8086, the $\overline{BHE}$ would also have to be latched.

The octal latch accepts eight inputs D_{I0} through D_{I7}. As long as the clock (CLK) input is at logic 1, the outputs of D-type flip flops follow the logic level of data applied to their corresponding inputs. When CLK is switched to logic 0, the current contents of D-type flip flops are latched. The latched information in the flip flops are not output at data outputs D_{O0} through D_{O7} unless the output enable ($\overline{OE}$) input is at logic 0. If $\overline{OE}$ is at logic 1, the outputs of the latch are in high impedence state. In 8086, the 20 address lines ((AD0 - AD15), A16 - A19) and Bus High Enable signal $\overline{BHE}$ are normally latched in the address bus latch.



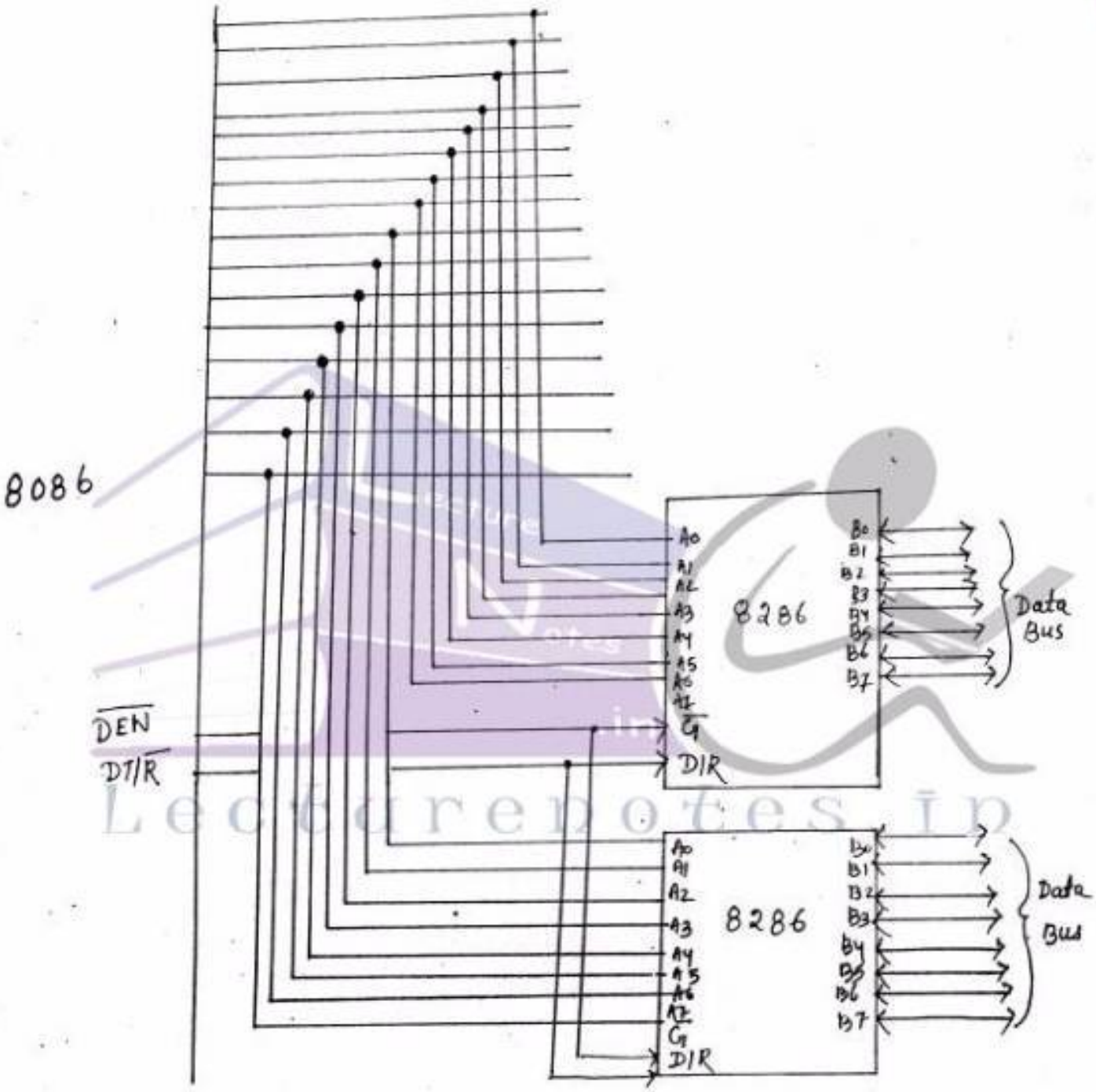
(Address latch circuit)

Transceivers (driver / receiver) are bidirectional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signal. In 8086, the 74LS 245 or the Intel 8286 (octal bus transceivers) are needed. They contain 16 tristate buffers, eight receivers and eight drivers. In 8086, two transceivers are required as it has 16-bit data lines.



The bidirectional input/output lines are called A0 through A7 and B0 through B7. The $\overline{G}$ input is used to enable the buffer for operation. The $\overline{DEN}$ of 8086 is connected to $\overline{G}$ of the transceiver. The $\overline{DEN}$ indicates valid data is available on the data bus. On the other hand, the logic level at the direction (DIR) input selects the direction in which data are transferred through the device. For instance, logic 1 at this input sets the transceiver to pass data from A lines to B lines. Switching DIR to logic 0 reverses the direction of data transfer.

Here the DIR input is driven by the signal data transmit/ receive ($DT/\overline{R}$).



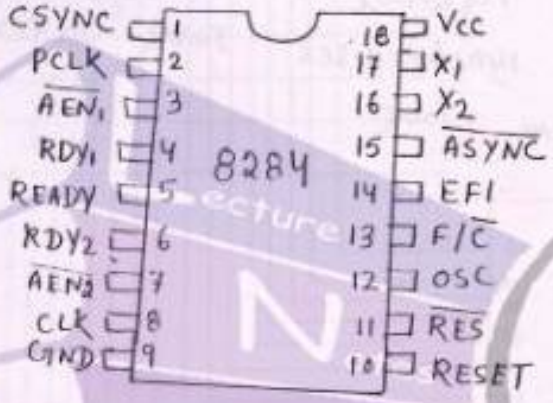
The system contains for the monitor and users pro storage. EPROMS are used for monitor storage, while R for users program storage. The system contain I/o devi for communication with the processor as well as some special purpose I/o devices.

The next component, other than the processor, that appears in the system is an 8284 clock generator. The clock generator generates the clock from crystal oscillator and then shapes it and divides it to make it more precise so that it can be used as an accurate timing reference for the system. The clock generator also synchronises some external signals with the system clock.

CLOCK GENERATOR (8284)

The 8284 provides the following basic functions or signals to 8086 microprocessor.

1. Clock generation.
2. RESET Synchronization
3. READY Synchronization



(PIN DIAGRAM OF 8284)

$\overline{AEN_1}$ and $\overline{AEN_2}$

The Enable pins are provided to qualify the bus ready signals, RDY_1 and RDY_2.

RDY_1 and RDY_2

The bus ready inputs are provided in conjunction with $\overline{AEN_1}$ and $\overline{AEN_2}$ pins to cause wait states in an 8086-based system.

ASYNC

The ready synchronization selection input selects either one or two stages of synchronization for RDY_1 and RDY_2 inputs.

READY

Ready is an output pin that connects to the 8086 READY input. This signal is synchronized with RDY_1 and RDY_2 inputs.

X_1 and X_2

The crystal oscillator pins connect to an external crystal used as the timing source for the clock generator and all its functions.

$F/\overline{C}$

The frequency/crystal select input chooses the clocking source for 8284. If this pin is held high, an external clock is provided to the EFI input pin; if it is held low, the internal crystal oscillator provides the timing signal.

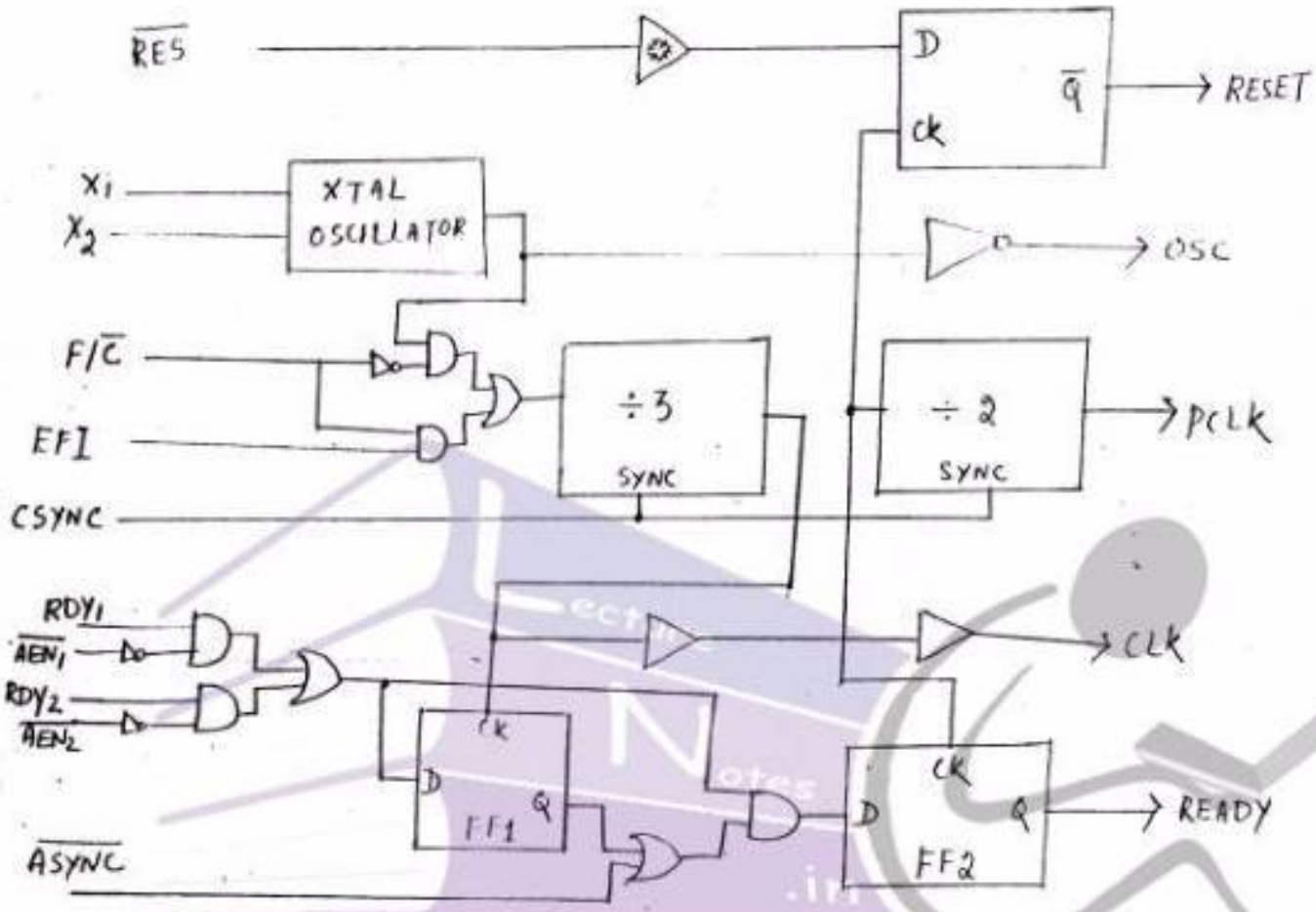
EFI

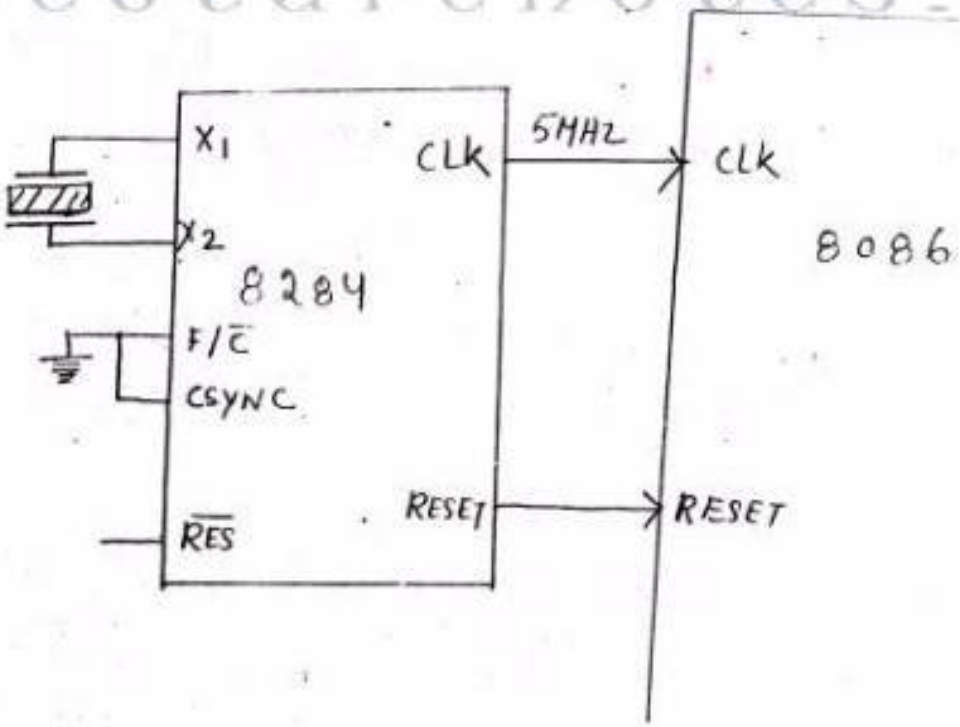
The external frequency input is used when the $F/\overline{C}$ pin is pulled high. EFI supplies the timing.

CLK

The clock output pin provides the CLK input signal to the 8086 microprocessor. The CLK pin has an output signal that is one-third of the

Operation of the 8284





crystal or EFI input frequency.

PCLK

The peripheral clock signal is one-sixth the crystal or EFI input frequency. The PCLK output provides a clock signal to the peripheral equipment in the system.

OSC

The oscillator output is also at the same frequency as the crystal or EFI input. The OSC output provides an EFI input to other 8284 clock generator.

RES

The reset input is an active low input to 8284.

RESET

The reset output is connected to 8086 RESET input pin.

CSYNC

The clock synchronization pin is used when the EFI input provides synchronization in systems with multiple processors. If the internal crystal oscillator is used this pin must be grounded.

GND Grounded

Vcc +5.0V ± 10% power supply.

Power Saving Options :—

→ The power requirement of a microprocessor board is a very important aspect so while designing the power supply, there are many issues to be considered.

→ There are power saving methods based on oscillator frequency, power-down and idle modes supported by the microcontroller device.

Fully static Operation –

→ The operating frequency of Atmel devices are 0 to 24MHz.

→ The important factors in selecting the oscillator frequency are the power dissipation and the speed of operations required.

→ Again, in few other applications, the power available for operating the instrument itself is limited e.g in battery operated instruments, the power consumption must be as low as possible.

→ In smart tx in instrumentation engineering applicati the power as well as signal (4-20 mA) both are transmitted over the two wires.

→ 4mA multiplied by the power supply voltage gives the minimum power available.
For a 24V supply, this comes to 0.95 mW. These the entire power consumption of the tx ckt must be well within 0.96 mW. so considering this, the operating frequency of the processor may be designed.

→ In larger timing generation application, the low freq. operation is justified.

Mindfire is a software service provider,
with unrelenting focus on optimal software development
and delivery.

Idle and Power Down Modes :-

→ Idle Mode —

→ It allows the CPU to sleep, but the on-chip peripherals remain operational. The internal-clock signal to CPU is gated off. Again, clock to timer, interrupt and serial port function continues.

→ The contents of on-chip RAM and all SFRs and complete CPU status including the program counter, PSW, stack pointer, Acc. are preserved. ie if a port pin is used to activate a solenoid valve, its state will continue to be the same even though the idle mode is initiated during the operation.

→ Again, Port 0 pins will float and port 2 will have address in case of external program memory and ALE and $\overline{PSEN}$ pins will be high.

→ Again, to enter into the processor's idle mode, there are many ways.

* An enabled interrupt can do this or hardware RESET may awake the processor out of idle mode. Activation of an enabled interrupt will cause the IDL bit in PCON to be cleared by the hardware and terminating the IDLE mode. Again RETI instruction puts the device into IDLE mode.

→ While returning from IDLE mode the program control goes to from where it entered into the IDLE mode before the RESET operation takes control over within 2 machine cycles.

Power-down Mode -

→ Here the oscillator is frozen and no clock is generated. Onchip RAM, SFRs maintain their values. Hardware RESET is the only way to come out of power down mode.

→ Reset activity will modify SFRs but the onchip RAM is preserved. Vcc can be reduced after entering into the power down mode to minimize power consumption.

→ Before activating RESET into operation, Vcc level must be ensured. Further RESET must be held active long enough to allow the oscillator to stabilize.

Mindfire is a software service provider,
with unrelenting focus on optimal software development
and delivery.