8/10/2017

# MODULE-6

## Basic principles of switching

Switches are devices capable of creating temporary connection b/w two / more devices linked to the switch. Some of them are connected to the n-system and others are used for routing

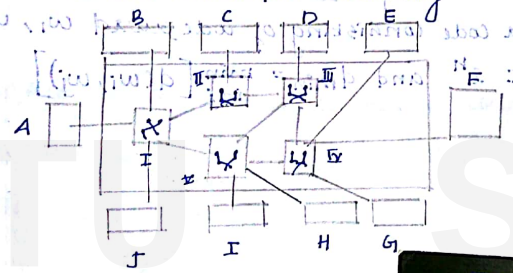
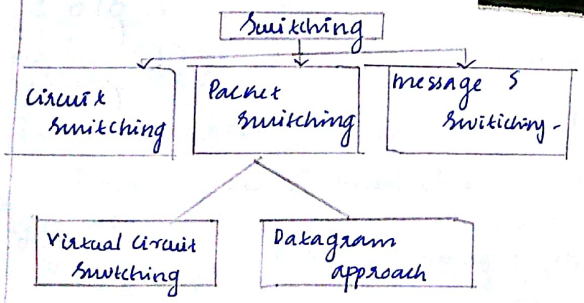
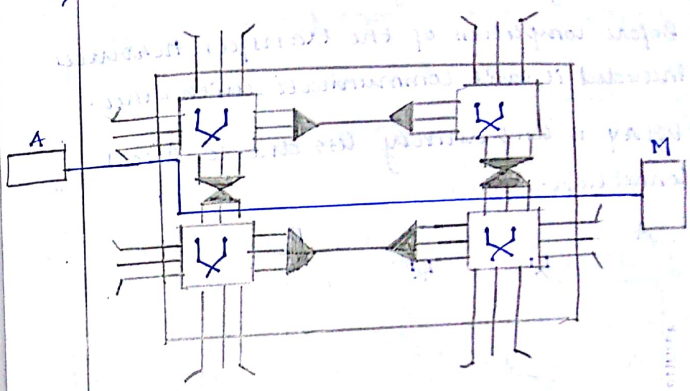



Fig. Switched ~~hardware~~ network.






→ Circuit switched network




→ Three phases:

1. Connection setup initialise
2. Data transfer
3. Connection teardown ... disconnected



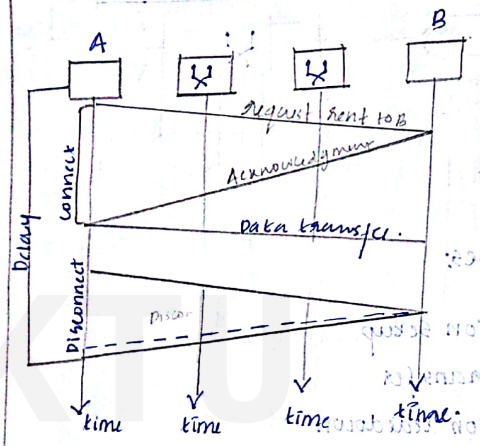
- A devices send a request to M if M is ready then it gives a acknowledgment then there is a data path
- Data path exist till ~~it~~ it completes the transferring after completion it disconnects

→ Efficiency of circuit switched n/w

It is not much efficient compared to technique.

(Switching)

- Before completion of the transfer resources included it can't communicate with other.
- DELAY is comparitively less due to direct connection.

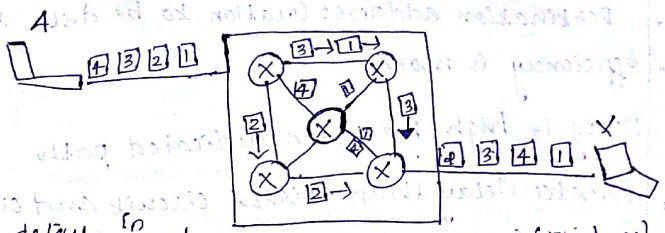



9/11/17 ② Packet Switching :-

① Datagram
② Virtual circuit

DATAGRAM network

- Packet is datagram.




A delay in n/w with four switches (Routers)

- Packets are transmitted randomly without any order.
- It is a connectionless approach (bcz this switch doesn't give information about the connection state.
- Implement in network layer.
- Routing table is present in every routers.

Routing table contains destination and packets.

| Dest address | o/p Port |
|---|---|
| 1232 | 1 |
| 4150 | 2 |
| 9130 | 3 |

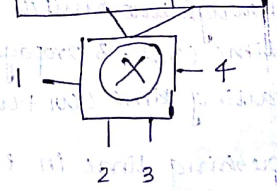
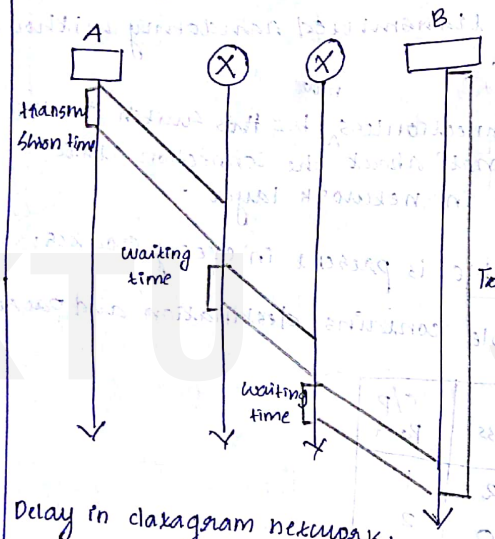



fig: Routing table in datagram network

- Destination address: location to be data tra
- Efficiency is more.
- Delay is high bcz not a dedicated path
- Greater delay than virtual circuit and circuit switching.




Delay in datagram network.

Here the packet travel through two switch there are three transmission time (3T), 3 propogation delay (3τ) and two waiting time ($w_1 + w_2$) while ignoring the processing time in each switch.

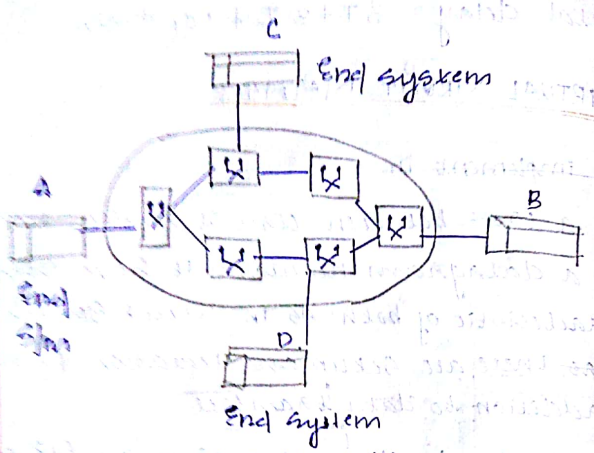
Total delay = $3T + 3\tau + w_1 + w_2$

## VIRTUAL CIRCUIT NETWORK



~~It is implement in~~

- It is a cross between circuit switch network and a datagram network. It have some characteristic of both. As in circuit switch ~~it has~~ there are setup and teardown phases in addition to data transfer
- Resources can be allocated during the setup phases as in a circuit switched network or on demand as in a datagram network.
- As in a datagram network data are packetized and each packet carries an address in the header. But the header has local jurisdiction not an end to end jurisdiction
- As in circuit switched n/w all packet follow same path established during the connection
- A virtual circuit network is normally implement in datalink layer while circuit switched n/w is implemented in physical layer and datagram n/w in the n/w layer.




→ OSI model 7 layers.

| | |
|---|---|
| Physical layer | — circuit switching |
| Datalink | — Virtual circuit |
| N/w layer | — Datagram. |
| Transport | — TCB |
| Session layer | — End to end connect° |
| Presentation | |
| Application layer. | |

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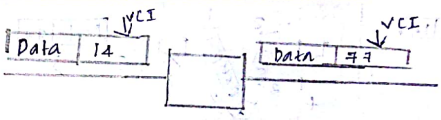
## Addressing

→ Global addressing.

→ Virtual circuit identifies

- local juricial / virtual valid addressing
- Globaly valid addressing is Global addressing

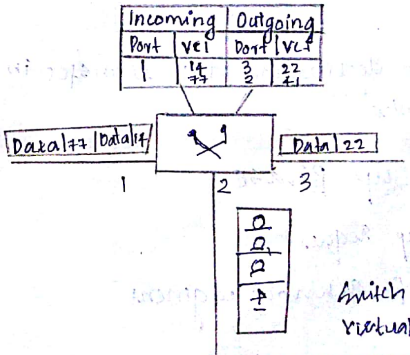
Virtual circuit identifies




THREE PHASES

* Set up phase
* Teal down phase
* Data transfer.

DATA TRANSFER PHASE

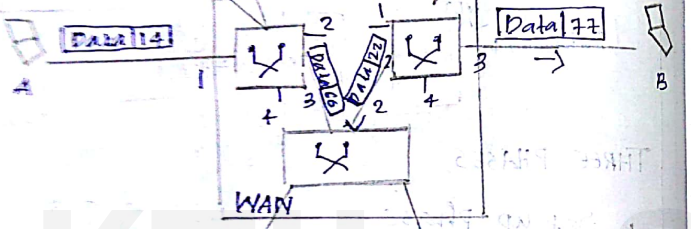



Switch and table in a virtual circuit n/w.

## Addressing

| Incoming | | Outgoing | |
|---|---|---|---|
| port | VCI | port | VCI |
| 1 | 14 | 3 | 66 |

| Incoming | | Outgoing | |
|---|---|---|---|
| port | VCI | port | VCI |
| 2 | 22 | 3 | 77 |




| Incoming | | outgoing | |
|---|---|---|---|
| Port | VCI | Port | VCI |
| 1 | 66 | 2 | 22 |

Source to destination data transfer in a virtual circuit n/w

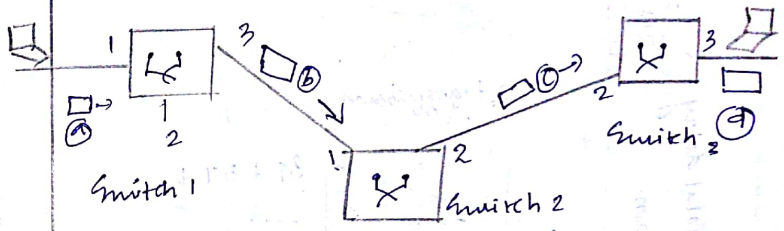
### Set up Phase

* Set up request
* Set up acknowledgment

→ **Set up request:**

| Incoming | | Outgoing | |
|---|---|---|---|
| Port | VCC | Port | VCI |
| 1 | 14 | 3 | |

| Incoming | | outgoing | |
|---|---|---|---|
| Port | VCI | Port | VCI |
| 2 | 22 | 3 | |



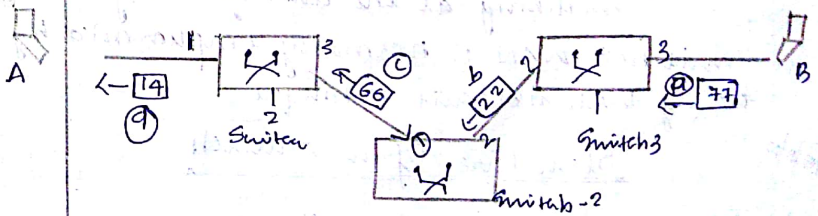

| Incoming | | outgoing | |
|---|---|---|---|
| Port | VCC | Port | VCC |
| 1 | 66 | 2 | |

Set up request in virtual circuit n/w.

→ **Set up Acknowledgment**

| Incom | | outgo | |
|---|---|---|---|
| Port | VCC | Port | VCI |
| 1 | 14 | 3 | 66 |

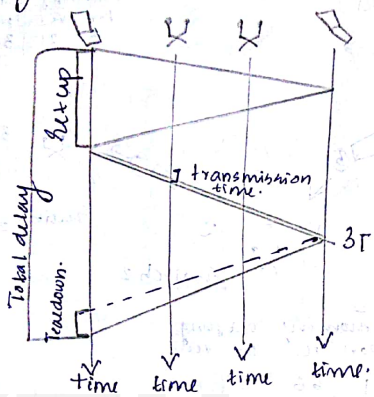
| Incoming | | outg | |
|---|---|---|---|
| Port | VCI | Port | VCI |
| 2 | 22 | 3 | 77 |




| Incoming | | outgo | |
|---|---|---|---|
| Port | VCI | Port | VCI |
| 1 | 66 | 2 | 22 |

Setup act in virtual circuit network.

- Efficiency is high compared to others.
- Delay in virtual circuit n/w.




Total delay = 3x + 3 T + setup delay + teardown delay

- Circuit switched technology in WAN

Switching at the datalink layer in a switched WAN is normally implemented by using virtual circuit technique.

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## Structure of a Switch

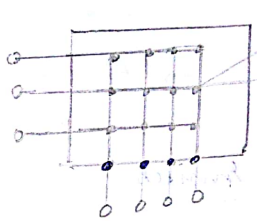
→ Structure of a circuit switch.

1) Two space division switch
2) Time division switch.

→ Space Division Switching

* Crossbar Switch
* Multi Stage Switch.

→ Crossbar Switch.

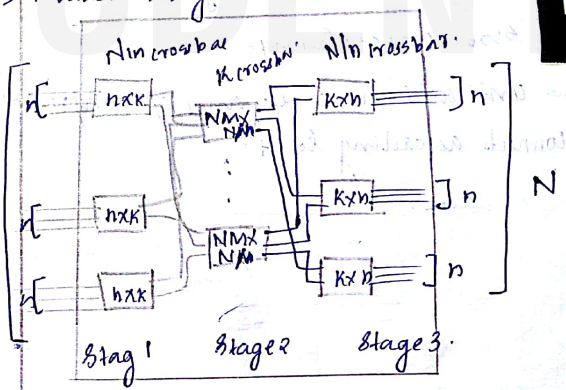


To control station.

- Cross points

To reduce no: of crosspoints we introduce next methods. ie

→ Multi Stage Switch.




multistage switch.

At stage-1 N/n (nxk) switches

At stage-2 we use k (N/n x N/n) switches

At stage-3 we use N/n (kxn)

$= N/n(nxk) + k(N/n+N/n) + N/n(kxn)$

$= 2kN + k(N/n)^2$

$N^2 > 2kN + k(N/n)^2$

⇒ Time division switch

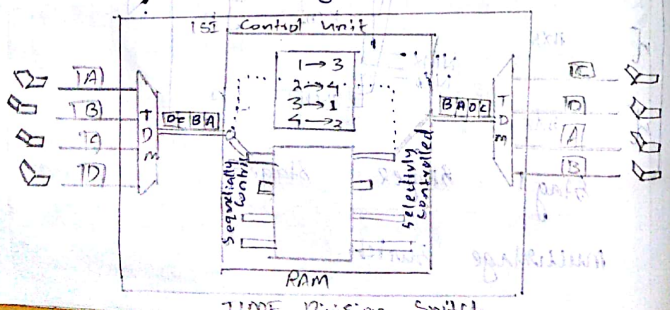
Time slot is the intelligent core portion.

* Time slot Interchange
* Time Division multiplexing.

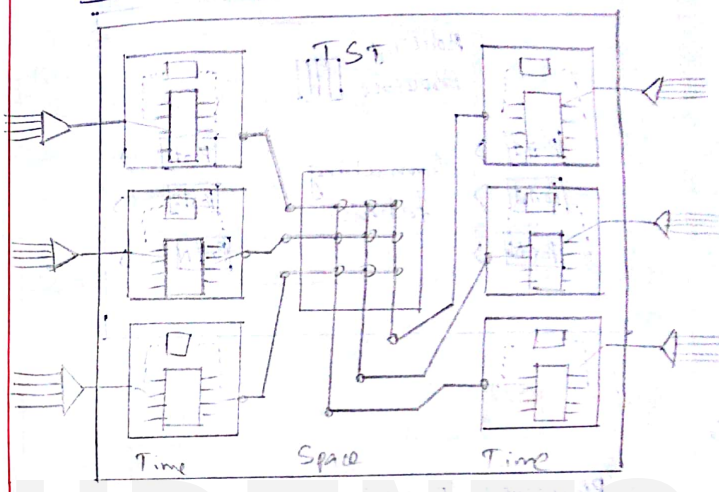
Fig: Time slot interchange.

Control unit will have i/p and o/p information

RAM connects according to it.




Time and space Division Switch

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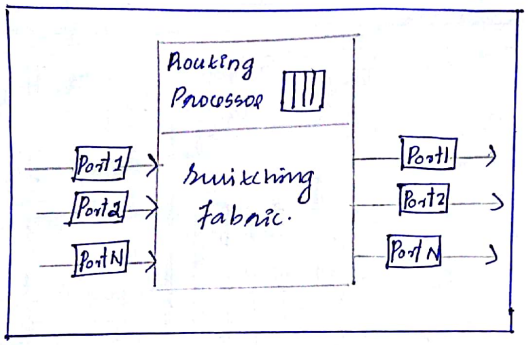
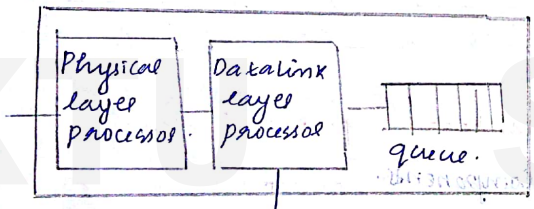
Structure of packet switch.

Four components.

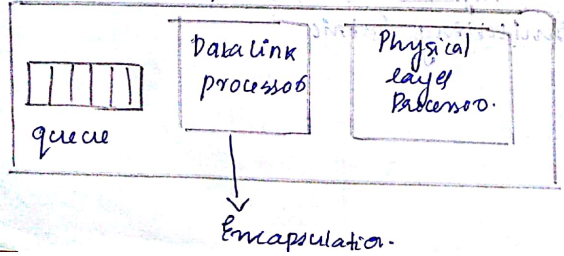
* Input port
* Output port
* Routing processor
* Switching fabric




Input port




Output port



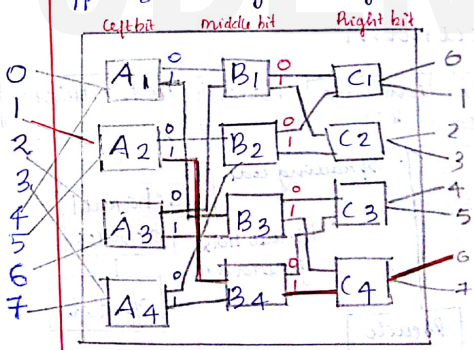

## Routing processor.

Routing processor performs the functions of network layer the destination address is used to find the address of the next hoppe & the o/p port number from which a the packet is sentout and this process is referred to as table lookup-up because the routing processor searches a the routing table

## Switching fabric:

1) Crossbar switch
2) Banyan switch

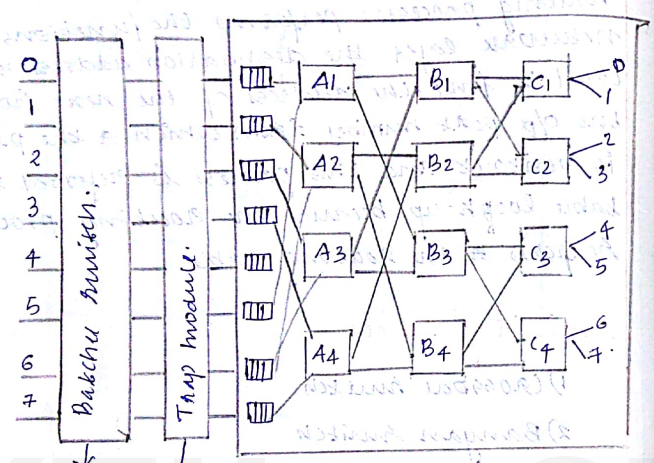
i/p = N , stage = $\log_2(N)$ → stage → n/2 switches
i/p = 8 , stage = $\log_2(8)$ = 2 no:of switches = 4



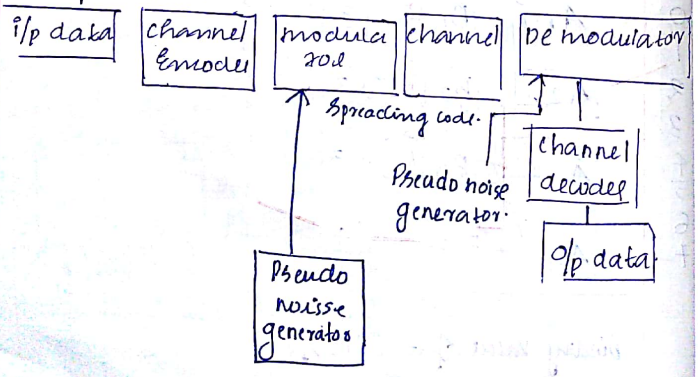

To get o/p = 6 ie i/p

Binary value of 6 $(110)_{BO}$

## Batcher- Banyan Switch.




## Concept of Spectrum




→

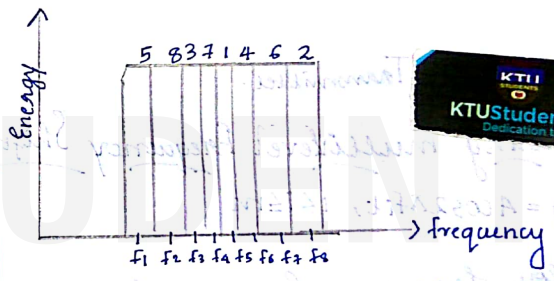
## General model of Spread Spectrum digital communication system.

1. Frequency hopping spread spectrum [FHSS]
2.

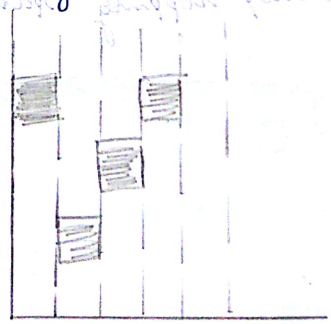
### FHSS

Spectrum with different frequencies.

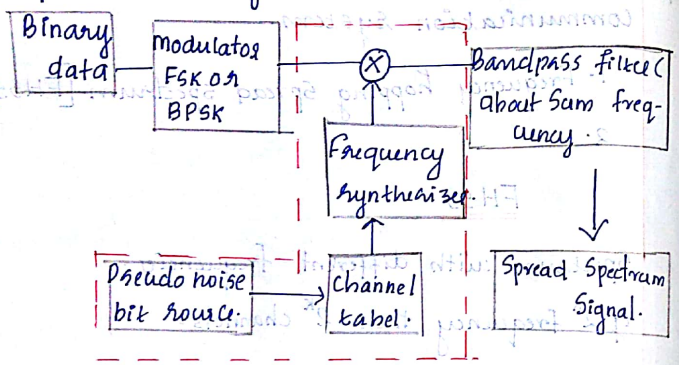
If $2^k$ frequency then $2^k$ channels.




Spreading code - 5 8 3 7 1 4 6 2



Input will be digital data




Transmitter.

⇒ FHSS using multilevel Frequency Shifting

$S_i(t) = A\cos 2\pi f_i t, \quad 1 \le i \le m$

1. Slow frequency hopping Spectrum: $T_c \geq T_s$
2. Fast frequency hopping Spectrum: $T_c < T_s$

FHSS performance consideration

Ratio of signal Energy Per bit $\frac{ED}{N_j} = \frac{G_{bwd}}{S_j}$

$S_j$: Jammer noise power

The gain in signal to noise ratio/ processing gain $= 2^k = \frac{\omega_s}{\omega_d}$