#### **BHARAT ACHARYA EDUCATION**



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### **ADDRESSING MODES OF 8051**

Addressing Modes is the manner in which operands are given in the instruction. 8051 supports the following 5 addressing modes:

### 1) IMMEDIATE ADDRESSING MODE

In this addressing mode, the **Data** is given **in** the **Instruction** itself. We put a "#" symbol, before the data, to identify it as a data value and not as an address.

**Eg:** MOV A, #35H ;  $A \leftarrow 35H$ 

MOV DPTR, #3000H ; DPTR ← 3000H

### 2) REGISTER ADDRESSING MODE

In this addressing mode, **Data** is given by **a Register** in the instruction.

The permitted registers are **A**, **R7** ... **R0** of each memory bank.

Note: Data transfer between two RAM registers is not allowed.

**Eg:** MOV A, R0 ;  $A \leftarrow R0$  ... If R0 = 25H, then A gets the Value 25H.

MOV R5, A ;  $R5 \leftarrow A$ 

MOV Rx, Ry ; NOT ALLOWED. That's because this would allow 64 combinations of registers

; As registers invite opcodes, this would need 64 opcodes!

# 3) DIRECT ADDRESSING MODE

Here, the **address** of the operand is given **in** the **instruction**.

Only Internal RAM addresses (00H...7FH) and SFR addresses (from 80H to FFH) allowed.

**Eg:** MOV A, 35H ;  $A \leftarrow Contents \ of \ RAM \ location \ 35H$ 

MOV A, 80H ;  $A \leftarrow Contents \ of \ Port \ 0 \ (SFR \ at \ address \ 80H)$ 

MOV 20H, 30H ; [20H] ← [30H]

; i.e. Location 20H gets the contents of Location 30H

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## 4) INDIRECT ADDRESSING MODE

Here, the address of the operand is given in a register.

Internal RAM and External RAM can be accessed using this mode.

The advantage of giving an address using a register is that we can increment the address in a loop, by simply incrementing the register, and hence access a series of locations.

### INTERNAL RAM: (8-BIT ADDRESS GIVEN BY RO OR R1)

**ONLY R1 or R0**, called as *Data Pointers*, can be used to specify **address** (00H ... 7FH). An "@" sign is present before the register to indicate that the register is giving an address.

Eg: MOV A, @R0 ;  $A \leftarrow [R0]$ 

; i.e.  $A \leftarrow Contents$  of Internal RAM Location whose address is given by R0. ; if R0 = 25H, then A gets the contents of Location 25H from Internal RAM

MOV @R1, A ;  $[R1] \leftarrow A$  i.e. Internal RAM Location pointed by R1 gets value of A.

## EXTERNAL RAM: (16 BIT ADDRESS GIVEN BY DPTR)

For the **External RAM, address** is provided by **R1 or R0,** or by **DPTR**. If DPTR is used to give an address, then the full 64KB range of External RAM from 0000H... FFFFH is available. This is because DPTR is 16-bit and  $2^{16} = 65536$ . An "X" is present in the instruction, to indicate External RAM.

Eg: MOVX A, @DPTR ;  $A \leftarrow [DPTR]^{\wedge}$ 

; A gets the contents of External RAM Location whose address is given by DPTR ; If DPTR = 2000H, then A gets contents of Location 2000H from External RAM

MOVX @DPTR, A :  $[DPTR]^{\wedge} \leftarrow A$ 

; i.e. A is stored at the External RAM Location whose address is given by DPTR

# EXTERNAL RAM: (8 BIT ADDRESS GIVEN BY RO OR R1)

If R0 or R1 is used to give an address, then only the first 256 locations of External RAM is available from 0000 H to 00FF H. This is because R0 or R1 are 8-bit and  $2^8$  = only 256.

Eg: MOVX A, @R0 ;  $A \leftarrow [R0]^{\land}$ 

; i.e. A gets the contents of External RAM Location whose address is given by R0; If R0 = 25H, then A gets contents of Location 0025H from the External RAM

MOV**X** @R1, A ;  $[RI]^{\wedge} \leftarrow A$ 

; i.e. A is stored at the External RAM Location whose address is given by R1

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### 5) INDEXED ADDRESSING MODE

This mode is used to access data from the Code memory (**Internal ROM** or **External ROM**). In this addressing mode, address is indirectly specified as a "SUM" of (A and DPTR) or (A and PC).

This is very useful because ROM contains permanent data which is stored in the form of Look Up tables. To access a Look Up table, address is given as a SUM or two registers, where one acts as the base and the other acts as the index within the table.

A "C" is present in such instructions, to indicate Code Memory.

**Eg:** MOVC A, @A+DPTR ;  $A \leftarrow Contents of a ROM Location pointed by <math>A+DPTR$ .

;  $If DPTR = 0400H \ and \ A = 05H$ ,

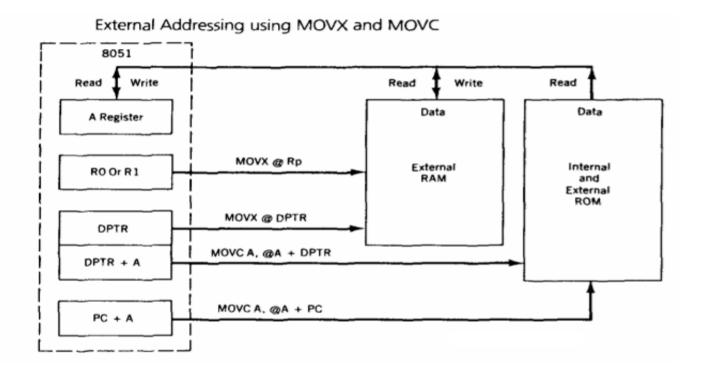
; then A gets the contents of ROM Location whose address is 0405 H.

MOVC A, @A+PC ;  $A \leftarrow Contents of a ROM Location pointed by <math>A+PC$ .

The same instruction may operate on Internal or External ROM, depending upon the address and on the value of  $\overline{\textbf{EA}}$  pin of 8051.

If the address is in the range of 0000... 0FFFH, then  $\overline{\textbf{EA}}$  pin will decide if it operates on Internal ROM or External ROM. IF  $\overline{\textbf{EA}} = 0$ , External ROM else Internal ROM.

If Address is 1000H and more, it will certainly be External ROM.



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