31/10/17

5. Digital Data Communication Techniques

Asynchronous and Synchronous Trasmission

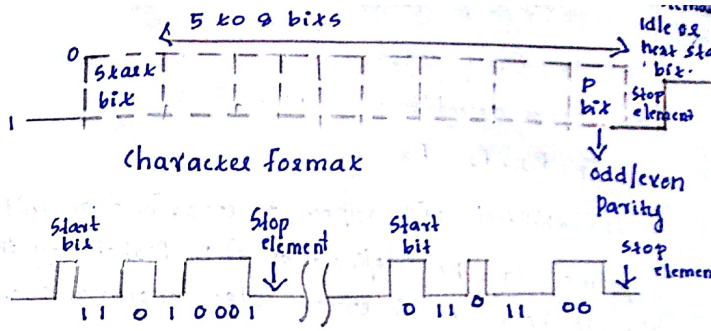
In Serial transmission signalling elements are send down the line one at a time. Each signalling element may be

* 1 bit eg: manchester code.
* 1 bit eg: NRZ, FSK
* more than one bit eg: QPSK

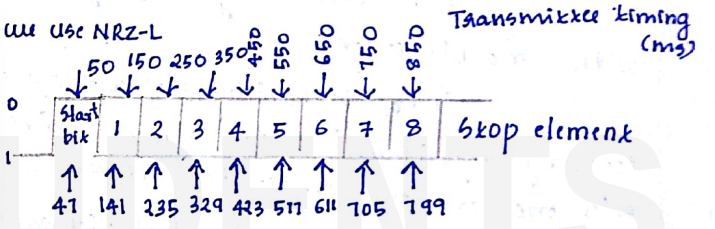
Various transmission impairments will corrupt the signal so that occational errors will occur. Inorder for the receiver to sample the incoming bit properly. it must know the arrival time and duration of each bit that it receives

Asynchronous transmission:

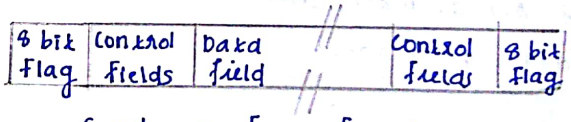
Data are transmitted one character at a time where each character is 5-8 bits in length. Timing / synchronzition must be maintined btw each character. The receiver has the opportunity to synchronise at the beginning of each new character.



8 bit asynchronous character stream.



Synchronous transmission



Synchronous frame format

Types of errors:

* Single bit error
* Burst error

→ Error detection: 3 probabilities.

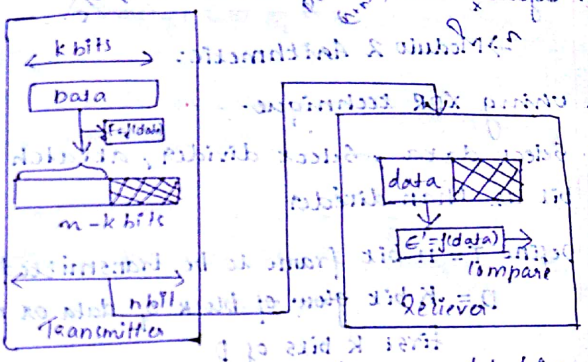
P_0, P_1, P_2, P_3

Probabilities with respect to error in transmitted frame can be defined as 1) P_0 - Probability that a bit retrieved in error also known as the bit error rate (BER)

2) P_1 - Probability that a frame arrive with no bit errors

3) P_2 - Probability that with an error detecting algorithm a wired frame arrives with one or more undetected errors.

4) P_3 - Probability that with an error detecting algorithm wherein a frame arrives with one or more detected bit error but no undetected bit errors.



E = E' = error detecting function.

d = error detecting code

Cyclic redundancy check:

→ error detecting method:

3 methods: 1) Modulo 2 Arithmetic
2) Polynomial
3) digital logic

Given, say D = 1010001101 (10 bits)

Pattern P = 11010 (6 bits)

Res. R = to be calculated (5-bits)

n = 15 ∴ n-k = 5 ∴ k = 10

∴ The message multiplied by

yielding

6/11/17 Cyclic Redundancy Check (CRC)

→ Modulo 2 Arithmetic:

- Using XOR technique.
- Select data, select divider, attatch one (zero) bit less than divider

Define T = n bit frame to be transmitted

D = K bit ~~flow of~~ block of data or msg, the first k bits of D

F = (n-K) bit ~~Forward Correction Sequence~~ [FCS] Frame check sequence (FCS), the last n-k bit of T

P = Pattern of n-k+1 bits this is a predetermined divisor

~~Give~~ $T = 2^{n-K} D + F$

Q → Quotient
R → Reminder

$$\frac{2^{n-K} D}{P} = Q + \frac{R}{P} \quad -①$$

$$T = 2^{n-k} D + R \quad -② \qquad \frac{T}{P} = \frac{2^{n-K} D + R}{P}$$

$$= \frac{2^{n-K} D}{P} + \frac{R}{P} = Q + \frac{R}{P} \text{ (from ①)} \quad (\text{in XOR } = 1+1=0, 0+0=0)$$

$$= Q + 0 = Q$$

1. Given

D = 1010001101 (10 bits)

Pattern, P = 110101 (6 bits)

F = to be calculate (5 bits)

i.e. n = 15, K = 10, n-k = 5.

2. The msg is multiplied by 2^5 yielding 2^5, yielding ~~11010~~ 101000110100000

3. The product is divided by P

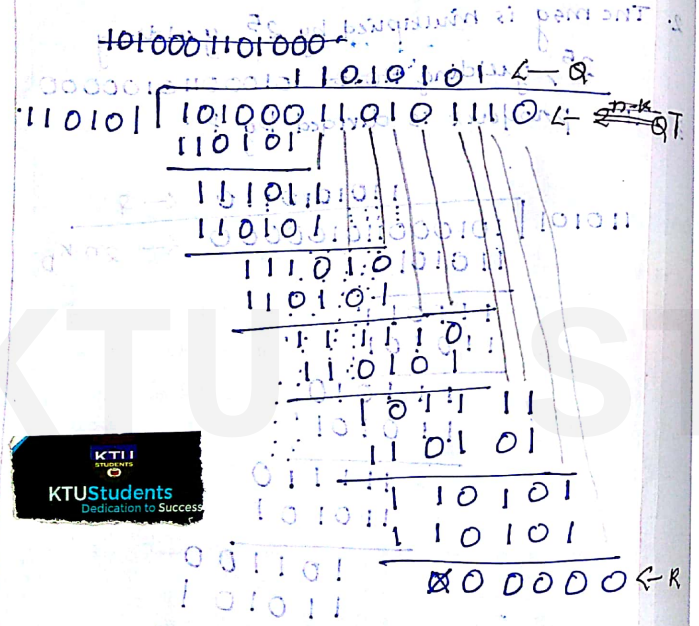
```
                     1101010110   <- Q
110101 | 101000110100000          <- 2^(n-K) D
         110101
         ------
          111011
          110101
          ------
            111010
            110101
            ------
              111110
              110101
              ------
                101100
                110101
                ------
                 110010
                 110101
                 ------
                  01110  <- R
```

~~No~~ Reminder is added to 2^5 D to give.

1010001101 01110

If there is no error the received receives intact

The received frame is divided by 110101



Because there is no remainder it is assumed that there have been no errors.

2) Polynomials:

Express all values as polynomials in a dummy variable x with binary co-efficient. The co-efficient corresponding to the binary number

eg: D = 110011

$D(x) = x^5 + x^4 + x + 1$

eg: 11001

$x^4 + x^3 + 1$

Arithmetic operation is again modulo 2

$$\frac{x^{n-k} p(x)}{p(x)} = Q(x) + \frac{R(x)}{P(x)}$$

$$T(x) = x^{n-k} D + R(x)$$

eg: D = 1010001101

P = 110101

$D(x) = x^9 + x^7 + x^3 + x^2 + 1$

$P(x) = x^5 + x^4 + x^2 + 1$

To find the ogmand dataword left shift the data word 5 bits. Multiplying by x^5

$X^5 D(X) = X^{14} + X^{12} + X^8 + X^7 + X^5$

$P(X) = X^5 + X^4 + X^2 + 1$

$X^5 + X^4 + X^2 + 1 \;\overline{)\; X^{14} + X^{12} + X^8 + X^7 + X^5}$ $\quad$ quotient X^9

$X^{14} + X^{13} + X^{11} + X^9$

$X^{13} + X^{12} + X^{11} + X^9 + X^8$

$X^{13} + X^{12} + \ldots X^{10} + X^8$

$X^{11} + X^{10} + X^9 + \ldots X^7$

$X^{11} + X^{10} + X^9 + \ldots X^6$

$X^9 + X^8 + X^7 + X^6 + X^5$

$X^9 + X^8 + X^6 + X^4$

$X^7 + X^5 + X^4$

$X^7 + X^6 + \ldots X^2$

$X^6 + X^5 + X^2$

$X^6 + X^5 + X^3 + X$

$X^3 + X^2 + X \leftarrow R$

The code word $= X^{14} + X^{12} + X^8 + X^7 + X^5 + X^3 + X^2 + X$

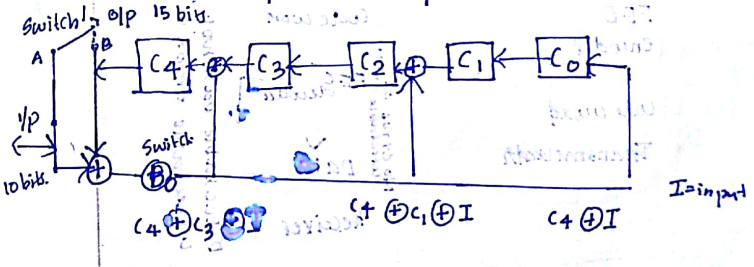
DIGITAL LOGIC

$D = 101000110$ & $P = 110101$

$D(X) = X^9 + X^7 + X^3 + X^2 + 1$ & $P(X) = X^5 + X^4 + X^2 + 1$

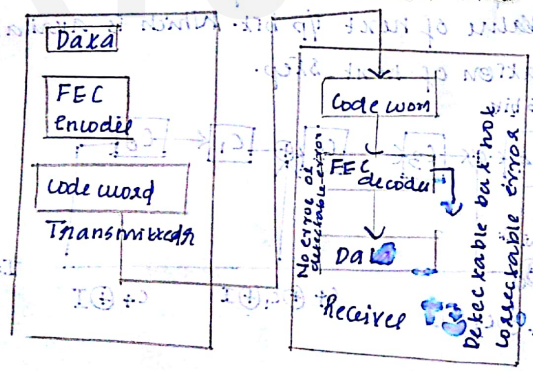
Since length of FCS is five (X^5). There should be five shift registers. The process begins with the shift registers cleared. The msg (dividend) is then entered one bit at a time starting with MSB. The table shows step by step operation as the i/p applied one bit at a time.

- Each row shows the values currently stored in the five shift register elements and the values that appear at the o/p of 3 XOR circuits the value of next i/p bit. Which is available for operation of next step.



	C_4	C_3	C_2	C_1	C_0	$C_4 \oplus C_3 \oplus I$		
initial	0	0	0	0	0	1	1	1
1:	1	0	1	0	1	1	1	0
2:	1	1	1	1	0	1	0	1
3:	1	1	1	0	0	1	1	0
4:	1	0	0	1	1	0	0	0
5:	1	0	0	1	0	0	1	0
6:	1	0	0	0	1	0	0	1
7:	0	0	0	1	0	0	1	1
8:	1	0	0	0	1	1	1	0
9:	1	0	1	1	1	0	0	1
10:	0	1	1	1	0	1	0	0

Error Correction



On the transmission end each k bit block of data is mapped into an n bit ($n > k$) called a code word. Using forward correction encoder. The code word is then transmitted during transmission some error may occur at the receiver the incoming signal is demodulated to produce a bit stream ~~ii~~ similar to original code word but may contain errors. This block is passed through forward error correction method with one of

1. If there are no bit error in i/p to the FEC decoder is identical to original code word & " decoder produces the " block as o/p
2. For certain error patterns it is possible for the decoder to detect & correct that error for
3. Certain error pattern the decoder can detect but not correct the errors. In this case decode simply reports an uncorrectable error.
4. For certain error pattern the decoder can't detect that any errors have occurred and maps the incoming n bit data block into a k bit block that differs from the ~~dif~~ original k-bit block.

HAMMING DISTANCE

~~To transmit k b~~

~~Ham~~ The hamming distance $d(v_1, v_2)$ btw two n-bit binary sequences v_1 and v_2 is

the no of bits in which v_1 and v_2 descending

eg: $v_1 = 01101$ $v_2 = 11000$ $d(v_1, v_2) = 3$

To transmit k-bit of data it is mapped into unique n-bit codeword.

eg:

Data block	Codeword
00	00000
01	00111
10	11001
11	11110

If we received 00100 which not in codecoord.

$d(00000, 00100) = 1$

$d(00111, 00100) = 2$

$d(11001, 00100) = 3$

$d(11110, 00100) = 4$

eg: 01010 is received.

$(00000, 01010) = 2$

$(11110, 01010) = 2$

The ratio of redundant bit to data bit $\frac{(n-k)}{k} / k$ is called redundancy of the code.

The ratio of data bits to total bit is called the code rate.

$(n-k)/k \quad k/n = \frac{2}{5}$

* The code rate is the measure of how much additional bandwidth required to carry data at the same data rate as without the code.

The design of code is equivalent to $vc = f(vd)$

vc : vector of n-code word bits.

vd : vector of k data bits.

For code consisting of code word $w_1, w_2 \ldots w_s$

$s = 2^n$ and $d_{min} = \min_{i \neq j} [d(w_i, w_j)]$