SPECIAL FUNCTION REGISTERS (SFRS) OF 8051

8051 has 21, 8-bit Special Function registers.

	NAME	FUNCTION	BYTE ADDRESS	BIT ADDRESS
Used for holding data and status during Programming	A*	Accumulator	0E0H	0E7H…0E0H
	B*	Arithmetic	0F0H	0F7H…0F0H
	PSW*	Program Status Word	0D0H	0D7H…0D0H
Used in instructions to point to memory	SP	Stack Pointer	81H	NA
	DPL	Address External Memory	82H	NA
	DPH	Address External Memory	83H	NA
Used by the respective I/O Ports	P0*	I/O Port latch	80H	87H…80H
	P1*	I/O Port latch	90H	97H…90H
	P2*	I/O Port latch	0A0H	0A7H…0A0H
	P3*	I/O Port latch	0B0H	0B7H…0B0H
Used by the Serial Port	SCON*	Serial Port Control	98H	9FH…98H
	SBUF	Serial Port Data Buffer	99H	NA
Used for Timer Control	TCON*	Timer/Counter Control	88H	8FH…88H
	TMOD	Timer/Counter Mode Control	89H	NA
	TL0	Timer 0 Low Byte	8AH	NA
	TL1	Timer 1 Low Byte	8BH	NA
	TH0	Timer 0 High Byte	8CH	NA
	TH1	Timer 1 High Byte	8DH	NA
Used for Interrupt Control	IE*	Interrupt Enable	0A8H	0AFH…0A8H
	IP*	Interrupt Priority	0B8H	0BFH…0B8H
Used for Power Control	PCON	Power Control	87H	NA

*Means the SFR is Bit Addressable

1) SFRs are **8-bit** registers.
   Each SFR has its own **special function**.
2) **They are** placed **inside** the **Microcontroller.** #Please refer Bharat Sir's Lecture Notes for this ...
3) They are used by the programmer to perform special functions like controlling the timers, the serial port, the I/O ports etc.
4) As SFRs are available to the programmer, we will use them in instructions.
   This causes another problem.
   SFRs are registers after all, and hence using them would tremendously increase the number of opcodes. ***(Refer to Bharat Sir's Lecture notes for more on this)***
5) To reduce the number of opcodes, **SFRs are allotted addresses.**
   These addresses must not clash with any other addresses of the existing memories.
6) Incidentally, the internal RAM is of 128 bytes and uses addresses only from 00H… 7FH.
   This gives an entire range of addresses from 80H… FFH completely unused and can be freely allotted to the SFRs.
7) **Hence SFRs are allotted addresses from 80H… FFH.**
   It is not a co-incidence that these addresses are free. It is how 8051 design was planned. The Internal RAM was restricted to 128 bytes instead of 256 bytes so that these addresses are free for SFRs.
8) Moreover, some SFRs are bit addressable, like Port 0.
   All 8-bits can be individually accessed from P0.0… P0.7, by instructions like SETB, CLR etc.
   But again, this will again tremendously increase the number of opcodes.
9) To avoid this problem, **even the bits of the SFRs are allotted addresses.**
   These are bit addresses, which are different from byte addresses.
   These bit addresses must not clash with those of the bit addressable area of the Internal RAM.
   Amazingly, even the bit addresses in the Internal RAM are 00H… 7FH (again 128 bits), keeping bit addresses 80H… FFH free to be used by the SFR bits.
10) **So bit addresses 80H… FFH are allotted to the bits of various SFRs.**
    (Watch Bharat Acharya Education, videos on YouTube for more on this)
11) Port 0 has a byte address of 80H and its bit addresses are from 80H… 87H.
    A byte operation at address 80H will affect entire Port0.
    E.g.:: MOV A, P0; this refers to Byte address 80H that's whole Port 0.
12) **A bit operation at 80H will affect only P0.0.**
    E.g.:: SETB P0.0; this refers to bit address 80H that's Port0.0