Lab 6: DSP Builder Overview

Objective: Utilize the DSP builder to implement a sample project in Simulink then export it to the FPGA

Reference Guide: DSP Builder User Guide – Section 2: Getting Started Tutorial
This is located in the Altera path in Windows under DSP builder.

Procedure: Creating the Amplitude Modulation Model

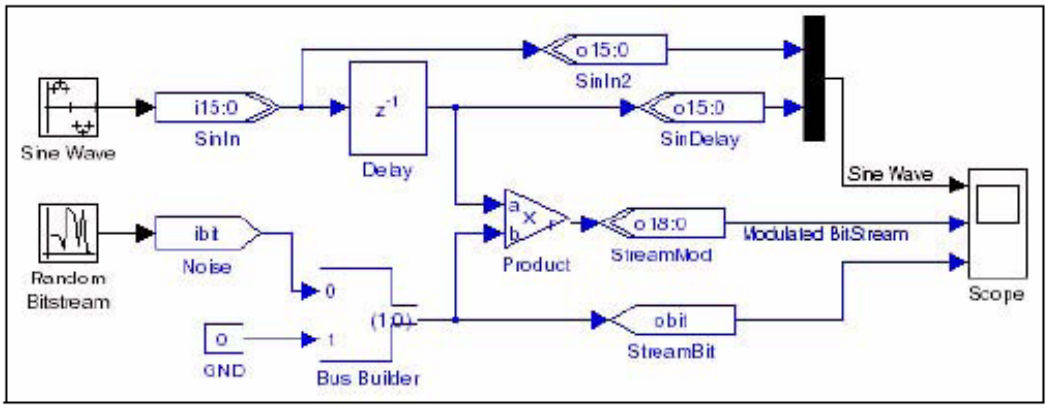


Figure 1: Overview of Simulink module

To create the amplitude modulation model, follow the instructions in the following sections.

Create a New Model
To create a new model, perform the following steps:
1. Start the MATLAB software.
2. On the File menu, point to New and click Model to create a new model window.
3. Click Save on the File menu in the new model window.
4. Browse to the directory in which you want to save the file. This directory becomes your working directory. This tutorial uses the working directory <*DSP Builder install path*>\DesignExamples\Tutorials\GettingStartedSinMdl\my_SinMdl.
5. Type the file name into the File name box. This tutorial uses the name singen.mdl.
6. Click Save.
7. Click the MATLAB Start button . Point to Simulink and click Library Browser.

Add the Sine Wave Block
Perform the following steps to add the Sine Wave block:
1. In the Simulink Library Browser, click Simulink and Sources to view the blocks in the Sources library.
2. Drag and drop a Sine Wave block into your model.
3. Double-click the Sine Wave block in your model to display the Block Parameters dialog box.
4. Set the Sine Wave block parameters as shown in Table 2–1.

Table 2–1. Parameters for the Sine Wave Block

Parameter	Value
Sine type	Sample based
Time	simulation time
Amplitude	2^15–1
Bias	0
Samples per period	80
Number of offset examples	0
Sample time	25e-9
Interpret vector parameters a 1-D	On

5. Click OK.

Add the SinIn Block

Perform the following steps to add the SinIn block:

1. In the Simulink Library Browser, expand the Altera DSP Builder Blockset folder to display the DSP Builder libraries (Figure 2–2).

The first time you do this it might take a while for the files to generate.

2. Select the IO & Bus library.
3. Drag and drop the Input block from the Simulink Library Browser into your model. Position the block to the right of the Sine Wave block.
4. Click the text under the block icon in your model. Delete the text Input and type the text SinIn to change the name of the block instance.
5. Double-click the SinIn block in your model to display the **Block Parameters** dialog box.
6. Set the SinIn block parameters as shown in Table 2–2.

Figure 2–2. Altera DSP Builder Folder in the Simulink Library Browser

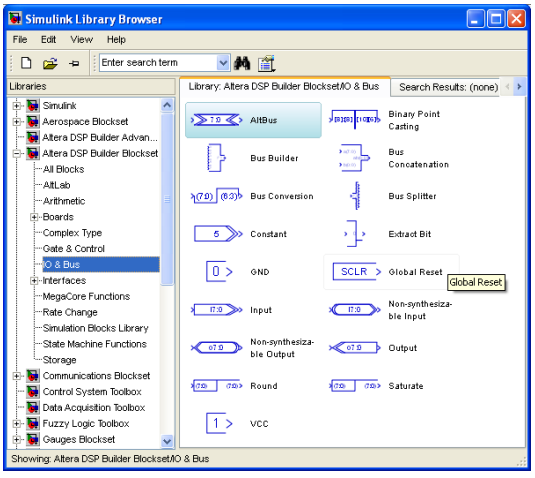


Table 2–2. Parameters for the SinIn Block

Parameter	Value
Bus Type	Signed Integer
[number of bits].[]	16
Specify Clock	Off

7. Click **OK**.
8. Draw a connection line from the right side of the Sine Wave block to the left side of the SinIn block by holding down the left mouse button and dragging the cursor between the blocks.

Add the Delay Block

Perform the following steps to add the Delay block:
1. Select the **Storage** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop the Delay block into your model and position it to the right of the SinIn block.
3. Double-click the Delay block in your model to display the **Block Parameters** dialog box.
4. Type 1 as the **Number of Pipeline Stages** for the Delay block.
5. Click the **Optional Ports** tab and set the parameters shown in Table 2–3.

Table 2–3. Parameters for the Delay Block.

Parameter	Value
Clock Phase Selection	01
Use Enable Port	Off
Use Synchronous Clear port	Off

6. Click **OK**.
7. Draw a connection line from the right side of the SinIn block to the left side of the Delay block.

Add the SinDelay and SinIn2 Blocks

Perform the following steps to add the SinDelay and SinIn2 blocks:
1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop two Output blocks into your model, positioning them to the right of the Delay block.
3. Click the text under the block symbols in your model. Change the block instance names from Output and Output1 to SinDelay and SinIn2.
4. Double-click the SinDelay block in your model to display the **Block Parameters** dialog box.
5. Set the SinDelay block parameters as shown in Table 2–4.

Table 2–4. Parameters for the SinDelay Block

Parameter	Value
Bus Type	Signed Integer
[number of bits].[]	16
External Type	Inferred

6. Click **OK**.
7. Repeat steps 4 to 6 for the SinIn2 block setting the parameters as shown in Table 2–5.

Table 2–5. Parameters for the SinIn2 Block

Parameter	Value
Bus Type	Signed Integer
[number of bits].[]	16
External Type	Inferred

8. Draw a connection line from the right side of the Delay block to the left side of the SinDelay block.

Add the Mux Block

Perform the following steps to add the Mux block:
1. Select the Simulink **Signal Routing** library in the Simulink Library Browser.
2. Drag and drop a Mux block into your design, positioning it to the right of the SinDelay block.
3. Double-click the Mux block in your model to display the **Block Parameters** dialog box.
4. Set the Mux block parameters as shown in Table 2–6.

Table 2–6. Parameters for the Mux Block

Parameter	Value
Number of Inputs	2
Display Options	bar

5. Click **OK**.
6. Draw a connection line from the bottom left of the Mux block to the right side of the SinDelay block.
7. Draw a connection line from the top left of the Mux block to the line between the SinIn2 block.
8. Draw a connection line from the SinIn2 block to the line between the SinIn and Delay blocks.

Add the Random Bitstream Block

Perform the following steps to add the Random Bitstream block:
1. Select the Simulink **Sources** library in the Simulink Library Browser.

2. Drag and drop a Random Number block into your model, positioning it underneath the Sine Wave block.
3. Double-click the Random Number block in your model to display the **Block Parameters** dialog box.
4. Set the Random Number block parameters as shown in Table 2–7.

Table 2–7. Parameters for the Random number Block

Parameter	Value
Mean	0
Variance	1
Initial seed	0
Sample time	25e–9
Interpret vector parameters as 1-D	On

5. Click **OK**.
6. Rename the Random Noise block Random Bitstream.

Add the Noise Block

Perform the following steps to add the Noise block:
1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop an Input block into your model, positioning it to the right of the Random Bitstream block.
3. Click the text under the block icon in your model. Rename the block Noise.
4. Double-click the Noise block to display the **Block Parameters** dialog box.
5. Set the Noise block parameters as shown in Table 2–8.

Table 2–8. Parameters for the Noise Block

Parameter	Value
Bus Type	Single Bit
Specify Clock	Off

6. Click **OK**.
7. Draw a connection line from the right side of the Random Bitstream block to the left side of the Noise block.

Add the Bus Builder Block

The Bus Builder block converts a bit to a signed bus. Perform the following steps to add the Bus Builder block:
1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a Bus Builder block into your model, positioning it to the right of the Noise block.
3. Double-click the Bus Builder block in your model to display the **Block Parameters** dialog box.
4. Set the Bus Builder block parameters as shown in Table 2–9.

Table 2–9. Parameters for the Bus Builder Block

Parameter	Value
Bus Type	Signer Integer
[number of bits].[]	2

5. Click **OK**.
6. Draw a connection line from the right side of the Noise block to the top left side of the Bus Builder block.

Add the GND Block

Perform the following steps to add the GND block:
1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a GND block into your model, positioning it underneath the Noise block.
3. Draw a connection line from the right side of the GND block to the bottom left side of the Bus Builder block.

Add the Product Block

Perform the following steps to add the Product block:
1. Select the **Arithmetic** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a Product block into your model, positioning it to the right of the Bus Builder block and slightly above it. Leave enough space so that you can draw a connection line under the Product block.
3. Double-click the Product block to display the **Block Parameters** dialog box.
4. Set the Product block parameters as shown in Table 2–10.

Table 2–10. Parameters for the Product Block

Parameter	Value
Bus Type	Inferred
Number of Pipeline Stages	0

5. Click **OK**.
6. Draw a connection line from the top left of the Product block to the line between the Delay and SinDelay blocks.

Add the StreamMod and StreamBit Blocks

Perform the following steps to add the StreamMod and StreamBit blocks:
1. Select the **IO & Bus** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop two Output blocks into your model, positioning them to the right of the Product block.
3. Click the text under the block symbols in your model. Change the block instance names from Output and Output1 to StreamMod and StreamBit.
4. Double-click the StreamMod block to display the **Block Parameters** dialog box.

5. Set the StreamMod block parameters as shown in Table 2–11.

Table 2–11. Parameters for the StreamMod Block

Parameter	Value
Bus Type	Signed Integer
[number of bits].[]	19
External Type	Inferred

6. Click **OK**.
7. Double-click the StreamBit block to display the **Block Parameters** dialog box.
8. Set the StreamMod block parameters as shown in Table 2–12.

Table 2–12. Parameters for the StreamMod Block

Parameter	Value
Bus Type	Single Bit
External Type	Inferred

9. Draw connection lines from the right side of the Product block to the left side of the StreamMod block, and from the right side of the Bus Builder block to the left side of the StreamBit block.

Add the Scope Block

Perform the following steps to add the Scope block:
1. Select the Simulink **Sinks** library in the Simulink Library Browser.
2. Drag and drop a Scope block into your model and position it to the right of the StreamMod block.
3. Double-click the Scope block and click the **Parameters** icon to display the **'Scope' parameters** dialog box.
4. Set the Scope parameters as shown in Table 2–13.

Table 2–13. Parameters for the Scope Block

Parameter	Value
Number of axes	3
Time range	auto
Tick labels	bottom axis only
Sampling	Decimation 1

5. Click **OK**.
6. Close the Scope.
7. Make connections to connect the complete your design as follows:
a. From the right side of the Mux block to the top left side of the Scope block.
b. From the right side of the StreamMod block to the middle left side of the Scope block.
c. From the right side of the StreamBit block to the bottom left of the Scope block.

d. From the bottom left of the Product block to the line between the Bus Builder block and the StreamBit block.

Add a Clock Block

Perform the following steps to add a Clock block:

1. Select the **AltLab** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a Clock block into your model.
3. Double-click on the Clock block to display the **Block Parameters** dialog box.
4. Set the Clock parameters as shown in Table 2–14.

Table 2–14. Parameters for the Clock Block

Parameter	Value
Real-World Clock Period	20
Period Unit:	ns
Simulink Sample Time	2.5e–008
Reset Name	aclr
Reset Type	Active Low
Export As Output Pin	Off

Simulating the Model in Simulink

To simulate your model in the Simulink software, perform the following steps:

1. Click **Configuration Parameters** on the Simulation menu to display the **Configuration Parameters** dialog box and select the **Solver** page.
2. Set the parameters shown in Table 2–15.

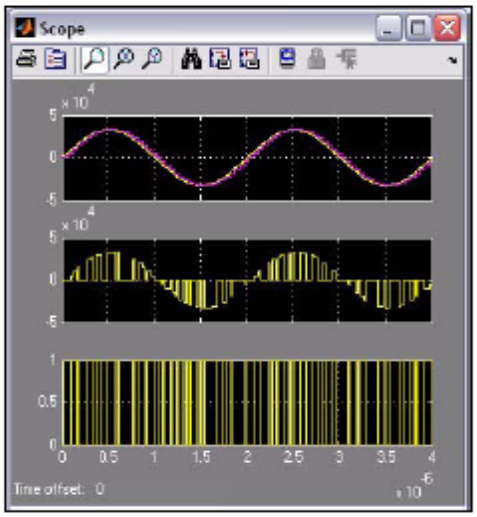
Table 2–15. Configuration Parameters for the singen Model

Parameter	Value
Start time	0.0
Stop time	4e–6
Type	Fixed-step
Solver	discrete (no continuous states)

3. Click **OK**.
4. Start simulation by clicking **Start** on the Simulation menu.
5. Double-click the Scope block to view the simulation results.
6. Click the **Autoscale** icon (binoculars) to auto-scale the waveforms.

Figure 2–18 shows the scaled waveforms.

Figure 2–18. Scope Simulation Results



Verification of Simulink Output: _____

Compiling the Design

To create and compile a Quartus II project for your DSP Builder design, and to program your design onto an Altera FPGA, you must add a Signal Compiler block.

Perform the following steps:

1. Select the **AltLab** library from the **Altera DSP Builder Blockset** folder in the Simulink Library Browser.
2. Drag and drop a Signal Compiler block into your model.
3. Double-click the Signal Compiler block in your model to display the **Signal Compiler** dialog box. The dialog box allows you to set the target device family. Use the Cyclone II.
4. Click **Compile**.
5. When the compilation has completed successfully, click **OK**.
6. Click **Save** on the File menu to save your model.

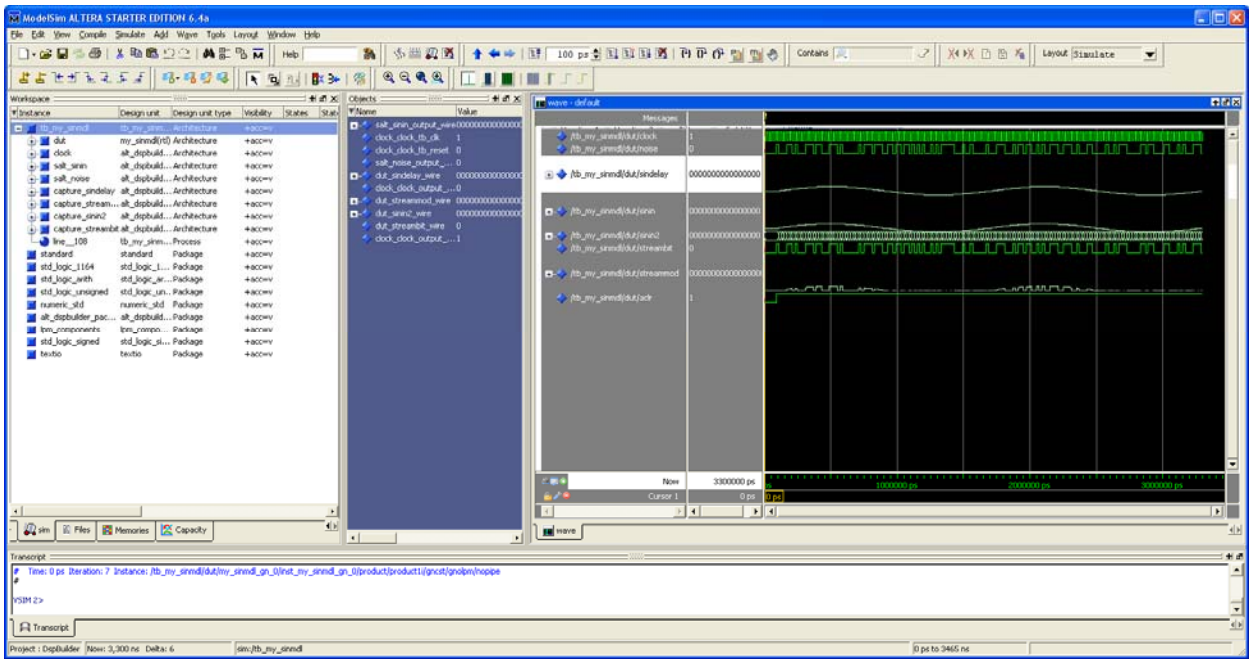
Performing RTL Simulation

To perform RTL simulation with the ModelSim software, you must add a TestBench block.

Perform the following steps:

1. Select the **AltLab** library from the **Altera DSP Builder BlockSet** folder in the Simulink Library Browser.
2. Drag and drop a TestBench block into your model.
3. Double-click on the new TestBench block.
4. Ensure that **Enable Test Bench generation** is on.
5. Click the **Advanced** tab.
6. Turn on the **Launch GUI** option. This option causes the ModelSim GUI to be

launched when ModelSim simulation is invoked.
7. Click **Generate HDL** to generate a VDHL-based testbench from your model.
8. Click **Run Simulink** to generate Simulink simulation results for the testbench.
9. Click **Run ModelSim** to load your design into ModelSim.
10. Change the format of the sinin, sindelay and streammod signals to analog by selecting the signal name in the Wave window and right-clicking on **Properties**. In the **Format** tab, select **Analog**, and specify height **50**, scale **0.001**.
11. Click **Zoom Full** on the right button pop-up menu in the ModelSim Wave window. The simulation results display as an analog waveform similar to that shown in the figure below.



Verification of ModelSim Output: _____

Adding the Design to a Quartus II Project

The Quartus II project created by the `Signal Compiler` block is used internally by DSP Builder. This section describes how to add your design to a new or existing Quartus II project.

Before following these steps, ensure that your design has been compiled using the `Signal Compiler` block as described in "Compiling the Design" on page 2–18.

Creating a Quartus II Project

To create a new Quartus II project, perform the following steps:
1. Start the Quartus II software.
2. Click **New Project Wizard** on the File menu in the Quartus II software and specify the working directory for your project. For example, **D:\MyQuartusProject**.
3. Specify the name of the project. For example, **NewProject** and the name of the top level design entity for the project.

1 The name of the top-level design entity typically has the same name as the

project.

4. Click **Next** to display the **Add Files** page. There are no files to add for this tutorial.
5. Click **Next** to display the **Family & Device Settings** page and check that the required device family is selected. This should normally be the same device family as specified for `Signal Compiler` in "Compiling the Design" on page 2–18.
6. Click **Finish** to close the wizard and create the new project.

1 When you specify a directory that does not already exist, a message asks if the specified directory should be created. Click **Yes** to create the directory.

Add the DSP Builder Design to the Project

To add your DSP Builder design to the project in the Quartus II software:
1. On the View menu in the Quartus II software, point to **Utility Windows** and click **Tcl Console** to display the Tcl Console.
2. Run the script in the Tcl Console by typing the following command:

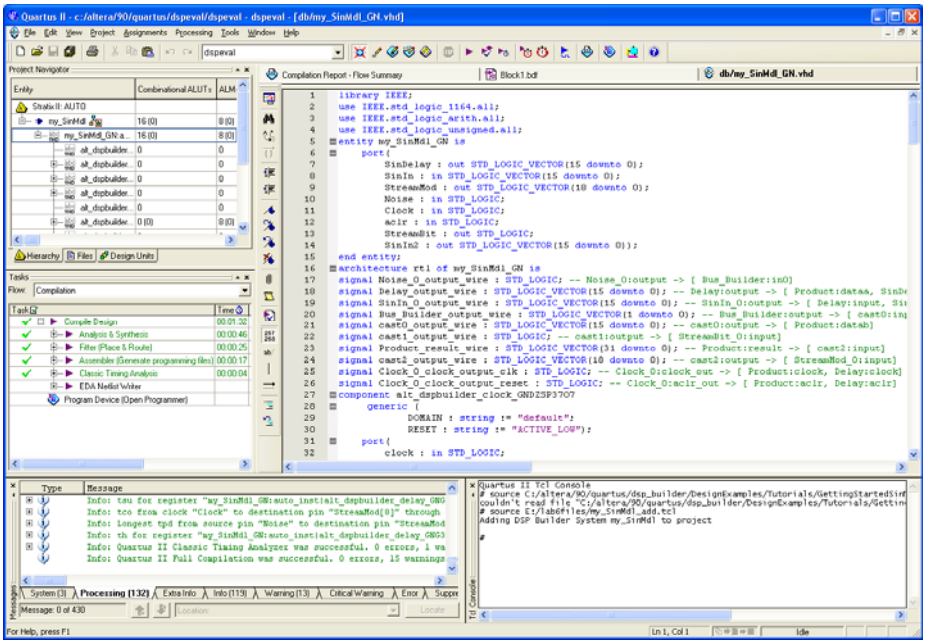
```
# source <install path>/ my_SinMdl.tcl
```

You must use / separators instead of \ separators in the command path name used in the Tcl console window. You can use a relative path if you organize your design data with the DSP Builder and Quartus II designs in subdirectories of the same design hierarchy.

An example instantiation is added to your Quartus II project.

3. Click the **Files** tab in the Quartus II software.
4. Right-click **my_SinMdl.mdl** and click **Select Set as Top-Level Entity**.
5. Compile the Quartus II design by clicking **Start Compilation** on the Processing menu.

The output should be a VHDL file as shown in the following screen capture:



Once the code is generated, a symbol can be created to add this to a Quartus II design….

Next part of the lab assignment is to implement the reference design for edge detection and update it to the Cyclone II. The webpage for the design can be found at:

http://www.altera.com/support/refdesigns/sys-sol/indust_mil/ref-edge-detection.html?GSA_pos=3&WT.oss_r=1&WT.oss=dsp%20builder%20edge%20detection

Verification: _____