Mentor - Mentee Training Plan

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Mentee: Tran Lam Hai An
AIS Solutions 2 Group

Version 1.0
Jun 2017

AGENDA

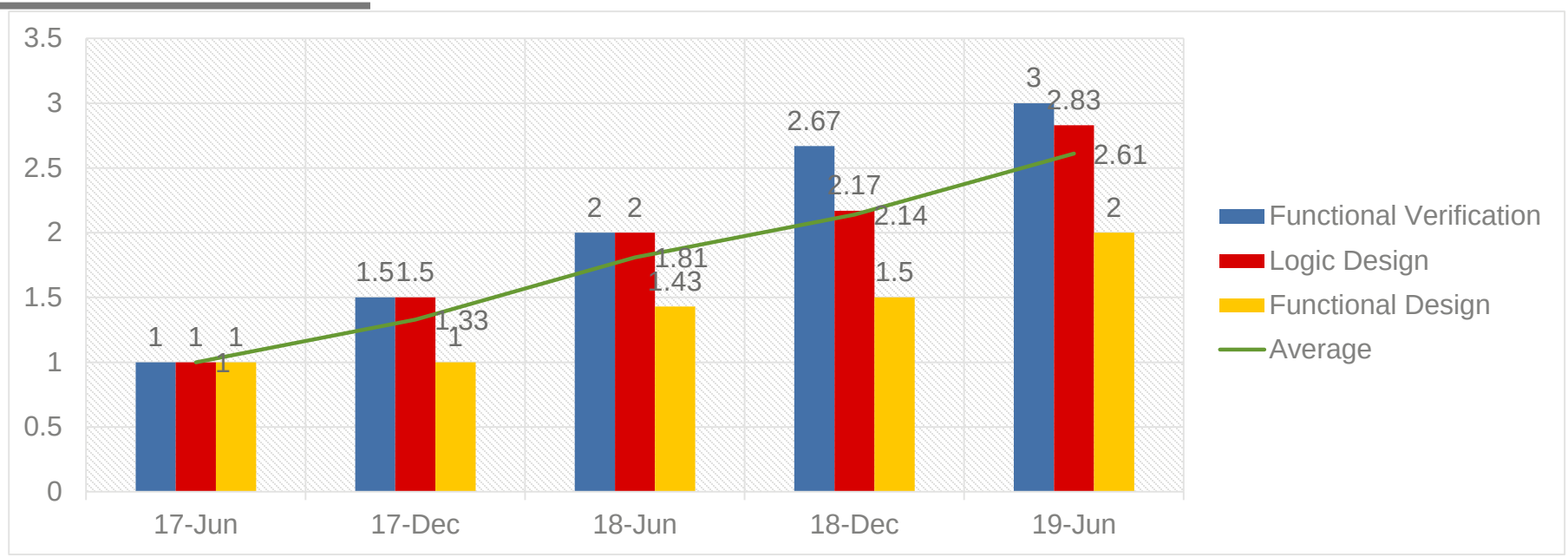
TARGET

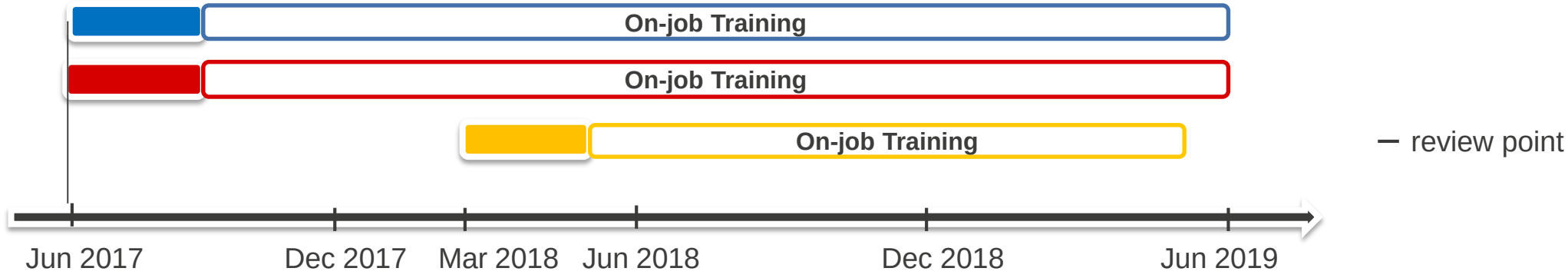
Become a **Functional Verification Engineer** with level **3** in Jun 2019.

ROLES	CURRENT LEVEL	TARGETED LEVEL
Functional Verification	1	3
Logic design	1	2.83
Functional Design	1	2
Average	**1**	**2.61**

	Skill	17-Jun	17-Dec	18-Jun	18-Dec	19-Jun
Functional Verification	To determine verification strategy	1	1	2	2	3
	To check specification	1	1	2	2	3
	To create verification item list (checklist)	1	2	2	3	3
	To create test patterns for functional verification	1	2	2	3	3
	To conduct test patterns verification of RTL	1	1	2	3	3
	To evaluate functional verification result	1	2	2	3	3
	Average	1	1.5	2	2.67	3
Logic Deign	To synthesis and to do formal verification	1	2	2	3	3
	To determine checker strategy	1	1	2	2	3
	To analyze and fix checker errors (HLDRC, DFTcheck)	1	2	2	2	3
	To analyze and fix checker errors (STAcheck)	1	2	2	2	3
	To create SDC (Synopsys design constraint)	1	1	2	2	2
	To analyze timing report and optimize timing	1	1	2	2	3
	Average	1	1.5	2	2.17	2.83
Functional Design	To create functional/logic specifications for chip design	1	1	1	1	2
	To create module design specifications	1	1	1	1	2
	To create LSI functional description at behavior level	1	1	1	1	2
	To create RTL description	1	1	2	2	2
	To create top level netlist	1	1	2	2	2
	To create timing budget	1	1	2	2	2
	To determine strategies of evaluation and testing	1	1	1	2	2
	Average	1	1	1.43	1.57	2
	Summary	1	1.33	1.81	2.14	2.61

SCHEDULE





– review point

PLAN TO ACHIEVE
Functional Verification

Module: LBSC/LPD

Skill	Input	Action	Output
To determine verification strategy (verification policy)	- Verification phase of project demand - Guideline	- Investigate design and choose verification solution - Make basic checking item list and its priority in verification	- Basic checking item lists - Checking item priority - Verifications plan and schedule
To check specification	- Hardware manual - Basic checking item of project	- Analyze basic checking item of the project - Self-investigate chip and module specification - Make document to explanation purpose	- Module checking items - Document explains for checking item
To create verification item list (checklist)	- Basic checklist of project - Hardware manual - Checking items - Verification plan	- Investigate module hardware manual. - Analyze basic checklist and module checking item - Create module verification checklist	Module verification item lists
To create test patterns for functional verification.	- Module verification checklist - Hardware manual, spec - RTL, net list	- Investigate module hardware manual and sample pettern - Create pattern cover check list	- Test pattern (CT,UT) - Test pattern description
To conduct functional verification of RTL	- Module verification item lists (CT,UT) - Module modification record - Module verification plan	- Analyze verification item lists - Analyze modification record - Estimate the bug curve of project - Modify inputs data if errors are found	- Bug-curve estimation (doc) - Verification coverage - Verification results
To evaluate functional verification result	- Module checklist and hardware manual. - Test pattern description - Verification result	-Analyze test pattern description, module checklist and hardware manual - Reading test pattern description - Evaluate coverage result - Using checker to judge verification	- Checked verifications result - Coverage result

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Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To determine verification strategy (verification policy)				1
To check specification				1
To create verification item list (checklist)	- Basic checklist of project - Hardware manual - Checking items - Verification plan	- Investigate module hardware manual. - Analyze basic checklist and module checking item - Q&A, confirm with mentor	Module verification item lists	**2**
To create test patterns for functional verification.				
To conduct functional verification of RTL	- Module verification item lists (CT,UT) - Module modification record - Module verification plan	- Analyze verification item lists - Analyze modification record - Confirm result with mentor	- Verification coverage - Verification results	**2**
To evaluate functional verification result	- Module checklist and hardware manual. - Test pattern description - Verification result	- Analyze test pattern description, module checklist and hardware manual - Reading test pattern description - Q&A, confirm with mentor	- Checked verifications result - Coverage result	**2**

RENESAS

Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To determine verification strategy (verification policy)	- Verification phase of project demand - Guideline	- Investigate design - Make basic checking item list and its priority in verification - Ivestigate and confirm result with mentor	- Basic checking item lists - Checking item priority - Verifications plan and schedule	2
To check specification	- Hardware manual - Basic checking item of project	- Analyze basic checking item of the project - Investigate and confirm understand with mentor	- Module checking items	2
To create verification item list (checklist)	- Basic checklist of project - Hardware manual - Checking items - Verification plan	- Investigate module hardware manual. - Analyze basic checklist and module checking item - Q&A, confirm with mentor	Module verification item lists	2
To create test patterns for functional verification.	- Module verification checklist - Hardware manual, spec - RTL, net list	- Investigate module hardware manual and sample pettern - Create pattern cover check list - Confirm result with mentor	- Test pattern (CT,UT) - Test pattern description	2
To conduct functional verification of RTL	- Module verification item lists (CT,UT) - Module modification record - Module verification plan	- Analyze verification item lists - Analyze modification record - Confirm with mentor	- Verification coverage - Verification results	2
To evaluate functional verification result	- Module checklist and hardware manual. - Test pattern description - Verification result	-Analyze test pattern description, module checklist and hardware manual - Reading test pattern description - Q&A, confirm with mentor	- Checked verifications result - Coverage result	2

Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To determine verification strategy (verification policy)	- Verification phase of project demand - Guideline	- Investigate design and choose verification solution - Make basic checking item list and its priority in verification - Ivestigate and confirm result with mentor	- Basic checking item lists - Checking item priority - Verifications plan and schedule	2
To check specification	- Hardware manual - Basic checking item of project	- Analyze basic checking item of the project - Investigate and confirm understand with mentor	- Module checking items - Document explains for checking item	2
To create verification item list (checklist)	- Basic checklist of project - Hardware manual - Checking items - Verification plan	- Investigate module hardware manual. - Analyze basic checklist and module checking item - Create module verification checklist	Module verification item lists	**3**
To create test patterns for functional verification.	- Module verification checklist - Hardware manual, spec - RTL, net list	- Investigate module hardware manual - Create pattern cover check list - Make plan and evaluate results	- Test pattern (CT,UT) - Test pattern description - Verification plan report	**3**
To conduct functional verification of RTL	- Module verification item lists (CT,UT) - Module modification record - Module verification plan	- Analyze verification item lists - Analyze modification record - Estimate the bug curve of project - Modify inputs data if errors are found	- Bug-curve estimation (doc) - Verification coverage - Verification results	**3**
To evaluate functional verification result	- Module checklist and hardware manual. - Test pattern description - Verification result	- Analyze test pattern description, module checklist and hardware manual - Reading test pattern description - Evaluate coverage result - Using checker to judge verification - Make verification report	- Checked verifications result - Coverage result - Verification report	**3**

Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To determine verification strategy (verification policy)	- Verification phase of project demand - Guideline	- Investigate design and choose verification solution - Make basic checking item list and its priority in verification	- Basic checking item lists - Checking item priority - Verifications plan and schedule	3
To check specification	- Hardware manual - Basic checking item of project	- Analyze basic checking item of the project - Self-investigate chip and module specification - Make document to explanation purpose	- Module checking items - Document explains for checking item	3
To create verification item list (checklist)	- Basic checklist of project - Hardware manual - Checking items - Verification plan	- Investigate module hardware manual. - Analyze basic checklist and module checking item - Create module verification checklist	Module verification item lists	3
To create test patterns for functional verification.	- Module verification checklist - Hardware manual, spec - RTL, net list	- Investigate module hardware manual and sample pettern - Create pattern cover check list	- Test pattern (CT,UT) - Test pattern description - Confirm result with mentor	3
To conduct functional verification of RTL	- Module verification item lists (CT,UT) - Module modification record - Module verification plan	- Analyze verification item lists - Analyze modification record - Estimate the bug curve of project - Modify inputs data if errors are found	- Bug-curve estimation (doc) - Verification coverage - Verification results - Confirm result with mentor	3
To evaluate functional verification result	- Module checklist and hardware manual. - Test pattern description - Verification result	-Analyze test pattern description, module checklist and hardware manual - Reading test pattern description - Evaluate coverage result - Using checker to judge verification	- Checked verifications result - Coverage result - Confirm check item or bug	3

PLAN TO ACHIEVE
Logic design

Module: LBSC/LPD

Skill	Input	Action	Output
To synthesize and do formal verification.	- Synthesis Env document. - Module RTL/IO file.	- Read synthesis environment document, focus to synthesis constrain and option - Investigate Formality document and do formality verification - Run synthesis and analyze log file and check result. Optimize net-list to solve timing error	- Synthesis Constraint explanation document. - Optimization guideline. - Gate net-list met project demand (timing, area...)
To determine checker strategy	- Project demand for checker item.	- Analyze project demand for checker item - Create checker running constrain - Give feedback to checker leader about checker running constrain	- Checker running constrain.
To analyze and fix checker error (HLDRC)	- HLDRC User's Guide. - Gate net-list.	- Read HLDRC User's guide - Make document to explain HLDRC error	- HLDRC contrains explantation (document). - HLDRC Error explantation (document).
To analyze and fix checker error (DFTcheck)	- DFT User's Guide. - Gate net-list.	- Read DFT User's guide - Make document to explain DFT error and DFT constrain	- DFTCheck constrain explanation (document). - DFTCheck Error explanation (document).
To analyze and fix checker error (STAcheck)	- STAcheck design rule. - Gate netlist	- Read STACheck design rule - Make document to explain STA error and STA constrain	- STAcheck constrain explanation (document). - STAcheck Error explanation (document).
To create SDC (synopsys design constraint)	- Module specification - SDC document - Sample individual constraint - Guideline	- Read module's Hardware manual - Learn how to make SDC file - Debug on STA environment - Confirm with mentor	SDC file
To analyze timing report and optimize timing	- Timing report - Module STA constrain.	- Check timing report and analyze each violation point. - Make Timing ECO to solve timing violation.	- Timing ECO command - No timing violation

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Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To synthesize and do formal verification.	- Synthesis Env document. - Module RTL/IO file.	- Read synthesis environment document, focus to synthesis constrain and option - Investigate Formality document and do formality verification - Confirm each error/warning with mentor	- Synthesis Constraint explanation document. - Optimization guideline.	2
To determine checker strategy				
To analyze and fix checker error (HLDRC)	- HLDRC User's Guide. - Gate net-list.	- Read HLDRC User's guide - Q&A, confirm each analysis with IP designer - Confirm each analysis with mentor	- HLDRC contrains explantation (document). - HLDRC Error explantation (document).	2
To analyze and fix checker error (DFTcheck)	- DFT User's Guide. - Gate net-list.	- Read DFT User's guide - Q&A, confirm each analysis with IP designer - Confirm each analysis with mentor	- DFTCheck constrain explanation (document). - DFTCheck Error explanation (document).	2
To analyze and fix checker error (STAcheck)	- STAcheck design rule. - Gate netlist	- Read STACheck design rule - Q&A, confirm each analysis with IP designer - Confirm each analysis with mentor	- STAcheck constrain explanation (document). - STAcheck Error explanation (document).	2
To create SDC (synopsys design constraint)				
To analyze timing report and optimize timing				

RENESAS

Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To synthesize and do formal verification.	- Synthesis Env document. - Module RTL/IO file.	- Read synthesis environment document, focus to synthesis constrain and option - Investigate Formality document and do formality verification - Confirm each error/warning with mentor	- Synthesis Constraint explanation document. - Optimization guideline.	2
To determine checker strategy	- Project demand for checker item.	- Analyze project demand for checker item - Confirm each analysis with mentor	- Checker running constrain.	2
To analyze and fix checker error (HLDRC)	- HLDRC User's Guide. - Gate net-list.	- Read HLDRC User's guide - Q&A, confirm each analysis with IP designer - Confirm each analysis with mentor	- HLDRC contrains explantation (document). - HLDRC Error explantation (document).	2
To analyze and fix checker error (DFTcheck)	- DFT User's Guide. - Gate net-list.	- Read DFT User's guide - Q&A, confirm each analysis with IP designer - Confirm each analysis with mentor	- DFTCheck constrain explanation (document). - DFTCheck Error explanation (document).	2
To analyze and fix checker error (STAcheck)	- STAcheck design rule. - Gate netlist	- Read STACheck design rule - Q&A, confirm each analysis with IP designer - Confirm each analysis with mentor	- STAcheck constrain explanation (document). - STAcheck Error explanation (document).	2
To create SDC (synopsys design constraint)	- Module specification - SDC document - Sample individual constraint - Guideline	- Read module's Hardware manual - Learn how to make SDC file - Debug on STA environment - Confirm with mentor about constraint	SDC file	2
To analyze timing report and optimize timing	- Timing report - Module STA constrain.	- Check timing report and analyze each violation point - Solving solution with mentor	- Timing ECO command - No timing violation	2

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Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To synthesize and do formal verification.	- Synthesis Env document. - Module RTL/IO file.	- Read synthesis environment document, focus to synthesis constrain and option - Investigate Formality document and do formality verification - Run synthesis and analyze log file and check result. Optimize net-list to solve timing error	- Synthesis Constraint explanation document. - Optimization guideline. - Gate net-list met project demand (timing, area...)	3
To determine checker strategy	- Project demand for checker item.	- Analyze project demand for checker item - Create checker running constrain - Give feedback to checker leader about checker running constrain	- Checker running constrain.	2
To analyze and fix checker error (HLDRC)	- HLDRC User's Guide. - Gate net-list.	- Read HLDRC User's guide - Make document to explain HLDRC error - Confirm each analysis with mentor	- HLDRC contrains explantation (document). - HLDRC Error explantation (document).	2
To analyze and fix checker error (DFTcheck)	- DFT User's Guide. - Gate net-list.	- Read DFT User's guide - Make document to explain DFT error and DFT constrain - Confirm each analysis with mentor	- DFTCheck constrain explanation (document). - DFTCheck Error explanation (document).	2
To analyze and fix checker error (STAcheck)	- STAcheck design rule. - Gate netlist	- Read STACheck design rule - Make document to explain STA error and STA constrain - Confirm each analysis with mentor	- STAcheck constrain explanation (document). - STAcheck Error explanation (document).	2
To create SDC (synopsys design constraint)	- Module specification - SDC document - Sample individual constraint - Guideline	- Read module's Hardware manual - Learn how to make SDC file - Debug on STA environment - Confirm with mentor about constraint	SDC file	2
To analyze timing report and optimize timing	- Timing report - Module STA constrain.	- Check timing report and analyze each violation point - Make Timing ECO to solve timing violation - Solving solution with mentor	- Timing ECO command - No timing violation	2

RENESAS

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Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To synthesize and do formal verification.	- Synthesis Env document. - Module RTL/IO file.	- Read synthesis environment document, focus to synthesis constrain and option - Investigate Formality document and do formality verification - Run synthesis and analyze log file and check result. Optimize net-list to solve timing error	- Synthesis Constraint explanation document. - Optimization guideline. - Gate net-list met project demand (timing, area...)	3
To determine checker strategy	- Project demand for checker item.	- Analyze project demand for checker item - Create checker running constrain - Give feedback to checker leader about checker running constrain	- Checker running constrain.	2
To analyze and fix checker error (HLDRC)	- HLDRC User's Guide. - Gate net-list.	- Read HLDRC User's guide - Q&A, confirm each analysis with IP designer - Make document to explain HLDRC error - Sefl-investigate and give solution for each error/warning	- HLDRC contrains explantation (document). - HLDRC Error explantation (document).	3
To analyze and fix checker error (DFTcheck)	- DFT User's Guide. - Gate net-list.	- Read DFT User's guide - Q&A, confirm each analysis with IP designer - Make document to explain DFT error and DFT constrain - Sefl-investigate and give solution for each error/warning	- DFTCheck constrain explanation (document). - DFTCheck Error explanation (document).	3
To analyze and fix checker error (STAcheck)	- STAcheck design rule. - Gate netlist	- Read STACheck design rule - Q&A, confirm each analysis with IP designer - Make document to explain STA error and STA constrain - Sefl-investigate and give solution for each error/warning	- STAcheck constrain explanation (document). - STAcheck Error explanation (document).	3
To create SDC (synopsys design constraint)	- Module specification - SDC document - Sample individual constraint - Guideline	- Read module's Hardware manual - Learn how to make SDC file - Debug on STA environment - Confirm with mentor about constraint	SDC file	2
To analyze timing report and optimize timing	- Timing report - Module STA constrain.	- Check timing report and analyze each violation point - Make Timing ECO to solve timing violation - Sefl-investigate and give solution for any violation	- Timing ECO command - No timing violation	3

RENESAS

PLAN TO ACHIEVE
Functional design

Module: LBSC/LPD

Skill	Input	Action	Output
To create functional/logic specifications for chip design	- Module design requirement - Module hardware manual	- Analyze design requirement and module hardware manual - Make the schematic to explain the connection between in-charged module and other modules	- Connection schematic between module with others in whole chip
To create module design specifications	- Required specification - Module hardware manual - Reference output from project - Guideline	- Analyze module design requirement, module hardware manual - Make design specification - Confirm with mentor	- Design specification - Interface specification
To create LSI functional description at behavior level	- Design document - Original IO - Module hardware manual	- Investigate module hardware manual and design document. - Change module IO file.	- Modified IO - Behavior description
To create RTL description	- Modification specification - Legacy design (RTL)	- Make RTL description - Code review and design review with mentor	- Modified RTL without errors
To analyze and fix RTL checker (Spyglass)	- Modified RTL file - Spyglass document - Spyglass environment	- Run spyglass. - Check spyglass log file and analysis each warning/error - Fix warning/error and run spyglass again to confirm - Check the result	- Spyglass log file - Spyglass Error explanation (document) - Final RTL
To create top level netlist	- Modified RTL/IO - Synthesis env.	- Analyze synthesis environment and make document to explain about synthesis constrain. - Run synthesis. - Analyze synthesis result, solve timing violation and checker error.	- Synthesis constrain explanation. - Chip top netlist. - Checker error explanation & confirmation (document)
To create timing budget	- Original IO file - IO timing budget constrain of project.	- Analyze original IO file and timing constrain of project. - Modified timing budget of module IO file.	- New IO timing budget for module

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Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To create functional/logic specifications for chip design	- Module design requirement - Module hardware manual	- Analyze design requirement and module hardware manual - Make the schematic to explain the connection between in-charged module and other modules - Confirm result with mentor	- Connection schematic between module with others in whole chip	**1**
To create module design specifications	- Required specification - Module hardware manual - Reference output from project - Guideline	- Analyze module design requirement, module hardware manual - Make design specification - Confirm with mentor	- Design specification - Interface specification	**1**
To create LSI functional description at behavior level	- Design document - Original IO - Module hardware manual	- Investigate module hardware manual and design document. - Change module IO file.	- Modified IO - Behavior description	**1**
To create RTL description	- Modification specification - Legacy design (RTL)	- Make RTL description - Code review and design review with mentor	- Modified RTL without errors	**1**
To analyze and fix RTL checker (Spyglass)	- Modified RTL file - Spyglass document - Spyglass environment	- Run spyglass. - Check spyglass log file and analysis each warning/error - Fix warning/error and run spyglass again to confirm - Check the result	- Spyglass log file - Spyglass Error explanation (document) - Final RTL	**1**
To create top level netlist	- Modified RTL/IO - Synthesis env.	- Analyze synthesis environment and make document to explain about synthesis constrain. - Run synthesis. - Analyze synthesis result, solve timing violation and checker error.	- Synthesis constrain explanation. - Chip top netlist. - Checker error explanation & confirmation (document)	**1**
To create timing budget	- Original IO file - IO timing budget constrain of project.	- Analyze original IO file and timing constrain of project. - Modified timing budget of module IO file.	- New IO timing budget for module	**1**

Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To create functional/logic specifications for chip design				1
To create module design specifications				1
To create LSI functional description at behavior level				1
To create RTL description	- Modification specification - Legacy design (RTL)	- Make RTL description - Code review and design review with mentor	- Modified RTL without errors	**2**
To analyze and fix RTL checker (Spyglass)	- Modified RTL file - Spyglass document - Spyglass environment	- Run spyglass. - Check spyglass log file and analysis each warning/error - Fix warning/error and run spyglass again to confirm - Check the result and confirm with mentor	- Spyglass log file - Spyglass Error explanation (document) - Final RTL	**2**
To create top level netlist	- Modified RTL/IO - Synthesis env.	- Analyze synthesis environment and make document to explain about synthesis constrain. - Run synthesis. - Analyze synthesis result, solve timing violation and checker error - Confirm result with mentor	- Synthesis constrain explanation. - Chip top netlist. - Checker error explanation & confirmation (document)	**2**
To create timing budget				1

Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To create functional/logic specifications for chip design				1
To create module design specifications				1
To create LSI functional description at behavior level				1
To create RTL description	- Modification specification - Legacy design (RTL)	- Make RTL description - Code review and design review with mentor	- Modified RTL without errors	2
To analyze and fix RTL checker (Spyglass)	- Modified RTL file - Spyglass document - Spyglass environment	- Run spyglass. - Check spyglass log file and analysis each warning/error - Fix warning/error and run spyglass again to confirm - Check the result	- Spyglass log file - Spyglass Error explanation (document) - Final RTL	2
To create top level netlist	- Modified RTL/IO - Synthesis env.	- Analyze synthesis environment and make document to explain about synthesis constrain. - Run synthesis. - Analyze synthesis result, solve timing violation and checker error - Confirm result with mentor	- Synthesis constrain explanation. - Chip top netlist. - Checker error explanation & confirmation (document)	2
To create timing budget	- Original IO file - IO timing budget constrain of project.	- Analyze original IO file and timing constrain of project. - Modified timing budget of module IO file. - Review result with mentor	- New IO timing budget for module	2

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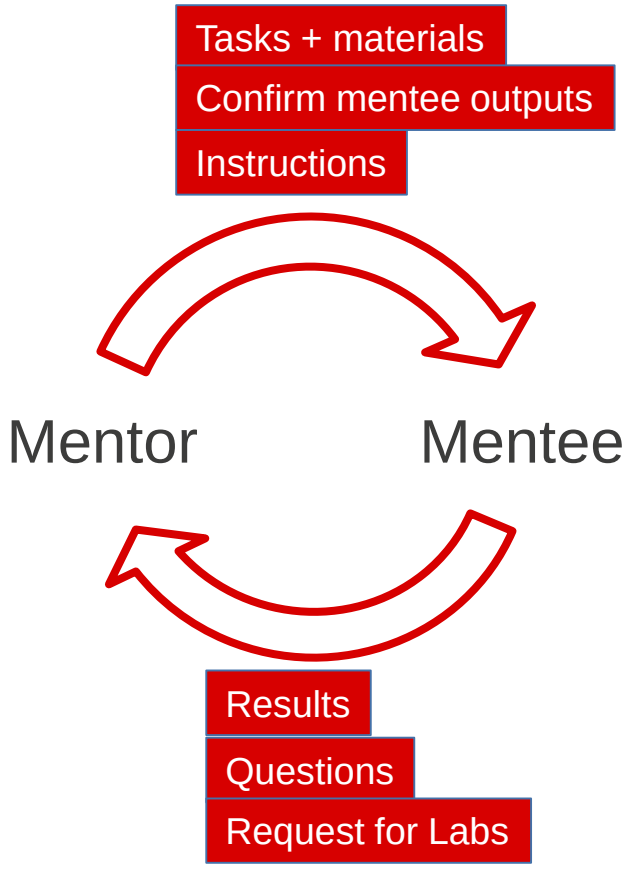
Module: LBSC/LPD

Skill	Input	Action	Output	Target Level
To create functional/logic specifications for chip design	- Module design requirement - Module hardware manual	- Analyze design requirement and module hardware manual - Make the schematic to explain the connection between in-charged module and other modules - Confirm result with mentor	- Connection schematic between module with others in whole chip	2
To create module design specifications	- Required specification - Module hardware manual - Reference output from project - Guideline	- Analyze module design requirement, module hardware manual - Make design specification - Confirm with mentor	- Design specification - Interface specification	2
To create LSI functional description at behavior level	- Design document - Original IO - Module hardware manual	- Investigate module hardware manual and design document. - Change module IO file.	- Modified IO - Behavior description	2
To create RTL description	- Modification specification - Legacy design (RTL)	- Make RTL description - Code review and design review with mentor	- Modified RTL without errors	2
To analyze and fix RTL checker (Spyglass)	- Modified RTL file - Spyglass document - Spyglass environment	- Run spyglass. - Check spyglass log file and analysis each warning/error - Fix warning/error and run spyglass again to confirm - Check the result	- Spyglass log file - Spyglass Error explanation (document) - Final RTL	2
To create top level netlist	- Modified RTL/IO - Synthesis env.	- Analyze synthesis environment and make document to explain about synthesis constrain. - Run synthesis. - Analyze synthesis result, solve timing violation and checker error - Confirm result with mentor	- Synthesis constrain explanation. - Chip top netlist. - Checker error explanation & confirmation (document)	2
To create timing budget	- Original IO file - IO timing budget constrain of project.	- Analyze original IO file and timing constrain of project. - Modified timing budget of module IO file. - Review result with mentor	- New IO timing budget for module	2

MENTOR – MENTEE INTERACTION



Convention		
Discussion channel	Email (Q&A, Weekly report)	
	Direct contact at desk	
	Meeting	
Review	6-month review	- Evaluate the result, compare with training plan target - Propose the next activities for the next 6-month
	3-month review	- Check the progress of training - Check whether the results are mapped with training plan - Propose the next activities to reach the 6-month target
	Monthly	- Summarize the results of tasks
	Weekly	- Review the task process