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Course: **Low Power VLSI**
Course code**: UE22EC342BB4**

Project

Power reduction of 6T SRAM using MTCMOS and Stacking

DEPARMENT OF ELECTRONICS AND COMMUNICATIONS
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6T SRAM

6T SRAM is a **memory cell** made up of **six transistors (6T)** that stores **one bit of data**

- **6 Transistors**:
  - **2 NMOS (access) transistors** – for read/write access
  - **2 PMOS + 2 NMOS** – cross-coupled inverters to store the bit
- **Nodes**: Q and $\overline{Q}$ (complementary outputs)
- **Lines**:
  - **BL, $\overline{BL}$ (Bit Lines)** – for data transfer
  - **WL (Word Line)** – controls access to the cell

Working Principle

1. Write Operation:

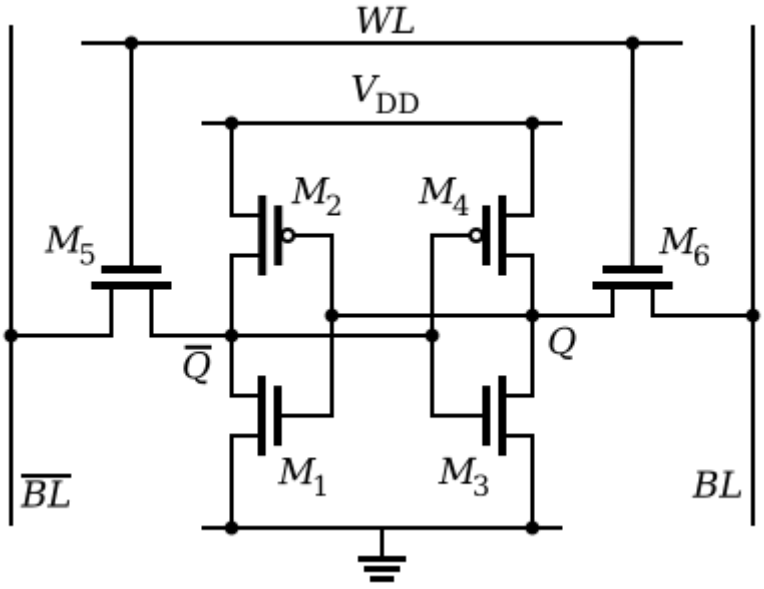
- Bit lines: BL and $\overline{BL}$ are set with input data and its complement
- WL = 1 → Access transistors turn ON
- Data is written into the cross-coupled inverters

2. Read Operation:

- Pre-charge both BL and $\overline{BL}$ to high
- WL = 1 → Connects cell to bit lines
- Depending on stored data, one bit line discharges → Sensed by sense amplifier

3. Hold State:

- WL = 0 → Access transistors OFF
- Cross-coupled inverters maintain the state (static)



Application

SRAM is widely used in CPU cache memory (L1, L2, L3) due to its high speed and low latency. It's also found in register files, embedded memory in ASICs/SoCs, FPGAs, and GPUs for fast data access. Networking devices use SRAM for buffering and lookups, while microcontrollers use it as internal RAM. Its main advantages are fast access, no refresh needed, and low idle power, making it ideal for performance-critical applications.

POWER REDUCTION TECHNIQUES:

1)MTCMOS

Basic Concept of MTCMOS

MTCMOS technique uses two types of transistors with different threshold voltages:

a) High-Threshold Voltage (Vth) Transistors: These transistors have very minimal leakage current which make them idea for using in standby or inactive mode. However, these transistor's switching speed is slower.

b) Low-Threshold Voltage (Vth) Transistors: These transistors have high leakage current but very fast switching speed and they offer improved performance. By utilizing these two types of transistors in MTCMOS design of the cell we can significantly decrease the leakage current during standby mode and deliver adequate performance during active modes

Power Gating

Power gating method is used in MTCMOS, which enables the supply voltage to the SRAM cell to be disconnected during standby or sleep mode. This is usually done by using a set of additional high-voltage transistors known as 'sleep' or 'header' and 'footer' transistors. The power supply is turned off by these sleep transistors when the SRAM cell is not in use, which results in reduction of leakage current to very negligible levels

2) Stacking Transistor-Based SRAM Design

The stacking transistor technique is employed in SRAM design to reduce leakage power by placing multiple transistors in series, thereby increasing the effective threshold voltage during standby, this technique leverages the "stacking effect," where transistors in series reduce the leakage current due to shared voltage drops across the stacked devices.

3) Combining Stacking and MTCMOS in SRAM Cells

The combined approach of stacking and MTCMOS in SRAM design brings together two complementary techniques:

a) Stacking Transistors: Reduces leakage by placing transistors in series, leveraging the stacking effect to increase the effective threshold voltage and reduce subthreshold leakage during standby mode.

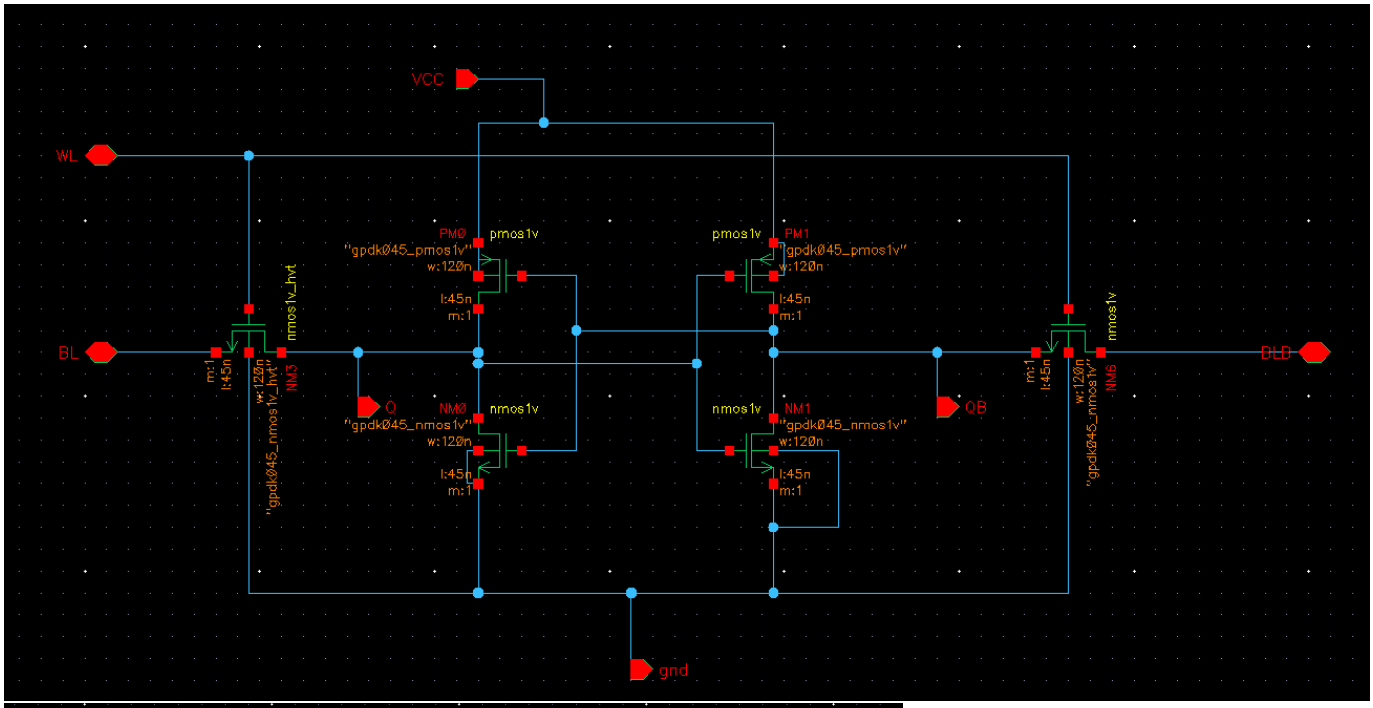
b) MTCMOS Power Gating: Sleep transistors are introduced to completely shut off power during idle states, which further minimizes leakage when the SRAM cell is not in use.

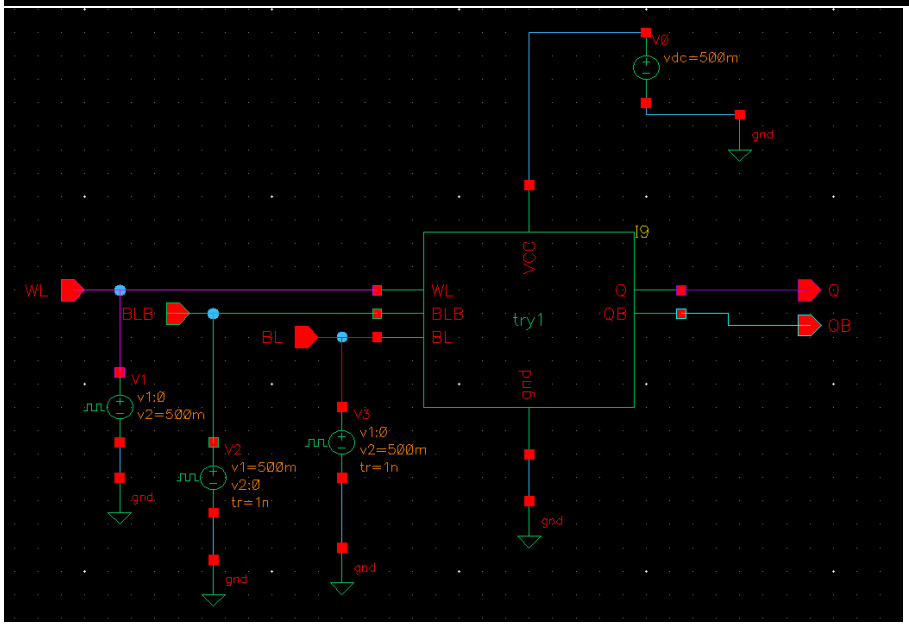
Experimental Setup:

Tool Used: Cadence Virtuoso
Technology Node: 90nm CMOS
SRAM Type: 6T Cell
Test Conditions: Standby Mode (Leakage Measurement)

CIRCUIT AND RESULTS:

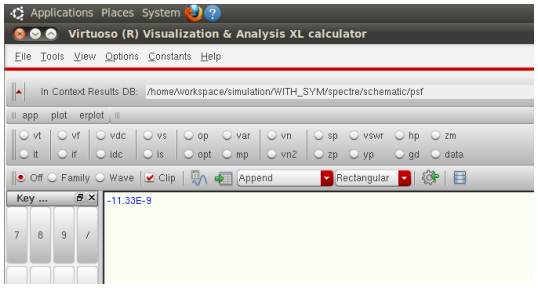
1)Conventional 6T SRAM



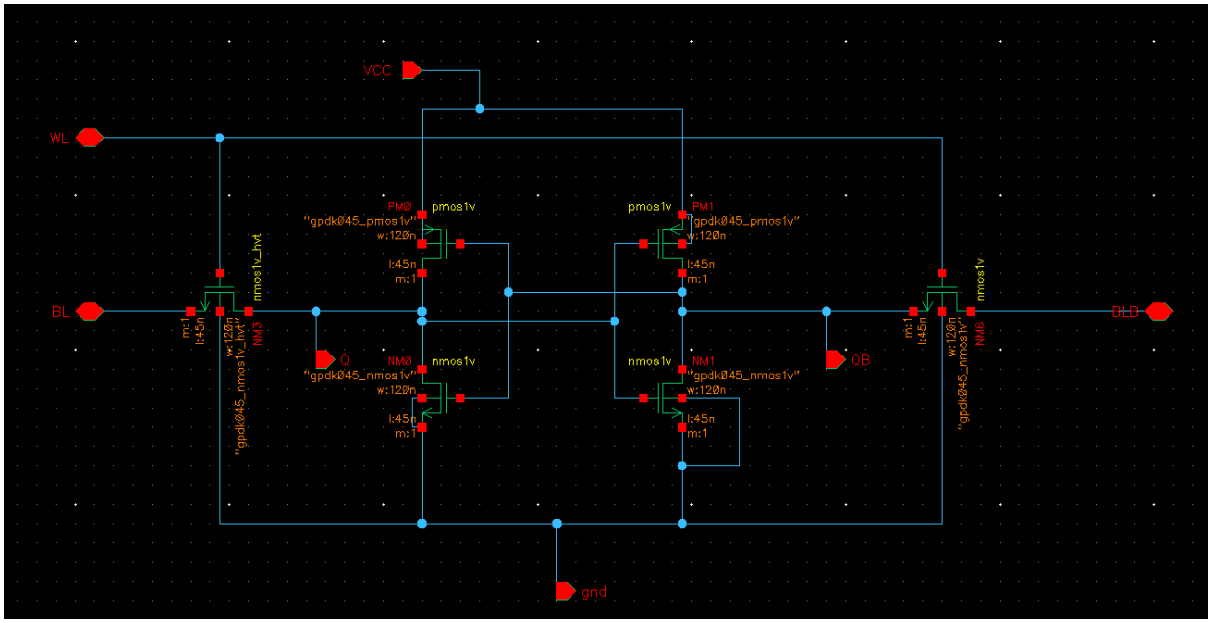


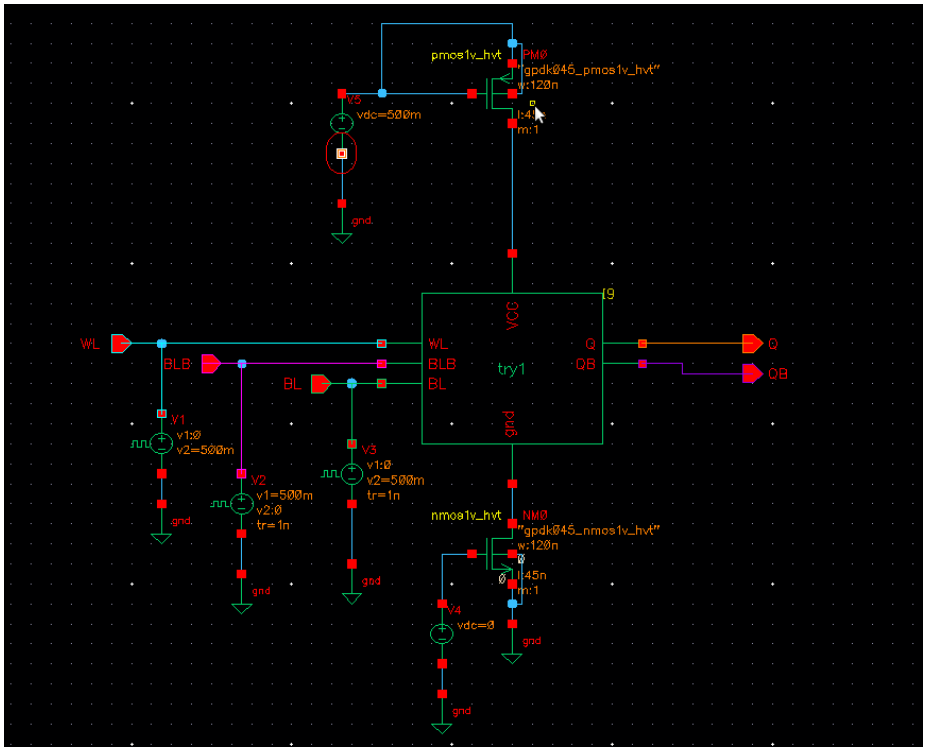
Waveform:

Leakage power:

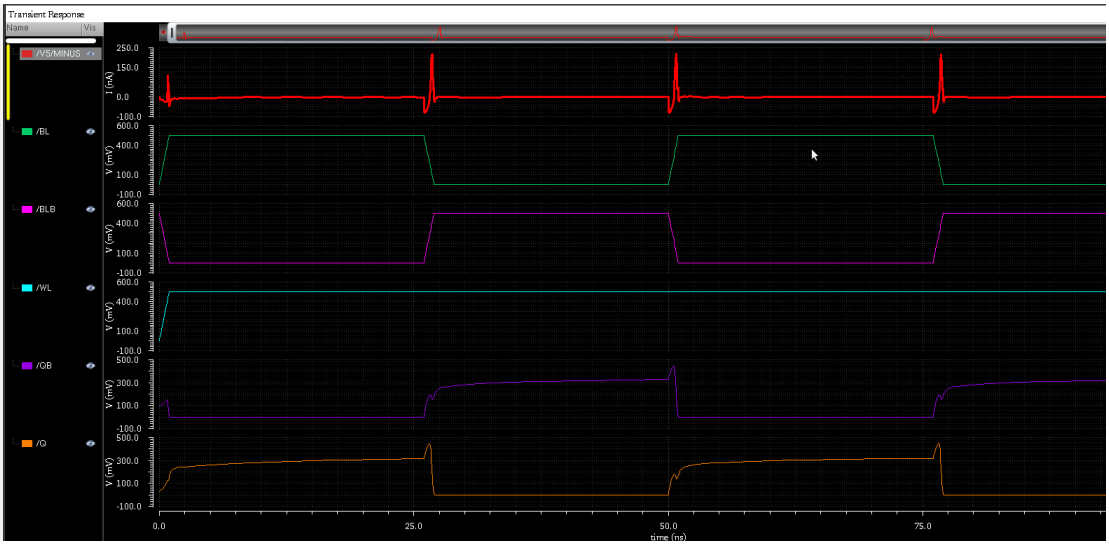


2) 6T SRAM with MTCMOS cells

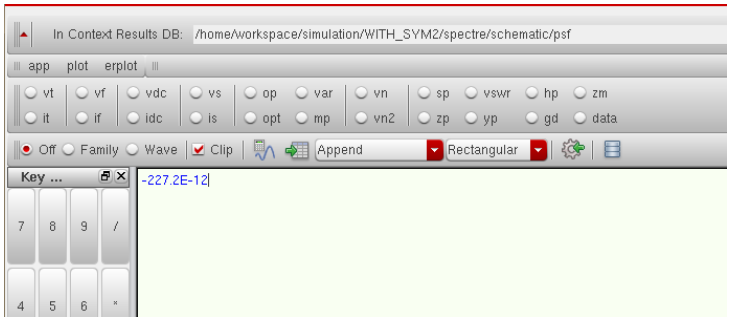




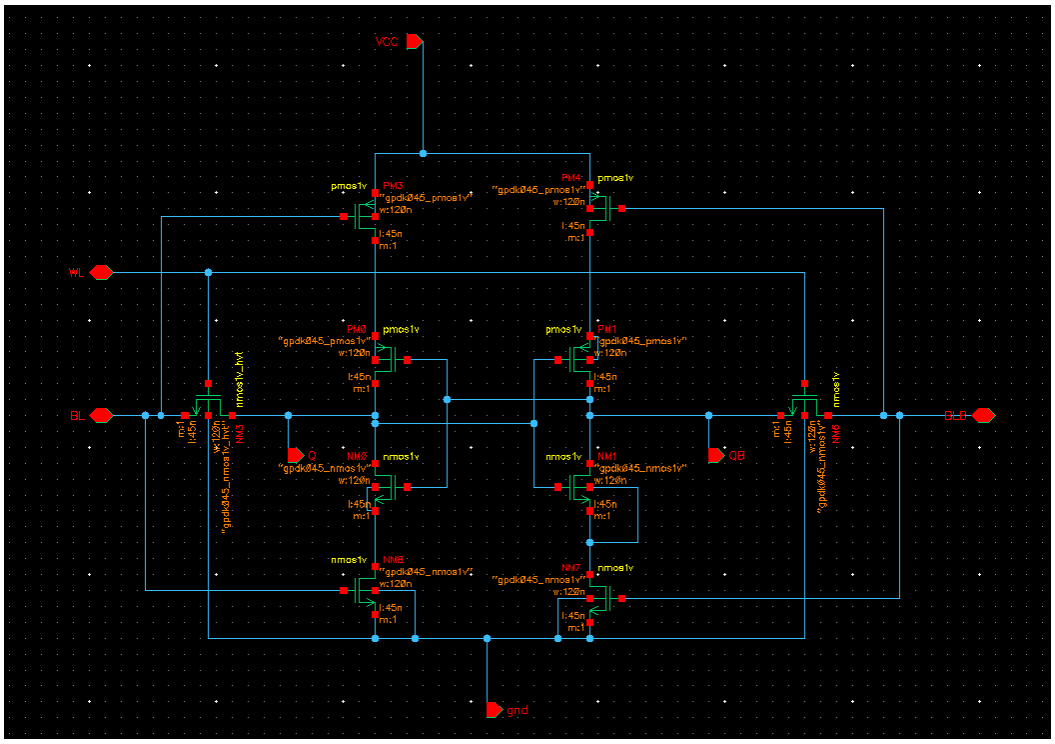
Waveform:

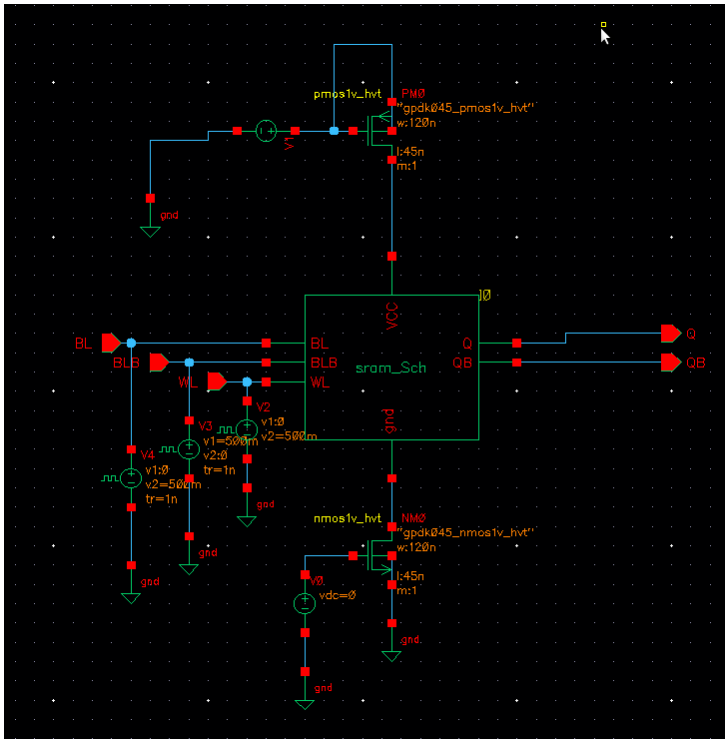


Leakage power:

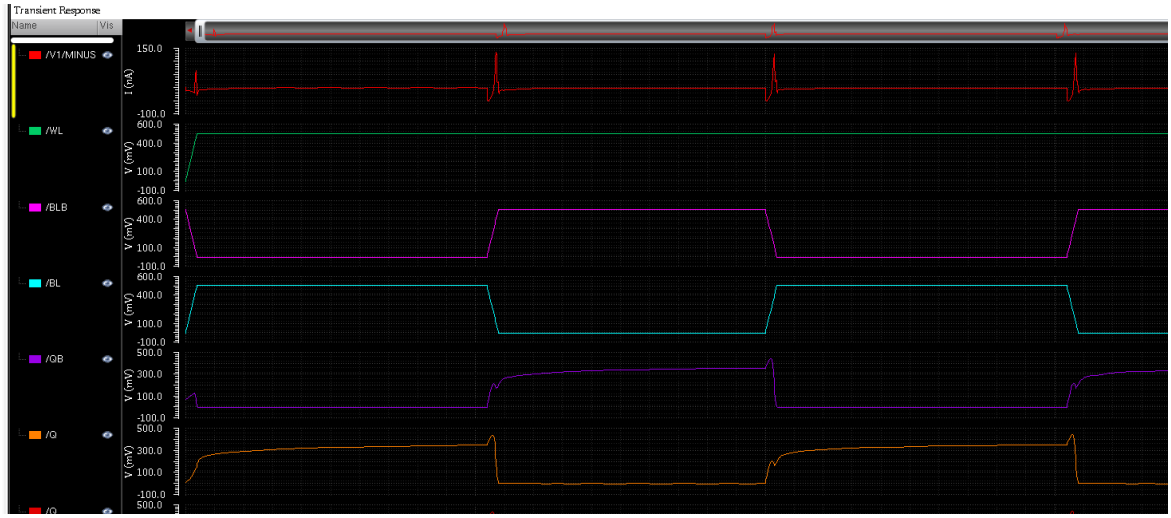


3) 6T SRAM with stacking and MTCMOS

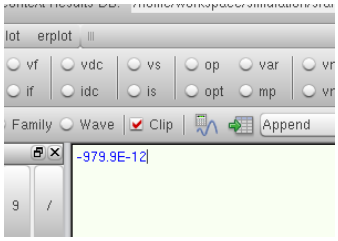




Waveform:



Leakage power:



LEAKAGE POWER ANALYSIS (45nm):

Conventional 6T SRAM: 11.33×10^{-9} W = 11.33nW

6T SRAM with MTCMOS: 227.2×10^{-12}W = 227.2pW

6T SRAM with stacking and MTCMOS: 979.9×10^{-12}W = 979.9pW

Leakage power reduction %

Reduction (%) $_{MTCMOS}$ = ((11.33n – 227.2p)/11.33n) x100 = 97.9%

Reduction (%) $_{stacking + MTCMOS}$ = ((11.33n – 979.9p)/11.33n) x100 = 91.3%

RESULT

Leakage power is reduced by 97.9% using MTCMOS technique

Leakage power is reduced by 91.3 % using MTCMOS + stacking technique

CONCLUSION

Conventional SRAM cell exhibited leakage power of 11.33 nW. By implementing MTCMOS techniques, power consumption was reduced to 227.2 pW. The MTCMOS + stacked SRAM cell provided the Leakage power of 979.9 pW because of the extra transistors the power is increase slightly compared to MTCMOS 6T SRAM. These results indicate the SRAM cell designs can effectively reduce power consumption, making them suitable for low-power applications in modern integrated circuits.