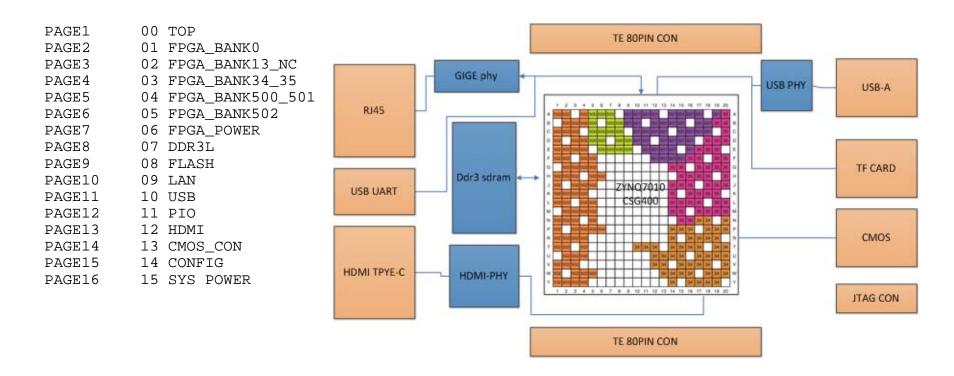
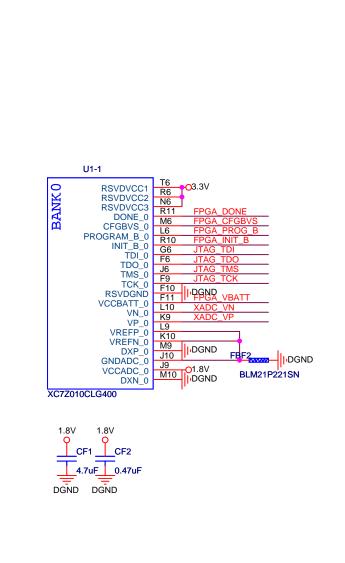
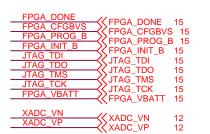
ZINGNANO V1.0



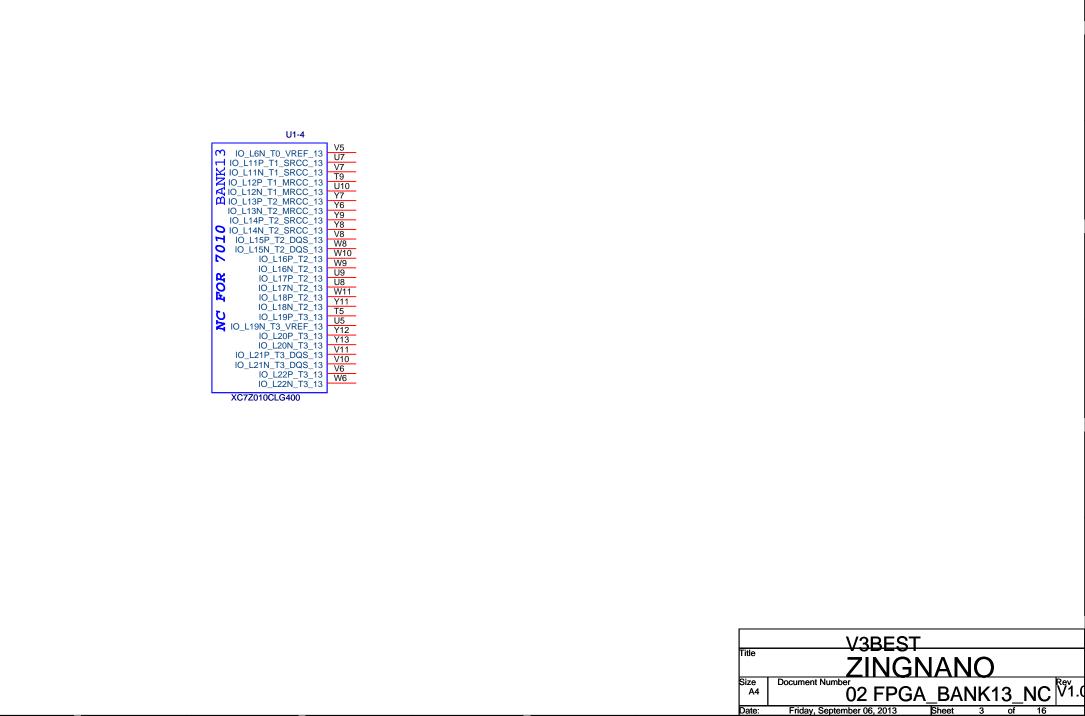
power on sequence 1 ISL8014A->1.0V

2 LM26420->1.8V,1.5V









5		4	3		
U1-2			U1-3		
	R19 HDMI G6			G14	CMOS RST
BANK 34 10_0_34	T11 HDMI DE		BANK 3 5 10_0_35	C20	CMOS_RS1
IO_L1P_T0_34	T10 HDMI VS		IO_L1P_T0_AD0P_35	B20	CMOS PIO1
IO_L1N_T0_34	T12 HDMI I2SCLK		IO_L1N_T0_AD0N_35	B19	CMOS D7
IO_L2P_T0_34	U12 HDMI I2SD		IO_L2P_T0_AD8P_35	A20	CMOS D4
IO_L2N_T0_34	U13 FPGA PUDC		IO_L2N_T0_AD8N_35	E17	PUSH
IO_L3P_T0_DQS_PUDC_B_34	V13 HDMI_I2SWS		IO_L3P_T0_DQS_AD1P_35	D18	CMOS_D10
IO_L3N_T0_DQS_34	V12 HDMI HS		IO_L3N_T0_DQS_AD1N_35	D19	CMOS D11
IO_L4P_T0_34	W13 HDMI_I2SMCLK		IO_L4P_T0_35	D20	CMOS_D8
IO_L4N_T0_34	T14 HDMI B4		IO_L4N_T0_35	E18	CMOS D9
IO_L5P_T0_34	T15 GPIOB1		IO_L5P_T0_AD9P_35	E19	CMOS_D5
IO_L5N_T0_34	P14 HDMI B2		IO_L5N_T0_AD9N_35	F16	CMOS_VS
IO_L6P_T0_34	R14 HDMI R7		IO_L6P_T0_35	F17	CMOS_HS
IO_L6N_T0_VREF_34	Y16 HDMI G0		IO_L6N_T0_VREF_35	M19	GPIOB0
IO_L7P_T1_34	Y17 HDMI_B5		IO_L7P_T1_AD2P_35	M20	GPIOA11
IO_L7N_T1_34	W14 HDMI_B0		IO_L7N_T1_AD2N_35	M17	HDMI_R6
IO_L8P_T1_34	Y14 HDMI_B1		IO_L8P_T1_AD10P_35	M18	GPIOA12
IO_L8N_T1_34	T16 HDMI_R5		IO_L8N_T1_AD10N_35	L19	GPIOA7
IO_L9P_T1_DQS_34	U17 GPIOA31		IO_L9P_T1_DQS_AD3P_35	L20	GPIOA28
IO_L9N_T1_DQS_34	V15 HDMI_B3		IO_L9N_T1_DQS_AD3N_35	K19	GPIOA3
IO_L10P_T1_34	W15 GPIOA33		IO_L10P_T1_AD11P_35	J19	GPIOA6
IO_L10N_T1_34 IO L11P T1 SRCC 34	U14 GPIOB2		IO_L10N_T1_AD11N_35 IO L11P T1 SRCC 35	L16	GPIOA_CLKP
IO_L11P_11_SRCC_34 IO_L11N_T1_SRCC_34	U15 GPIOB3		IO_L11P_11_SRCC_35 IO_L11N_T1_SRCC_35	L17	GPIOA_CLKN
IO L12P T1 MRCC 34	U18 HDMI_CLK		IO_L11N_11_3RCC_33	K17	CMOS_PCLK
IO_L12P_T1_MRCC_34	U19 GPIOA24		IO_L12P_T1_MRCC_35	K18	GPIOA14
IO_L12N_T1_MRCC_34	N18 MCLK		IO_L13P_T2_MRCC_35	H16	CMOS_XCLK
IO L13N T2 MRCC 34	P19 GPIOA17		IO L13N T2 MRCC 35	H17	CMOS_STROBE
IO_L13N_T2_WRCCC_34	N20 GPIOA15		IO L14P T2 AD4P SRCC 35	J18	GPIOA0
IO L14N T2 SRCC 34	P20 GPIOA16		IO L14N T2 AD4N SRCC 35	H18	CMOS_D1
IO_L15P_T2_DQS_34	T20 HDMI_R4		IO L15P T2 DQS AD12P 35	F19	CMOS_PIO0
IO L15N T2 DQS 34	U20 GPIOA20		IO L15N T2 DQS AD12N 35	F20	LEDG2
IO_L16P_T2_34	V20 HDMI_G3		IO_L16P_T2_35	G17	CMOS_D3
IO L16N T2 34	W20 GPIOA27		IO L16N T2 35	G18	CMOS_D2
IO L17P T2 34	Y18 GPIOA29		IO L17P T2 AD5P 35	J20	GPIOA1
IO L17N T2 34	Y19 GPIOA26 V16 HDMI B6		IO L17N T2 AD5N 35	H20 G19	GPIOA2
IO_L18P_T2_34			IO_L18P_T2_AD13P_35	G20	CMOS_D0 LEDG1
IO L18N T2 34	W16 GPIOA30 R16 HDMI B7		IO L18N T2 AD13N 35	H15	CMOS PWD
IO_L19P_T3_34	R17 HDMI G5		IO_L19P_T3_35	G15	LEDG3
IO_L19N_T3_VREF_34	T17 HDMI G7		IO_L19N_T3_VREF_35	K14	GPIOA8
IO_L20P_T3_34	R18 GPIOA23		IO_L20P_T3_AD6P_35	J14	GPIOA10
IO_L20N_T3_34	V17 HDMI G1		IO_L20N_T3_AD6N_35	N15	GPIOA32
IO_L21P_T3_DQS_34	V18 GPIOA25		IO_L21P_T3_DQS_AD14P_35	N16	HDMI R2
IO_L21N_T3_DQS_34	W18 HDMI G2		IO_L21N_T3_DQS_AD14N_35	L14	GPIOA9
IO_L22P_T3_34	W19 HDMI G4		IO_L22P_T3_AD7P_35	L15	GPIOA18
IO_L22N_T3_34	N17 HDMI R0		IO_L22N_T3_AD7N_35	M14	HDMI R1
IO_L23P_T3_34	P18 GPIOA13		IO_L23P_T3_35	M15	GPIOA22
IO_L23N_T3_34	P15 HDMI R3		IO_L23N_T3_35	K16	GPIOA5
IO_L24P_T3_34	P16 GPIOA19		IO_L24P_T3_AD15P_35	J16	LEDG0
IO_L24N_T3_34	T19 GPIOA21		IO_L24N_T3_AD15N_35	J15	GPIOA4
IO_25_34			IO_25_35		
XC7Z010CLG400			XC7Z010CLG400	•	
FPGA_PUDC 4.7K RF	1 DGND				
• • •	μ·				

HDMI CLK >>> HDMI_CLK ->>HDMI_DE 12,13 12,13 HDMI DE HDMI_HS HDMI_VS ⟨HDMI_HS 12,13 12,13 HDMI_R[7:0] HDMI_R[7:0] HDMI_G[7:0] HDMI_B[7:0] HDMI_B[7:0] HDMI_B[7:0] 12,13 12,13 12,13 HDMI_I2SD CMOS_D[11:0] CMOS_D[11:0] 14
CMOS_PCLK CMOS_PIO[1:0] 14
CMOS_HS CMOS_PCLK 14
CMOS_VS CMOS_HS 14 ⟨CMOS_XCLK 14 CMOS_RST CMOS_ACER 14
CMOS_PWD CMOS_STROBE 14 LEDG[3:0] **≪**LEDG[3:0] 12 ✓ PUSH

✓ MCLK 12 12 ⟨GPIOA_CLKP 12 GPIOA_CLKN GPIOA[33:0] ₩ GPIOA_CLKN GPIOA[33:0] GPIOB[3:0] 12 12

V3BEST Title

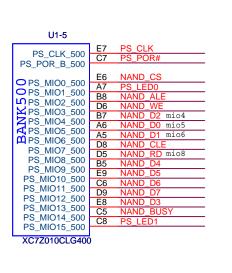
ZINGNANO

03 FPGA_BANK34_35

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Sheet

Size A4 Date: Friday, September 06, 2013



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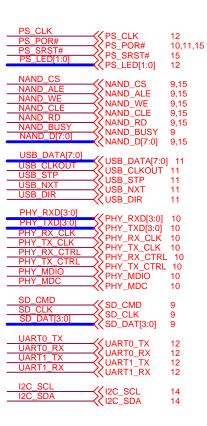
	0.0	E11	DC MIO VDEE		
PS	S MIO VREF 501	B10	PS_MIO_VREF PS_SRST#		
PS SRST B 501		B10	P5_5R51#		
		A19	PHY_TX_CLK		
\vdash	PS MIO16 501	E14	PHY TXD0		
20	PS_MIO17_501	B18	PHY TXD1		
N	PS_MIO18_501	D10	PHY TXD2		
K	PS_MIO19_501	A17	PHY TXD3		
Z	PS_MIO20_501	F14	PHY TX CTRL		
BANK	PS_MIO21_501	B17	PHY RX CLK		
Щ	PS_MIO22_501	D11	PHY RXD0		
	PS_MIO23_501	A16	PHY RXD1		
	PS_MIO24_501	F15	PHY RXD2		
	PS_MIO25_501	A15	PHY RXD3		
	PS_MIO26_501	D13	PHY RX CTRL		
	PS_MIO27_501	C16	USB DATA4		
	PS_MIO28_501	C13	USB DIR		
	PS_MIO29_501	C15	USB STP		
	PS_MIO30_501	E16	USB NXT		
	PS_MIO31_501	A14	USB DATA0		
	PS_MIO32_501	D15	USB DATA1		
	PS_MIO33_501	A12	USB_DATA2		
	PS_MIO34_501	F12	USB_DATA3		
	PS_MIO35_501 PS_MIO36_501	A11	USB_CLKOUT		
	PS_MIO36_501 PS_MIO37_501	A10	USB_DATA5		
	PS_MIO37_501 PS_MIO38_501	E13	USB_DATA6		
	PS_MIO36_501	C18	USB_DATA7		
	PS_MIO39_501 PS_MIO40_501	D14	SD_CLK		
	PS MIO40_501	C17	SD_CMD		
	PS MIO41_501	E12	SD_DAT0		
	PS MIO43 501	A9	SD_DAT1		
	PS MIO43_501	F13	SD_DAT2		
	PS MIO45 501	B15	SD_DAT3		
	PS MIO46 501	D16	UART0_RX		
	PS MIO47 501	B14	UART0_TX		
	PS MIO48 501	B12	UART1_TX		
	PS MIO49 501	C12	UART1_RX		
	PS MIO50 501	B13	I2C_SCL		
	PS MIO51 501	B9	I2C_SDA		
	PS MIO52 501	C10	PHY_MDC		
	PS MIO53 501	C11	PHY_MDIO		
XC	C7Z010CLG400				

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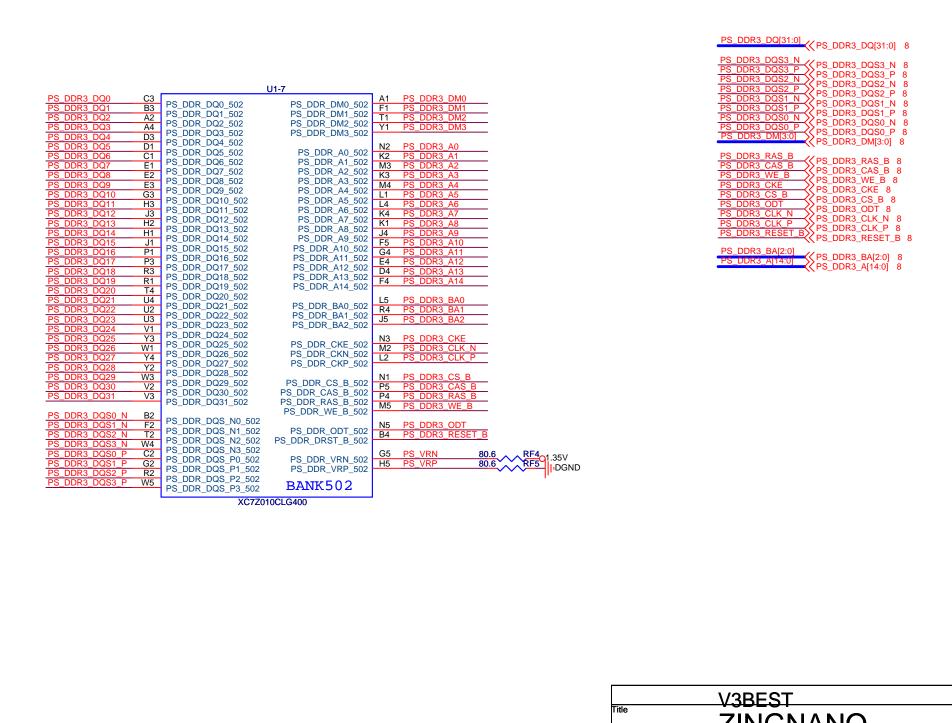
U1-6

PS_MIO_VREF	RF2 10K RF3 10K	I-DGND
PS_MIO_VREF	RF3 10K	ACCO MIO
PS_MIO_VREF	CF7 0 47uF	I'DGND
	0.47uF	II-DOIND

set to 0.9V with VCCO_MIO1 at 1.8V. In any other case, tie to VCCO_MIO1







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