SNOWLeo Hardware Userguide

Ver:1.0

威视锐科技
V3 Technology,Ltd

Change list

Version	Date	Detail
1.0	5.12.2013	V1.0

Table of Contents

Change list ..... - 2 -
Table of Contents ..... - 3 -
1. Overview ..... - 4 -
application fields ..... - 4 -
related documents ..... - 4 -
2. *Contents* ..... - 5 -
3. Hardware Features ..... - 6 -
3.1 ZYNQ SOC ..... - 7 -
3.2 Clock resource ..... - 8 -
3.2.1 PS system clock ..... - 8 -
3.2.2 PL clock ..... - 9 -
3.3 DDR3 device ..... - 9 -
3.4 Flash ..... - 12 -
3.5 USB2.0 ULPI ..... - 13 -
3.6 10/100/1000 MHz Ethernet interface ..... - 15 -
3.7 User peripheral ..... - 16 -
3.7.1 Leds ..... - 16 -
3.7.2 user push button ..... - 16 -
3.8 JTAG connector ..... - 17 -
3.9 SDIO connector ..... - 18 -
3.10 USB_UART interface ..... - 19 -
3.11 HDMI interface ..... - 20 -
3.12 XADC ..... - 21 -
3.13 expansion interface ..... - 22 -
3.13.1 CMOS FPC connector ..... - 22 -
3.13.2 TE_5177984 ..... - 23 -
4. ZYNQ configure and boot ..... - 26 -
4.1 xilinx usb cable ..... - 26 -
4.2 ZYNQ boot mode ..... - 29 -
4.2.2 program nand flash and boot ..... - 29 -

1. Overview

TheSNOWLeoembeddedprocessingmodulecombinesXilinx'Zynq-7000ExtensibleProcessingPlatform(EPP)devicewithfastDDR3SDRAM,NANDflash,aGigabitEthernetPHY,HDMI andthusformsacompleteandpowerfulembeddedprocessingsystem.TheSNOWLeoEmbeddedProcessingmodulereducesdevelopmenteffort,redesignriskandimprovestime-to-marketforyourembeddedsystem.

application fields

- Automotive driver assistance, driver information, and infotainment
- Broadcast camera
- Industrial motor control, industrial networking, and machine vision
- IP and Smart camera
- LTE radio and baseband
- Medical diagnostics and imaging
- Multifunction printers
- Video and night vision equipment

related documents

- ✓ 《SNOWLeo Hardware user guide》
- ✓ 《SNOWLeo quick start》

2. *Contents*

SNOWLeoSDR Kit Contents		
order	**content**	**quantity**
1	SNOWLeo SDR with MYRIAD moudule	1
2	USB2.0-micro cable	1
3	USB2.0 OTG hub	1
4	HDMI typeC-HDMI typeA	1
5	TF Card (4G)	1
6	Antenna	1

3. Hardware Features

SNOWLeo hardware resources,below

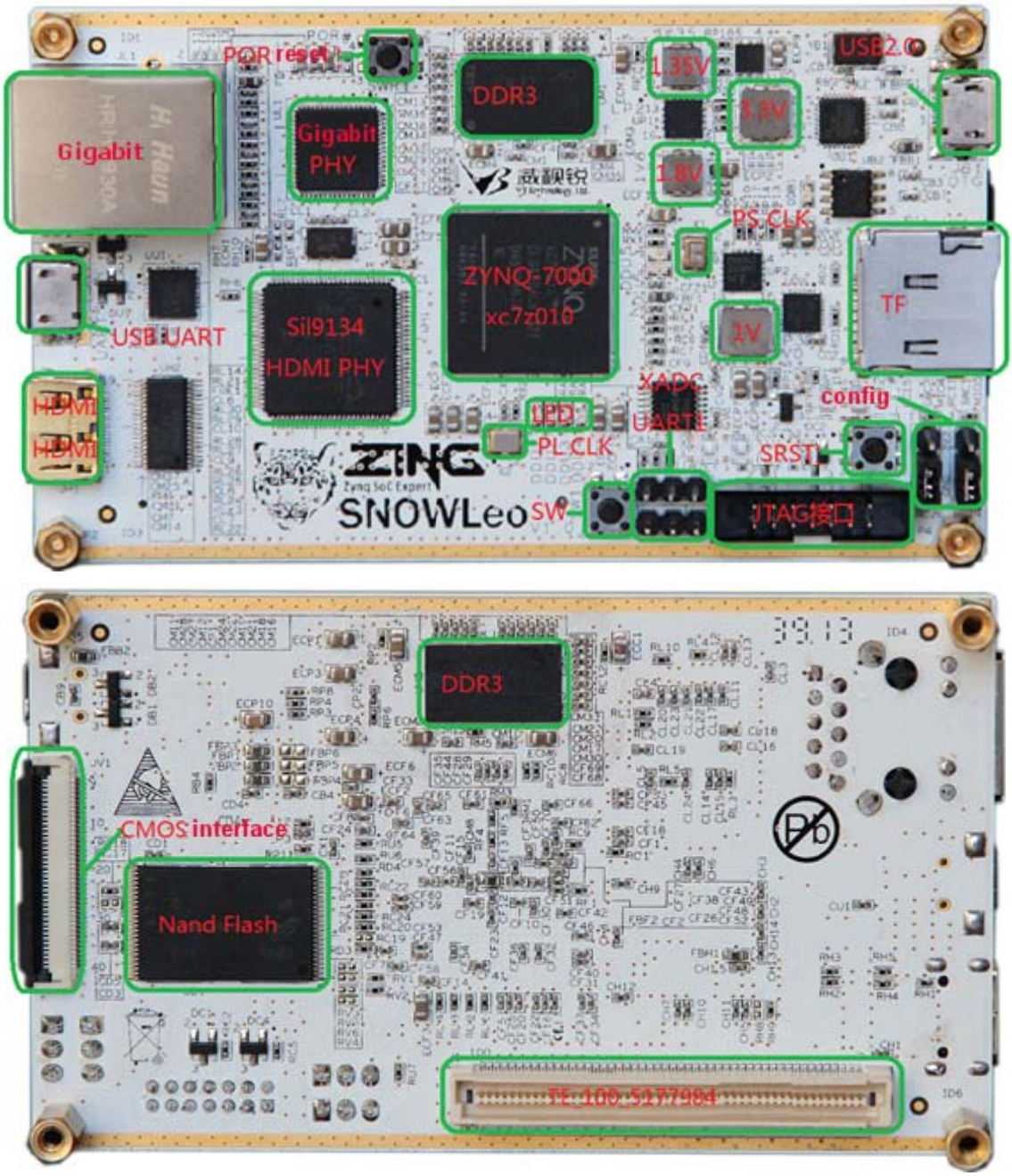


Figure 3.1 SNOWLeo hardware diagram

Hardware resource features：

- ✧ Zynq-7000 XC7Z010-1CLG400C；
- ✧ 512MB DDR3 device x2；
- ✧ 4GB Nand flash

- PS oscillator：33.333MHz LVCMOS oscillator
- PL oscillator：50MHz LVCMOS oscillator
- USB2.0 ULPI PHY and Interface, USB3320C-EZK
- SDIO interface；
- USB_UART PHY and interface,CP2103
- HDMI PHY and TYPEC interface, SII9134
- Gigabit PHY and RJ45, 88E1116
- User peripheral: POR Reset Button,push button, LEDs
- XADC 3pin connector、UART1 3pin connector
- JTAG 14pin connector
- expansion interface：CMOS FPC connector and TE5177984 100pin connector；
- Power DCDC: 3.3V,1.8V,1.35V,1V

3.1ZYNQ SOC

The Zynq-7000 architecture conveniently maps the custom logic and software in the PL and PS respectively. It enables the realization of unique and differentiated system functions. The integration of the PS with the PL provides levels of performance that two-chip solutions (e.g., an ASSP with an FPGA) cannot match due to their limited I/O bandwidth, loose-coupling and power budgets.

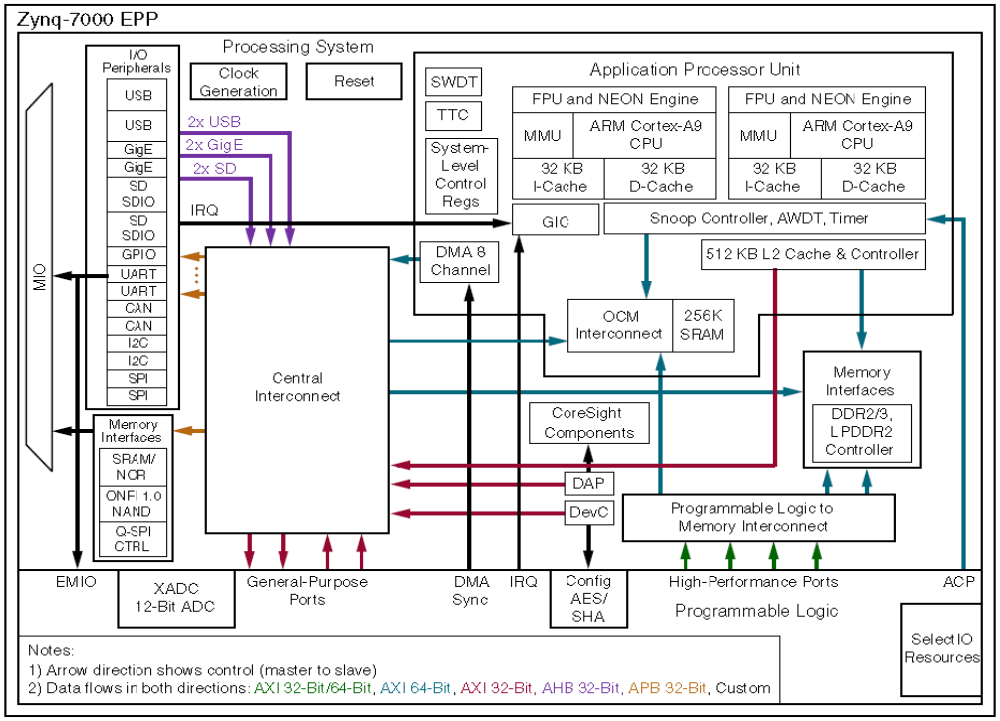


Figure3. 2 ZYNQ EPP Overview

3.2 Clock resource

3.2.1 PS system clock

Crystal oscillator X1 offer the 33.333MHz to PS system, schematic in figure 3.3，

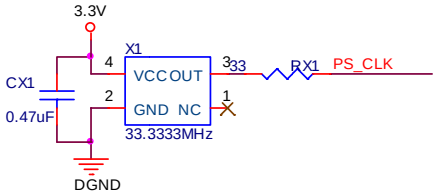


Figure3.3 PS clock system

PS clock pin list in able 3.1。

Table 3.1 PS clock pin list

PS clock	Signal name	ZYNQ pin name
X1	PS_CLK	E7

All of the clocks generated by the PS clock subsystem are derived from one of three programmable PLLs: CPU, DDR and I/O. Each of these PLLs is loosely associated with the clocks in the CPU, DDR and peripheral subsystems. In figure 3.4, detail information can be acquired in ug585-Zynq-7000-TRM（download）。

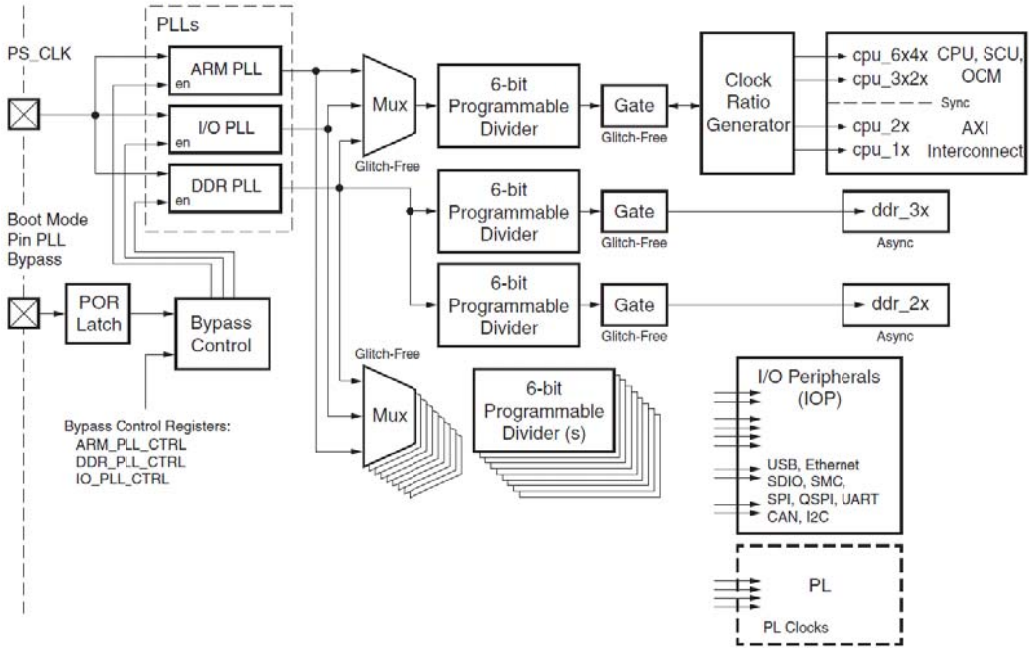


Figure 3.4 PS clock tree

3.2.2 PL clock

ZYNQEPP offer a single clock 50MHz for PL, LVCMOS. schematic in figure 3.5，

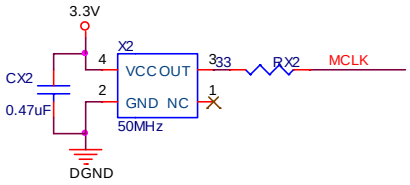


Figure 3.5 PL clock

Table 3.2 PL clock pin list

PL clock	Signal name	ZYNQ pin list
X2	MCLK	N18

3.3 DDR3 device

Two DDR3L component installed on SNOWLeo. The memory model is MT41K128M16JT by MICRON. DDR3L is low voltage version which powered by 1.35V DCDC. Twochipsareconnectedinparalleltoachieve32bitdatawidth, 512MB. DDR3L SDRAMrunsatupto533MHz.
NoexternalterminationisimplementedonthehardwareItisthusstronglyrecommendedtoenabletheDDR3SDRAMdevice ’son-dietermination(ODT)feature.Thechipselectisalwaysactive,usetheclockenablesignaltodisablethedeviceifnotused.

Table 3.3 DDR3LSDRAMtypes

Type	Size	Configuration	Manufacture
MT41K128M16JT	256MB	128M x 16bit	MICRON

Table3.4 shows DDR3LSDRAM Parameters.

Table 3.4 DDR3LSDRAM Parameters

Parameter	Value
Memory Type	DDR3
DRAMBusWidth	32bit
OperatingFreq	533MHz
DRAMICBuswidth	16bits
DeviceCapacity	1024bits
SpeedBin	DDR3_1066
Bank Bits	3
Row Bits	14
Column Bits	10
CAS latency	7
CAS write latency	6

CAS to RAS delay	4
Precharge time	6
tRC	49.5 ns
tRASmin	36 ns
tFAW	45 ns

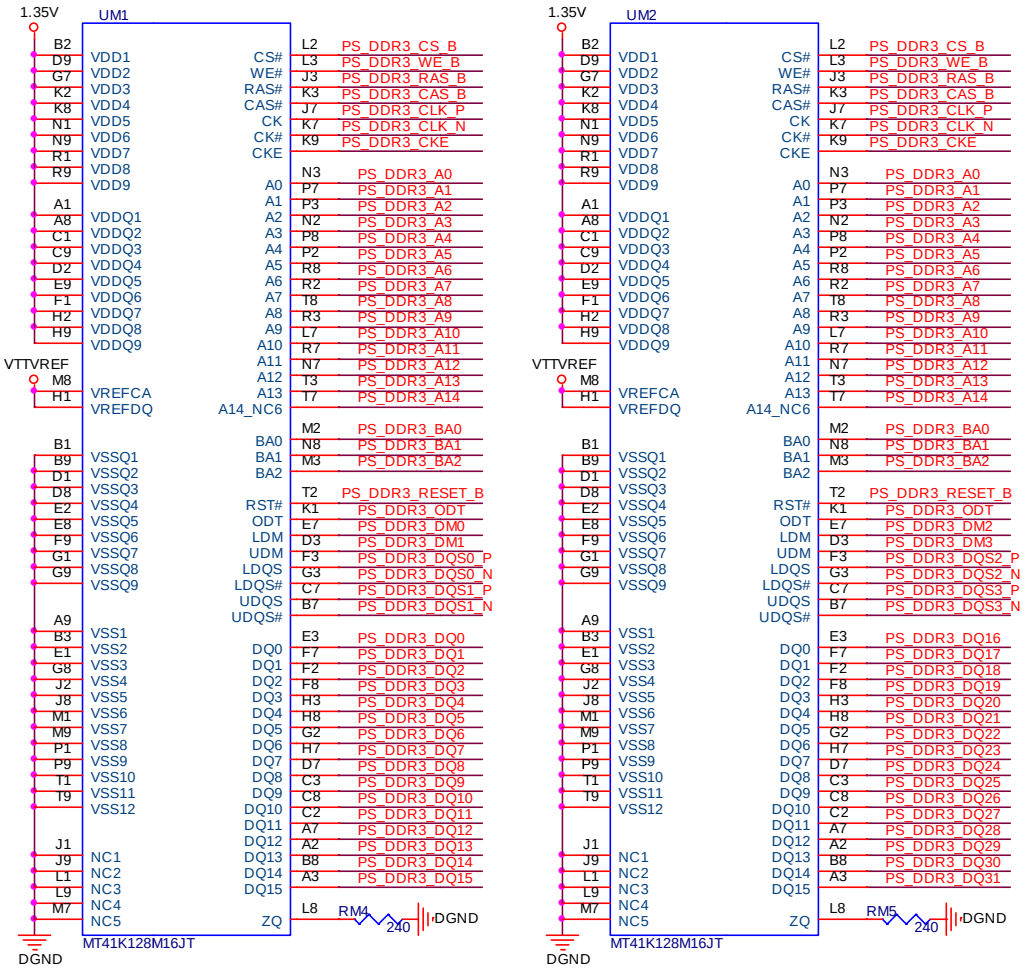


Figure 3.6 DDR3L SDRAM schematic

Table 3.5 DDR3L SDRAM pin list

ZYNQ pin list	Signal name	DDR3 device pin name	Component name
C3	PS_DDR3_DQ0	DQ0	UM1
B3	PS_DDR3_DQ1	DQ1	UM1
A2	PS_DDR3_DQ2	DQ2	UM1
A4	PS_DDR3_DQ3	DQ3	UM1
D3	PS_DDR3_DQ4	DQ4	UM1
D1	PS_DDR3_DQ5	DQ5	UM1
C1	PS_DDR3_DQ6	DQ6	UM1
E1	PS_DDR3_DQ7	DQ7	UM1
E2	PS_DDR3_DQ8	DQ8	UM1

E3	PS_DDR3_DQ9	DQ9	UM1
G3	PS_DDR3_DQ10	DQ10	UM1
H3	PS_DDR3_DQ11	DQ11	UM1
J3	PS_DDR3_DQ12	DQ12	UM1
H2	PS_DDR3_DQ13	DQ13	UM1
H1	PS_DDR3_DQ14	DQ14	UM1
J1	PS_DDR3_DQ15	DQ15	UM1
P1	PS_DDR3_DQ16	DQ16	UM2
P3	PS_DDR3_DQ17	DQ17	UM2
R3	PS_DDR3_DQ18	DQ18	UM2
R1	PS_DDR3_DQ19	DQ19	UM2
T4	PS_DDR3_DQ20	DQ20	UM2
U4	PS_DDR3_DQ21	DQ21	UM2
U2	PS_DDR3_DQ22	DQ22	UM2
U3	PS_DDR3_DQ23	DQ23	UM2
V1	PS_DDR3_DQ24	DQ24	UM2
Y3	PS_DDR3_DQ25	DQ25	UM2
W1	PS_DDR3_DQ26	DQ26	UM2
Y4	PS_DDR3_DQ27	DQ27	UM2
Y2	PS_DDR3_DQ28	DQ28	UM2
W3	PS_DDR3_DQ29	DQ29	UM2
V2	PS_DDR3_DQ30	DQ30	UM2
V3	PS_DDR3_DQ31	DQ31	UM2
A1	PS_DDR3_DM0	DM0	UM1
C2	PS_DDR3_DQS0_P	DQS0_P	UM1
B2	PS_DDR3_DQS0_N	DQS0_N	UM1
F1	PS_DDR3_DM1	DM1	UM1
G2	PS_DDR3_DQS1_P	DQS1_P	UM1
F2	PS_DDR3_DQS1_N	DQS1_N	UM1
T1	PS_DDR3_DM2	DM2	UM2
R2	PS_DDR3_DQS2_P	DQS2_P	UM2
T2	PS_DDR3_DQS2_N	DQS2_N	UM2
Y1	PS_DDR3_DM3	DM3	UM2
W5	PS_DDR3_DQS3_P	DQS3_P	UM2
W4	PS_DDR3_DQS3_N	DQS3_N	UM2
N2	PS_DDR3_A0	A0	UM1，UM2
K2	PS_DDR3_A1	A1	UM1，UM2
M3	PS_DDR3_A2	A2	UM1，UM2
K3	PS_DDR3_A3	A3	UM1，UM2
M4	PS_DDR3_A4	A4	UM1，UM2
L1	PS_DDR3_A5	A5	UM1，UM2
L4	PS_DDR3_A6	A6	UM1，UM2

K4	PS_DDR3_A7	A7	UM1，UM2
K1	PS_DDR3_A8	A8	UM1，UM2
J4	PS_DDR3_A9	A9	UM1，UM2
F5	PS_DDR3_A10	A10	UM1，UM2
G4	PS_DDR3_A11	A11	UM1，UM2
E4	PS_DDR3_A12	A12	UM1，UM2
D4	PS_DDR3_A13	A13	UM1，UM2
F4	PS_DDR3_A14	A14	UM1，UM2
L5	PS_DDR3_BA0	BA0	UM1，UM2
R4	PS_DDR3_BA1	BA1	UM1，UM2
J5	PS_DDR3_BA2	BA2	UM1，UM2
L2	PS_DDR3_CLK_P	CK	UM1，UM2
M2	PS_DDR3_CLK_N	CK_B	UM1，UM2
N3	PS_DDR3_CKE	CKE	UM1，UM2
M5	PS_DDR3_WE_B	WE_B	UM1，UM2
P5	PS_DDR3_CAS_B	CAS_B	UM1，UM2
P4	PS_DDR3_RAS_B	RAS_B	UM1，UM2
B4	PS_DDR3_RESET_B	RESET_B	UM1，UM2
N1	PS_DDR3_CS_B	CS_B	UM1，UM2
N5	PS_DDR3_ODT	ODT	UM1，UM2
G5	PS_VRN		
H5	PS_VRP		
H6	VTTVREF		
P6	VTTVREF		

3.4 Flash

SNOWLeo has two flash Component , nand flash and tf card. This section is nand flashcanbeusedtostoretheFPGAbitstreams,ARMapplicationcode(e.g.thebootloader)andotheruserdata.Itisconnectedto theEPPMIOport

Table 3.6 Flash type

Flash Type	Chip Type	Size
NAND Flash	MT29F4G08ABADAWP	4Gb

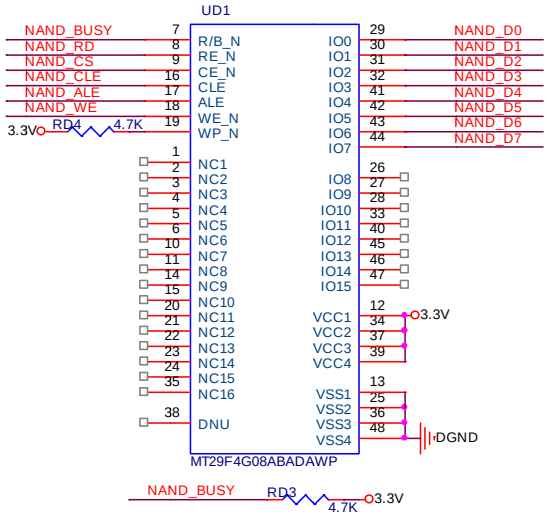


Figure 3.7 nand flash schematic

Table 3.7 nand flash pin list

ZYNQ pin list	Signal name	Nand flash pin name
C5/MIO14	NAND_BUSY	R/B_N
D5/MIO8	NAND_RD	RE_N
E6/MIO0	NAND_CS	CE_N
D8/MIO7	NAND_CLE	CLE
B8/MIO2	NAND_ALE	ALE
D6/MIO3	NAND_WE	WE_N
A6/MIO5	NAND_D0	IO0
A5/MIO6	NAND_D1	IO1
B7/MIO4	NAND_D2	IO2
E8/MIO13	NAND_D3	IO3
B5/MIO9	NAND_D4	IO4
E9/MIO10	NAND_D5	IO5
C6/MIO11	NAND_D6	IO6
D9/MIO12	NAND_D7	IO7

3.5 USB2.0 ULPI

The USB controller is capable of fulfilling a wide range of applications for USB 2.0 implementations as a host, a device, or On-the-Go. The USB controller I/O uses the ULPI protocol to connect external ULPI PHY via the MIO pins. The ULPI interface provides an 8-bit parallel SDR data path from the controller's internal UTMI-like bus to the PHY. The ULPI interface minimizes device pin count and is controlled by a 60 MHz clock output from the PHY. A 24MHz crystal oscillator offers the clock for USB3320C。

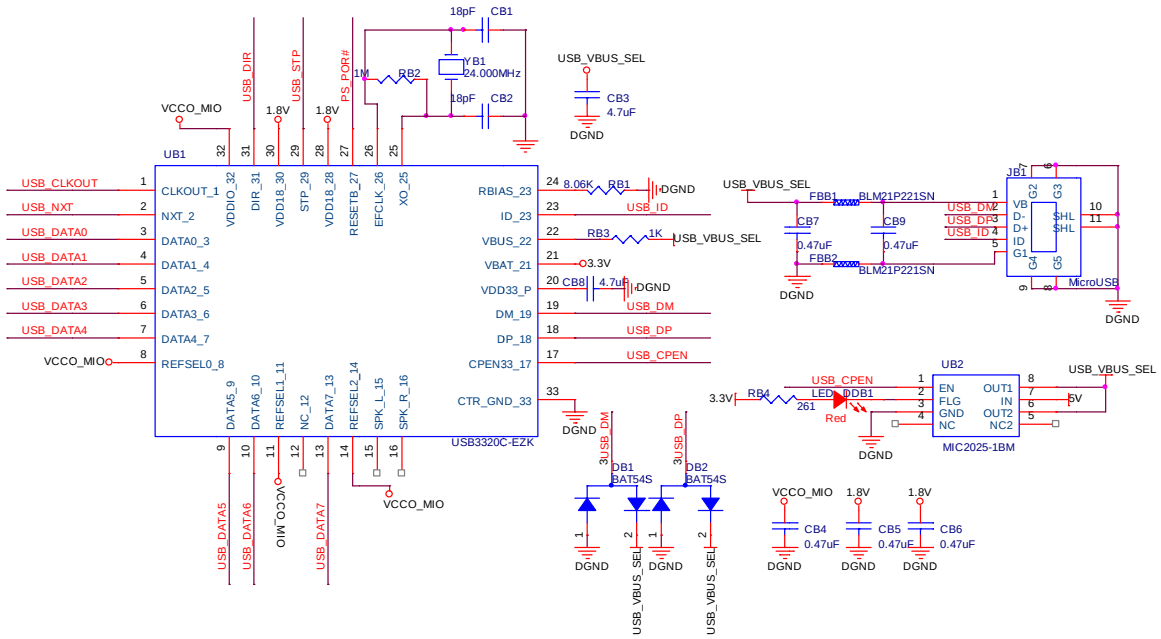


Figure 3.8 USB3320C schematic

Table 3.8 USB pin list

ZYNQ EPP			Signal name	USB3320 pin
Pin name	bank	Pin list		
PS_MIO36	501	A11	USB_CLKOUT	1
PS_MIO31	501	E16	USB_NXT	2
PS_MIO32	501	A14	USB_DATA0	3
PS_MIO33	501	D15	USB_DATA1	4
PS_MIO34	501	A12	USB_DATA2	5
PS_MIO35	501	F12	USB_DATA3	6
PS_MIO28	501	C16	USB_DATA4	7
PS_MIO37	501	A10	USB_DATA5	9
PS_MIO38	501	E13	USB_DATA6	10
PS_MIO39	501	C18	USB_DATA7	13
PS_MIO30	501	C15	USB_STP	29
PS_MIO29	501	C13	USB_DIR	31

USB interface pin description in table3.9

Table3.9 USB interface pin description

USB interface		Signal name	description	USB3320 pin
pin	name			
1	VBUS	USB_VBUS_SEL	5V power from host	22

2	DM	USB_DM	Differential signal -	19
3	DP	USB_DP	Differential signal +	18
4	ID	USB_ID	Usb ID	23
5	GND	GND	ground	33

3.6 10/100/1000 MHz Ethernet interface

Thereisone10/100/1000Ethernet PHYontheSNOWLeoboard,connectedtotheEPPviatheRGMIIinterface.TheRGMIIinterfaceisconnectedtotheMIOport forusewiththeintegratedMAC.ThecentertapvoltageisalsoprovidedbytheSNOWLeoembeddedprocessingmodule.The LEDsignalsareactivelow. Figure 3.10 shows the Ethernet PHY circuit

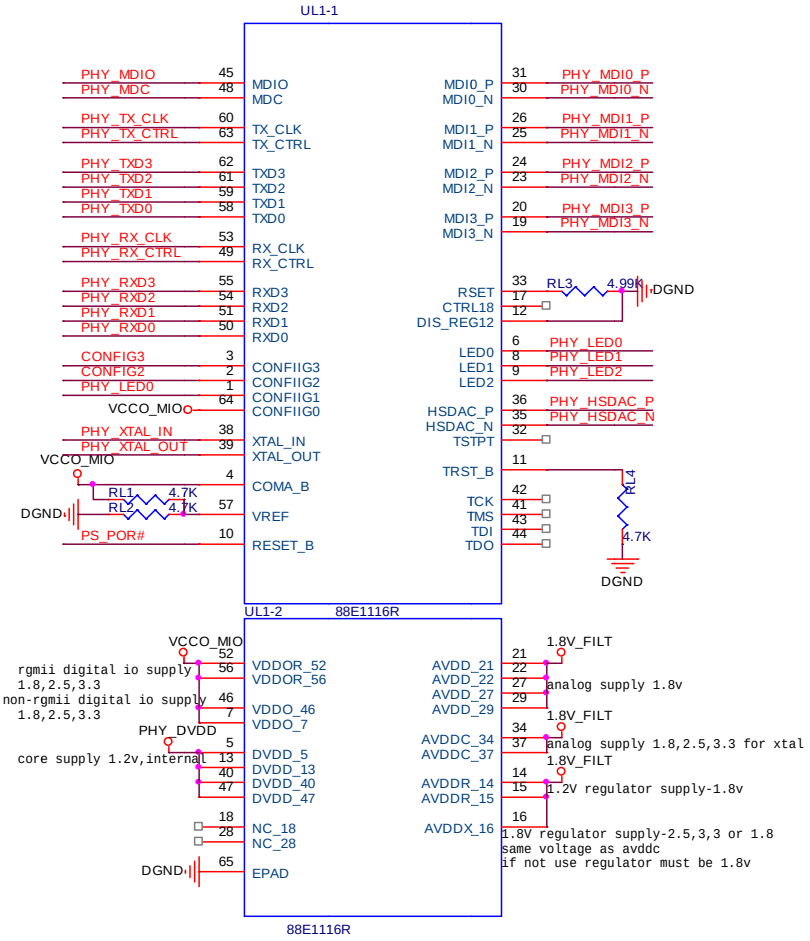


Figure 3.10 Ethernet PHY schematic

Ethernet PHY pin list shows in table3.10

Table 3.10 Ethernet PHY pin list

ZYNQ EPP			Signal name	M88E1116R PHY	
Pin name	bank	Pin list		Pin list	Pin name
PS_MIO53	501	C11	PHY_MDIO	45	MDIO
PS_MIO52	501	C10	PHY_MDC	48	MDC
PS_MIO16	501	A19	PHY_TX_CLK	60	TX_CLK

PS_MIO21	501	F14	PHY_TX_CTRL	63	TX_CTRL
PS_MIO20	501	A17	PHY_TXD3	62	TXD3
PS_MIO19	501	D10	PHY_TXD2	61	TXD2
PS_MIO18	501	B18	PHY_TXD1	59	TXD1
PS_MIO17	501	E14	PHY_TXD0	58	TXD0
PS_MIO22	501	B17	PHY_RX_CLK	53	RX_CLK
PS_MIO27	501	D13	PHY_RX_CTRL	49	RX_CTRL
PS_MIO26	501	A15	PHY_RXD3	55	RXD3
PS_MIO25	501	F15	PHY_RXD2	54	RXD2
PS_MIO24	501	A16	PHY_RXD1	51	RXD1
PS_MIO23	501	D11	PHY_RXD0	50	RXD0

3.7 User peripheral

3.7.1 Leds

SNOWLeo includes six leds. Two leds connect to PS，other four leds connect to PL.

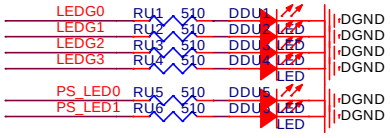


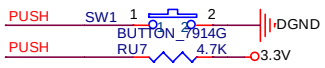
Figure 3.11 led schematic

Table 3.11 led pin list

Device name	Signal name	ZYNQ pin list
DDU1	LEDG0	J16
DDU2	LEDG1	G20
DDU3	LEDG2	F20
DDU4	LEDG3	G15
DDU5	PS_LED0	A7
DDU6	PS_LED1	C8

3.7.2 user push button

SNOWLeo has three push button. One for users, two reest button.



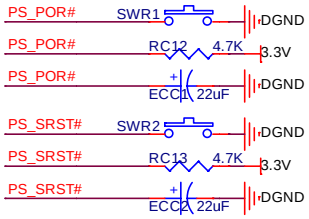


Figure3.12 push button schematic

Table3.12push button pin list

Device name	Signal name	ZYNQ pin list
SW1	PUSH（user push button）	E17
SWR1	PS_POR#（power on reset button）	C7
SWR2	PS_SRST#（system reset button）	B10

3.8 JTAG connector

TheARMandFPGAJTAGinterfacesareconnectedtoasingleJTAGchain. ThisinterfacecanbeusedtodebugtheARMprocessor aswellastoconfigureanddebugtheFPGAlogic.

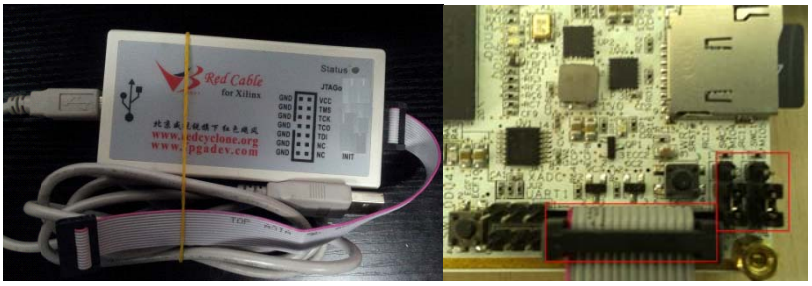


Figure3.13 redcable for xilinx and jtag connector

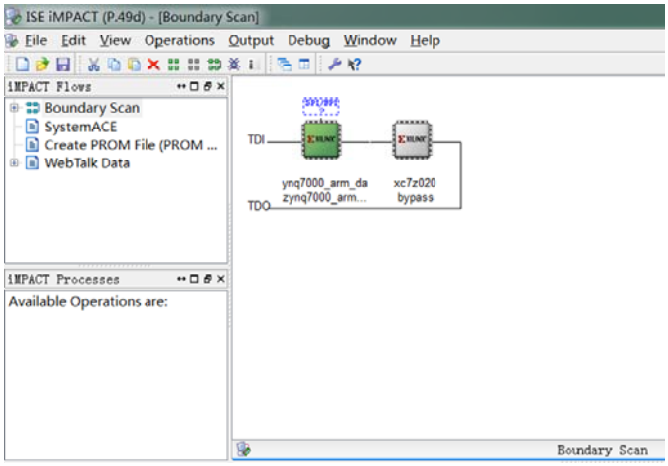


Figure 3.14 xilinx impact

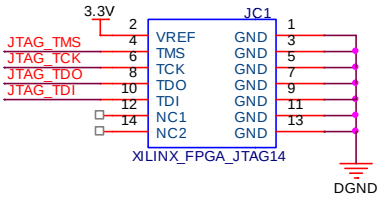


Figure 3.15 JTAG connector schematic

Table3.13 JTAG pin list

Signal name	ZYNQ pin list
JTAG_TCK	F9
JTAG_TMS	J6
JTAG_TDI	G6
JTAG_TDO	F6

3.9 SDIO connector

The SD/SDIO controller communicates with SD memory cards. The SDIO interface is routed through the MIO. TXS02612 changed the 1.8V form ZYNQ EPP PS 501BANK to 3.3V SDIO standard voltage.

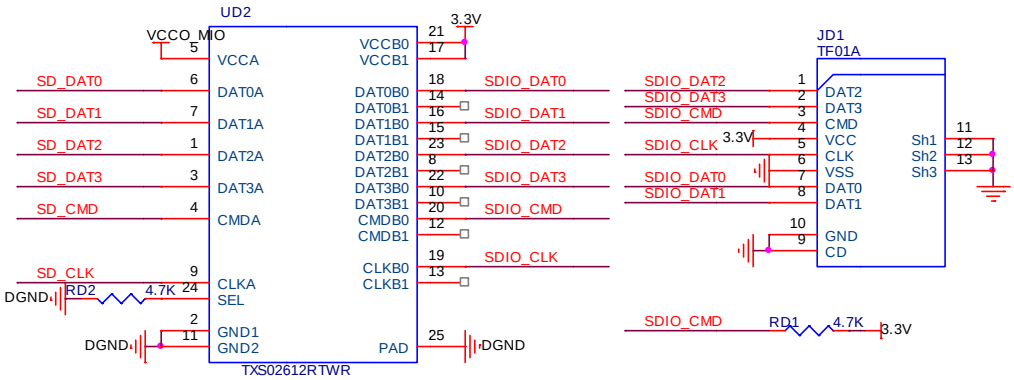


Figure 316 TF card interface schematic

Table3.14 SDIO pin list

UD2pin name	Signal name	ZYNQ pin list
CLKA	SD_CLK	D14
CMDA	SD_CMD	C17
DAT0A	SD_DAT0	E12
DAT1A	SD_DAT1	A9
DAT2A	SD_DAT2	F13
DAT3A	SD_DAT3	B15

Table3.15 voltage converter IC description

Signal name	UD2voltage converter		SDIO connector	
	Pin list	Pin name	Pin list	Pin name

GND	N/A	N/A	9	CD
SDIO_CMD	20	CMDB0	3	CMD
SDIO_CLK	19	CLKB0	5	CLK
SDIO_DAT2	23	DAT2B0	1	DAT2
SDIO_DAT1	16	DAT1B0	8	DAT1
SDIO_DAT0	18	DAT0B0	7	DAT0
SDIO_DAT3	22	DAT3B0	2	DAT3

3.10 USB_UART interface

The CP2103 is a highly-integrated USB-to-UART Bridge Controller providing a simple solution for updating RS-232/RS-485 designs to USB using a minimum of components and PCB space. SNOWLeo is powered by USB bus power.

Silicon Labs provides the driver for com vcp on PC. VCP driver should be installed before pc connects to SNOWLeo.

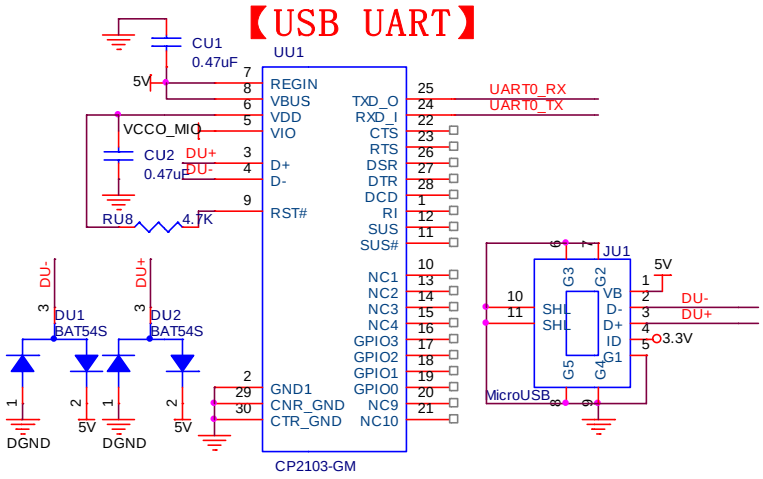


Figure 3.17 CP2103GM schematic

Table 3.16 USB_UART pin list

ZYNQ EPP			UART direction	Signal name	CP2103GM	
Pin name	BANK	Pin list			Pin list	UART
PS_MIO46	501	B14	TX,data output	UART0_TX	24	RXD,data input
PS_MIO47	501	D16	RX,data input	UART0_RX	25	TXD,data output

3.11 HDMI interface

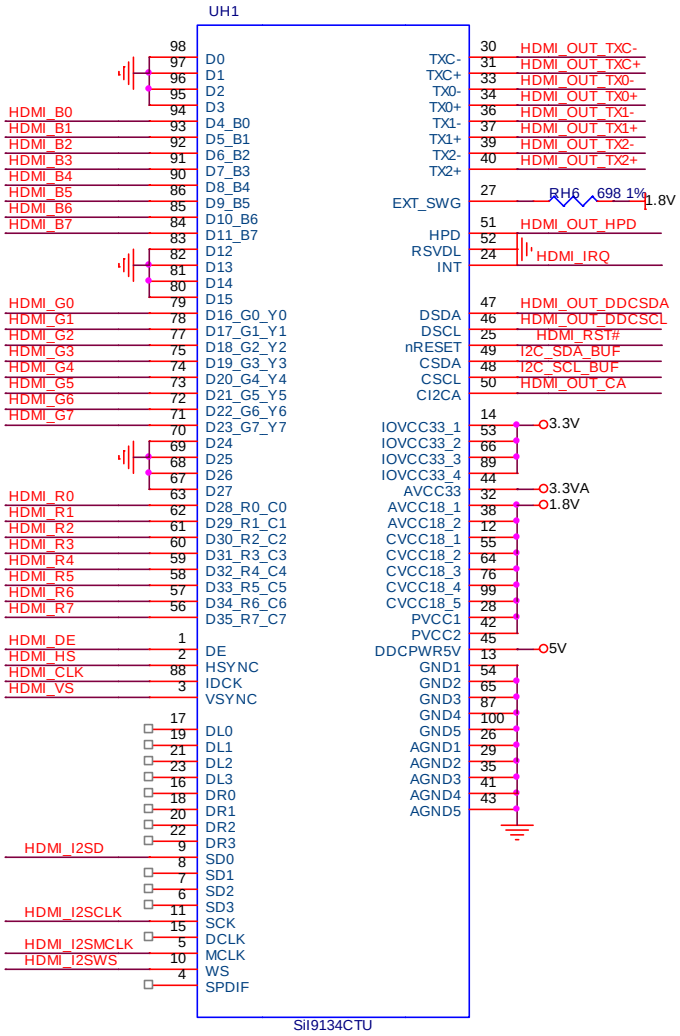


Figure 3.18 HDMI schematic

Table3.17 HDMI pin list

ZYNQ pinlist	Signal name	Sil9134CTU	
		Pin list	Pin name
N17	HDMI_R0	63	D28_R0_C0
M14	HDMI_R1	62	D29_R1_C1
N16	HDMI_R2	61	D30_R2_C2
P15	HDMI_R3	60	D31_R3_C3
T20	HDMI_R4	59	D32_R4_C4
T16	HDMI_R5	58	D33_R5_C5
M17	HDMI_R6	57	D34_R6_C6
R14	HDMI_R7	56	D35_R7_C7
Y16	HDMI_G0	79	D16_G0_Y0
V17	HDMI_G1	78	D17_G1_Y1
W18	HDMI_G2	77	D18_G2_Y2

V20	HDMI_G3	75	D19_G3_Y3
W19	HDMI_G4	74	D20_G4_Y4
R17	HDMI_G5	73	D21_G5_Y5
R19	HDMI_G6	72	D22_G6_Y6
T17	HDMI_G7	71	D23_G7_Y7
W14	HDMI_B0	94	D4_B0
Y14	HDMI_B1	93	D5_B1
P14	HDMI_B2	92	D6_B2
V15	HDMI_B3	91	D7_B3
T14	HDMI_B4	90	D8_B4
Y17	HDMI_B5	89	D9_B5
V16	HDMI_B6	88	D10_B6
R16	HDMI_B7	87	D11_B7
T11	HDMI_DE	1	DE
T10	HDMI_VS	3	VSYNC
V12	HDMI_HS	2	HSYNC
U18	HDMI_CLK	5	MCLK
T12	HDMI_I2SCLK	11	SCK
U12	HDMI_I2SD	9	SD0
W13	HDMI_I2SMCLK	5	DCLK
V13	HDMI_I2SWS	10	WS
B13	I2C_SCL_BUF	48	CSCL
B9	I2C_SDA_BUF	49	CSDA

3.12 XADC

The Xilinx analog mixed signal module, referred to as the XADC, is a hard macro. It has JTAG and DRP interfaces for accessing the XADC's status and control registers in the 7-series FPGAs. Zynq-7000 AP SoC devices add a third interface, the PS-XADC interface for the PS software to control the XADC. The Zynq-7000 APSoC devices combine a flexible analog-to-digital converter with programmable logic to address a broad range of analog data acquisition and monitoring requirements.

The XADC has two 12-bit 1 mega samples per second (MSPS) ADCs with separate track and hold amplifiers,an analog multiplexer (up to 17 external analog input channels),and on-chip thermal and on-chip voltage sensors.

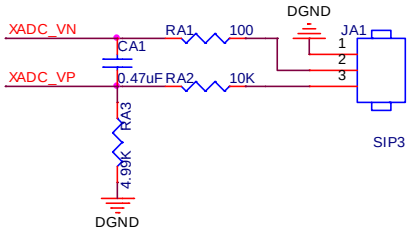


Figure 3.19 XADC schematic

Table3.18 XADCpin list

Signal name	ZYNQ pin list
XADC_VN	L10
XADC_VP	K9

XADC(JA1) is ZYNQ EPP dedicated VP / VN analog input.

Table3.19 XADC parameter

parameter	value
VCC_ADC	1.8V
VREF_ADC	1.25V
ADC range	0—1V
ADC sample rate	1MSPS
ADC channels	16

3.13 expansion interface

SNOWLeo includes two expansion interface,cmos FPC connector and TE_5177984 connector。

3.13.1 CMOS FPC connector

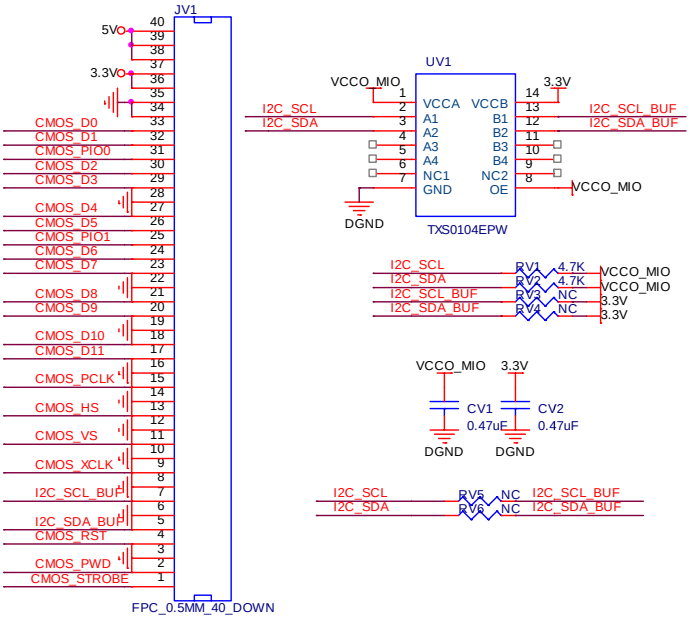


Figure 3.20 cmos connector

Table 3.20 cmos pin list

JV1 pin list	Signal name	ZYNQ pin list
33	CMOS_D0	G19
32	CMOS_D1	H18
30	CMOS_D2	G18
29	CMOS_D3	G17
27	CMOS_D4	A20

26	CMOS_D5	E19
24	CMOS_D6	C20
23	CMOS_D7	B19
21	CMOS_D8	D20
20	CMOS_D9	E18
18	CMOS_D10	D18
17	CMOS_D11	D19
13	CMOS_HS	F17
11	CMOS_VS	F16
15	CMOS_PCLK	K17
10	CMOS_PIO0	F19
31	CMOS_PIO1	B20
25	CMOS_PWD	H15
4	CMOS_RST	G14
1	CMOS_STROBE	H17
9	CMOS_XCLK	H16
7	I2C_SCL_BUF	B13
5	I2C_SDA_BUF	B9

3.13.2 TE_5177984

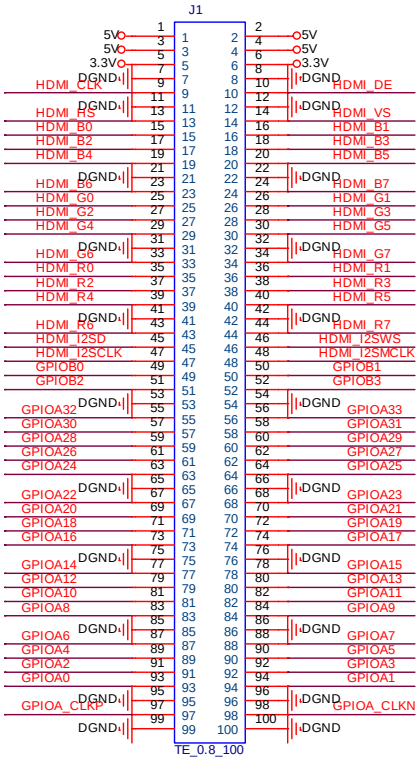


Figure 3.21 JE1 schematic

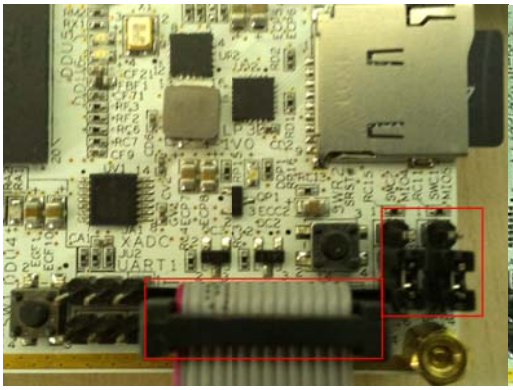
Table3.2.12 JE1 pin list

J1 pin list	Signal name	Zynq pin list	J1 pin list	Signal name	Zynq pin list
1	5V		2	5V	
3	5V		4	5V	
5	3.3V		6	3.3V	
7	DGND		8	DGND	
9	HDMI_CLK	U18	10	HDMI_DE	T11
11	DGND		12	DGND	
13	HDMI_HS	V12	14	HDMI_VS	T10
15	HDMI_B0	W14	16	HDMI_B1	Y14
17	HDMI_B2	P14	18	HDMI_B3	V15
19	HDMI_B4	T14	20	HDMI_B5	Y17
21	DGND		22	DGND	
23	HDMI_B6	V16	24	HDMI_B7	R16
25	HDMI_G0	Y16	26	HDMI_G1	V17
27	HDMI_G2	W18	28	HDMI_G3	V20
29	HDMI_G4	W19	30	HDMI_G5	R17
31	DGND		32	DGND	
33	HDMI_G6	R19	34	HDMI_G7	T17
35	HDMI_R0	N17	36	HDMI_R1	M14
37	HDMI_R2	N16	38	HDMI_R3	P15
39	HDMI_R4	T20	40	HDMI_R5	T16
41	DGND		42	DGND	
43	HDMI_R6	M17	44	HDMI_R7	R14
45	HDMI_I2SD	U12	46	HDMI_I2SWS	V13
47	HDMI_I2SCLK	T12	48	HDMI_I2SMCLK	W13
49	GPIOB0	M19	50	GPIOB1	T15
51	GPIOB2	U14	52	GPIOB3	U15
53	DGND		54	DGND	
55	GPIOA32	N15	56	GPIOA33	W15
57	GPIOA30	W16	58	GPIOA31	U17
59	GPIOA28	L20	60	GPIOA29	Y18
61	GPIOA26	Y19	62	GPIOA27	W20
63	GPIOA24	U19	64	GPIOA25	V18
65	DGND		66	DGND	
67	GPIOA22	M15	68	GPIOA23	R18
69	GPIOA20	U20	70	GPIOA21	T19
71	GPIOA18	L15	72	GPIOA19	P16
73	GPIOA16	P20	74	GPIOA17	P19
75	DGND		76	DGND	
77	GPIOA14	K18	78	GPIOA15	N20
79	GPIOA12	M18	80	GPIOA13	P18

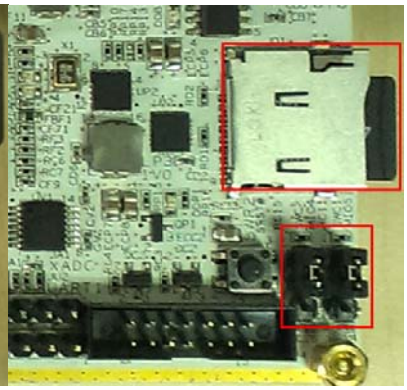
81	GPIOA10	J14	82	GPIOA11	M20
83	GPIOA8	K14	84	GPIOA9	L14
85	DGND		86	DGND	
87	GPIOA6	J19	88	GPIOA7	L19
89	GPIOA4	J15	90	GPIOA5	K16
91	GPIOA2	H20	92	GPIOA3	K19
93	GPIOA0	J18	94	GPIOA1	J20
95	DGND		96	DGND	
97	GPIOA_CLKP	L16	98	GPIOA_CLKN	L17
99	DGND		100	DGND	

4. ZYNQ configure and boot

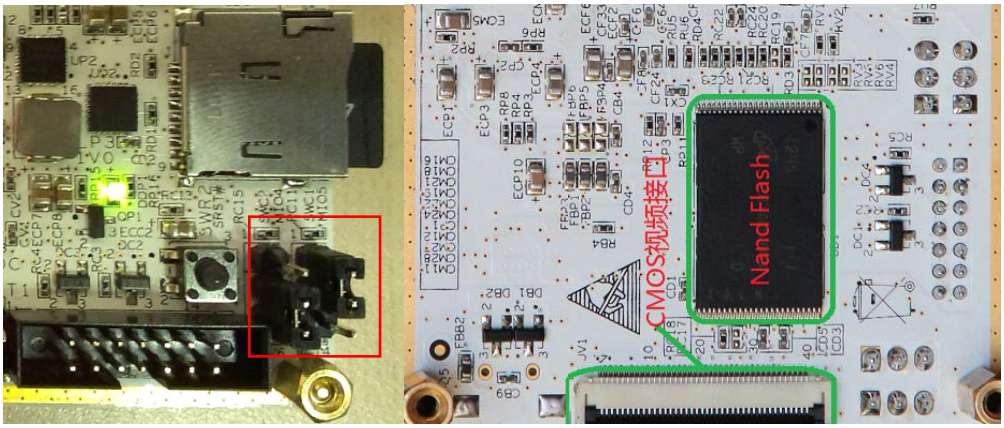
This section mainly introduces the configure and boot method of SNOWLeo kit. ZYNQ support JTAG nand flash and TF card boot method. Jtag usb cable is redcable for xilinx。ZYNQ jtag usage is same as general FPGA.



JTAG boot pin jump



TF card boot pin jump



Nand flash boot pin jump

Figure4.1 ZYNQ boot pin jump

4.1 xilinx usb cable

redcable for xilinx usb to configure zynq. Flash and fpga can be programmed by jtag connector. USB-A connects to PC and 14pin connects to PCB board

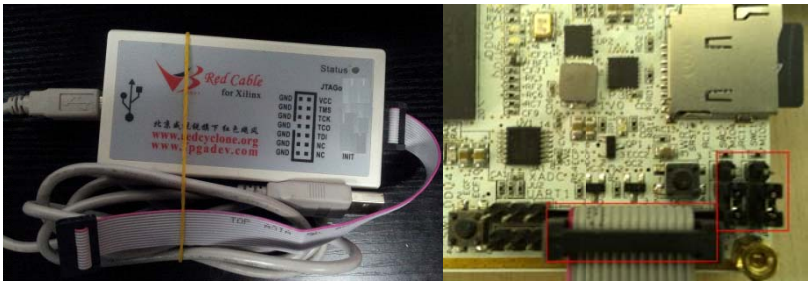


Figure4.2 JTAG connect

1 connect jtag and pin jumped as below figure 4.3

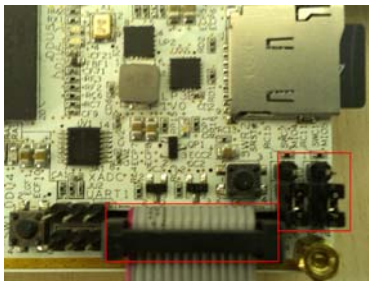


Figure 4.3 JTAG

2 open SDK of xilinx program bit to FPGA

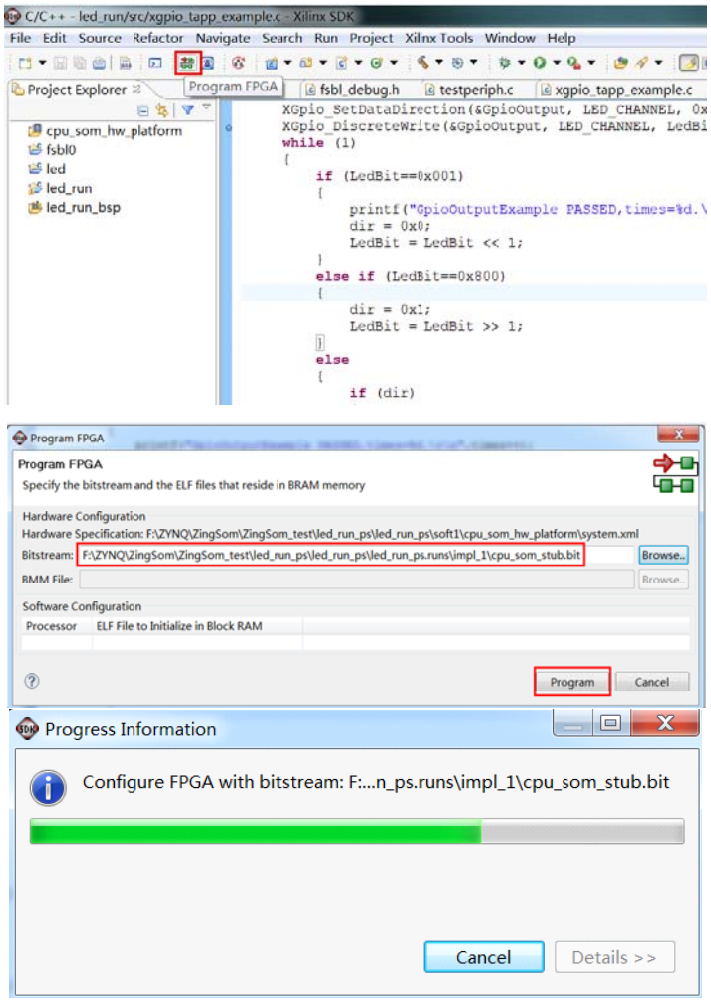


Figure4.4 program bit file

When FPGA config done，FPGA_DONE will be pull high, and DC1 led lighting off。

3 run arm application program

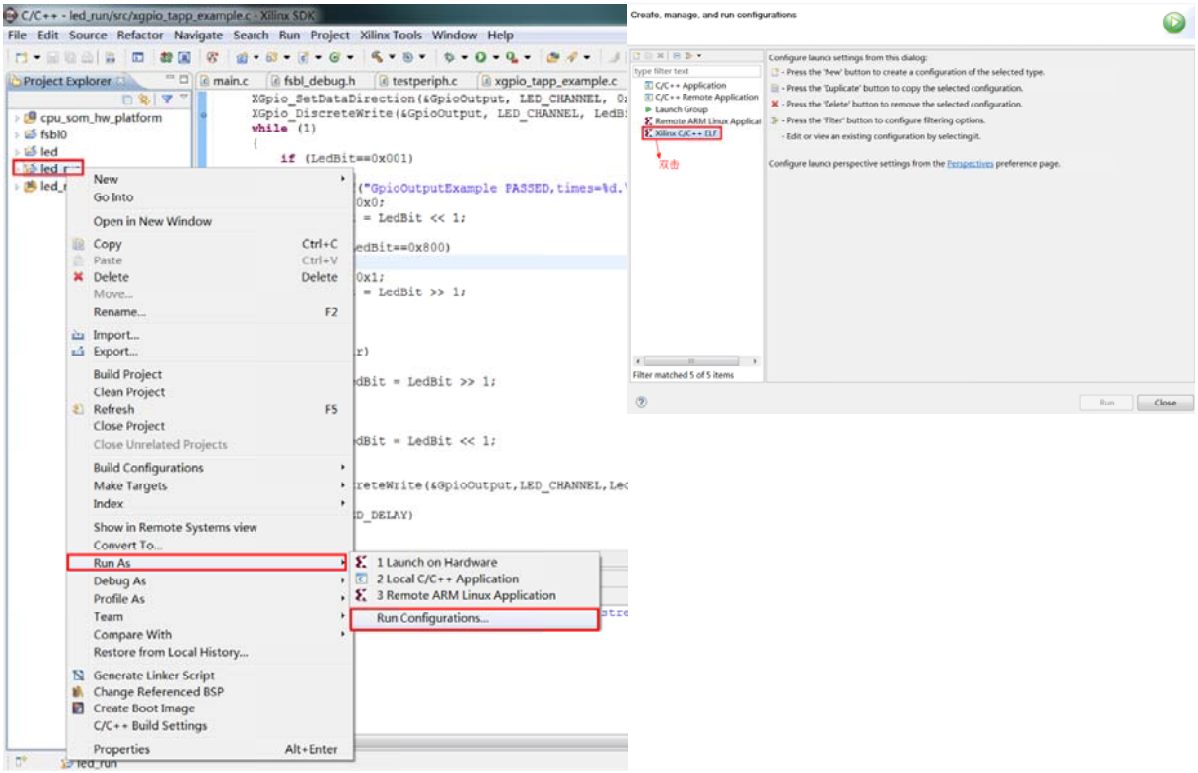
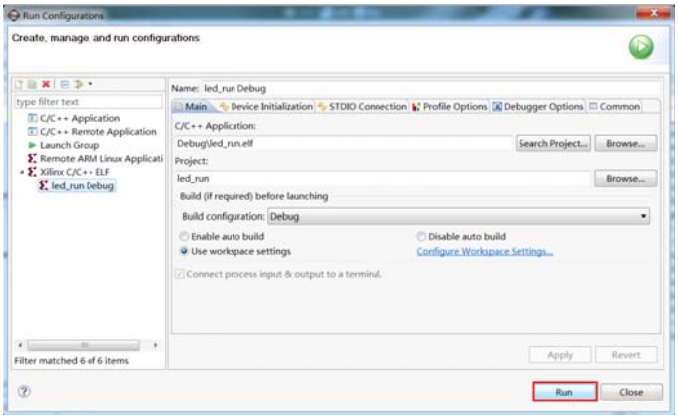


Figure4.5 application program

4 application is running



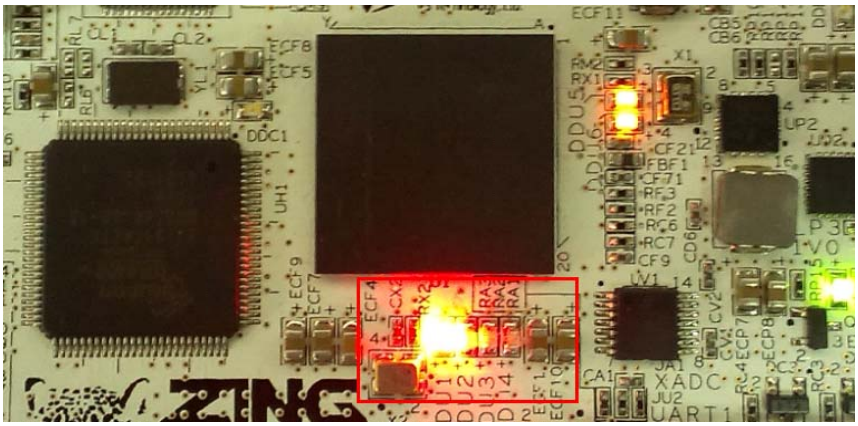


Figure4.6 application is running

4.2 ZYNQ boot mode

ZYNQ supports boot imge from nand flash and TF card, by MIO3~MIO4, two jump.

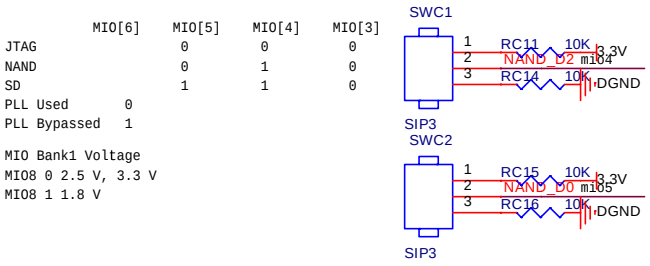


Figure4.7 ZYNQ boot select

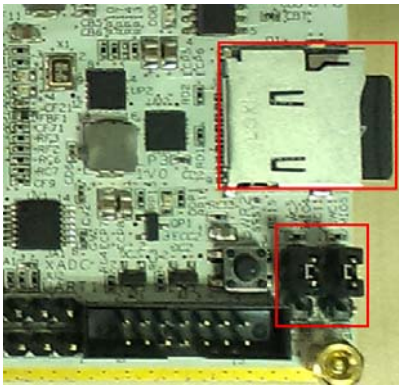


Figure4.8 boot using tf card

4.2.2 program nand flash and boot

1 configure boot jumper and power on board

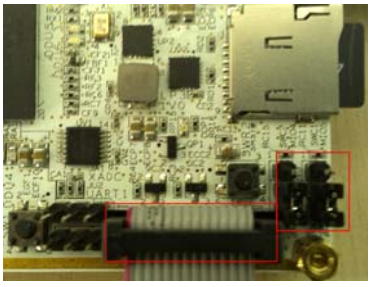


Figure4.9 boot using nand flash

2 select flash type and related files

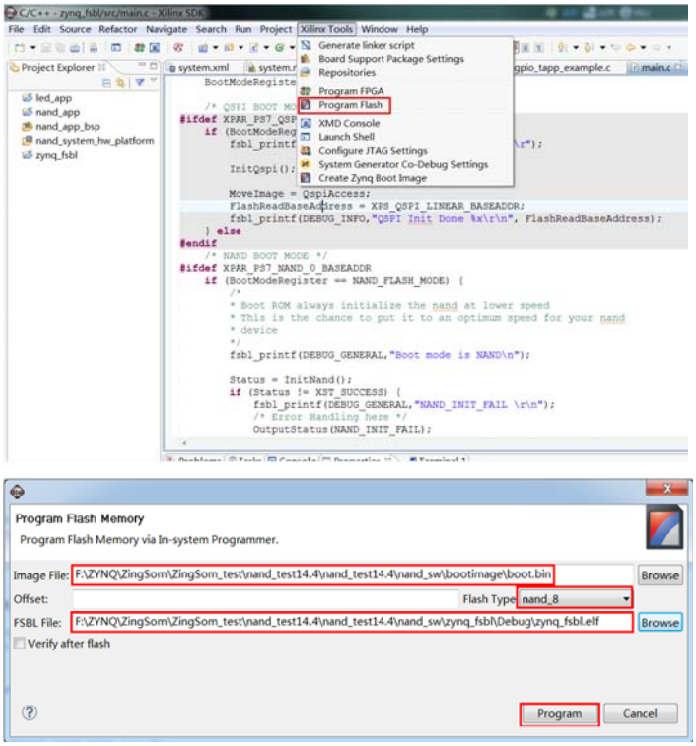


Figure4.10 flash type and related files

3 Process information to print

Figure4.11 Process information to print

4 after program 100% , power off board. Then jump to nand flash boot mode,power on,running!

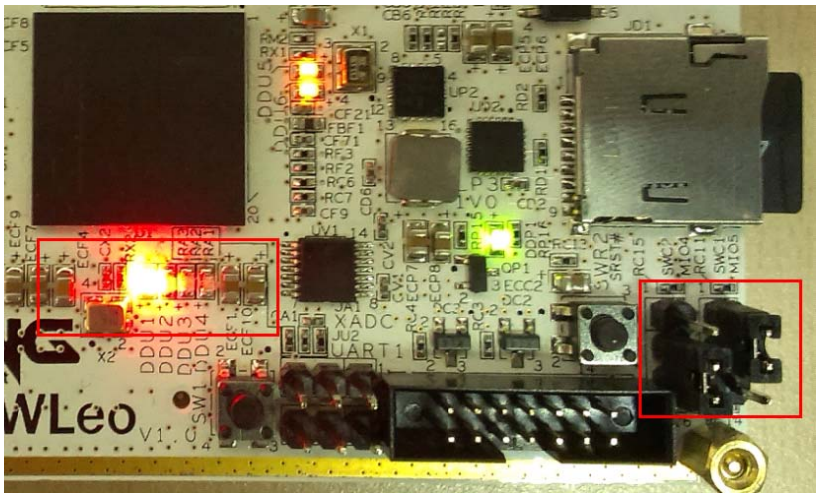


Figure 4.12 nand flash boot running