HPSDR – Ethernet DFC Protocol

Revisions

Rev	Date	Changes	By
1.0	4 Aug 14	First release for Angelia (ANAN-100D) board	VK6PH
1.1	24 Nov 14	Added Discovery option and Hermes version	VK6PH
1.2	17 Jan 15	Reversed order of Bytes so not required at PC	VK6PH

Protocol Overview (V1.2):

This protocol is for experimental purposes. It enables an openHPSDR board e.g. Hermes or ANAN-10/100/200 to send raw ADC samples at 61.44 Msps via raw Ethernet frames to an associated PC or Single Board Computer.

The ADC(s) on the board are clocked at 122.88 MHz. 16 bit samples are fed to a FIFO that is clocked at 61.44 MHz in order to decimate by two. The FIFO output is clocked at 125 MHz and provides 8 bit data for the Ethernet controller.

Hence the Ethernet bit rate is 61.44 x 16 = 983.04 Mbps.

Data is sent to/from the hardware using raw Ethernet frames. This minimizes the packet overhead in order to provide the fastest data rate.

If an Alex board is connected to the hardware then the 30MHz LPF is engaged and no HPFs are selected.

Protocol – From PC to board

Discovery

In order to determine the MAC address of the board the PC sends the following raw Ethernet packet:

<FF:FF:FF:FF:FF:FF> <source MAC> <0xE000> <0x00> <60 bytes of zero>

Where <source MAC> is the MAC address of the associated PC.

The board will respond with

<PC MAC> <Board MAC> <0xE000> <0x00> <60 bytes of zero>

The 'Board MAC' can then be used with subsequent commands.

The following commands are then available:

<board MAC> <source MAC> <0xE000> <n> < 60 bytes of zero>

Where n =

0x00 = stop sending data
0x01 = send ADC0 data
0x03 = send counter data
0x05 = send ADC1 data (Note: only relevant for Angelia and Orion boards)

Alternatively, the data stream can be started using immediately as follows:

<FF:FF:FF:FF:FF:FF> <source MAC> <0xE000> <0x01> <60 bytes of zero> for ADC0

<FF:FF:FF:FF:FF:FF> <source MAC> <0xE000> <0x05> <60 bytes of zero> for ADC1

<FF:FF:FF:FF:FF:FF> <source MAC> <0xE000> <0x03> <60 bytes of zero> for counter data

Protocol – From HPSDR to PC

When the send bit is set the board will send raw Ethernet frames to the MAC address of the associated PC as follows:

<source MAC> <board MAC> <0xEFFF> <payload = 1,500 bytes>

When the source is set to ADC the payload consists of consecutive ADC samples in the form <ADC[7:0], ADC[15:8]>.

When the source is set to counter the payload consists of consecutive counts from a 16 bit counter that increments at the sample rate (61.44Msps) and has the form <count[7:0], count[15:8]>. This function enables the user to determine if packets are being dropped.

Note: The FPGA code does not presently provide a facility to load new versions of code. In which case to load new version of code, or revert to a previous version, Bootloader mode will be required.