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| **Cairo University Faculty of Engineering**  **Electronics & Comm. Dept.** | **Fourth Year 2020 / 2021**  **Electronics ELC401A** |

**CMOS Operational Amplifier Design**

# Design

The purpose of this project is to design and simulate a folded-cascode operational amplifier used as a buffer.

**Use Current Mirror to Generate *I*3**

***V*b1**

***V*DD**

***I3 I3***



***I3 = ½ I1 + I2***

***V*b2**

**Use Optimum**

**Bias Gen.**

***V*in+**

***V*in-**

## *I2*

***Vout***

***V*b3**

## *I2*

**Use Optimum Bias Gen.**

## *I1*

1. **Specifications**

Vout will be connected to Vin- with short circuit in order to act like buffer this feedback loop will create poles which we will determine its stability because we want it -ve feedback not +ve feedback

You are required to design the single-ended single-stage op-amp shown such that:

* + *V*DD = 3.3V (use **HG devices** with thick oxide and thus will not breakdown for high voltage)--done
  + *V*inCM = VDD / 2 (input common-mode voltage)--done
  + *A*DC > 55 dB (DC differential gain)---done=75dB
  + GBW > 100 MHz for a load capacitance of *C*L=2pF---done=141MHz

– Slew Rate > 100 V/𝜇𝑠𝑒𝑐

* + Output Swing > 1.5Vpp (Definition of swing is when the DC-gain drops by 10dB)
  + Input referred thermal noise density < 10𝑛𝑉/√𝐻𝑧 (Ignore 1/f noise)
  + PM > 60o=== done 65degrees
  + Minimize Vb power consumption
* Do not use ideal current sources (assume that you have only one current source of 25μA coming

from VDD). Use biasing circuit to generate I1 and optimum bias for Vb1, Vb2, and Vb3.

* Design all current mirrors to provide close to optimum compliance voltage (to obtain maximum output swing). BUT Adjust *V*DS of any transistor in the current mirror (or current source) to ( *V*eff + 100mV ) in order to improve 𝑟𝑜 of this transistor.

# Simulations

* Simulate the circuit (DC analysis - save operating point, AC analysis)
  + 1.Print all transistor operating point information (DC)
  + 2.Plot the gain and phase versus frequency (AC). Show open-loop gain and PM
  + 3.Plot the common-mode rejection ratio (CMRR)
  + 4.Plot the power supply rejection ratio (PSRR)
* Place the op-amp in a unity feedback (**Buffer**) configuration:
  + 5.Simulate stability using STB analysis(Stability Analysis) and IPROBE
  + 6.Plot STB gain and phase versus frequency (AC) and calculate open-loop gain and PM
  + 7.What is the difference between those results and previous open-loop AC results?
  + 8.Plot the DC-gain versus *V*out (report when DC-gain drops by 10dB to verify specifications)
  + 9.Plot the closed-loop (CL) frequency response. What is ACL and BWCL (comment)?
  + 10.Simulate input-referred noise and tabulate top 4 contributors @10MHz (comment).
  + 11.Simulate the slew rate and verify the specifications.
  + 12.Apply a sine input signal of 1Vpp @10MHz and plot Vout (add proper input DC value). Plot DFT (in dB) and calculate harmonic distortion HD2, HD3, and THD (comment).
  + 13.Plot Vout for a small step input of 100mV (add proper input DC value). Calculate the fractional gain error (FGE) and 1% settling time (compare with hand analysis).

# Assessment

* The total grade of this project is **5 points.**
* You are required to deliver a report that contains:

1. **Schematic diagrams** (snapshots from Cadence showing dimensions and values)
2. **Design procedure** (hand calculations)
3. **Simulation results** (snapshots from Cadence)
4. **Discussion** of your results and conclusions

* Any missing item from the **4 items above will be penalized in the report grading.** Please be aware that ‘bad’ presentation (report document, figures, etc.) of your work is going to affect your grade.
* Report size shouldn’t exceed **15 pages**. A 0.5 point will be deducted for each extra page.