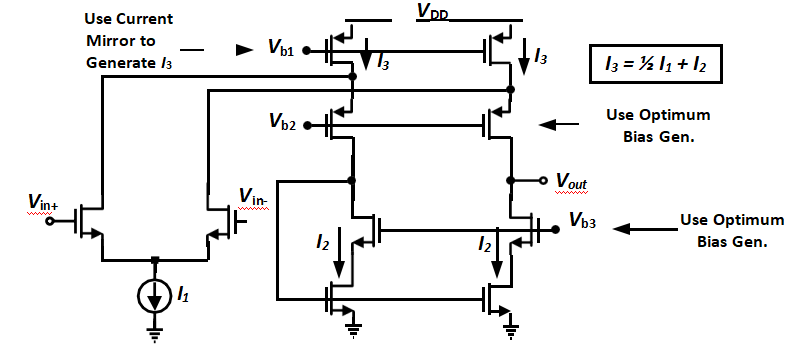
|  |  |
| --- | --- |
| **Cairo University Faculty of Engineering**  **Electronics & Comm. Dept.** | **Fourth Year 2020 / 2021**  **Electronics ELC401A** |

**CMOS Operational Amplifier Design**

# Problem Definition: Folded-Cascode Operational Amplifier for Buffer Use



M10

M9

M8

M7

M6

M5

M3

M4

M2

M1

M0

## 1.1. Specifications🡺Problem Analysis

You are required to design the single-ended single-stage op-amp shown such that:

* + *V*DD = 3.3V🡺🡺Tsmc130nm Nmos3v/Pmos3v of Vth=650mv
  + *V*inCM = VDD / 2 = 1.65 V VDS1 , VDS2 is fixed at a certain value
  + *A*DC > 55 dB (DC differential gain)🡺🡺Vds=Veff+100mV
  + GBW > 100 MHz for a load of 2pF🡺Inv. Prob.🡺 Tunable Range for Bias of I1

– Slew Rate > 100 V/𝜇𝑠𝑒𝑐 🡺🡺Small Signal Analysis

* + Output Swing > 1.5Vpp 🡺🡺 Large Signal Analysis
  + Input referred thermal noise density < 10𝑛𝑉/√𝐻𝑧
  + PM > 60 degrees🡺🡺Inversely Proportional with GBW🡺 Tunable Range for Bias of I1
  + Minimize power consumption🡺🡺Vb Power Consumption

## 1.2. Large Signal Analysis

**Specs & Givens**:

* O/P Swing = 1.5Vpp
* Vth=650 mV
* VDS=Vov+100mV
* VDD=3.3 V

**Solution:**

* Step1: Determine Over drive Voltage
* Step2: Determine Vb1 from overdrive voltage and VDS=Vov+100mV
* Step3: Determine Vb2 from Vb1, overdrive voltage and VDS=Vov+100mV

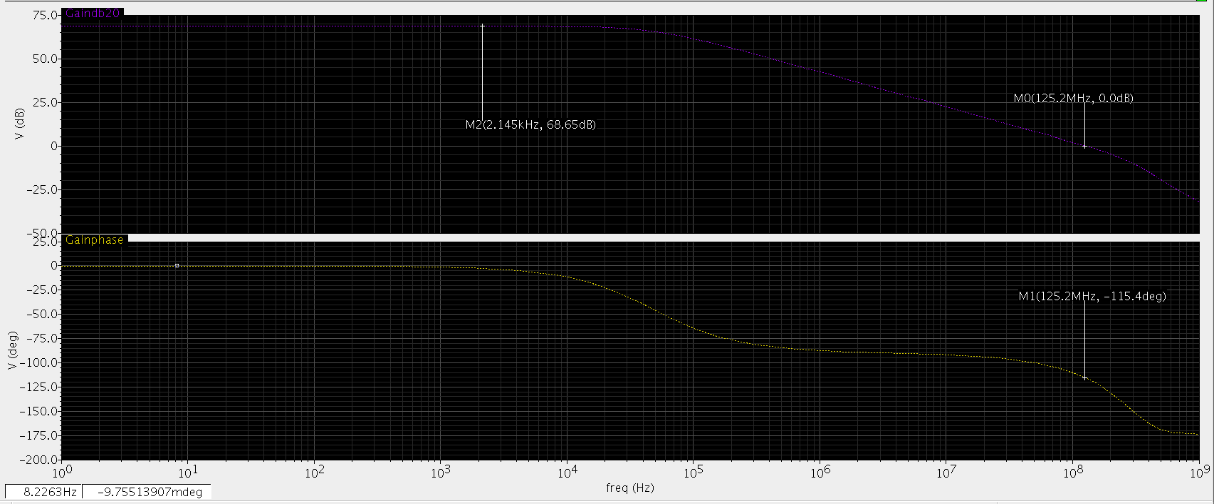
1. **Small Signal Analysis**

# Simulations

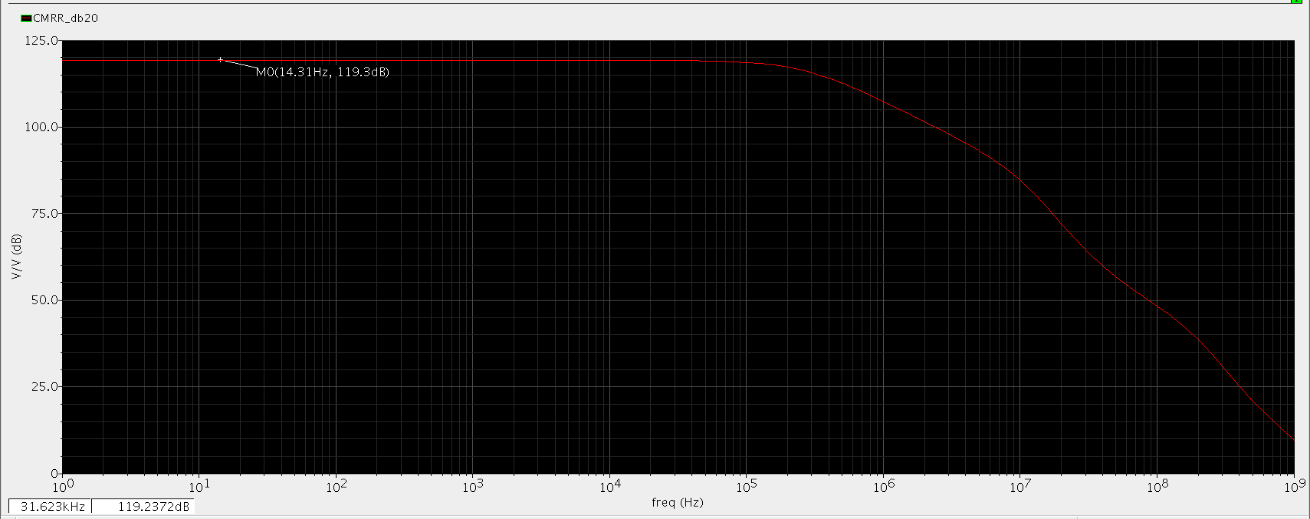
1. Simulate the circuit (DC analysis - save operating point, AC analysis)

1. Print all transistor operating point information (DC)

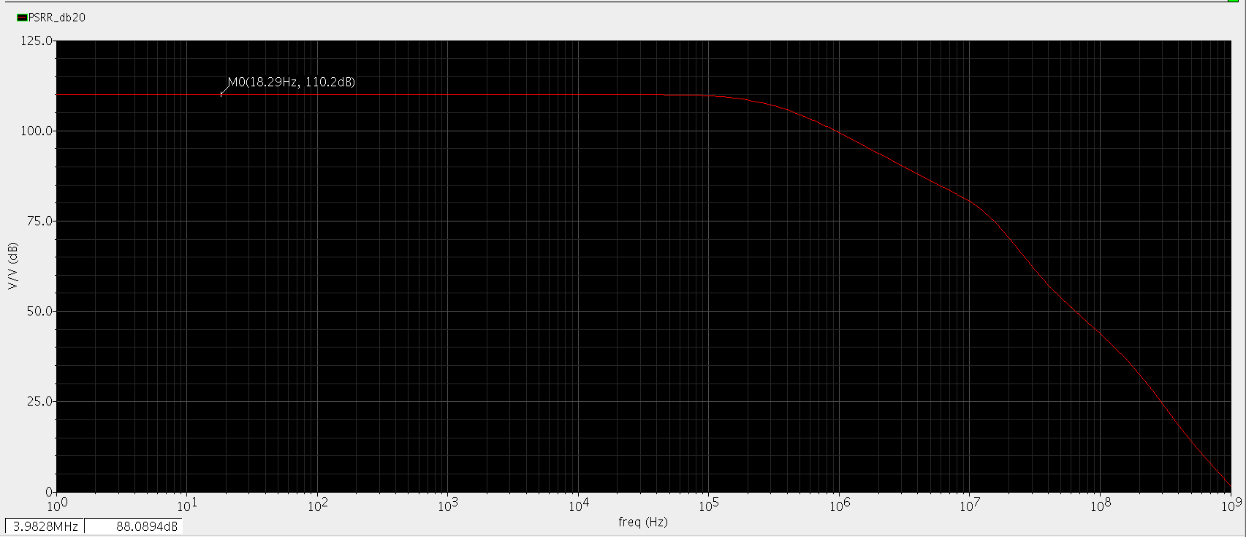
2. Plot the gain and phase versus frequency (AC). Show open-loop gain and PM



3. Plot the common-mode rejection ratio (CMRR)

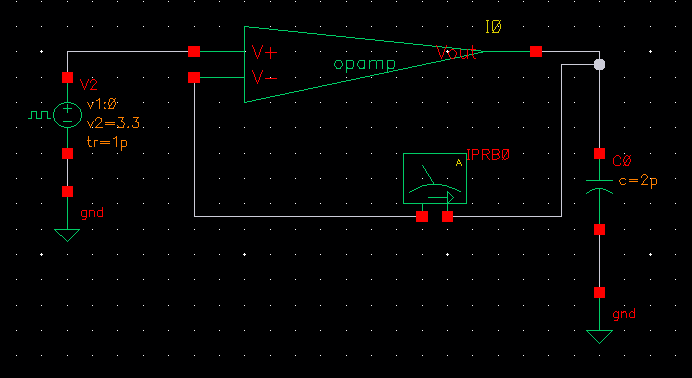


4. Plot the power supply rejection ratio (PSRR)

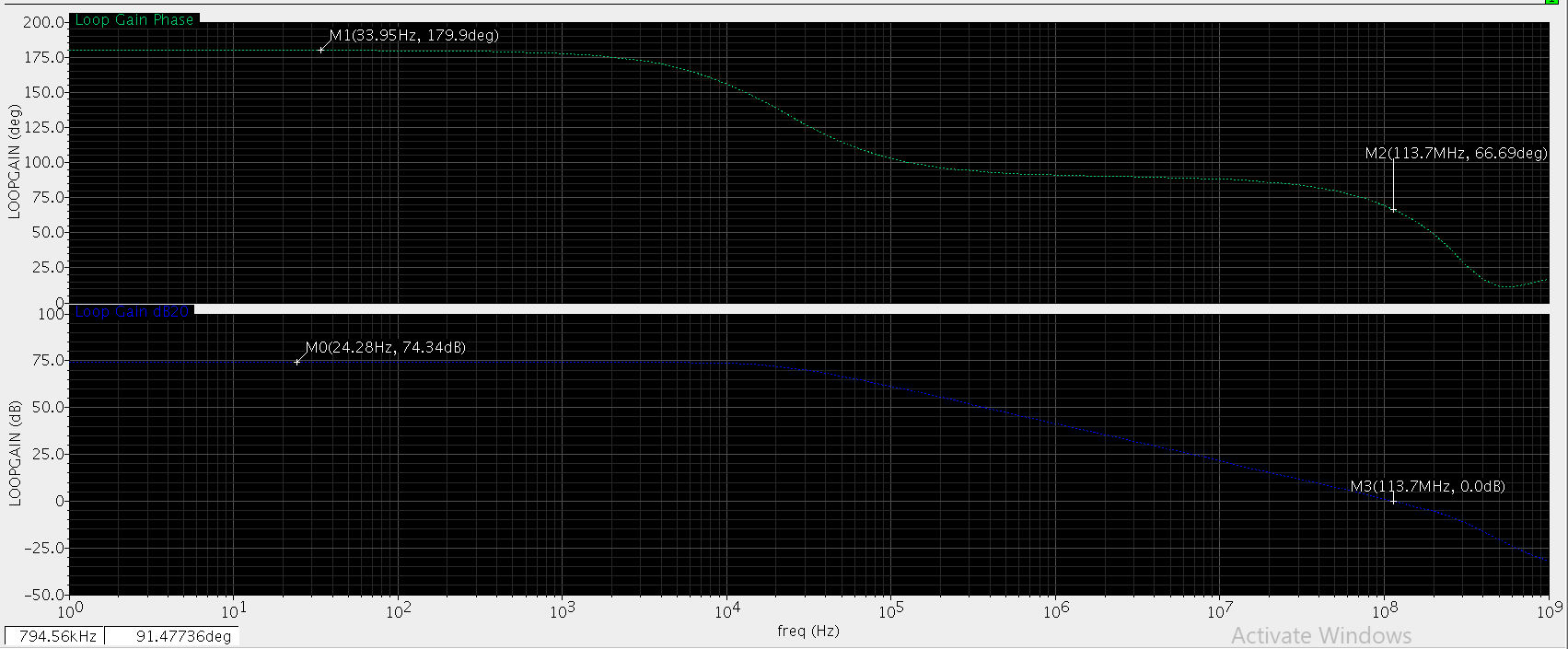


1. Place the op-amp in a unity feedback (**Buffer**) configuration:

5. Simulate stability using STB analysis(Stability Analysis) and IPROBE



6. Plot STB gain and phase versus frequency (AC) and calculate open-loop gain and PM

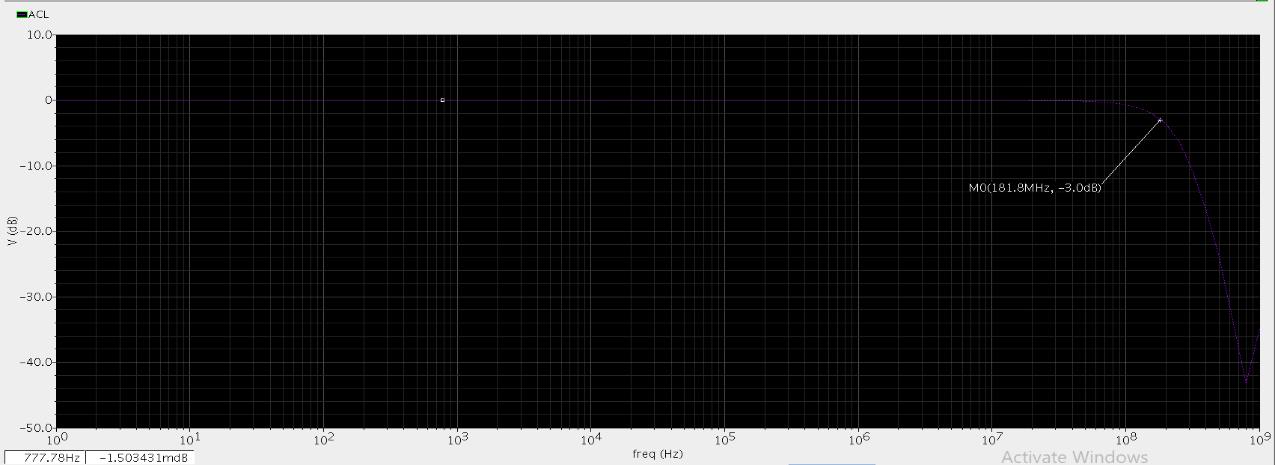


7. What is the difference between those results and previous open-loop AC results?

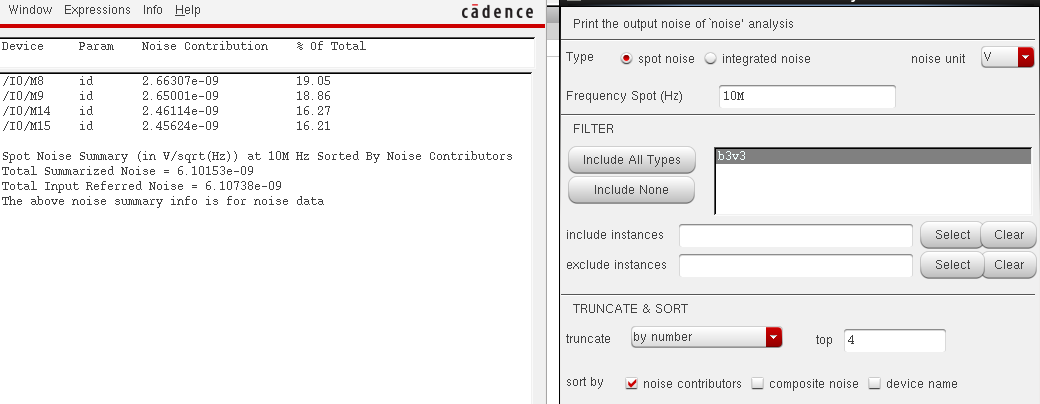
Using Probe sees another capacitance when measuring at input port of the opamp

8. Plot the DC-gain versus *V*out (report when DC-gain drops by 10dB to verify specifications)

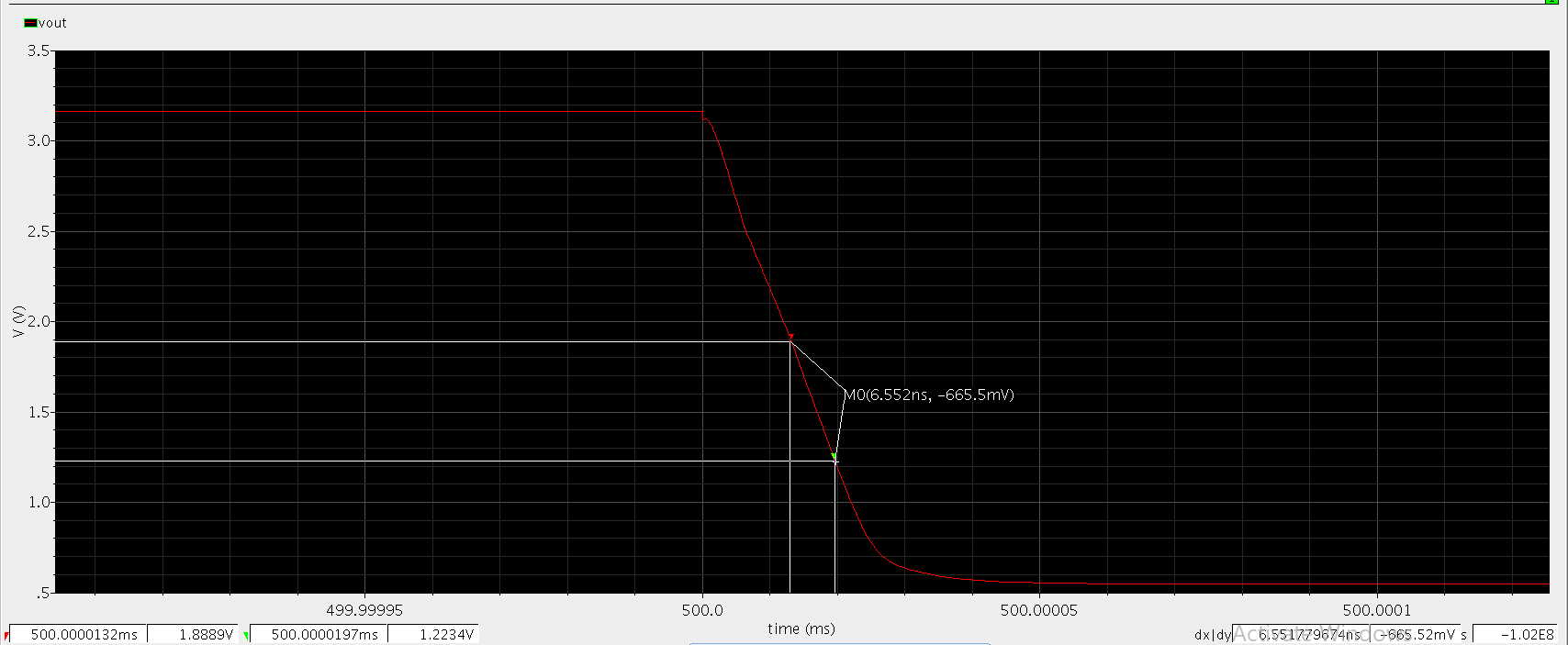
9. Plot the closed-loop (CL) frequency response. What is ACL and BWCL (comment)?



10. Simulate input-referred noise and tabulate top 4 contributors @10MHz (comment).



11. Simulate the slew rate and verify the specifications.



12. Apply a sine input signal of 1Vpp @10MHz and plot Vout (add proper input DC value). Plot DFT (in dB) and calculate harmonic distortion HD2, HD3, and THD (comment).

13.Plot Vout for a small step input of 100mV (add proper input DC value). Calculate the fractional gain error (FGE) and 1% settling time (compare with hand analysis).