Cairo University
Faculty of Engineering
Electronics & Comm. Dept.

جامعة القاهرة

Fourth Year
2020 / 2021
Electronics Project
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Phase Locked Loop (PLL)

I. Theoretical:

a) What is the application of Clock and Data Recovery (CDR) circuit? Describe briefly how to use a PLL in CDR applications.
b) Describe briefly how to use a PLL in modulation/demodulation applications.
c) Describe briefly the operation of a Delay Locked Loop (DLL) and mention the advantages & disadvantages compared to a PLL.
d) Show the schematic of a dual-modulus (2/3) divider. **Hint:** This is composed of a divide-by-2 and a divide-by-3 circuits. Simulate the divider in both modes using ideal logic (using Cadence).
e) What is an all-digital PLL (ADPLL)? Show the block diagram and the main building blocks.

II. Simulations

The purpose of this part is to simulate the (linear) PLL circuit in Simulink environment. As discussed in the lecture, the PLL is widely employed in communication and electronic application as it has many functions. In this project, you are going to simulate the PLL as a circuit that performs synchronization between two signals that have different phase and frequency.
Figure 1 shows a typical PLL circuit. It has three components: a phase detector, a loop filter and a voltage-controlled oscillator.

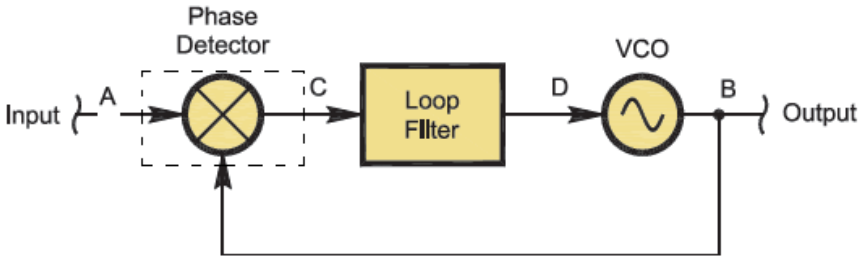

Figure 1: Typical PLL circuit

You are required to simulate the linear PLL using the Simulink model **provided** by MATLAB Central on MathWorks website. The block diagram for the PLL circuit is given in Figure 2.

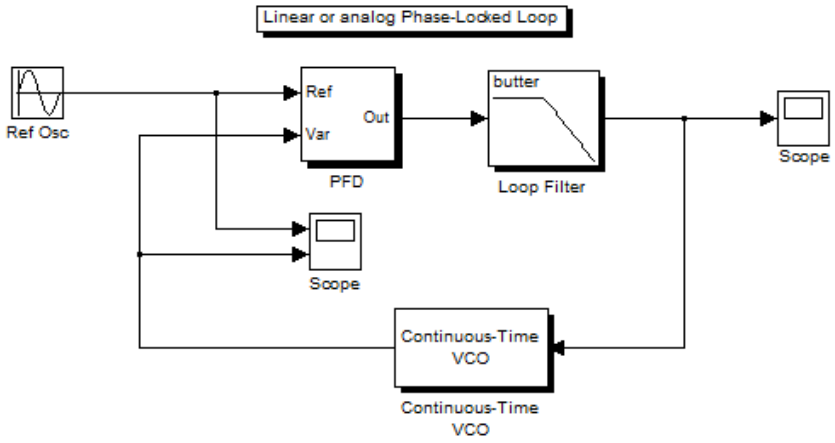

Figure 2: Linear PLL model

Although you will be given the model in Figure 2 as it is (so you do not need to build this model from scratch), it is better that you learn a little bit about Simulink if this is the first time you work with it. You may browse the internet for many tutorials. For instance, the following sites provide good starting point:
http://faculty.washington.edu/lum/website_professional/matlab/tutorials/Simulink_Tutorial/simulink_tutoritu.pdf
http://www.isa.uma.es/C14/Documentos/Document%20Library/semin_simulink.pdf

The model in Figure 2 has three main components:

- The phase frequency detector (*PFD*).
- The loop filter (*LF*)
- The voltage controlled oscillator (*VCO*)

These are the main components that we are going to test.

The other blocks are as follows:

- *The oscillator*: the signal generator that generates the sinusoid signal we want to synchronize with
- *The scope*: a visualization block that displays the signal with time

You are required to do the following:

1. Get the linear model and open it with Simulink to identify each block and its function.
2. What is the type of this PLL?
3. In your report, briefly discuss the function of the three main components of this circuit based on what you understand from the provided documents.
4. Test the circuit for the following setup:
   - The input is a sinusoid with frequency equal to 10^6Hz and zero initial phase
   - The VCO has a free running frequency of 10^6Hz and gain K_{VCO} of 10^5Hz/Volt
   - The low pass filter has a pass-band edge frequency 10^6Hz, order 7, and Butterworth type

   Plot the curves of the two scopes, i.e. copy these curves in your report with appropriate titles and labels.
5. Repeat part (4) with the following setup change:
   - The input is a sinusoid with frequency equal to 10^6Hz and $\pi/3$ initial phase
6. Repeat part (4) with the following setup change:
   - The input is a sinusoid with frequency equal to 10^6Hz and $\pi/5$ initial phase

Note: what you are doing in parts (4-6) is testing the PLL function for different phase inputs.
Comment on the plots of parts (4-6). What is the behavior of the filter output and what is its steady state value? How does this steady state value affect the VCO? What is the value of the phase difference between the input and the VCO? Is this phase difference changing? Explain why.

7. Test the circuit for the following setup:
   - The input is a sinusoid with frequency equal to $(10^6 + 10^4)$Hz and 0 initial phase
   - The VCO has a free running frequency of 10^6Hz and gain K_{VCO} of 10^5Hz/Volt
   - The low pass filter has a pass-band edge frequency 10^6Hz, order 7, and Butterworth type

   Plot the curves of the two scopes, i.e. copy these curves in your report with appropriate titles and labels.
8. Repeat part (7) with the following setup change:
   - The input is a sinusoid with frequency equal to $(10^6 - 10^4)$Hz and 0 initial phase
9. Repeat part (7) with the following setup change:
   - The VCO has a free running frequency of 10^6Hz and gain K_{VCO} of $2x10^5$Hz/Volt

Comment on the plots of parts (7-9). What is the behavior of the filter output and what is its steady state value? How does this steady state value affect the VCO? What is the value of the phase difference between the input and the VCO? What is the effect of increasing K_{VCO}? Explain why.
Note: what you are doing in parts (7-9) is testing the PLL function for different frequency inputs.

10. Repeat part (7) with the following setup change:
    - The low pass filter has a pass-band edge frequency 10^5Hz, order 7, and Butterworth type

Comment on the plots of part (10). What is the behavior of the filter output and what is the time it takes to reach steady state value compared to that in part (7)? Explain why.

11. Repeat part (7) with the following setup change:
    - The input is a sinusoid with frequency equal to $(10^6 + 10^5)$Hz and 0 initial phase

Comment on the plot of part (11). There is a big difference in the behavior of the PLL when using this setup compared to what you should have observed in parts (7-10). Can you think of the reason (you may refer to the documents mentioned in the introduction section)?

III. Project Assessment

- The total grade of the project is **5 points.**
- The project can be done by group of 4 students (or less).
- To assess your project, the defined steps required in part I and II are required to be clearly shown in your final delivery. Please make sure to *stick* with these steps. Any missing item will be penalized in the report grading.

1- The figures that you are going to show must be well presented. They must have clear labels, titles, and maybe legends.
2- Enumerate your answers appropriately.
3- Please make a soft copy of your Simulink model ready.

Please be aware that 'bad' presentation (report document, figures, etc.) of your work is going to affect your grade.

- Report size shouldn't exceed 15 pages. A 0.5 point will be deducted for each extra page.
- Deadline to submit the project report is **Jan. 9th, 2021.**
- Please submit the report to elc401f2020@gmail.com with the subject "PLL_Project".
- Any copied reports or groups more than 4 will be given Zero.