Faculty of Engineering

Cairo University

1 : 16 Wilkinson Power divider (2 x 8 grid)

Course[ELC 305A]

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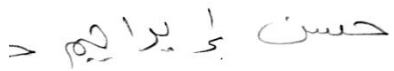

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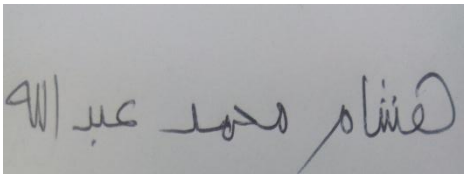

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1 . Introduction

Power combiners and dividers are very important components in a microwave circuit . If we want to obtain powers that are of equal phase and amplitude at the ports , we often use Wilkinson Power divider (WPD) . It's widely used because it is simple , provides high isolation for all ports and low insertion loss among output ports of the microwave circuit .

Wilkinson Power dividers (WPD's) are often used as feeders in power amplifier networks , antenna arrays due to their advantage of high isolation between output ports which reduces crosstalk among them . A 1 : 2 WPD works as a divider if we inject power from the input port (port (1)) and as a combiner if we inject powers from ports (2,3) and receive them from 4 . Although it's a lossy three – port network , it appears lossless when the output ports are matched; that is, only reflected power from the output ports is dissipated. All of this advantages encouraged us to use the Wilkinson Power divider (WPD) as the unit of our 1 : 16 power divider .

In this report , we present a simple design for a 16 – way equal power divider that is used to feed an antenna array . The layout was intended to be as compact as possible as we want this circuit to operate at a center frequency that is equal to 4 GHz.

2. Problem Description and Solution Approach :

2.1.Problem description

Designing a circuit that can be a feeder to multiple ports that are close to each other is one of the biggest challenges nowadays . This is due to the trade – offs between increasing number of ports and the crosstalk between them . This challenges us to provide very high output isolation in our circuit to avoid this type of crosstalk and to ensure that each port (which may be fed to an antenna or a power amplifier) will receive the intended amount of power and meets the design specifications .

Other challenges can be summarized in these points :

1) Size issues that causes much headache for larger number of ports .
2) Broadening bandwidth of the circuit so that we still have the same features for a larger fractional bandwidth .
3) Suppressing harmonics that distorts the original signal .
4) Decreasing transmission losses which is still the most critical problems and the bottle neck of most of the designs .
5) Design of a compact power divider for un-equal power division is one of the biggest challenges that RF designer seek solutions for nowadays [1] . However we don't consider this problem because our divider's function is a 16 – way equal power division .

In our specific case , We want to design a 16 – way power divider in the form of a (2x8 Grid) . These elements are half – wave length apart at center frequency 4 GHz . The following table summarizes the specifications of our design :

Table 1 : Specifications of the 16-way Wilkinson

Specification	Required
Center Frequency	4 GHz
Fractional Bandwidth	10 %
Input / Output return loss	>12 dB
Excess Insertion loss	As low as possible
Output Isolation	>30 dB
Phase and magnitude response	Balanced

2.2. Solution Approach

As discussed before , we used Wilkinson power divider for its simple design , high output isolation , high return loss and the ability to be scaled easily. A 1 : 2 WPD is shown in figure 1 . For N-way power dividers , we have many configurations . Two of which are the tree and the chain . For the tree configuration , we can cascade WPD's as levels . Each level has a total WPD's of (2^L) where L is the level index (0, 1 , 2 ...etc) . So , it resembles the binary formula and mainly used for N-way power dividers ,where N is a multiple of 2 . This configuration as shown in figure 2 .

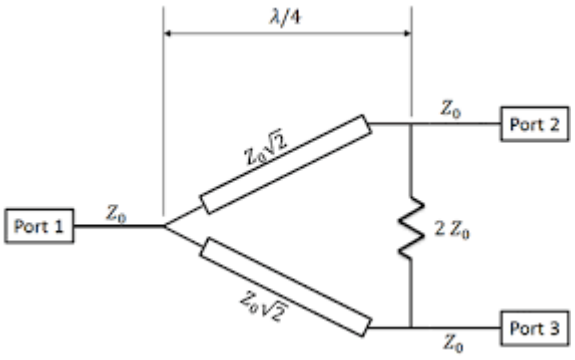

Figure 1 : a 1 : 2 Wilkinson Power Divider

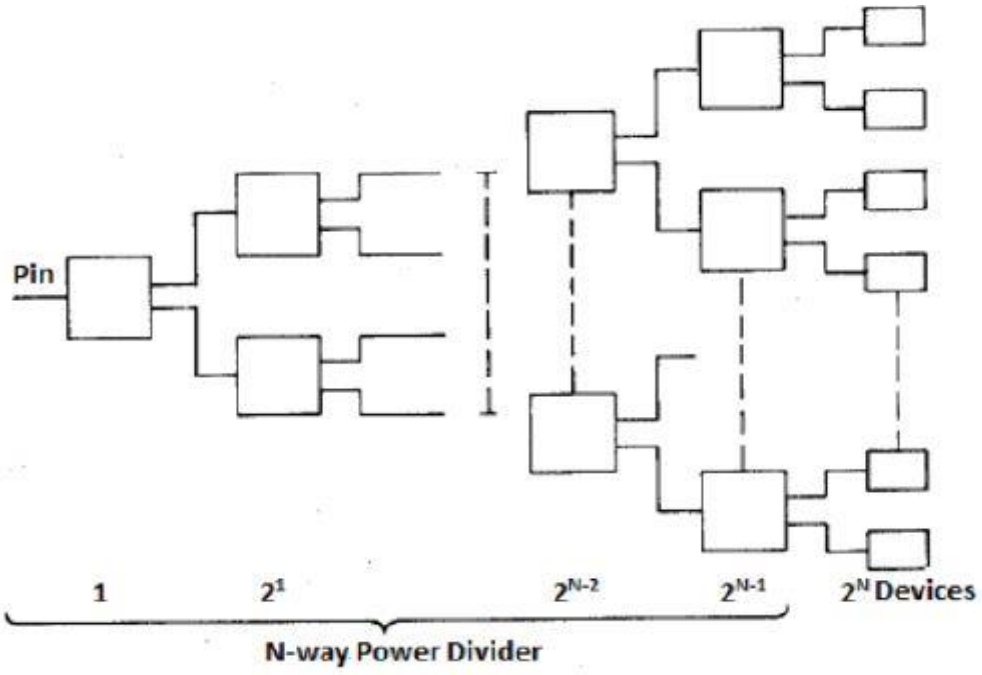

Figure 2 : N-way power divider using Tree approach

The design parameters of this circuit are easy to manipulate . If the ratio between the two output ports of a 1 : 2 WPD is K (P2/P3 = K) , the following equations summarizes the design parameters :

$$K = \frac{P_3}{P_2}$$

$$Z_{03} = Z_0 \sqrt{\frac{1 + K^2}{K^3}}$$

$$Z_{02} = Z_{03} K^2$$

For equal power division , We put K = 1 which yields the results for the 1:2 WPD shown in figure 1 .

Another unpopular configuration , is the chain configuration shown in figure 3 but it's not good for a 2 x 8 Grid .

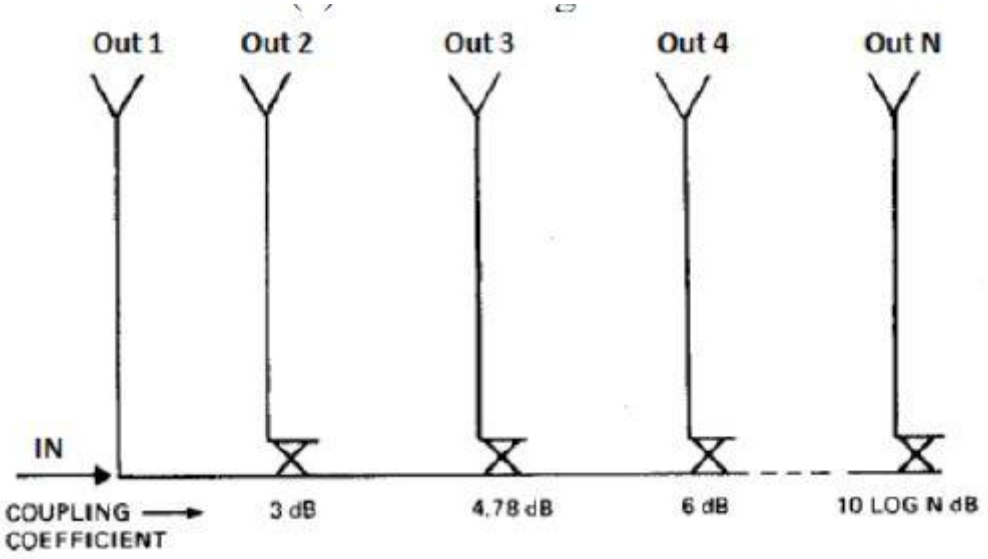

Figure 3 : Power divider using chain configuration

2.3.Design Methodology and tools used

Our goal is to design a 1 : 16 WPD that is arranged in a 2x8 Grid that may be used to feed an antenna Array . We used ADS tools for the schematics , layout and EM simulation . The steps of the design from the very beginning till the layout are as follows :

1) We started by simulating a 1 : 16 Wilkinson power divider using ideal Circuit elements (TLIN in the schematic view of ADS) and of course it met all the specs.
2) We then simulated the same circuit after implementing it using printed lines (MLIN in the schematic view of ADS). We used the substrate material (Rogers3003) with the following parameters (Thickness = 60 mil , Dielectric constant = 3 , tand = 0.001)
3)We then implemented the 1 : 2 WPD with the configuration in figure 4 . This will be the unit of our full design . In the next sections a detailed description will be given about each step .

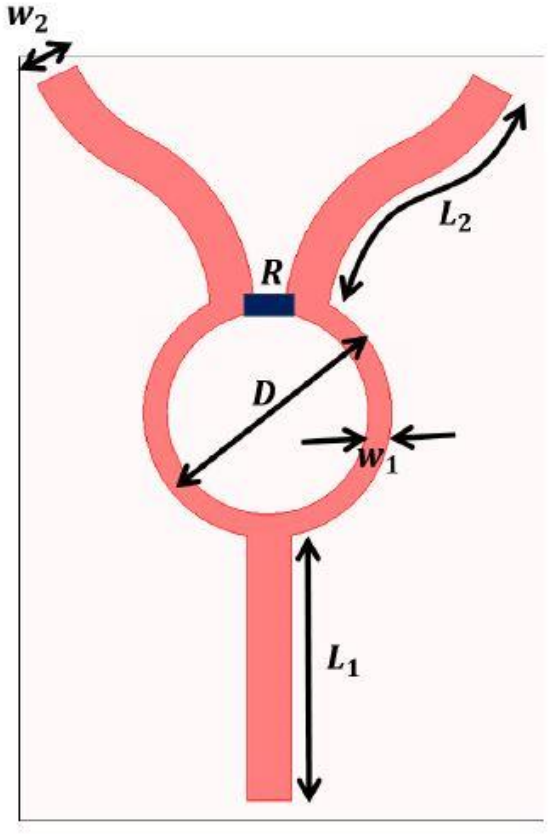

Figure 4 : Layout of a 1 : 2 Wilkinson power divider

3.Results and Figures

3 . 1. Schematics of ideal circuit elements implementation (TLIN):

In this section we used ideal transmission lines (TLIN) to simulate the ideal case where we don't take losses and discontinuities into consideration . In figure 5 ,we show the schematics of the ideal TLIN . It's composed of a quarter wave and half wave ideal sections as well as an ideal 100-ohm resistor .

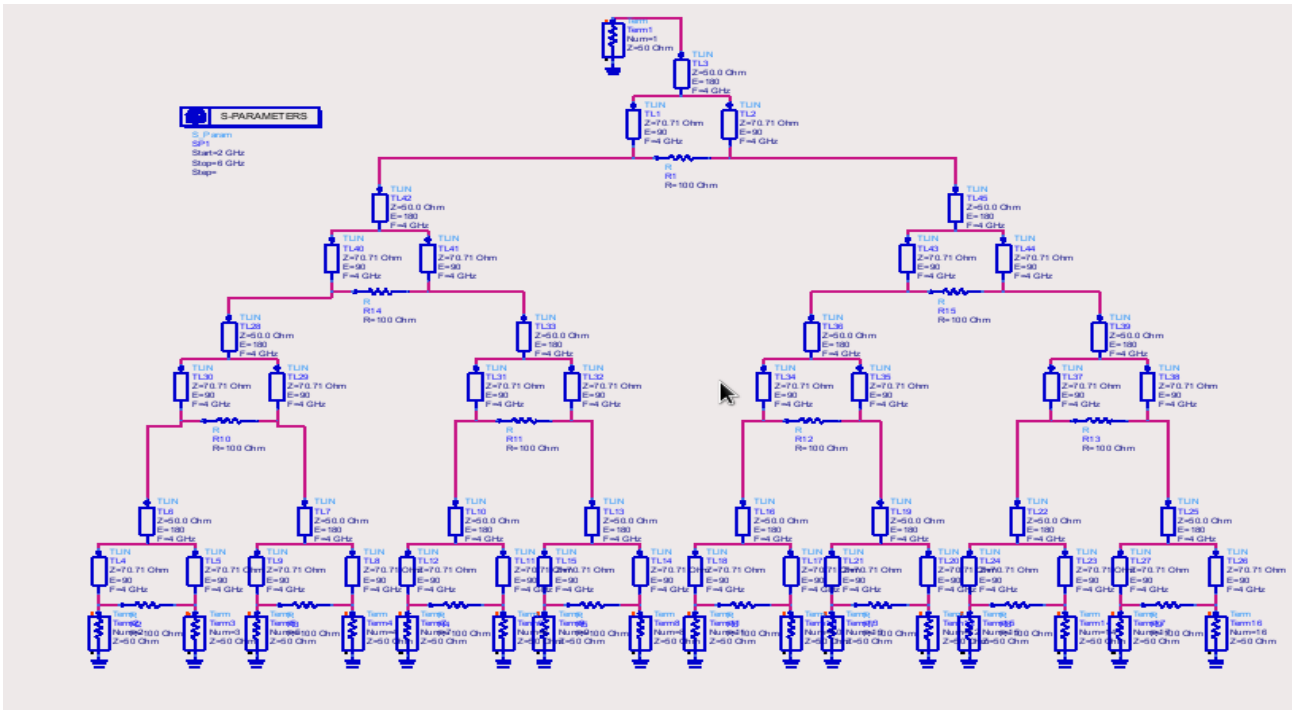

Figure 5 : Schematics of Ideal TLIN

3. 2 . Figures and charts of ideal circuit elements implementation (TLIN) :

In this section , we show the graphs of the following parameters :

1 . Input return loss :
It's shown in figure 6 that it's below than -100 dB .
2 . Output return loss :
It's shown in figure 7 that it's below than -120 dB .
3. Output isolation :
It's shown in figure 8 that it ranges from -40 : -60 dB for different ports.

4. Insertion loss : It's shown in figure 9 that it's about -12.05 dB with almost zero excess insertion loss. We also notice that we satisfy bandwidth.

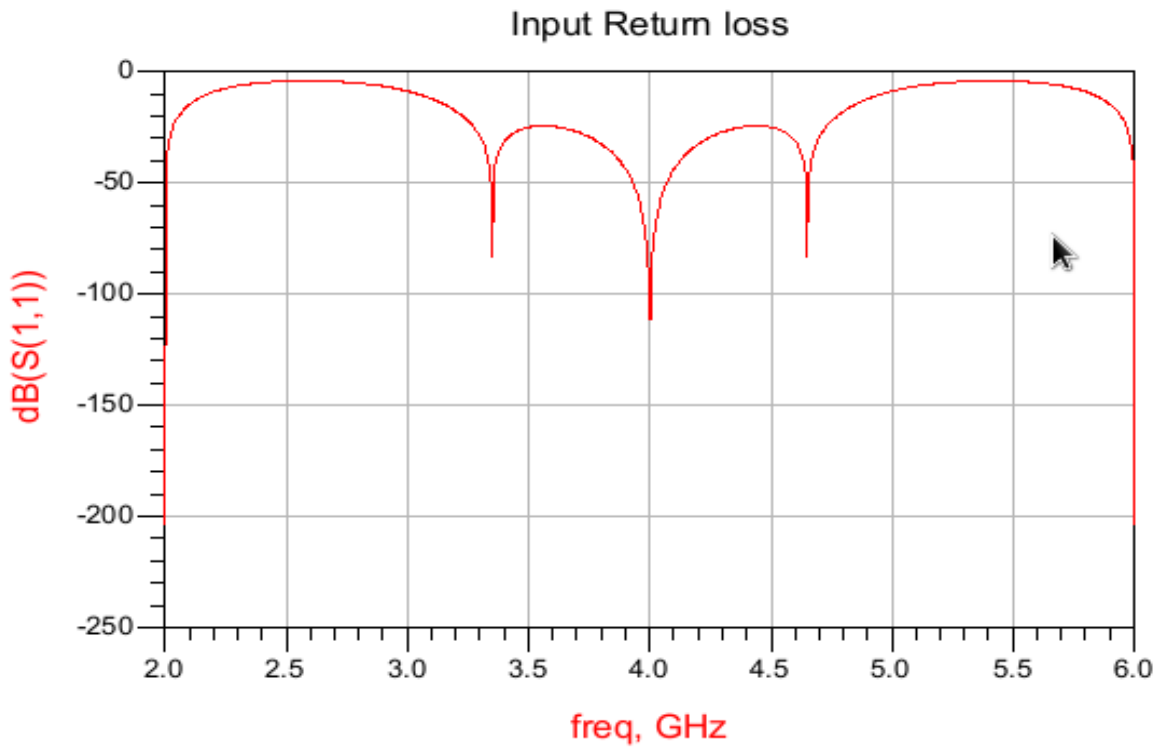

Figure 6 : Input return loss (about 100 dB)

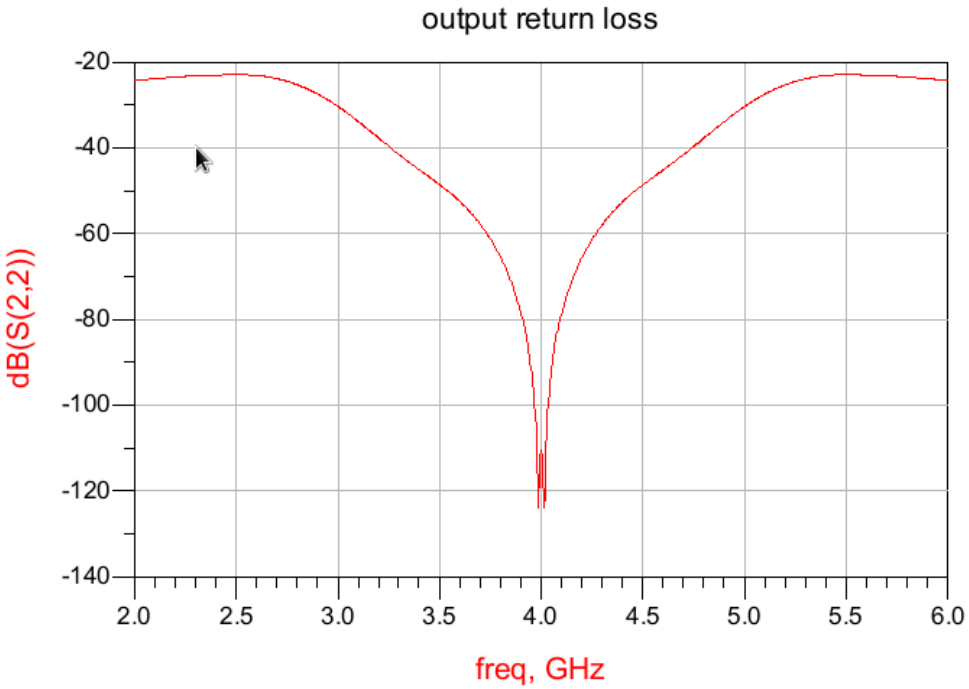

Figure 7 : Output return loss

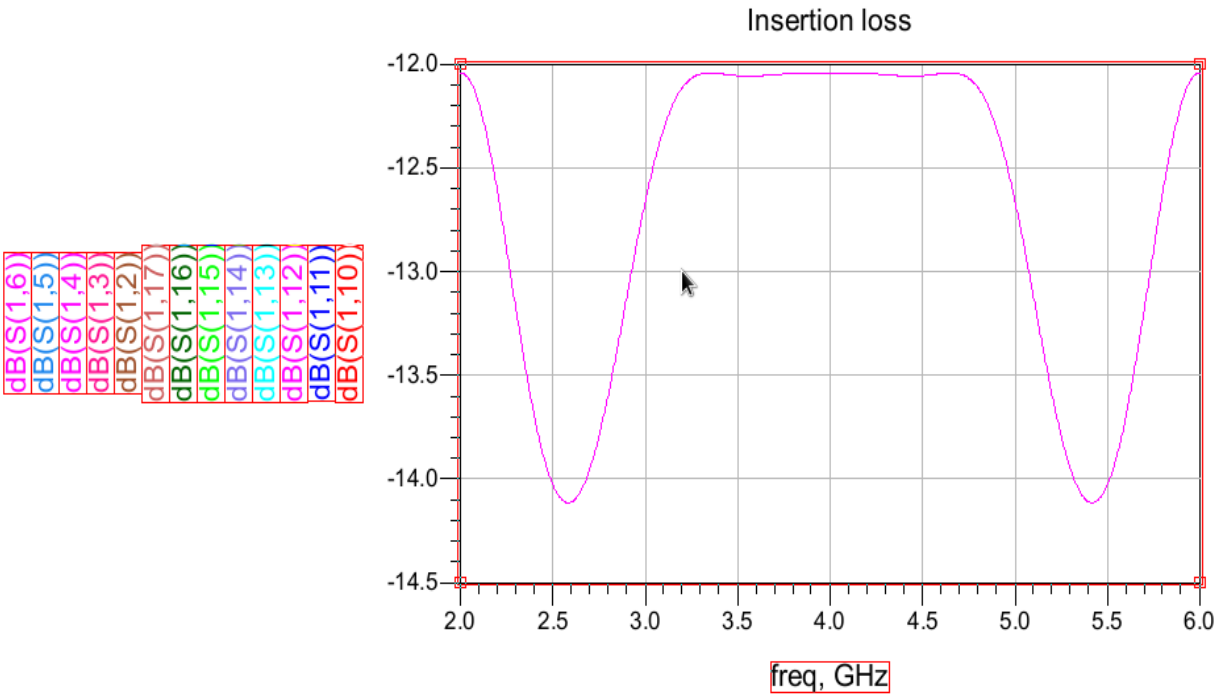

Figure 8 : Insertion loss

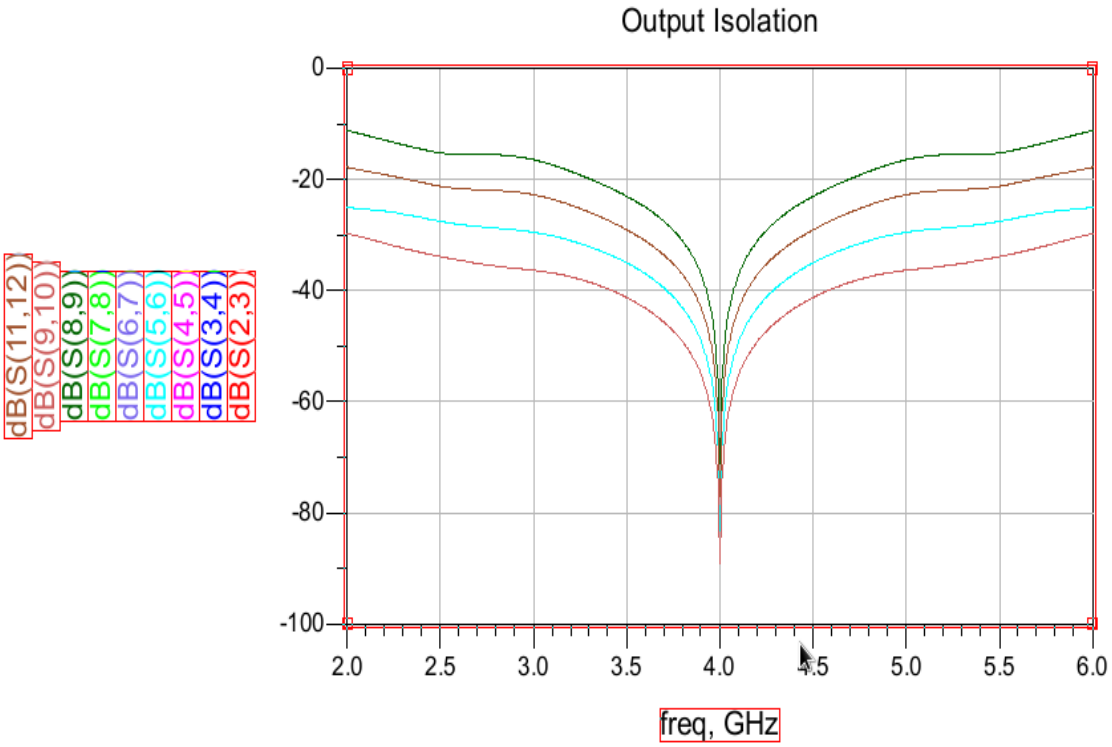

Figure 9 : Output Isolation

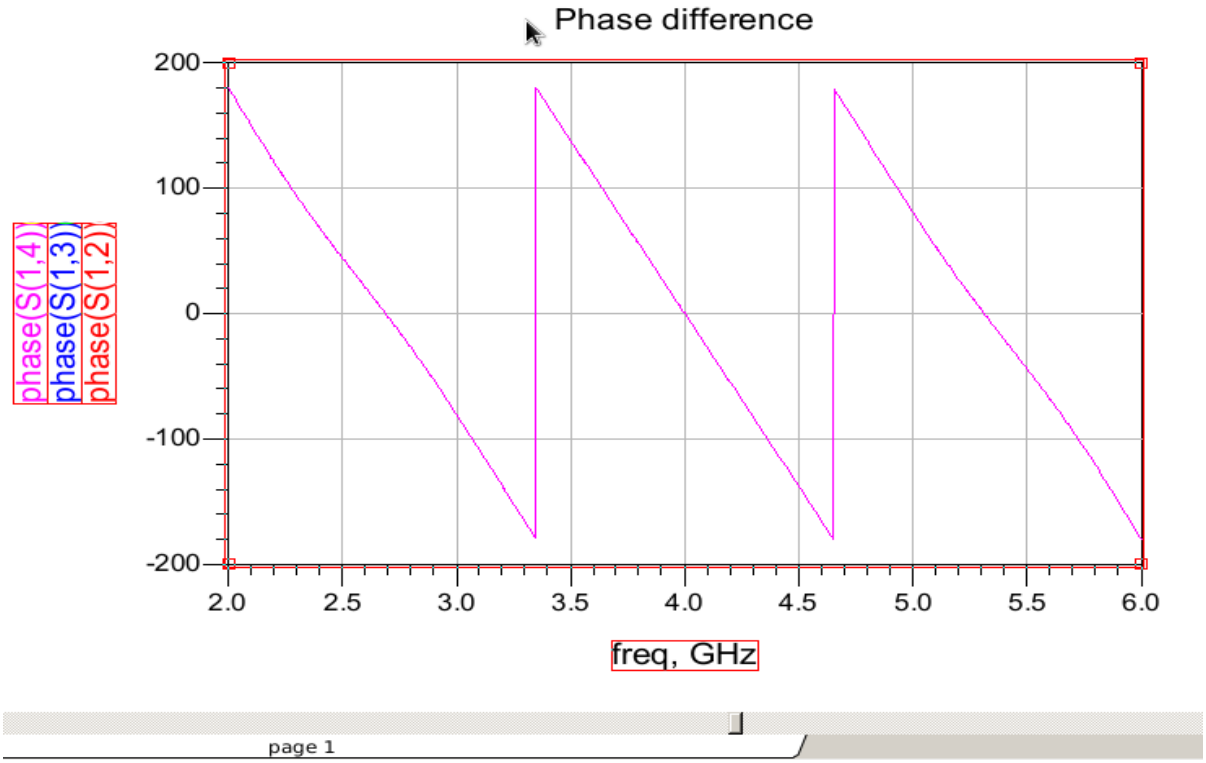

Figure 10 : Phase difference between outputs (ports 2 , 3,4)

Comment :

It's clear from all figures that we satisfy the 10 % fractional bandwidth .
We also notice that outputs are in phase with almost 0 phase difference .

3.3 . Schematics based on Printed lines implementation and their calculations

- We used the substrate 3003 (Rogers Material) for its high performance in RF frequencies (It has a low Er and of a low loss tangent) . In Table 2 , we list the values of lengths and widths of microstrip printed lines and their other parameters . These values are calculated using ADS LineCalculator . For the Half –wave length section , we used the element "MLIN" shown in figure 13 . For the Quarter – wave length section , we used the element "MCURVE2" with angle = 90 deg and parameters listed in table2 as show in figure 11 . Figure 13 presents parameters in LineCalc of the Quarter-wave .

Table 2 : Parameters of the non-ideal Wilkinson power divider

Parameter	Values
Effective Permittivity	3
Tan d	0.001
Thickness	60 mils
Length of half-wave Section	23.89 mm
Width of half –wave section	3.826 mm
Length of quarter-wave section	11.945
Width of half –wave section	2.11 mm
Resistance	100 ohms

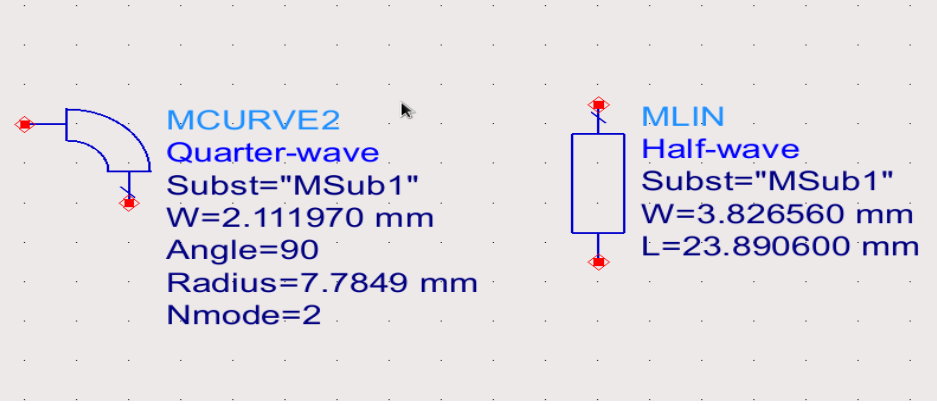

Figure 11 : Half-wave and quarter wave sections of a non-ideal microstrip line

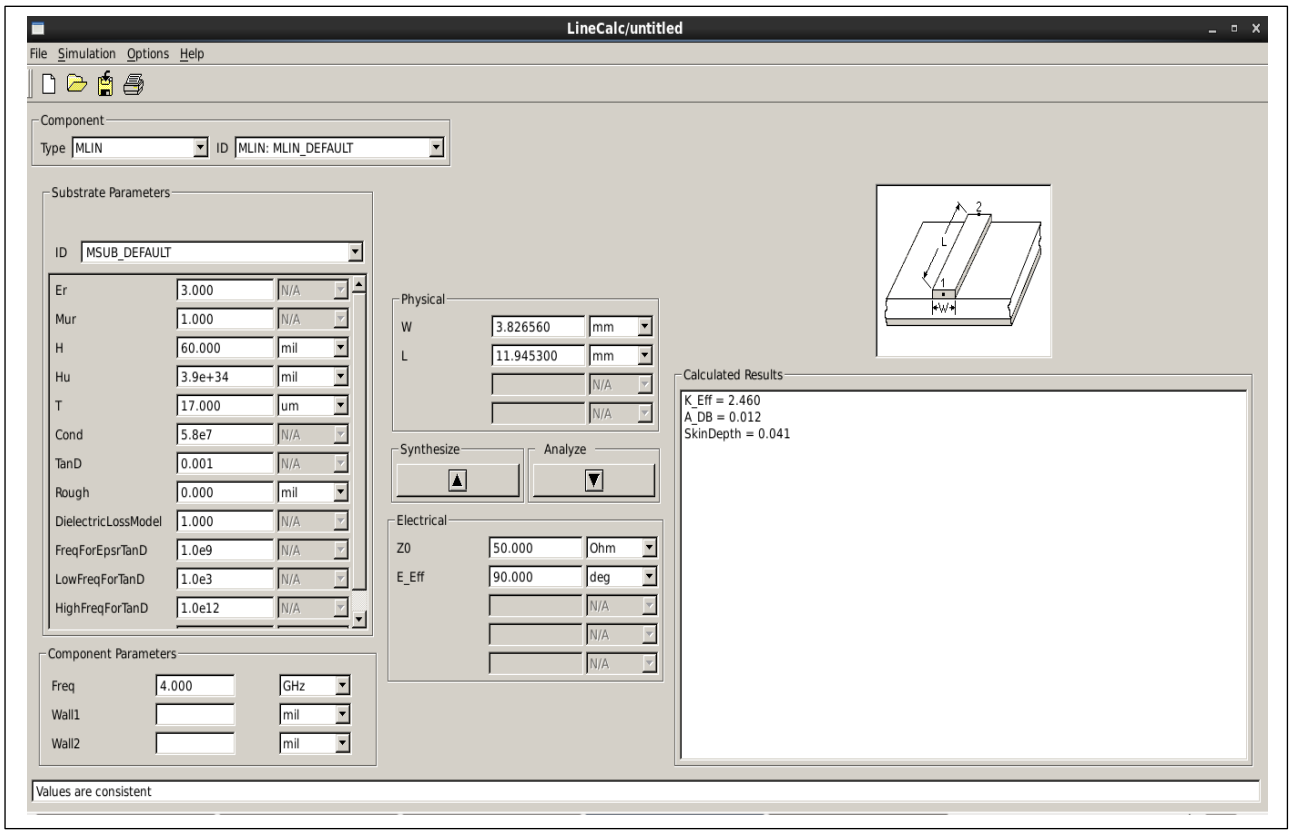

Figure 12 : Microstrip substrate characteristics at center frequency 4Ghz for QW section

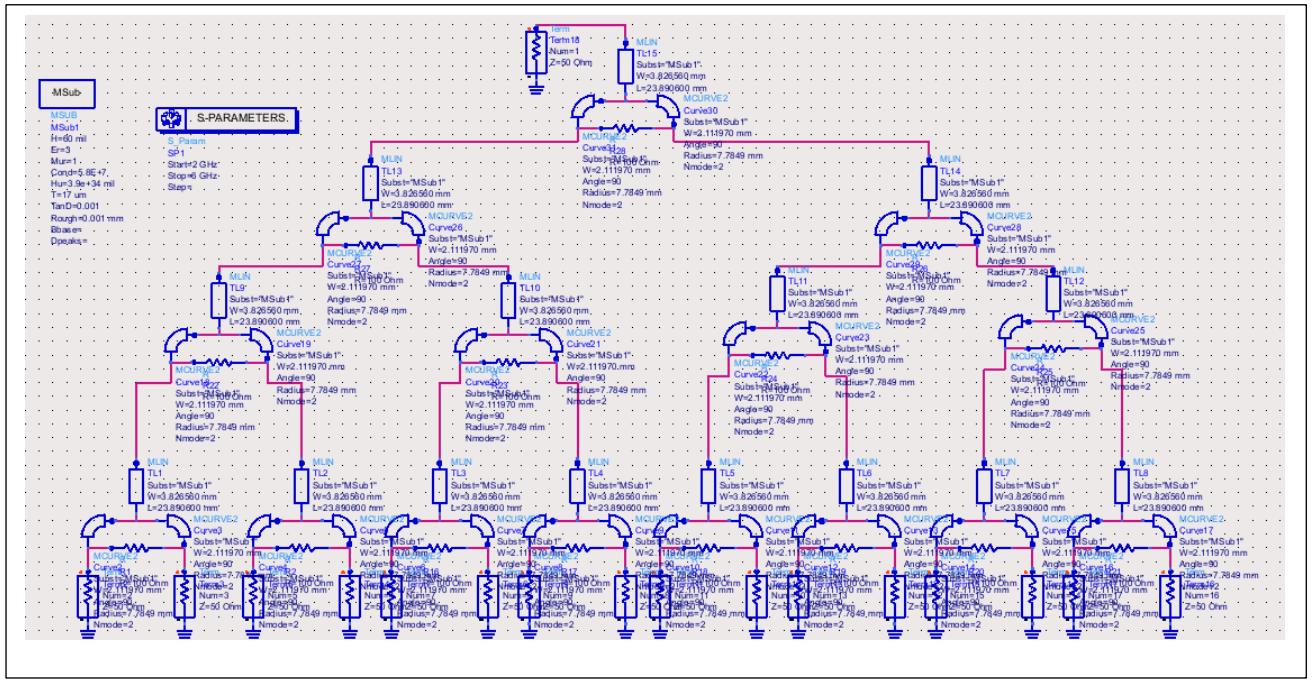

Fig 13 : Schematics of a 16 – way Wilkinson Power Divider with substrate Rogers(3003)

3.4 . Figures and charts of the simulation of printed microstrip lines

In this section , we show the figures of the following parameters :

1) The input return loss S(1,1) is required to be > 12 dB for a 10% percent fractional bandwidth . It is shown in figure 14 that it's 65 dB at the center frequency . We see also that it satisfies the 10% fractional bandwidth.

2)The output return loss S(2,2) is required to be > 12 dB for 10 % fractional bandwidth which is shown in figure 15 that we satisfy this specification .

3) The insertion loss (for example (S(1,5)) is shown in figure 17 and it's around 12.2 dB with almost 0.14 excess insertion loss (ideally = 12.04) which is so small .

4) The output isolation is the scattering parameter between two output ports has two cases:

-Worst case when output ports are very close to each other so isolation between them is just 100 ohm resistor like between port 2&3

-Best case when output ports are apart from like between port 2&16.

As shown in figure 16 We satisfy that bandwidth is >30 dB .

5) We see clearly in figure 18 that the phase is almost balanced with about -3 degrees phase difference

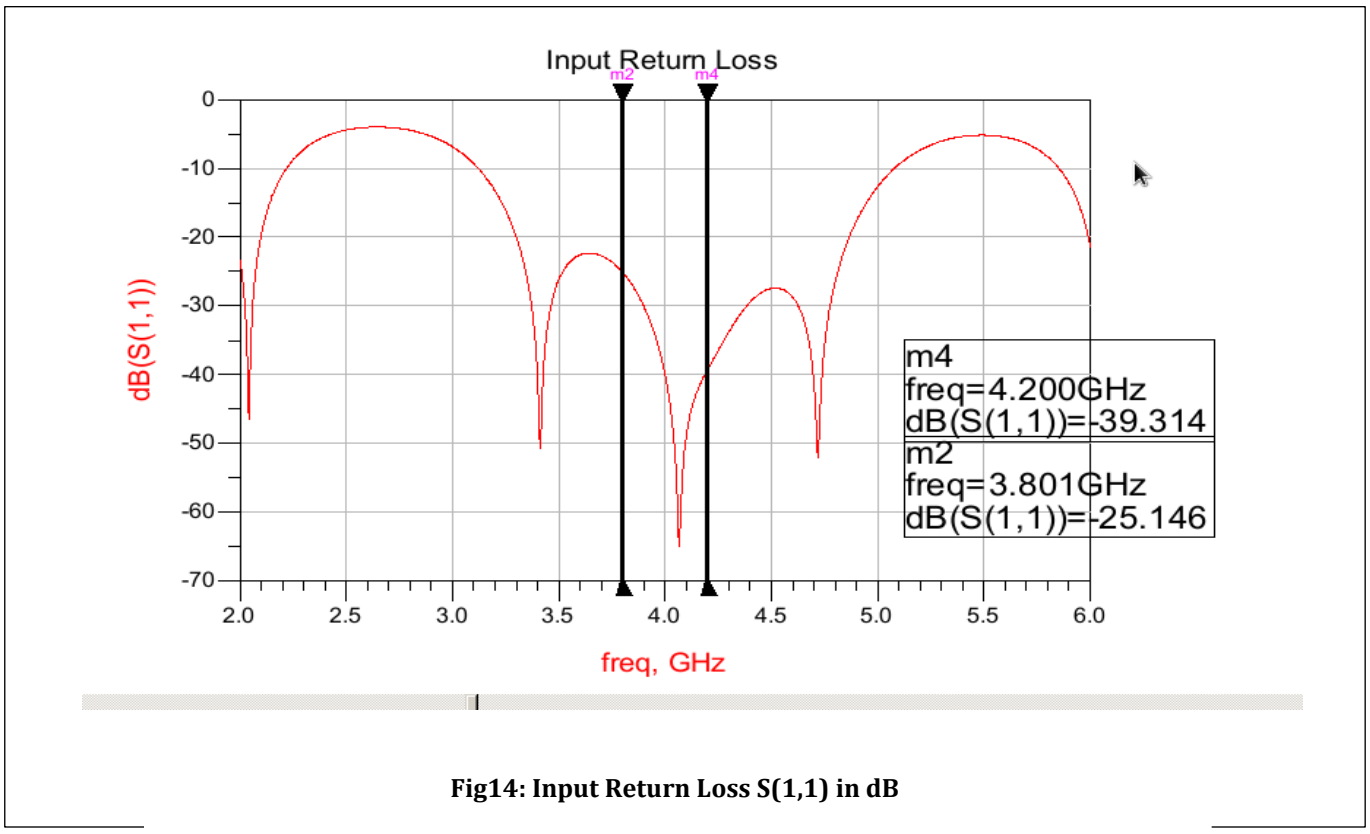

Fig14: Input Return Loss S(1,1) in dB

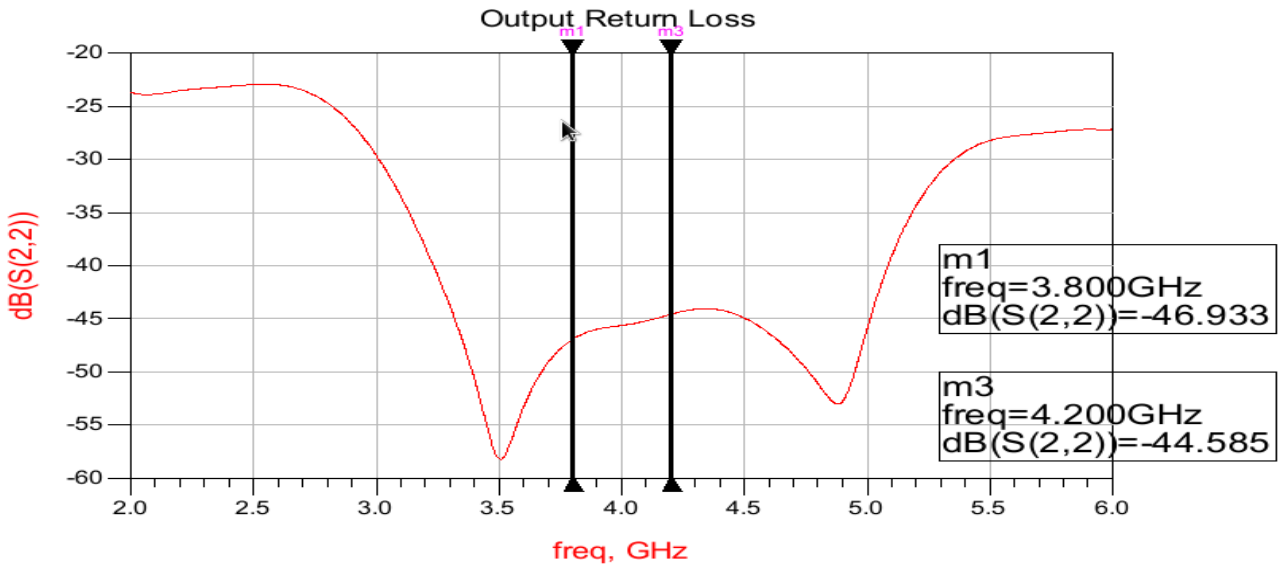

Figure 15 : Output return Loss (S(2,2))

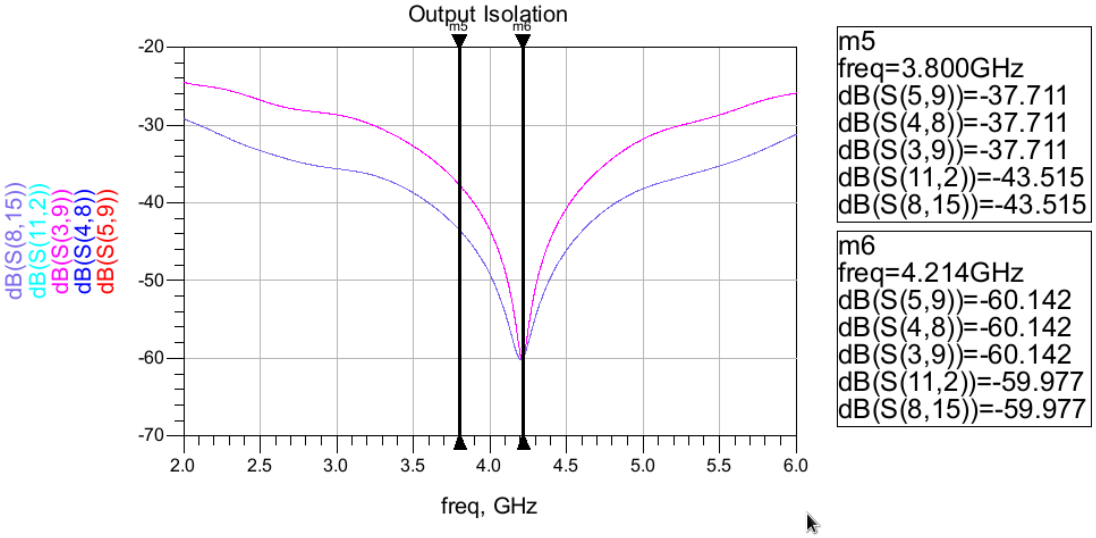

Figure 16: Output Isolation in dB

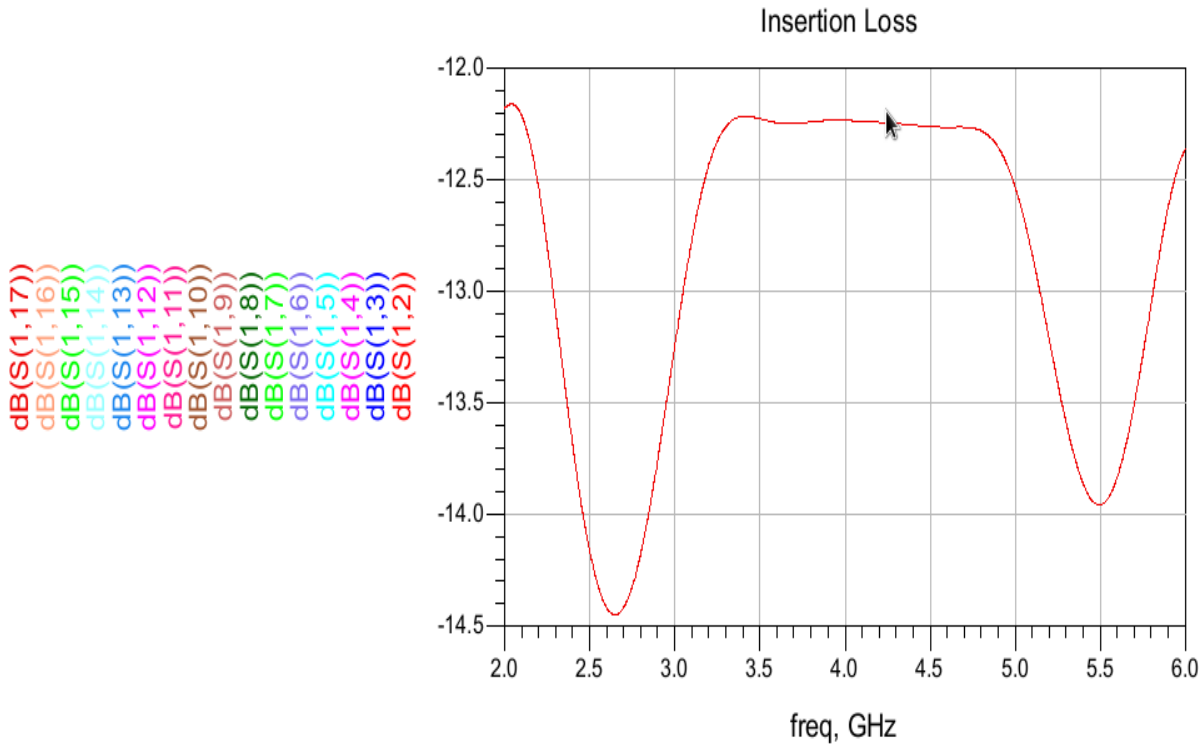

Figure 17 : Insertion loss in dB

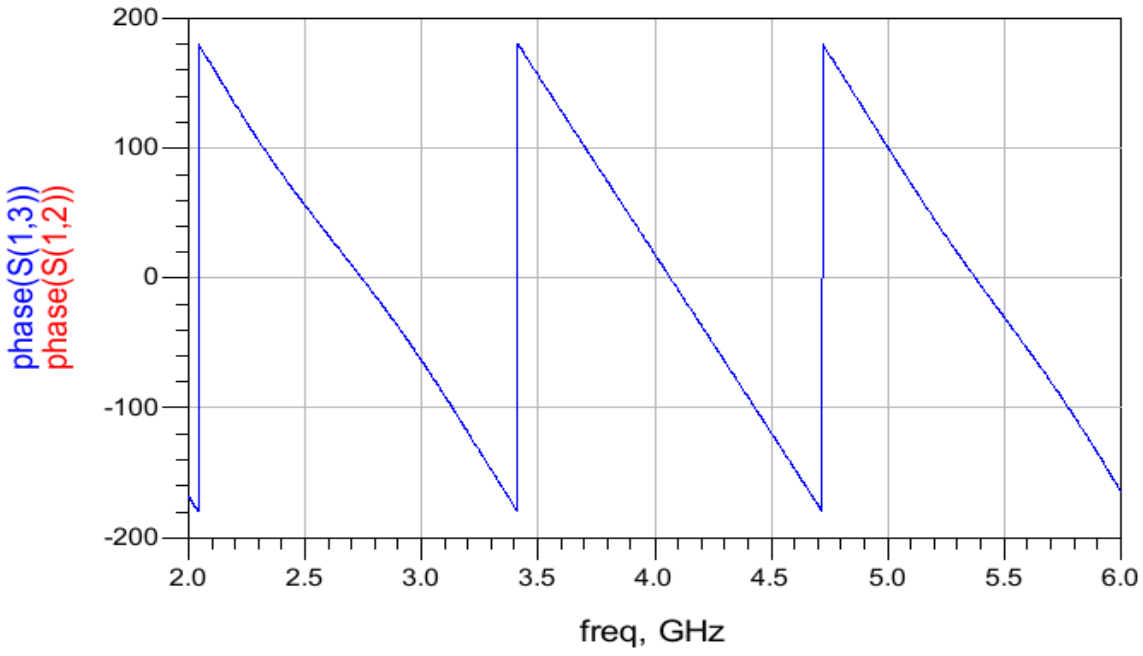

Figure 18 : phases of output port(2,3)

4 . Layout of the power divider (2x8 grid)

In this section , we show how we designed the 2x8 Wilkinson power divider grid . This configuration is useful as a feeder for an antenna array with the same configuration such as the one shown in figure 19 .

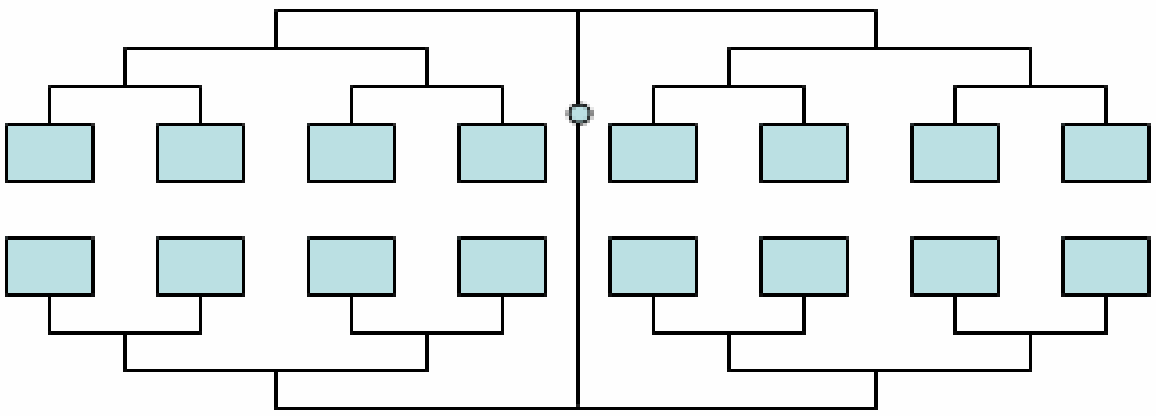

Figure 19 : 2x8 Antenna array

4.1. Layout design procedure

In this section we show the procedure we took to design our 2x8 power divider .

First of all , we designed a 1:2 WPD to be the unit PWD that we used to construct the full layout later on . In figure 20 , a snapshot of the 1: 2 PWD is shown . We took care of the junctions and discontinuities and relieved it using curved and tapered edges that also provides the same lengths and width of the original design (for the HW and QW sections) . We also designed the WPD so that there is a half – wave length separation between all output ports . We used an SMT resistor to reduce the area of the layout and make it as compact as possible . The 2 – D view of the full layout of this grid is shown in figure 21 . Another 3-D view of the layout is shown in figure 22 .

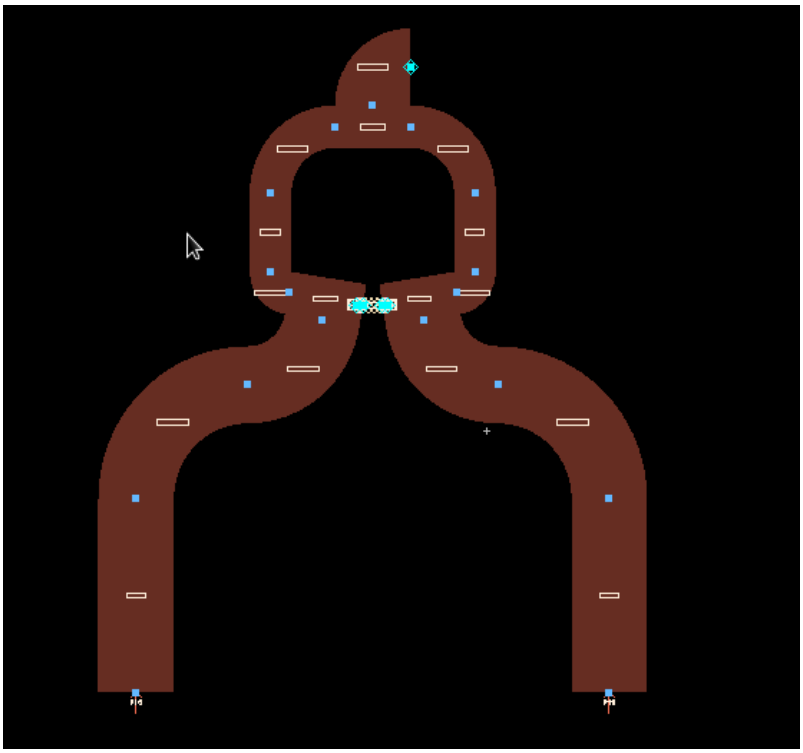

Figure 20 : Layout of the 1 : 2 Wilkinson power divider (2-D)

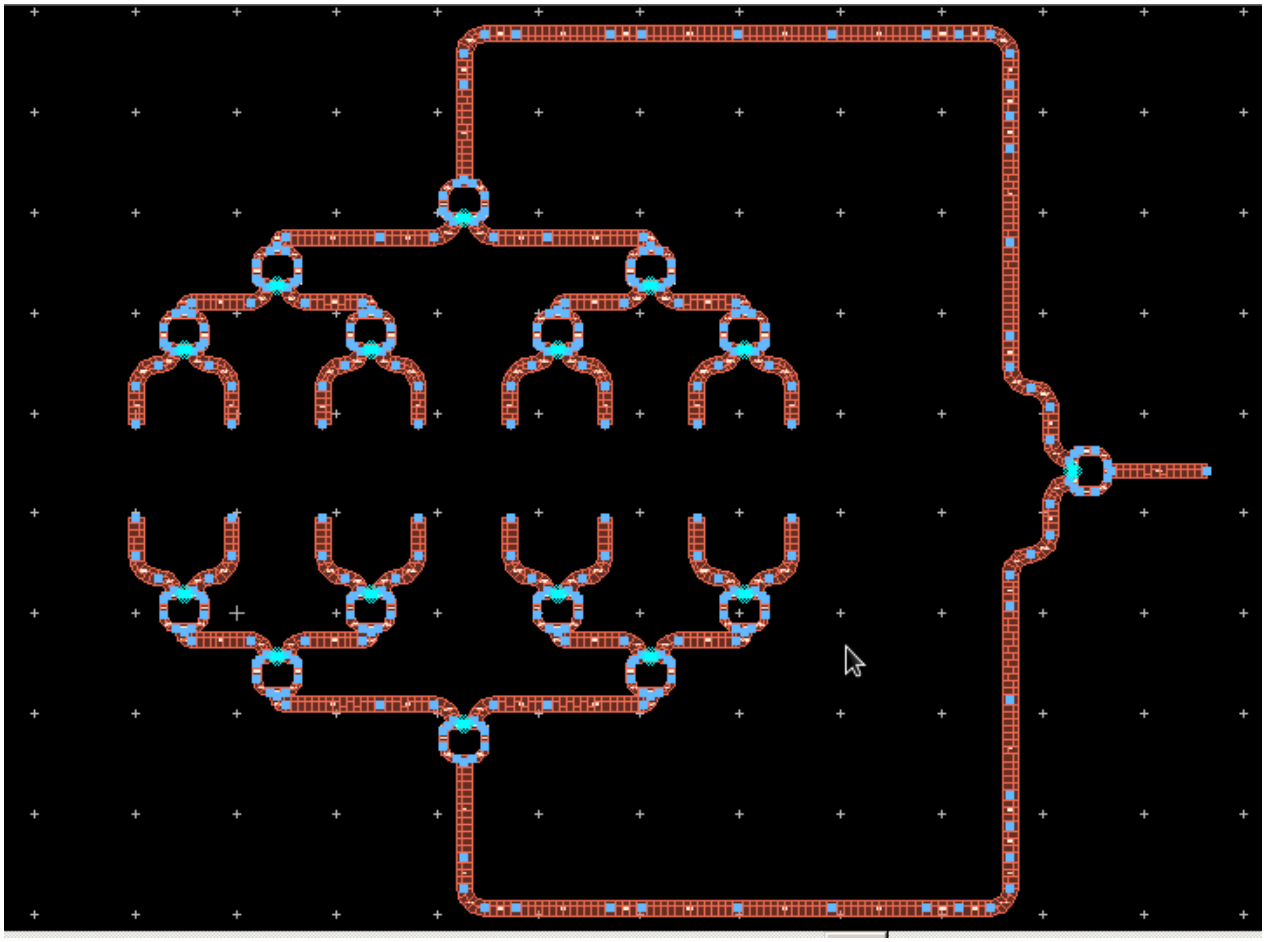

Figure 21 : The full (2-D) view of the 2x8 Power divider

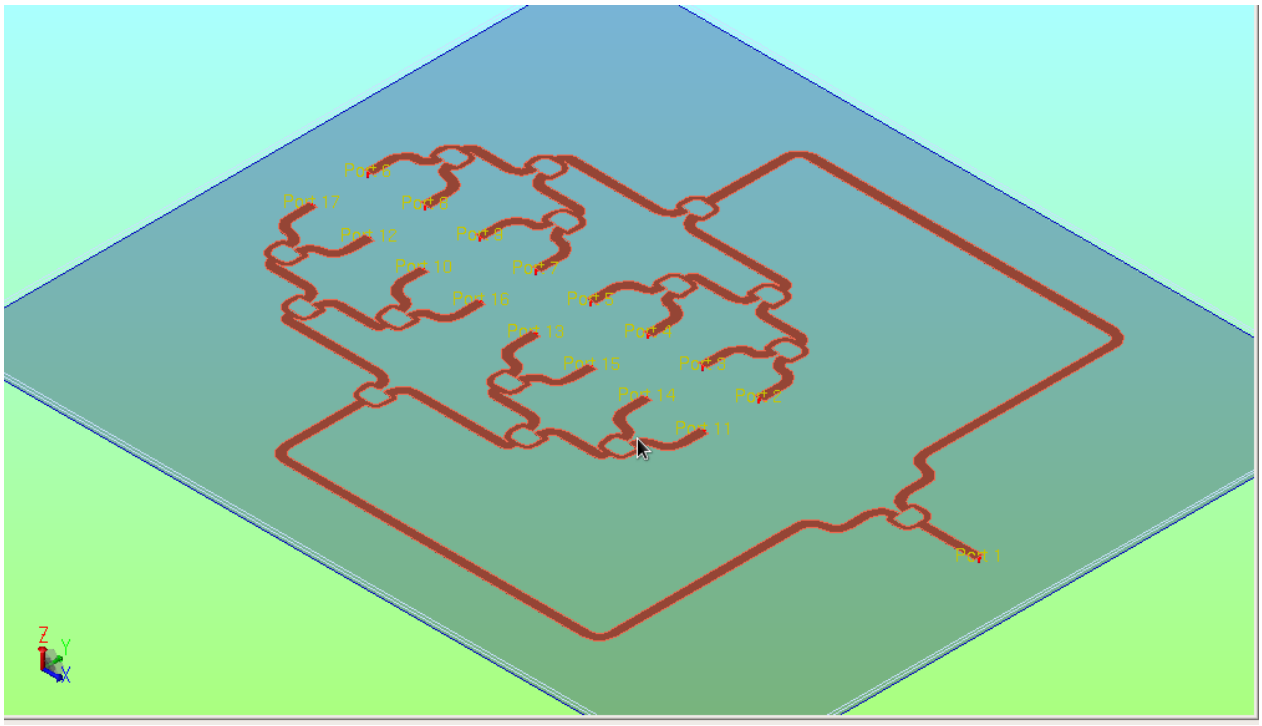

Figure 22 : A 3-D view of the 2x8 Grid

4.2.Simulation of the layout including discontinuities

In this section , We converted the layout into schematics view again so that we can simulate it again to see the S parameters of the layout and compare it with the ideal case after adding the junctions and discontinuities that mimic our specifications .

Figure 23 a , b shows a schematic view of the layout input and output ports ,Figure 24 Shows A full schematic view of the 2x8 Grid.

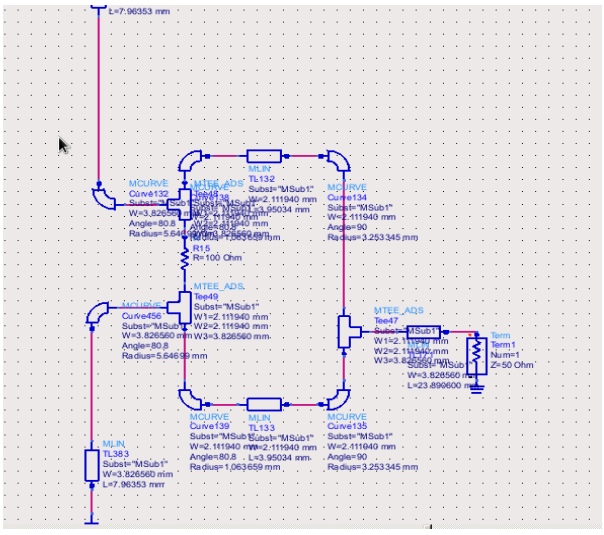

Figure 23 . a : input port

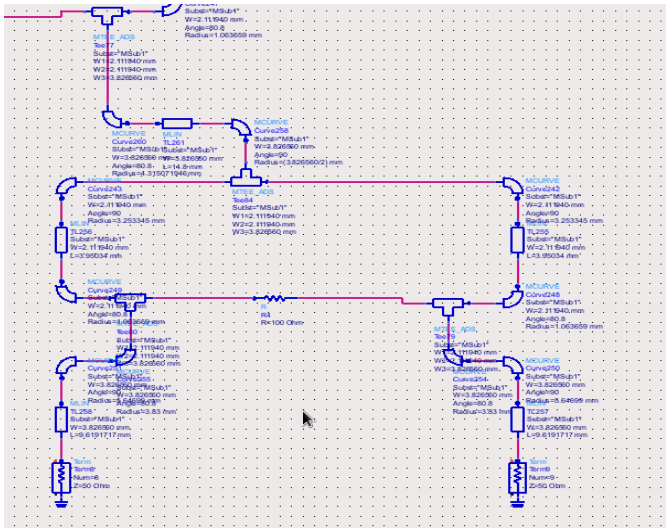

Figure 23 . b : Output Port

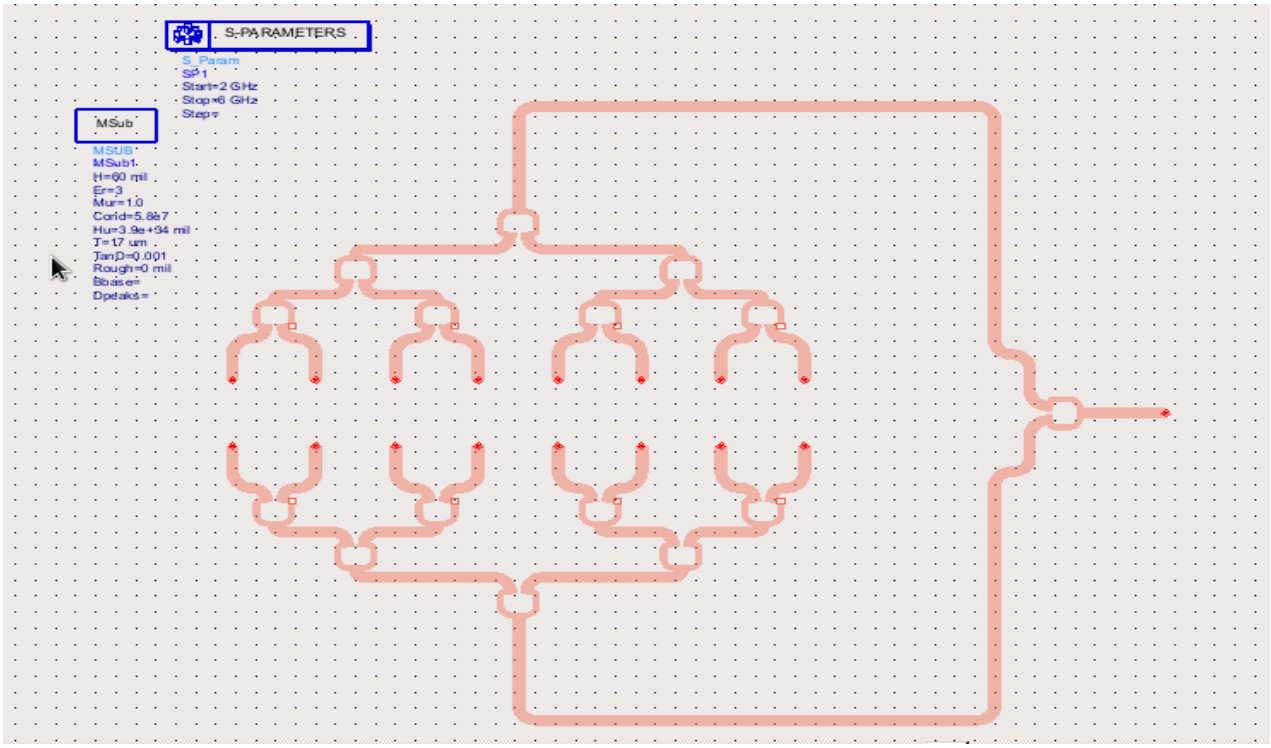

Figure 24 : A full schematic view of the 2x8 Grid

4.2.1. Input Return loss

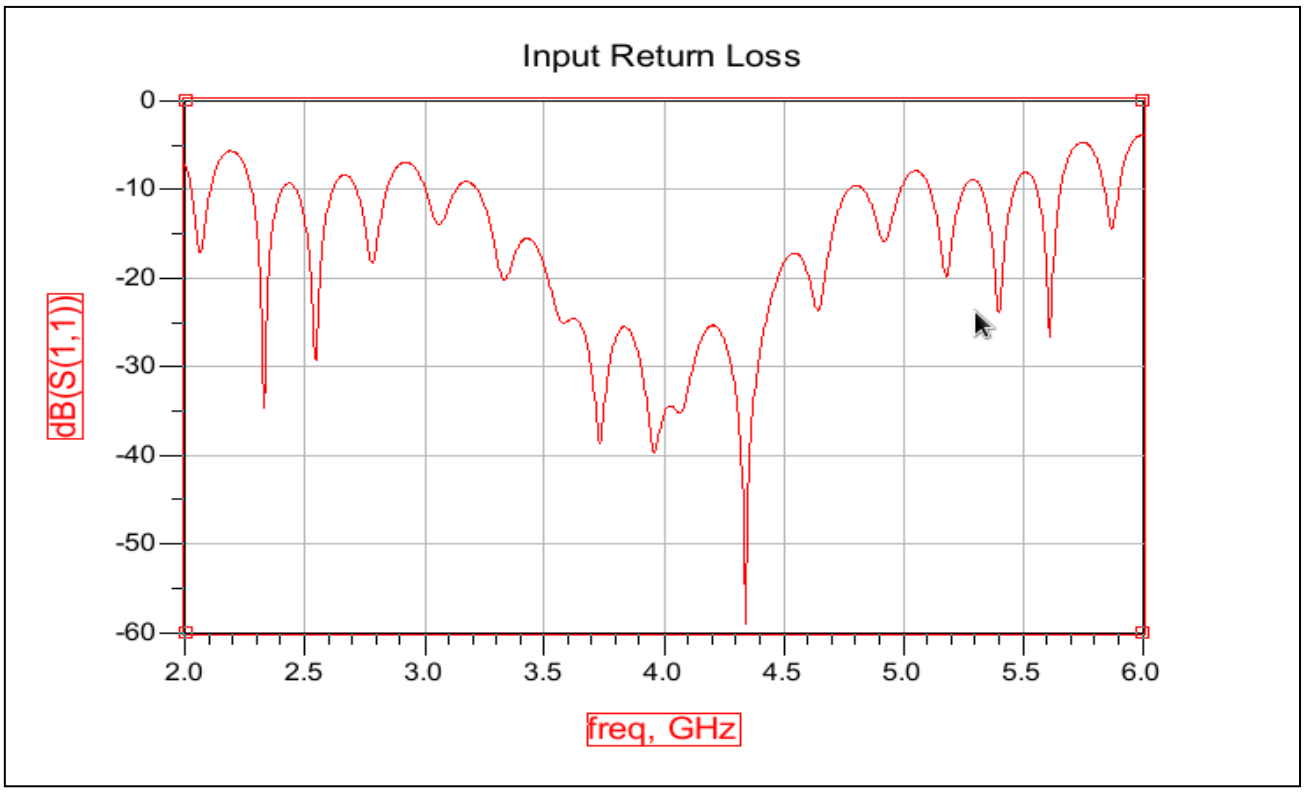

Figure 25 : Input return loss of the 2x8 Grid

4.2.2.Output Return loss

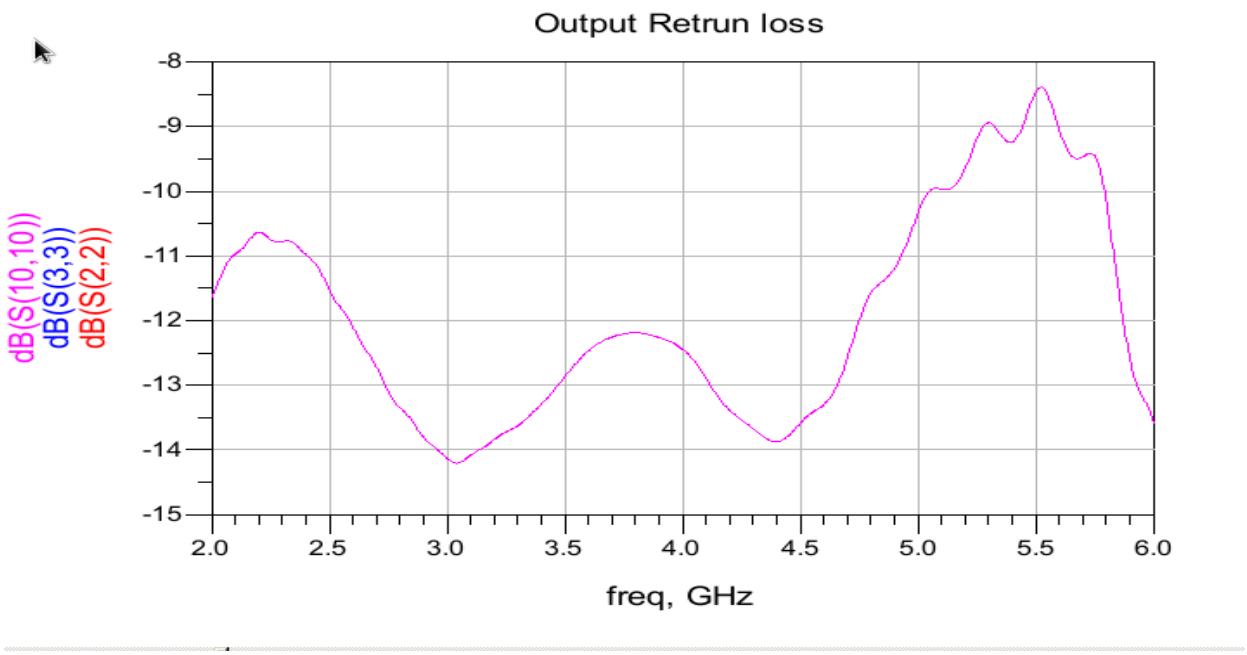

Figure 26 : Output Return Loss of the 2x8 Grid

4.2.3 . Insertion Loss

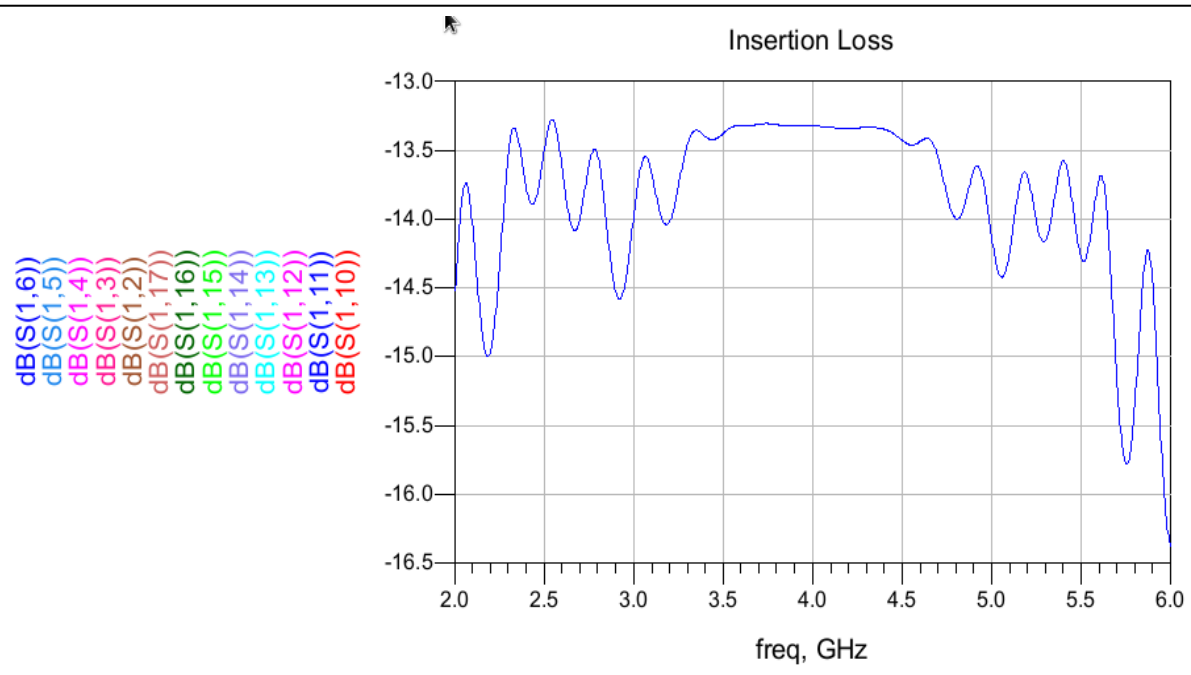

Figure 27 : Insertion Loss of the 2x8 Grid

4.2.4. Output Isolation

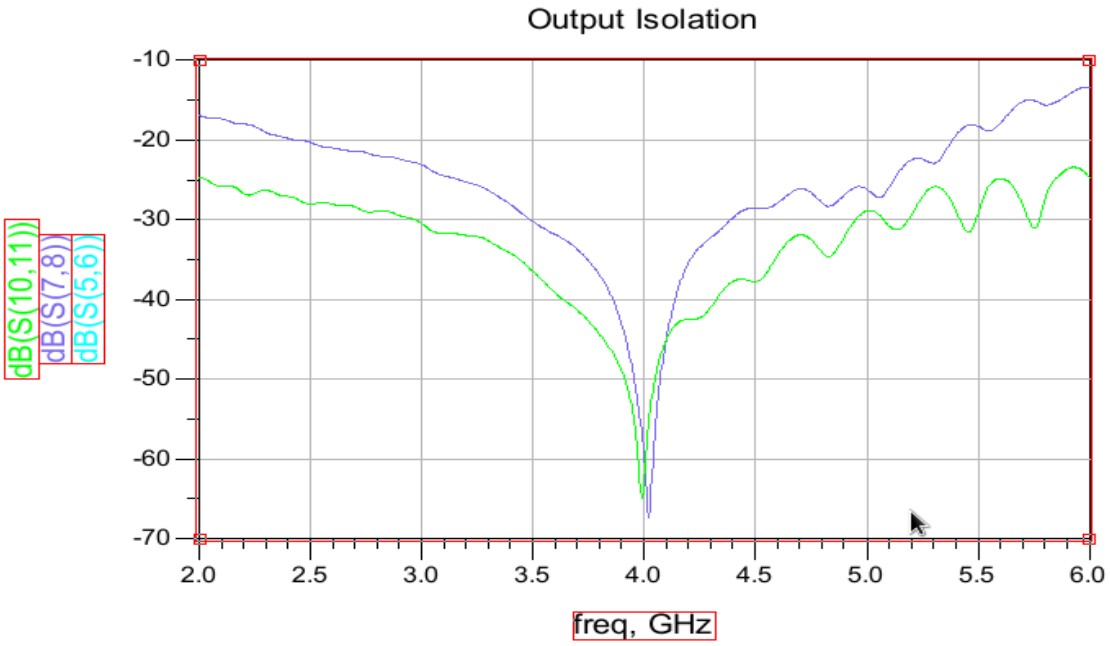

Figure 28 : Output Isolation of the 2x8 Grid

4.2.5. Phase difference between outputs

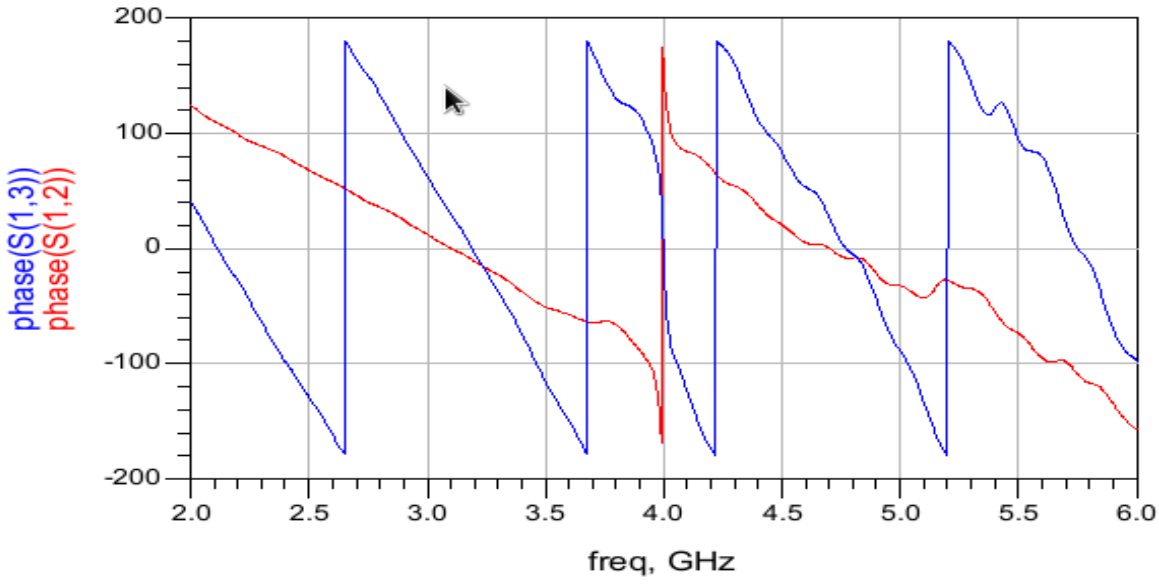

Figure 29 : Phase difference between outputs of the 2x8 Grid

5. EM Simulation of the layout

In this section , we simulated our design with EM simulation of ADS . We simulated using 50 points and covered a range of frequencies of about 3-5 GHZ .

5.1. EM simulation Setup

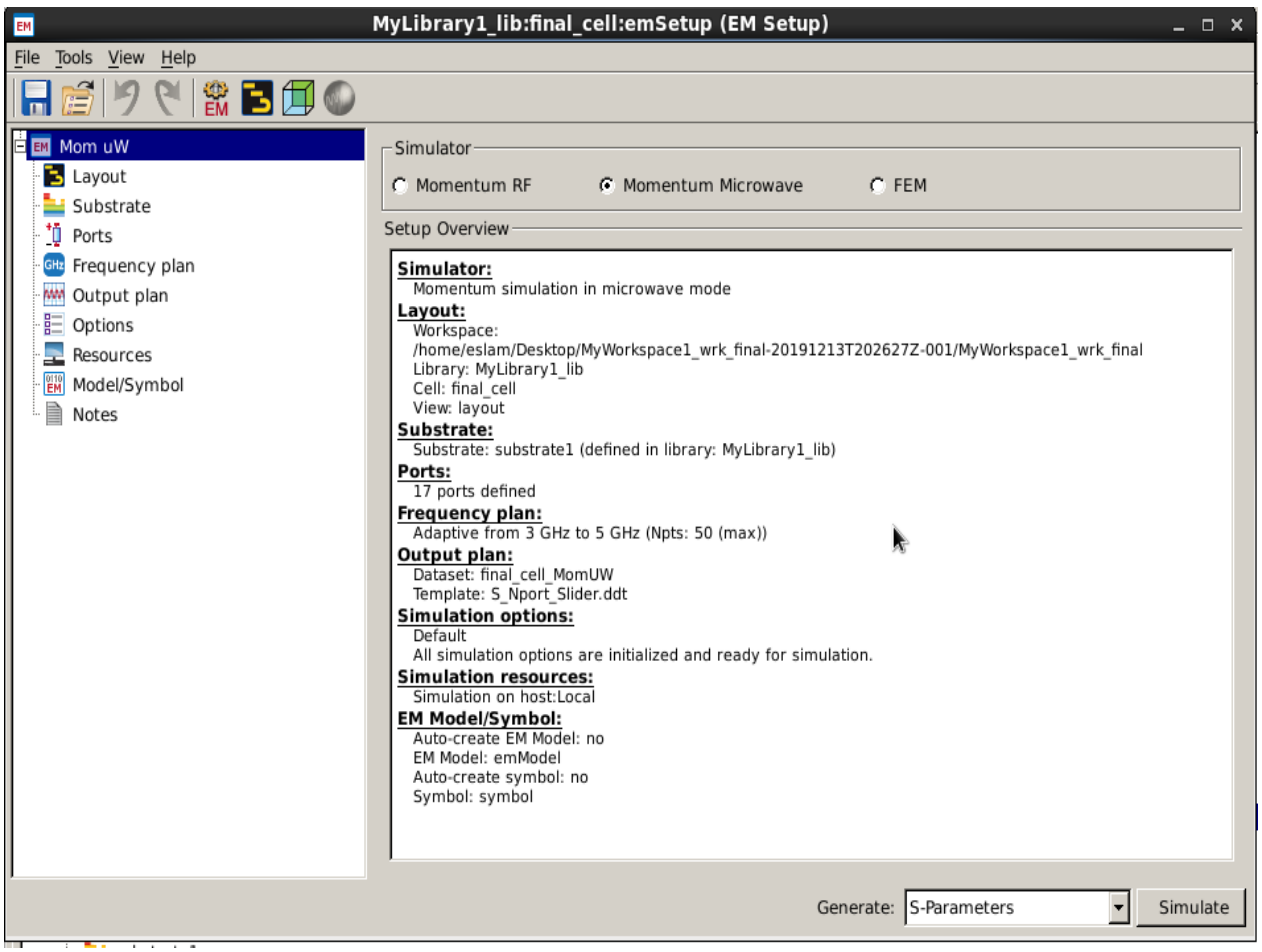

Figure 30 : EM simulation Setup

5.2. Figures and charts of the EM simulation

5.2.1.Input Return loss

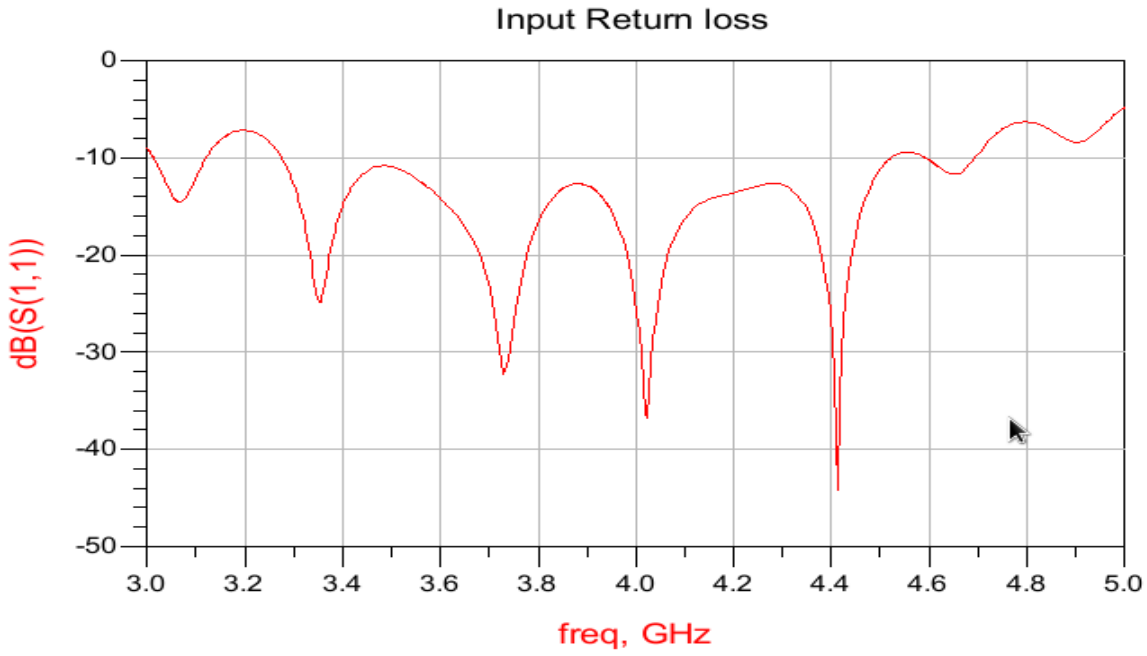

Figure 31 : Input return loss of EM simulation

5.2.2. Output Return Loss

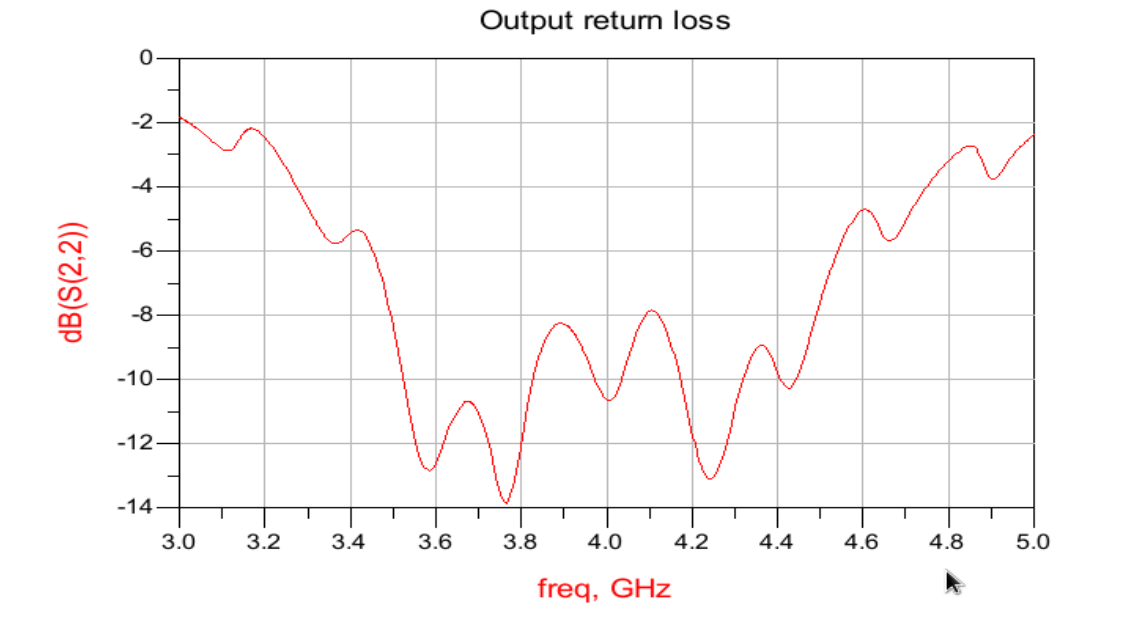

Figure 32 : Output return loss of the EM simulation

5.2.3. Phase between outputs

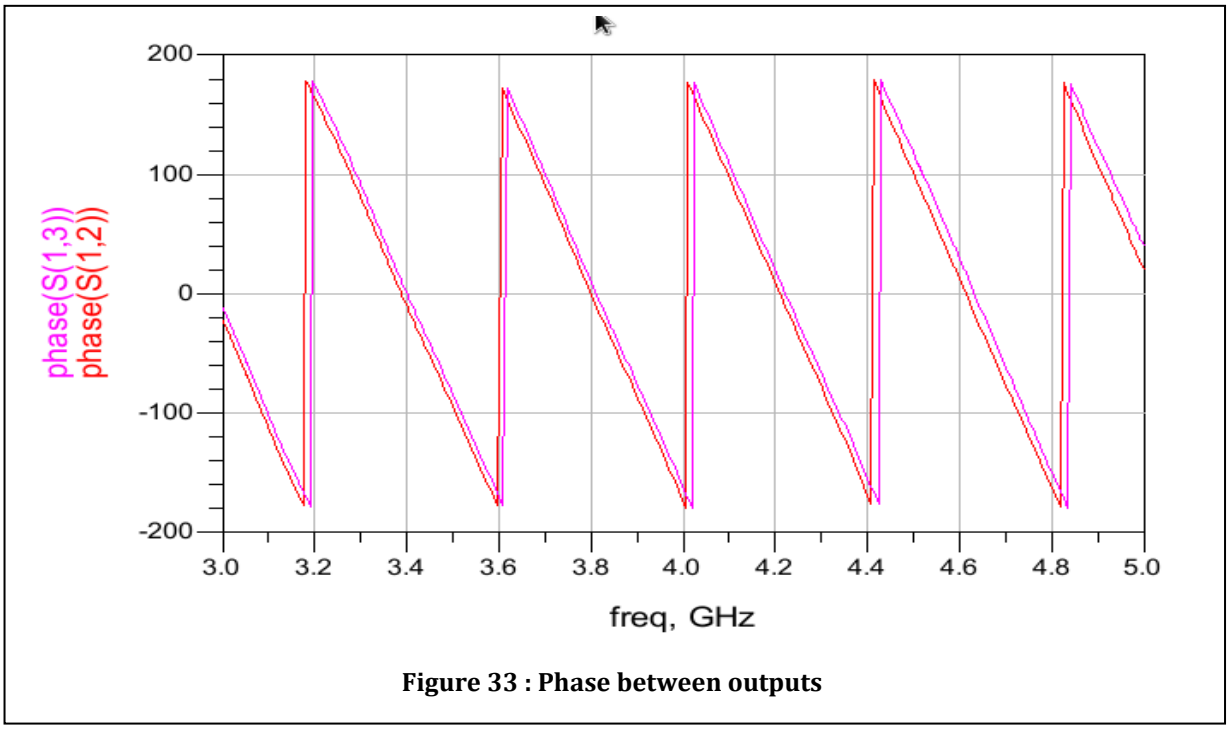

Figure 33 : Phase between outputs

5.2.4.Insertion Loss

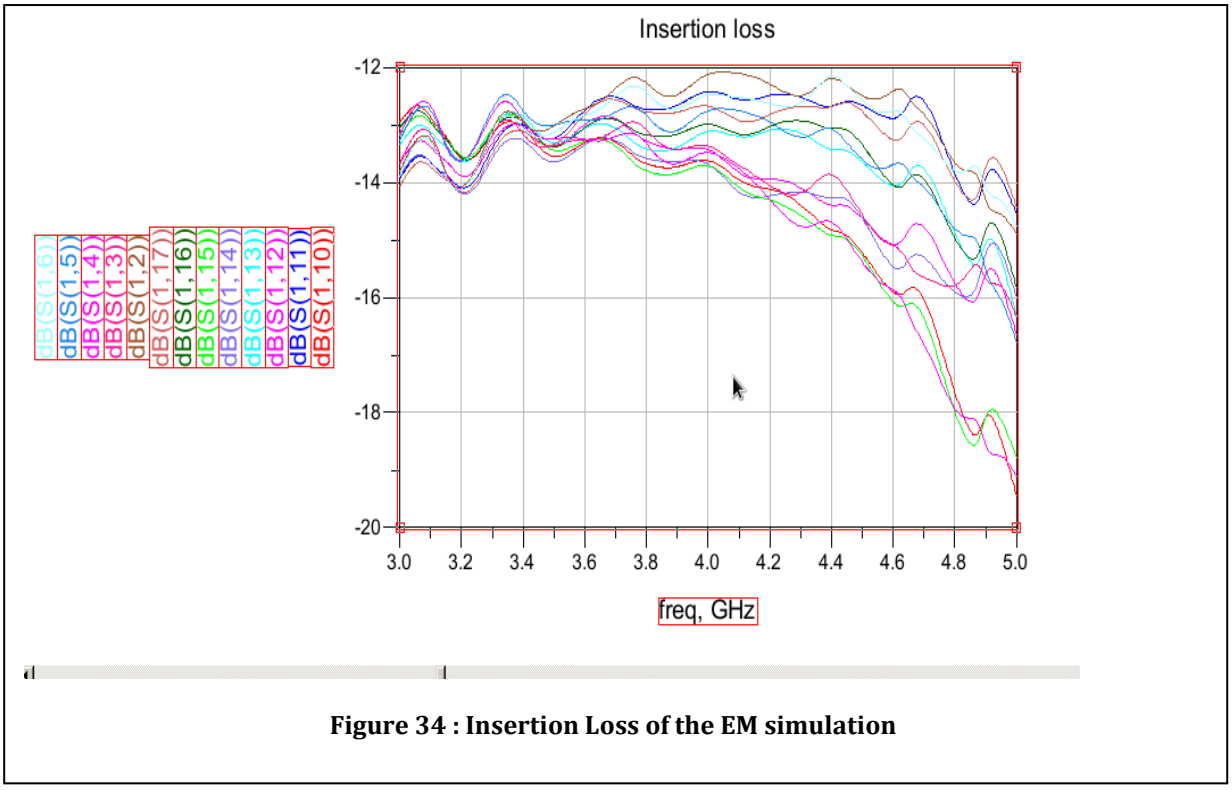

Figure 34 : Insertion Loss of the EM simulation

6.Discussion and conclusion

We have clearly seen through the proposed results that they are more accurate while using ideal transmission lines as microstrip lines decrease efficiency due to dielectric and conductor losses as well as radiation caused by corners. No one can deny its advantages in supporting multiple frequency bands and its ease in PCB fabrication but drawbacks must be put into our consideration as well

We conclude that the Wilkinson power divider is the most efficient power divider for our application . The main disadvantage of that design is that it consumes larger area for more output ports . It also has problems with the resistors but we solved it by using an SMD resistor of very small size to avoid lumped components problems .

References :

1) Avneet Kaur , Jyoteesh Malhotra , " Recent Trends and Challenges in Microwave Power Divider" Conference paper , DOI: 10.14257/ijgdc.2016.9.8.19 , August 2016

2) ISM Band 1:16 Wilkinson Power Divider