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A 4.1 GHz–9.2 GHz Programmable Frequency Divider for Ka Band PLL Frequency Synthesizer

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Received: 28 September 2020; Accepted: 24 October 2020; Published: 26 October 2020

Abstract: High speed divider is highly desired in the millimeter wave (mmW) frequency synthesizer design. A high operating frequency, low power consumption 90-nm CMOS programmable pulse swallow multi-modulus-divider is presented in this paper. High speed true-single-phase-clock D-flip-flop (TSPC DFF) is used in the counter in order to obtain a high operating frequency. It can operate at a frequency range from 4.1 GHz to 9.2 GHz, with a division ratio of 101–164. It has a power efficiency of 3.1 GHz/mW, and it can be used to provide a high quality reference frequency in the mmW phase-locked loop.

Keywords: CMOS; high speed; counter; prescaler; TSPC; multi-modulus-divider; phase-locked loop

1. Introduction

Due to the requirement of modern high-rate communication, ultra-wide-band transceivers are of demand. To generate a high quality carrier signal for modulating and demodulating in the transmitters and receivers is a challenge in the mmW integrated circuit design [1]. Phase-locked-loop (PLL) is always used to generate a carrier signal. It can multiply a low reference frequency by a ratio to obtain a high frequency signal [2–4]. The usage of PLL is more and more important in mmW circuit design like 5G communication system and radar, as the quality of the signal is important in modulating and demodulating in the transmitter and receiver. A divider is an important part in the PLL system, it divides the high-frequency signal from the output of the voltage-controlled oscillator (VCO) to the reference frequency [5].

Two types of dividers are used in the frequency synthesizer, prescaler and multi-modulus-dividers (MMD). The division ratio of the prescaler is a constant and it has a high operating frequency with a high power consumption [6]. MMD's operating frequency is lower compared with the prescaler, but the division ratio of MMD can be adjusted by digital control. As the VCO in the PLL operates at the highest frequency in the PLL, the output signal of VCO will be sent to several prescaler at first [7], and the output low frequency signal from the prescaler is divided to the reference frequency by the MMD [8]. A high operating frequency and low power consumption pulse swallow MMD is presented in this paper. The improvement of low operating frequency of such MMD is a challenge [9–13]. The operating frequency of N/N + 1 prescaler and counters is the restriction of the operating frequency. In recent years, high operating N/N + 1 prescaler is reported in the papers. However, high operating counter is still a challenge and it restricts the operating frequency range of MMD.

In this design, besides a high operating frequency N/N + 1 prescaler, high operating frequency TSPC DFFs are used in the programmer counter, which improves the upper limited frequency of the counters and the whole system, with less power consumption. In the following section, a high operating frequency MMD is presented. Section 2 introduce the circuit design of MMD. Section 3 presents the measured result. And the conclusion is in the Section 4.

2. Materials and Methods

2.1. Analysis of Dividers in PLL

In a Ka band phase-locked-loop system shown in Figure 1, two types of dividers (prescalers and MMD) are used in the systems as illustrated in part one. The division ratio of a MMD is restricted by two limited condition,

$$\text{mmd\_ratio}_{\text{min}} < \frac{f_{\text{pll\_out\_min}}}{2^N \cdot f_{\text{ref}}} \quad (1)$$

$$\text{mmd\_ratio}_{\text{max}} > \frac{f_{\text{pll\_out\_max}}}{2^N \cdot f_{\text{ref}}} \quad (2)$$

where $\text{mmd\_ratio}_{\text{min}}$ and $\text{mmd\_ratio}_{\text{max}}$ stand for the minimum and maximum division ratio of MMD, $f_{\text{pll\_out\_min}}$ and $f_{\text{pll\_out\_max}}$ are the minimum and maximum frequency of the PLL output, N is the amount of the prescaler in the PLL system and the prescaler has a constant division ratio.

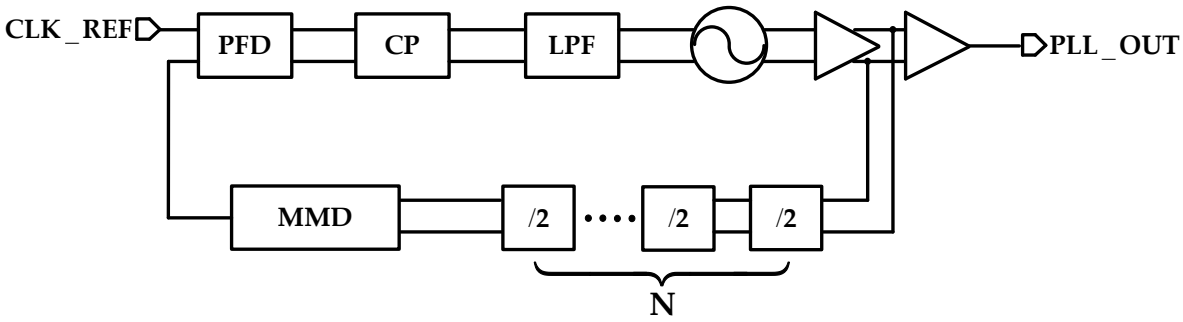


Figure 1. Block diagram of a Ka band PLL.

In the design of a PLL, the division ratio range can be determined due to the output frequency range and reference frequency. The typical type of prescaler used in Ka band PLL is current-mode logic (CML) latch [14] and injection-locked frequency divider (ILFD) [15], as shown in Figure 2a,b. Both CML latch and ILFD occupy a large area due to the load inductors and resisters [16]. And the static power they consume is large, which will influence the performance of the PLL [17]. If the division ratio of the MMD increases by one time, the prescaler used in the system can take one off. Therefore, the area of the whole system and the power consume of the whole system can be reduced [18].

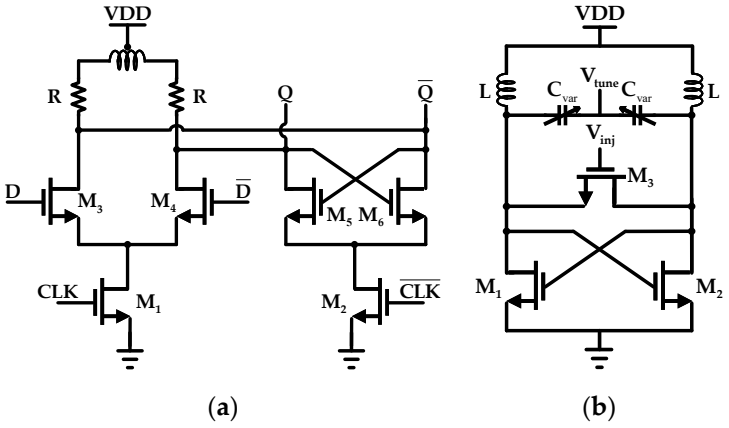


Figure 2. (**a**) A topology of CML divider; (**b**) A topology of ILFD.

A 2/3 divider-chain is a common structure of MMD [19–25]. The division ratio of such MMD ranges from 2^n to $2^{n+1} - 1$, where n is the amount of the 2/3 divider cell. This structure can obtain a high division ratio with a simple circuit design. It can also obtain a high operating frequency

compared with other MMD structures, but the power efficiency of such a structure is quite low. It is not practical in most case as the division ratio is restricted to a certain range, though it can be overcome by alter the structure of divider chain [9,20], which will increase the power consumption of the MMD. Pulse swallow divider can overcome this problem [11]. It can alter the division ratio arbitrary, while it is not easy to achieve a high operating frequency, which restrict the usage of such structure in the mmW PLL design.

In order to obtain a high operating frequency pulse swallow MMD, the component of MMD should be specially designed. The demand of the operating frequency increases by one times as the division ratio multiplies by two if the reference frequency is certain. In the meanwhile, counter bit size of counter P and counter S increase, and the structure of the circuit is more complex, which is more difficult to obtain a high operating frequency.

2.2. Circuit Design of MMD

The structure of pulse-swallow MMD is shown in Figure 3. The structure of MMD contains three parts: dual-modules prescaler, program counter (counter P) and swallow counter (counter S).

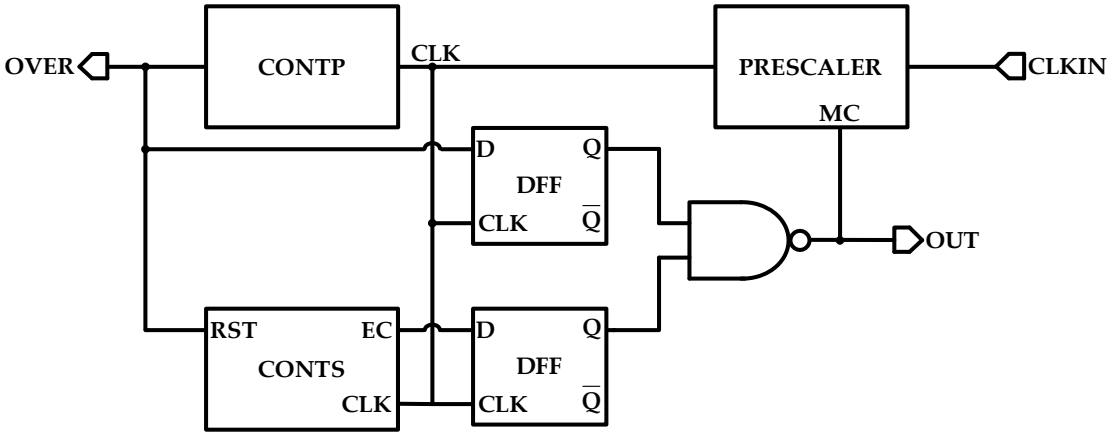


Figure 3. The structure of the pulse-swallow MMD.

2.2.1. N/N + 1 Dual-Modulus Divider

A 2/3 dual-modulus prescaler is the basic dual-modulus prescaler, which is shown in Figure 4a [26]. As dual-modulus prescaler works at the highest frequency of the MMD, the frequency range of the prescaler will restrict the working frequency of the whole system, especially for the upper limit [27]. In order to achieve a high working frequency prescaler, a high operating frequency DFF is of demand. TSPC DFF combines the advantage of low power cost and high operating frequency. So TSPC-logic prescaler is widely used in the MMD [28]. The logic of the TSPC prescaler can be simplified in order to obtain high speed and high working frequency [29].

For any integer N, N/N + 1 prescaler can be designed by using 2/3 prescaler and DFF. In this design, a TSPC 4/5 prescaler is chosen, as shown in Figure 4b. The divider cell can operate at div-4 mode as the control bit MC is high, and as MC is low, the prescaler works at div-5 mode. Figure 5 shows the input signal sensitivity of the prescaler, and it can be seen from Figure 5 that working frequency range of the prescaler in div-4 mode and div-5 mode is similar. The performance of the prescaler satisfies the demand of high working frequency and wide range working band in this design.

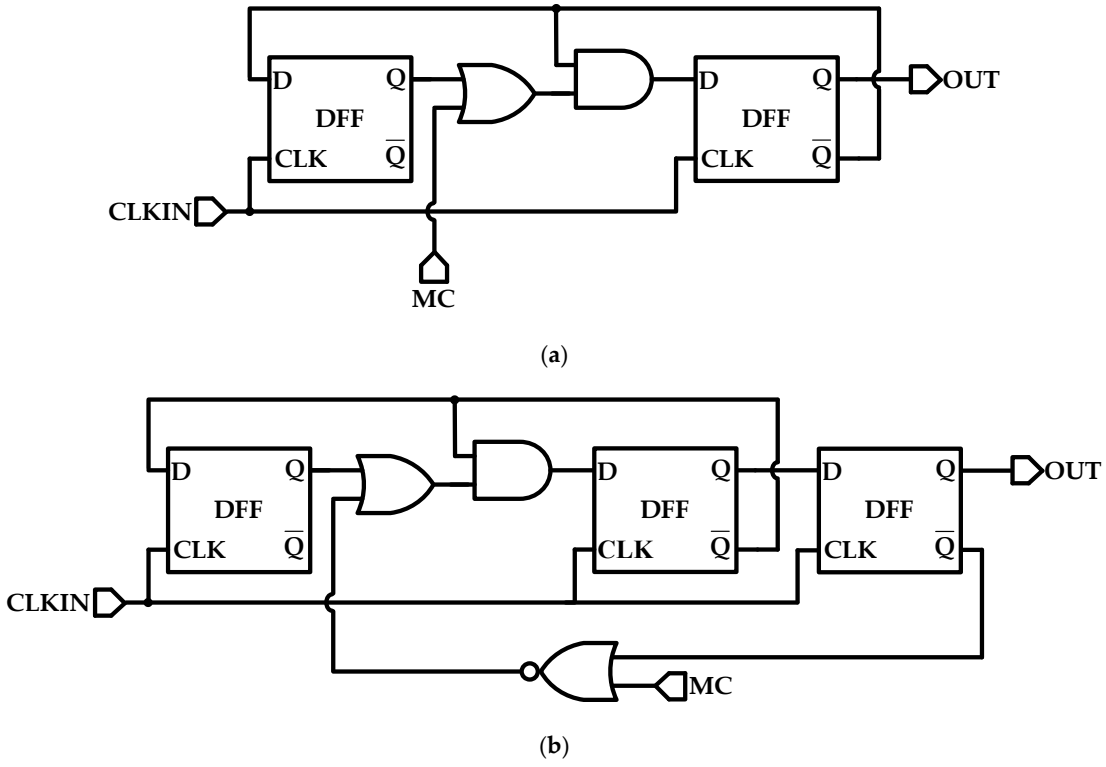


Figure 4. (**a**) Block diagram of the2/3 prescaler; (**b**) Block diagram of 4/5 prescaler.

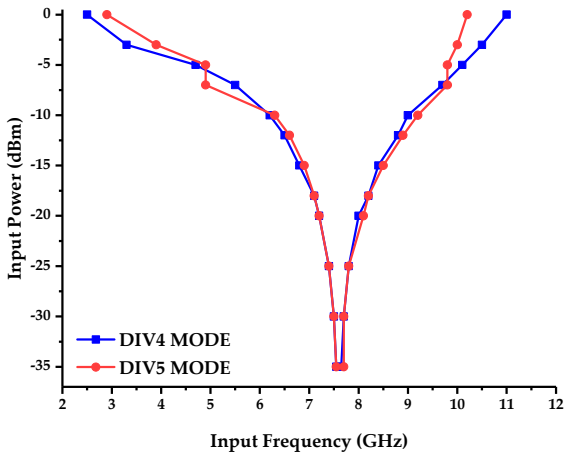


Figure 5. Simulation result of the input sensitivity curves of the prescaler.

2.2.2. Program Counter and Swallow Counter

A program counter and swallow counter has a similar structure. The structure of counter P and counter S is shown in Figure 6. A six-bit counter is used as counter P, while counter S is four-bit. Both counter P and counter S are down counters. Take counter S as an example. The output of the DFF divider chain can be regarded as a code. The code is reset to 0000 as the reset bit is active. The code state will change to 1111 when the next clock edge come. The code will minus one as the following clock edge come, until the code change to $\overline{C_3C_2C_1C_0}$, the counter stops counting. As the first state of code is 0000, the counter counts S + 1 rather than S until it stops.

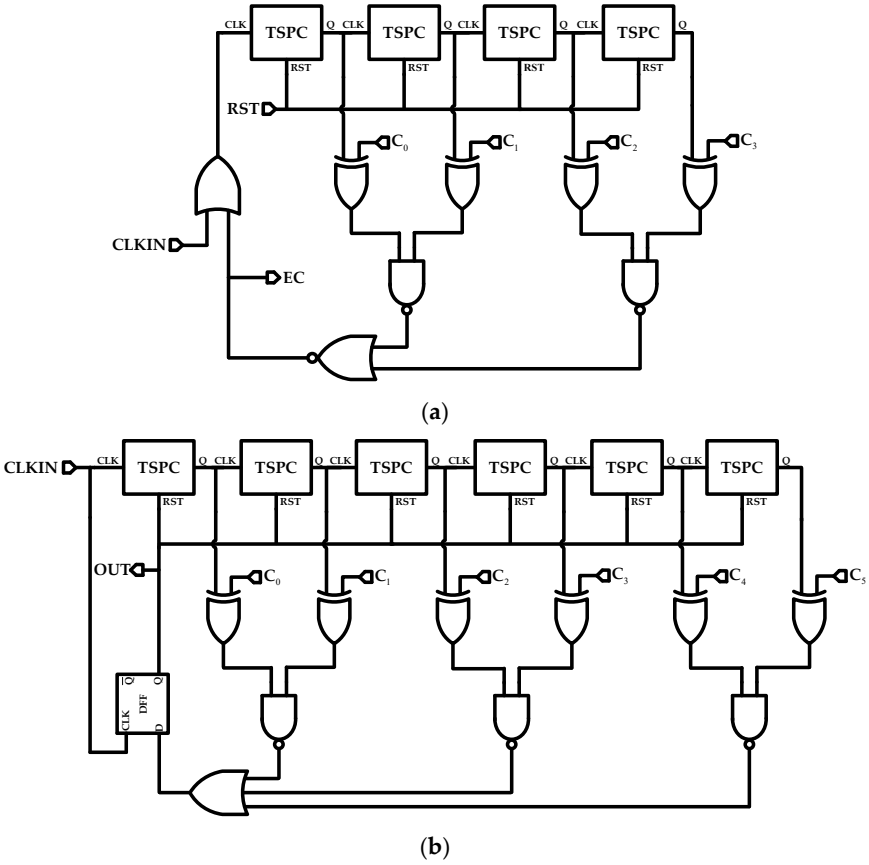


Figure 6. (**a**) Block diagram of counter S; (**b**) Block diagram of counter P.

Counter P has the similar principle of counter S. As the codes turn to $\overline{C_5C_4C_3C_2C_1C_0}$ from 000000, the reset bit reset the counter and the codes turn to 000000. However, each stage has a time delay. Due to the time delay, wrong state may occur when the code turns. For example, when the codes turn from 000000 to 111111, there are five temporary states 000001, 000011, 000111, 001111, 011111 occur. These code states may cause wrong result of the reset signal, which will cause error count. In order to avoid the wrong state, a DFF is added before the output as shown in Figure 6b. And the DFF has another effect as a retiming block [22]. It performs duty-cycle equalization function of the reset signal. Because of the adding of the retiming DFF, the counter counts P + 3 rather than P.

In the meanwhile, the time delay between each stage of DFF will accumulate. If the accumulated time delay of the DFF divider chain is larger than the clock period, error state will appear. Therefore, for those counters with several DFFs, the time delay of each DFF should be considered in the design, and the working frequency of DFF should be in the range of the frequency of the input signal. For a counter with a six DFF-stage chain, the input signal of the first DFF is the output of the N/N + 1 prescaler, which has a frequency of f_{dm_out}. The input signal frequency of the last stage of the divider-chain is $f_{dm\_out}/32$. This means that the design of divider should both consider the high working frequency condition and low working frequency condition.

DFF based on transmission gate is a conventional structure and it is widely used as a divider. The circuit of such DFF is shown in Figure 7a. The DFF based on transmission gate has a good low working frequency performance, but the time delay of such DFF is large and it cannot work at a high frequency. Therefore, a TSPC DFF is used in the counter. It has a smaller time delay, and it can work at a higher frequency than the conventional structure, which satisfies the demand of high operating frequency. The circuit is shown in Figure 7b.

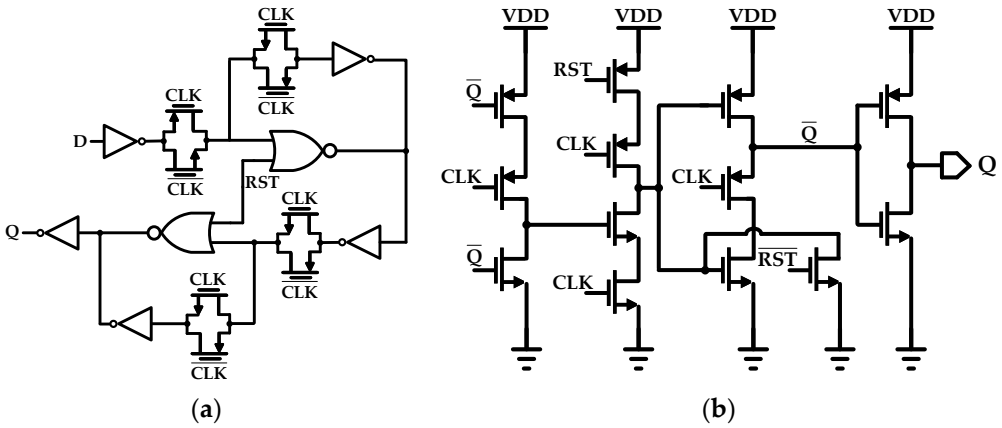


Figure 7. (**a**) Circuit of the conventional DFF; (**b**) Circuit of TSPC DFF.

The conventional DFF, based on transmission gate and TSPC DFF, are designed and simulated. As the input signal is 1 GHz pulse signal, the time delay of two DFF in −40, 50 and 125 °C is simulated. The result is shown in the Table 1 and Figure 8. It can be seen from the Table 1 and Figure 8 that the time delay of rising edge of the TSPC is much smaller than the conventional DFF, and the time delay of the falling edge is also smaller when the TSPC is used.

Table 1. Time delay of the two structure of the DFF.

	Time Delay (Rising Edge)	Time Delay (Falling Edge)
−40 °C TSPC	19 ps	69.5 ps
−40 °C Conventional	93.5 ps	76 ps
50 °C TSPC	17.5 ps	62 ps
50 °C Conventional	85.5 ps	68 ps
125 °C TSPC	20.5 ps	76 ps
125 °C Conventional	102.5 ps	82 ps

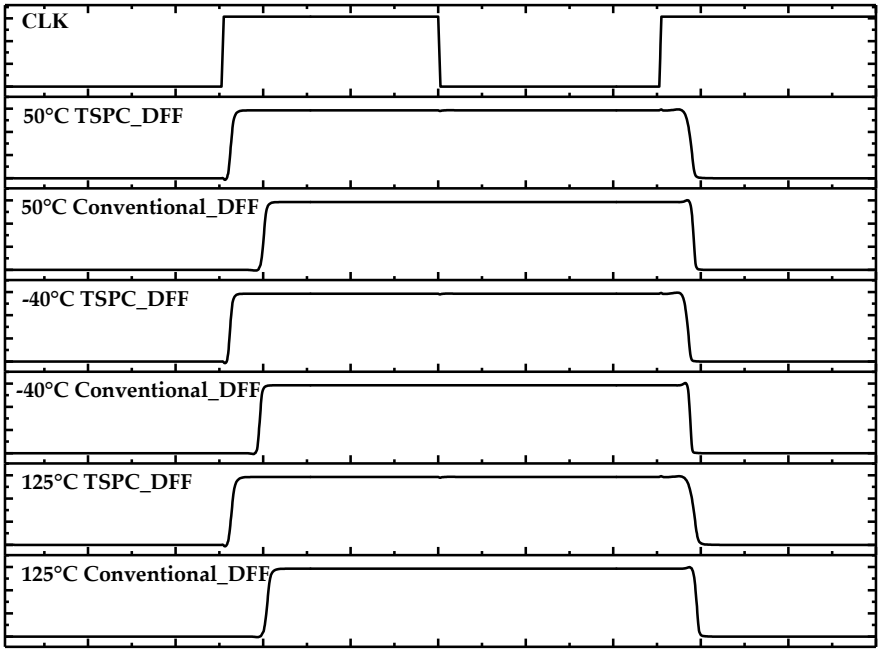


Figure 8. Simulation result and comparison of time delay between the conventional structure (transmission-gate based) and TSPC DFF.

Time delay of the counter is different as the code state change. Take counter P as an example. The largest time delay occurs when the code turns from 100000 to 011111. The time delay is $5t_{rise} + t_{fall}$, which is much smaller by using the designed TSPC-DFF chain than using the conventional DFF chain. The calculated theoretically maximum working frequency in 50 °C of counter P based on TSPC DFF is 6.67 GHz, 3.3 times larger than using conventional DFF. The power consumption of the TSPC is also smaller than the conventional transmission-based DFF, which is important for the low-power design.

The input clock of the counter P and counter S is the output signal of prescaler, which is nearly a pulse signal. The operating frequency range of the DFF when the input signal is a pulse signal is simulated. It can work at a frequency range of 25 MHz to 12 GHz, with a pulse signal input.

As counter P provides the reset signal of the counter S, the counter S has a same period of the counter P's reset signal. It counts P + 3 before the reset signal is active. The period of the clock signal is not a constant, it varies due to the N/N + 1 prescaler. Assume the MC in Figure 3 is active, the prescaler counts P-S + 2 before the prescaler works at div-5 modes. The state will maintain until it counts S + 1. So the division ratio can be expressed as in (3). The duty cycle of the output signal should be considered in the design. Duty cycle will influence the drive capability, and it is important for the high speed circuit [11]. The duty cycle of MMD can be adjusted by adjusting P and S. It can be expressed as in (4):

$$\text{mmd\_ratio} = \text{NP} + 3\text{N} + \text{S} + 1 \tag{3}$$

$$\text{duty\_cycle} = \frac{\text{NP} - \text{NS} + 2\text{N}}{\text{NP} + 3\text{N} + \text{S} + 1}. \tag{4}$$

For a certain division ratio, there are a lot of schemes by choosing different P and S. Duty cycle should be considered as a factor when choosing P and S.

3. Measurement Results

The division ratio of the MMD is selected from 101 to 164. The duty cycle of the output signal of MMD is also specially designed by adjusting counter P and counter S. Counter P can count from 23 to 38 while counter S can count from 9 to 15, which are controlled by a six-bit encoder, and it is integrated in the chip. A $\Sigma - \Delta$ modulator is used in the chip for providing a division ratio of MMD, and it can also be used for fraction division in the PLL, it is controlled by a serial peripheral interface (SPI), which provides a division ratio of eight-bit integer and 24-bit decimal.

Fabricated in TSMC 90 nm CMOS technology, the chip photo of MMD and test structure is shown in Figures 9 and 10. It occupies an area of 0.1063 mm^2, and the core MMD part area is 0.0091 mm^2. The power source of MMD and SPI is separated in order to avoid the noise from the digital modules. The power is provided by the external LDO chip. The MMD designed in the paper has been used in a Ka band fractional-N PLL and the PLL has been fabricated and measured. Agilent E8257D signal generator provides input signal of the MMD. Keysight N9030B signal analyzer is used to measure phase noise of PLL.

The measured sensitivity curve of different division ratio is shown in Figure 11a. Working range has a little difference with different division ratio. It can be seen from the figure that it can work with a common operating frequency ranges from 4.1 GHz to 9.2 GHz as the input power is 0 dBm.

The measured power consumption with a 9.5 GHz input signal at a division ratio of 164 is 13.8 mW, which contains the power consumption of $\Sigma - \Delta$ modulator. $\Sigma - \Delta$ modulator consumes most of power in the whole system. Simulation result of power consumption of MMD core is shown in Figure 11b.

The simulated power efficiency of the MMD is nearly a constant. The simulated power consumption and power efficiency of MMD with 9.5 GHz input and a division ratio of 164 is 2.88 mW and 3.1 GHz/mW. In the meanwhile, the simulated power consumption of the whole system is 13.22 mW. The simulated result has a similar result compared with the measured result. The simulated result of the power consumption of the MMD core is convincible.

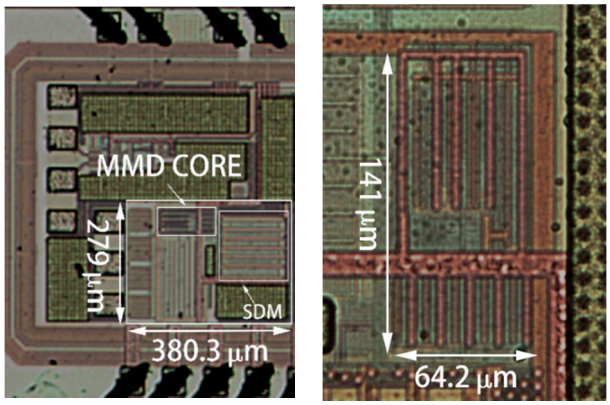


Figure 9. (**a**) Die micrograph of MMD, including Σ − Δ modulator and MMD core; (**b**) Die micrograph of MMD core.

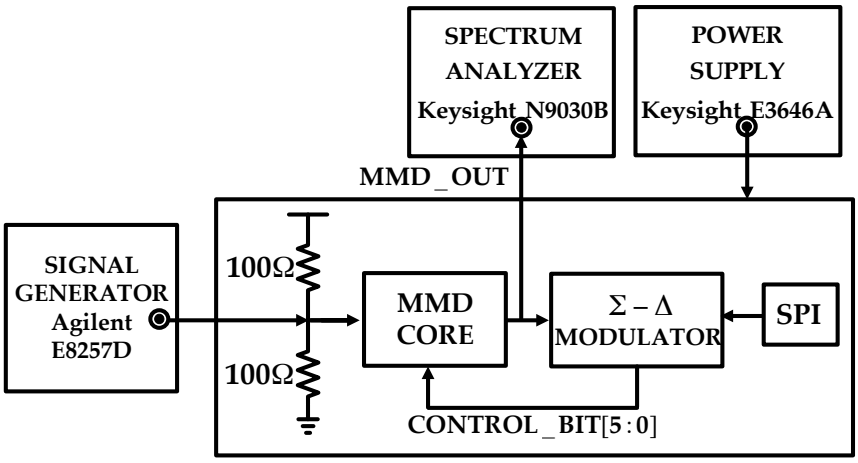


Figure 10. Test structure.

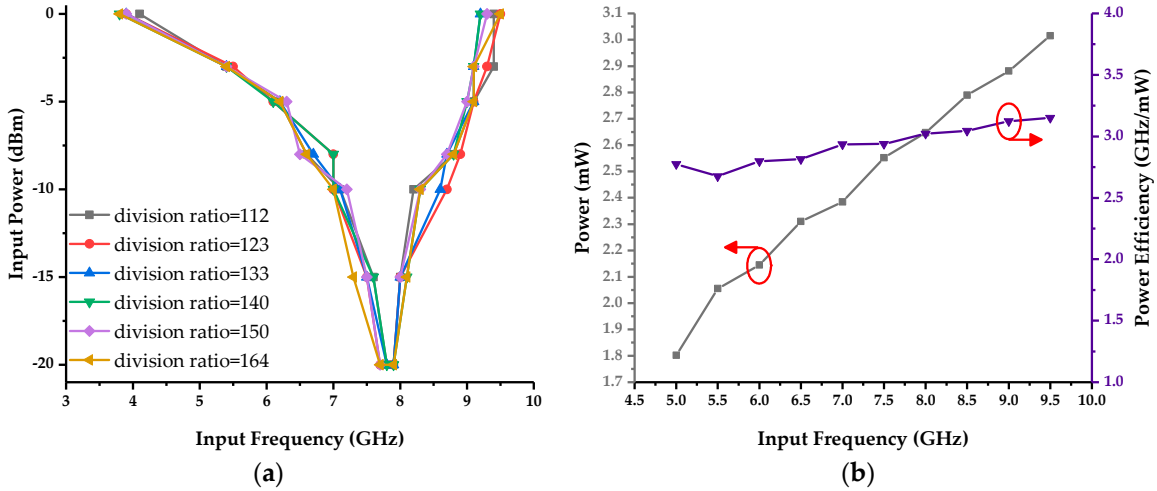


Figure 11. (**a**) Measured input sensitivity curve of MMD in different division ratio; (**b**) Simulated power and power efficiency of the proposed MMD.

The chip photo of the PLL of the architecture shown in Figure 1 with the designed MMD is presented in Figure 12. The amount of prescaler N is two. The prescalers provide a constant division ratio of 4. Figure 13 and Table 2 shows the phase noise of different output frequency and different

division ratios of the whole PLL system. The reference frequency of the PLL is 45 MHz. When PLL works at the frequency of 24.93 GHz, with a MMD division ratio of 138.5, phase noise at 1 MHz offset is −91.55 dBc/Hz. When the division ratio of MMD is an integer 139, the output frequency of PLL is 25.02 GHz, phase noise at 1 MHz offset is −97.14 dBc/Hz. It can be indicated that MMD can work well in the PLL systems.

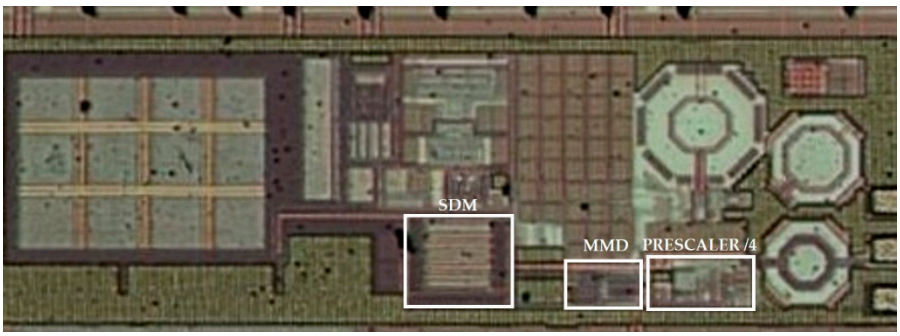
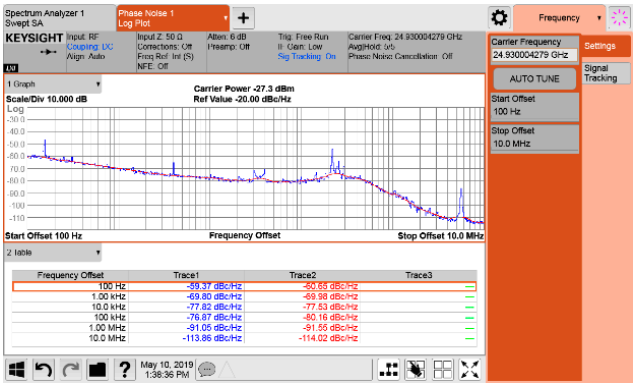


Figure 12. The die photograph of the PLL.



(**a**)

(**b**)

Figure 13. (**a**) Phase noise of PLL as the division ratio = 138.5; (**b**) Phase noise of PLL as the division ratio = 139.

Table 2. Phase noise of PLL different division ratios.

Frequency Offset	Division Ratio = 138.5	Division Ratio = 139
10 kHz	−77.82 dBc/Hz	−71.41 dBc/Hz
100 kHz	−78.87 dBc/Hz	−71.94 dBc/Hz
1 MHz	−91.05 dBc/Hz	−97.40 dBc/Hz

The comparison between the designed MMD and existing MMD is shown in the Table 3. As shown in table, the designed MMD has the higher operating frequency with a wide range of operating frequency compared with the previous work, and it achieves a low power design, which is more suitable in the mmW integrated circuit design.

Table 3. Comparison of the performance of the pervious works.

Parameter	This Work	[8]	[10]	[11]	[30]	[31]
Tech (nm)	90	65	130	180	90	65
Division-ratios	101–164	16–127	128–192	1–256	64–4096	24–80
Frequency range (GHz)	4.1–9.2	6 ***	2–3 *	2.3 ***	0.016–2	0.1–6.5
Power (mW)	2.88 * (13.8 **)	NA	NA	3.4	3.5	1
Power efficiency (GHz/mW)	3.1 * (0.69 **)	NA	NA	0.68	0.71	6.25
Area (mm^2)	0.0091	NA	NA	0.0372	NA	NA

* Simulated result of MMD. ** Measure result including $\Sigma - \Delta$ modulator. *** Only maximum operating frequency.

4. Conclusions

A high operating frequency, ultra-wide-band MMD is presented in this paper. Theoretical analysis of high operating frequency prescaler, counter P and counter S is presented in the paper. The proposed MMD is designed and fabricated in 90 nm CMOS technology. MMD core occupies an area of 0.0091 mm^2. The measured result shows that it can have an operating range from 4.1 GHz to 9.2 GHz, with a power efficiency of 3.1 GHz/mW, which satisfy the demand of low power and wide band in the modern communication systems.

Author Contributions: Conceptualization, Y.Z. and Z.C.; methodology, Y.Z. and Z.L.; validation, Y.Z. and Z.L.; writing—original draft preparation, Y.Z.; writing—review and editing, X.L. and Z.C.; supervision, Z.C. and X.W.; project administration, Z.C. and X.W.; funding acquisition, X.L. and Z.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by National Natural Science Foundation of China, grant number 61801027; China Postdoctoral Science Foundation, grant number 2018M631356; 111 Project of China, grant number B14010; Beijing Nova Program of Science and Technology, grant number Z191100001119078.

Conflicts of Interest: The authors declare no conflict of interest.

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