PLL Project

EECE Department

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Submitted to Eng. **Bassem Abdel-Aziz**

Submitted by:

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| --- | --- | --- |
| Name | section | BN |
| Abdel-Rahman Abdel-Azeem | 2 | 60 |
| Mohamed Mahmoud Gaber | 3 | 60 |
| Abdel-Rahman Ayman Mahmoud | 2 | 55 |
| Hisham Mohamed Abdullah | 4 | 51 |

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Simulation:

7-

Sinusoidal input with Frequency= Hz, initial phase= 0

VCO frequency =Hz, Kvco = Hz/v and BW=

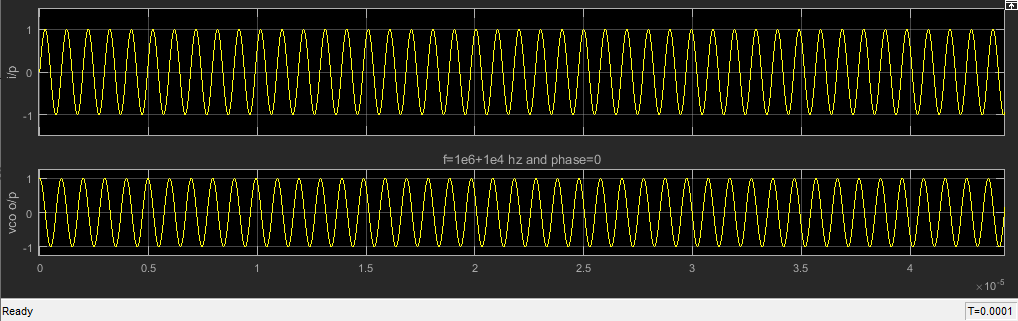


Figure 1: Input & Output part7

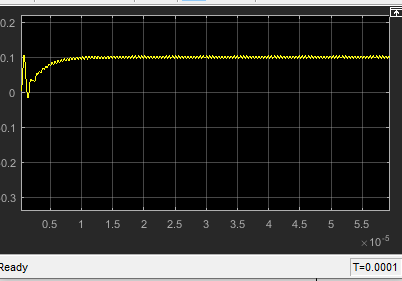


Figure 2: LPF output

8- Frequency = Hz

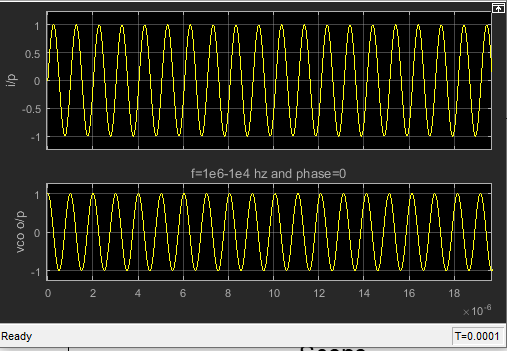


Figure 3: Input & Output part8

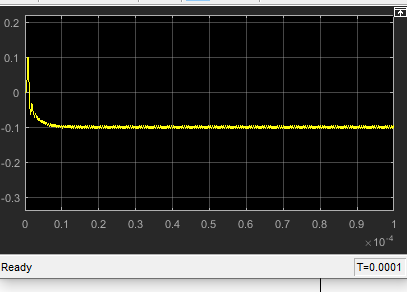


Figure 4: LPF output part 8

9 – Kvco =2\* Hz/v

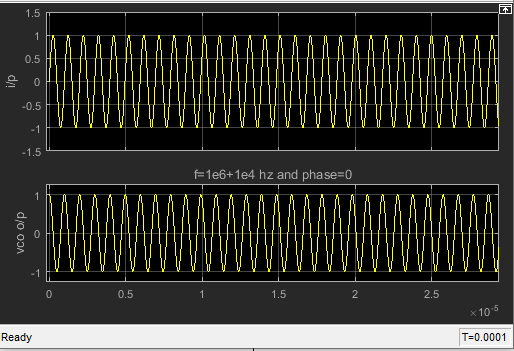


Figure 5: Input & Output part 9

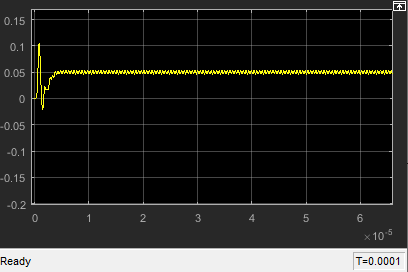


Figure 6: LPF output part 9

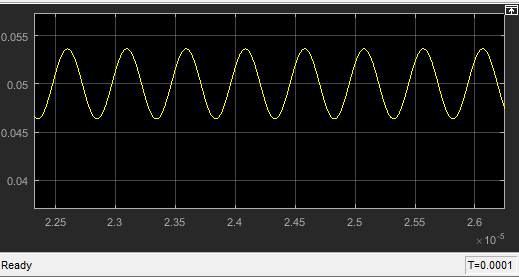


Figure 7 : ripples of part 9

Comments on 7-9:

Φe = ∆∅ = ∗ ∆𝑡

VCout = Kpd\* Φe

Wout= Wo+ Kvco\*VCout

* The behavior of the Filter in 7,8&9 🡪 it will settle at 0.1, -0.1 and 0.05 volts with some ripples.
* phase

Φe )7 = + ΔΦ

Φe )8 = - ΔΦ

Φe )9 = + ΔΦ/2

* increasing VCO gain will decrease SS value of filter as the filter will need less voltage to achieve required F lock

10- BW= Hz

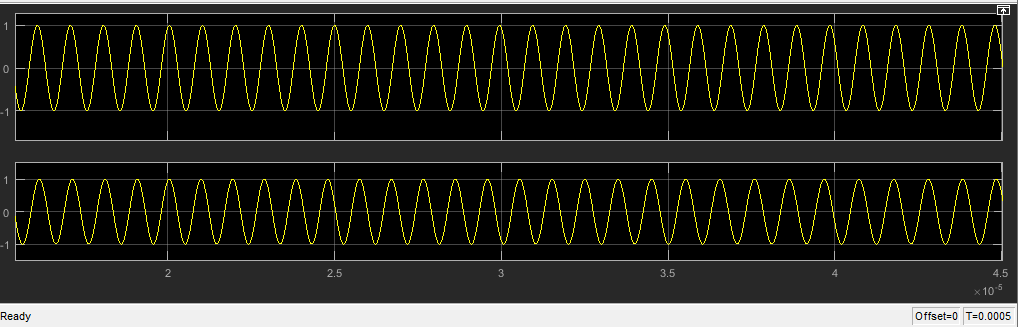


Figure 8: Input & Output part10

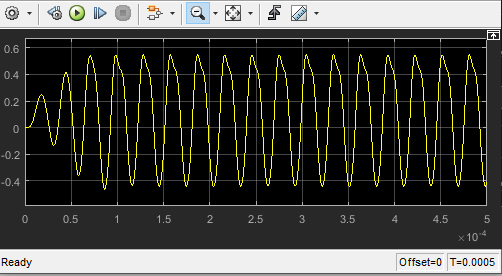


Figure 9: LPF output part 10

Comments:

* output doesn’t lock to the input.
* ζ if decreases 🡪 ζ increases, speed decreases 🡪 stability decreases.
* Vcout is critically stable
* Φe will be changed In a specific range.

11- frequency =HZ

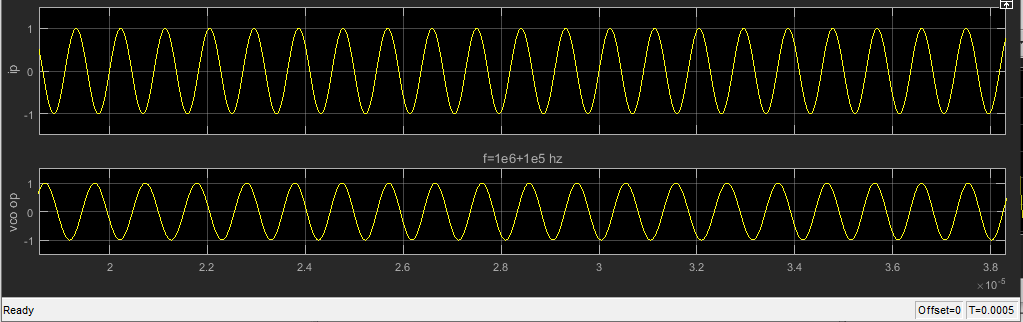


Figure 10: Input & Output part11

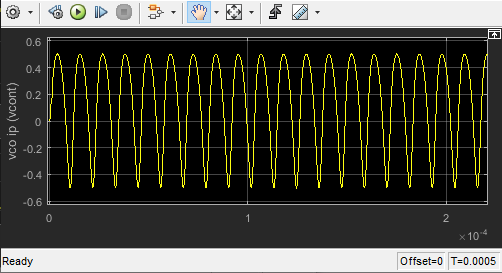


Figure 11: LPF output part11

Comments:

* Win= ( rad/s , the O/p of the filter will be oscillated without ripples at low time because of low frequency of Vcout.
* And this oscillates because the increase of ΔW 🡪 increase ΔVcout & ΔW > Wlpf