



Sunrise 3.0 (X3M)

Datasheet

Rev. 1.0

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
0.1	2019-12-10	Initial draft.
0.2	2020-02-02	Corrected JTG_TDI/SPI1_MOSI and JTG_TDO/SPI1_MISO.
0.3	2020-03-16	<ul style="list-style-type: none">Corrected typos.Added electrical characteristic data.
0.4	2020-03-30	<ul style="list-style-type: none">Corrected typos.Added Boot Strap Pins Definitions.
0.5	2020-04-23	<ul style="list-style-type: none">Corrected typos.Modified the MIPI Rx Port name to be consistent with the ball name.Updated BPU computing power information.
0.6	2020-05-21	<ul style="list-style-type: none">Added H.264 Supporting SVC-T description.Corrected IPU descriptions and block diagram.Updated I2S operating mode and supporting 64 KHz sampling rate.
0.7	2020-06-18	<ul style="list-style-type: none">Added the usage descriptions of MIPI CSI TX 8M@30fps for bypass and display path.Updated the CR5 cache size in the block diagram.Updated DDR4/LPDDR4 data rate.Corrected SIF descriptions.Updated thermal resistance parameter.
0.8	2020-07-20	<ul style="list-style-type: none">Added video codec/network interface description.Corrected SPI/Memory visibility typo.Corrected DDR pin list and DDR interface timing.Corrected ESD table.Corrected electrical specifications.
0.81	2020-08-24	Corrected IPU description.
0.9	2020-12-26	<ul style="list-style-type: none">In Table 2-32, updated the BIFSPI minimal



	<p>Cycle time value.</p> <ul style="list-style-type: none">Updated Figure 1-1 X3M Chip Block Diagram, Figure 1-2 Standalone as AP with Mono Camera and Figure 1-3 Standalone as AP with Multiple Cameras.In Table 2-4, updated pin attributes of SD0, SD1, SD2 and BT1120 OUT.In Table 2-7:<ul style="list-style-type: none">Updated the description of VDD_USB and added analog power supplies VP and VPH.Updated the maximum VDDQ_DDR power supply value.Updated the minimum VAA power supply value.Removed VAA_DDR.In Table 2-16:<ul style="list-style-type: none">Changed BP_DAT input leakage current to 50.Updated the typical values of RTT/ROnPu/RonPd.In Table 2-30, updated the Maximum Frequency/Cycle value of each speed mode.Updated Figure 3-1 Power Domain Block Diagram and Figure 3-2 Power Group Tree.In Section 3.2.3, added notes for BIFSPI_RSTN and BIFSD_RSTN below Table 3-2.In Table 3-2, added SW reset sources for DDRC module.In Table 3-3, updated J3 detailed power group information.In Table 3-7, added IRQ124 and IRQ 125.In Section 4.3.1.1, updated the total number of SPIs to 95.In Section 6.1.1:<ul style="list-style-type: none">Updated the introduction to MIPI CSI Host.Updated MIPI Host features.In Section 6.7.1, updated the introduction to IAR.
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		<ul style="list-style-type: none">In Section 6.8.1, updated the introduction to MIPI CSI Device.
0.91	2020-02-09	<ul style="list-style-type: none">In Table 1-3, updated DDR(2~4G) visibility for DMAC and SPAcc(M).Added Section 9.6 Lite PWM.In Table 2-10, updated the CDM value to 400.
1.0	2021-02-26	<ul style="list-style-type: none">Updated Figure 2-1 X3M FCBGA483 Package Outline.In 1.3 Features, updated MIPI CSI video input features.Added A.1 Reflow Profile.



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1 Overview

1.1 General Product Description

The Sunrise 3.0 (X3M) is a highly-integrated, high-performance and power-efficient artificial intelligence System-on-Chip (SoC) powered by Horizon Robotics. Based on the dual-core BPU with Bernoulli-architecture, X3M supports real-time pixel-level video segmentation, structured video analysis and attention-based vision perception. Video streams (max. resolution up to 8Mpixel@30fps) inputs from MIPI CSI-2 Receivers (Rx) or DVP are processed by the image signal processing (ISP) and video processing units before being passed to BPU for artificial intelligence inference computing such as video object detection, sentiment segmentation, scene parsing, etc.

The X3M SoC also integrates a quad-core Cortex A53 CPU, an image signal processing (ISP) unit for wide/high dynamic range (WDR or HDR) camera input images, video signal processing units supporting noise reduction (3DNR), lens distortion correction (LDC), rotation and scaling, H.265/H.264/MJPEG video codecs, a DDR controller for DDR4/LPDDR4/LPDDR4X, one USB 3.0 host/device dual-role module, a Gigabit Ethernet MAC with RMII/RGMII interface, video bypassing or display output interface, two I2S ports for audio or speech, other integrated on-chip modules and rich off-chip sensors or connectivity peripheral interfaces, which enable greater flexibility and faster delivery for customers to implement their own products for different kinds of targeted applications.

The X3M supports advanced perception capabilities and features that enable artificial intelligent Internet-of-Things (AIoT) functions, through precise detection, recognition and understanding of traffic participants and monitoring environments, including vehicles, pedestrians, human count, human shopping behavior statistics in store, face detection/recognition, car license plate recognition, etc.

Except of video/image artificial intelligence detections, segmentation and recognitions, the X3M BPU can also support intelligent speech algorithms like keyword spotting, speech recognition, text-to-speech and so on to make AIoT device more complete.

The advanced toolkit from Horizon Robotics provides a Linux-based training framework and development environment to assist customers in rapid application implementation and deployment. The BPU toolkit also supports floating point neural network model to fixed point neural network model conversion.

1.2 Chip Block Diagram

Figure 1-1 shows the chip-level functional block diagram of the X3M, providing a view of the major subsystems (CPU subsystem, BPU subsystem, DDR subsystem, VIO subsystem, VSP subsystem, PMU subsystem, peripheral interface, memories, etc.) and logical connectivity.

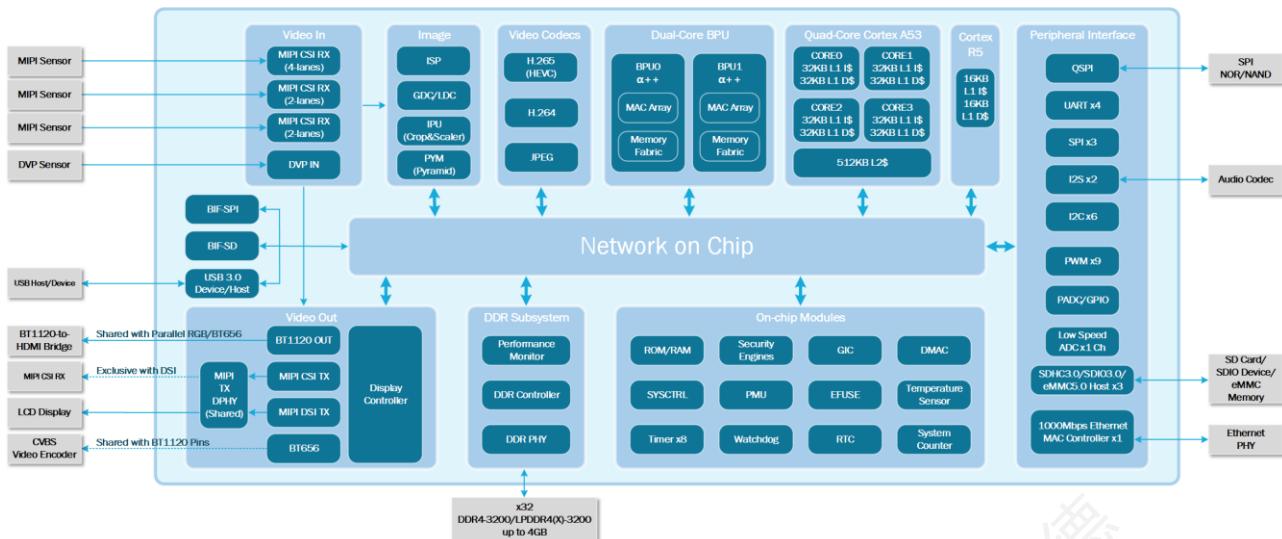


Figure 1-1 X3M Chip Block Diagram

1.3 Features

General

- TSMC 16nm FFC (FinFET Compact Technology) Process.
- FCBGA483 Package with 0.65 mm ball pitch, 15 mm x 15 mm body size.
- Operating temperature: -25 ~ 85 °C.
- Designed for different kinds of AIoT applications.

CPU

- Quad-core Arm® Cortex® A53, with 32 KB/32 KB L1 I/D and 512 KB L2 cache.
- Supports FPU and NEON.
- Separate VDD_CPU voltage domain.
- Typ. Operating Frequency: 1.2 GHz@ nominal VDD_CPU operating voltage.
- Max. Operating Frequency: 1.5GHz@ maximum VDD_CPU operating voltage.
- Supports Dynamic Voltage and Frequency Scaling (DVFS).
- Integrated GIC400 Interrupt Controller.
- CoreSight® debug and trace, including self-hosted debug.
- One Arm® Cortex® R5 is integrated to help off-load Cortex®A53 CPU loading.
 - 500MHz operating frequency with 16KB L1 I-cache and 16KB L1 D-cache.

BPU

- Dual-core Bernoulli-architecture BPU consisting of BPU0 and BPU1, capable of effective 5 Trillion operations per second (TOPS) computing performance on deep neural network inferences.
- Separate power domain for each core, VDD_CNN0 for BPU0, VDD_CNN1 for BPU1.
- Typical operation frequency: 1.0GHz@ nominal VDD_CNN0/1 operating voltage.



- Maximum operation frequency: 1.2GHz@ maximum VDD_CNN0/1 operating voltage.
- Supports Dynamic Voltage and Frequency Scaling (DVFS).
- Supports separate power-down for each core.
- Supports mainstream neural networks.
- Advanced toolkit supported by Horizon Robotics.

DDR

- Supports x32 off-chip DDR4/LPDDR4/LPDDR4X DRAM.
- Up to 4 GB capacity supported.
- Separate VDD_DDR voltage domain for DDR Controller and DDR PHY.
- Support DDR4 maximum speed up to DDR4-3200 MT/s.
- Support LPDDR4/LPDDR4X maximum speed up to LPDDR4-/LPDDR4X-3200 MT/s.
- Embedded performance monitor measuring bandwidth, latency, and other metrics on internal bus and DDR Controller, used for debug and performance optimization.

Video Input Interface

- Supports MIPI CSI video input:
 - 3 MIPI CSI Rx Ports: CSI-Rx1/3 (1 clock lane+4 data lanes), CSI-Rx0 (1 clock lane + 2 data lanes), and CSI-Rx2 (1 clock lane + 2 data lanes).
 - Up to 2.0Gbps per data lane, peak transmission rate of 8Gbps over four data lanes and 4Gbps over two data lanes.
 - Up to 4096 x 2160 pixels@30fps+ video input with limited video h-blank duration.
 - Supports RAW 8-/10-/12-/14-/16-bit format and 8-/10-bit YUV 422 format.
- Supports parallel DVP video input:
 - 12-bit data bus interface.
 - Input clock up to 160MHz.
 - Up to 1080P@30fps video input.
 - Supports RAW 8-/10-/12-bit format and 8-/10-bit YUV 422 format.
 - Supports 1.8V/3.3V input voltages signaling.
- Inserts Frame ID into input YUV 422 video stream to synchronize intelligent analysis results and video frames.
- Supports video in-to-out bypass:
 - MIPI CSI RX to MIPI CSI TX back-to-back bypass.
- Supports multi-camera video inputs through 3 MIPI CSI RX ports:
 - CSI-Rx1/3: 1 clock lane + 4 data lanes supports up to 4 virtual channels.
 - CSI-Rx0: 1 clock lane + 2 data lanes supports up to 2 virtual channels.
 - CSI-Rx2: 1 clock lane + 2 data lanes supports up to 2 virtual channels.



Image Signal Processing (ISP)

- Built-in Image Signal Processor (ISP) supporting RAW to YUV conversion.
- Supports High Dynamic Range (HDR) sensors:
 - Supports Digital Overlap (DOL) HDR sensor.
 - Supports linearized HDR sensors.
 - Supports native (on sensor) companded HDR sensors.
- Supports Auto-Exposure, Auto-White balance, and Auto-Focus (3A) histogram statistics.
- Supports Lens Shading Correction.
- Supports Defect Pixel Correction (DPC).
- Supports Spatial Noise Reduction.
- Supports Temporal Noise Reduction (3DNR).
- Supports Color Noise Reduction.
- Supports purple fringing Correction.
- Supports Lens Distortion Correction (LDC).
- Supports Crop from input image.
- Supports 3D Color Look-up Table (LUT).
- Supports RGB Sharpening and Edge Enhancement.
- Supports Gamma Correction.
- Lens GDC and Fisheye correction.
- ISP tuning tool on the PC.

Video/Image Processing Units

- Image Processing Unit (IPU):
 - Supports cropping and scaling, storing images into DDR in YUV420 semi-planar format.
 - Supports multi-camera division, cutting side-by-side images or de-multiplexing 6 virtual channels, storing images of each channel into DDR separately.
 - Supports on-screen display (OSD).
- Pyramid (PYM):
 - Input images from IPU (online mode) or from DDR (offline mode).
 - Input image size up to 8Mpixels.
 - Generates multi-layer pyramid images with various dimensions.
 - Configurable layers, Region of Interest (ROI), and scaling factors.

Video Output Interface

- Supports MIPI CSI TX video output:
 - 1 clock lane and up to 4 data lanes.
 - Supports up to 4 virtual channels.



- Up to 8Mpixels@30fps video output.
- Supports RAW 8-/10-/12-/14-/16-bit format and 8-/10-bit YUV 422 format.
- Supports MIPI DSI TX video output:
 - 1 clock lane and up to 4 data lanes.
 - Up to 1920x1080@60fps video output.
 - Supports 8-bit YUV 422 format.

Note:

MIPI CSI TX and DSI TX cannot work simultaneously due to sharing one MIPI TX DPHY.

- Supports parallel RGB video display output:
 - 24-bit (RGB888) or 16-bit (RGB565) data bus interface.
 - Output clock up to 148.5MHz.
 - Up to 1920x1080pixels@60fps video output.
- Supports BT1120 video output:
 - 16-bit data bus interface.
 - Output clock up to 148.5MHz.
 - Up to 1920x1080pixels@60fps video output.
 - Only 8-bit YUV 422 format.
- Supports BT656 video output:
 - 8-bit data bus interface.
 - Output clock up to 27MHz.
 - Up to 720x576@30fps video output for off-chip CVBS video encoder.
- Supports 1 User Interface (UI) layer alpha blending.

Video Codecs

- Supports H.265 (HEVC) encoding and decoding:
 - Main profile@L5.1.
 - Resolution up to 8Mpixels@30fps.
 - I/P/B Slices supported.
- Supports H.264 encoding and decoding:
 - Baseline/Main/High profiles@L5.1.
 - Resolution up to 8Mpixels@30fps.
 - H.264 supports SVC-T Encoding.
- H265/H264 encoding and decoding performance:
 - 3840 x 2160 @60fps encoding or decoding + 1280 x 720 @30fps encoding or decoding.
 - 4096 x 2160 @60fps encoding or decoding.
 - 3840 x 2160 @30fps encoding or decoding + 1920 x 1080 @30fps encoding or decoding + 1280 x 720 @30fps encoding or decoding.



- 3840 x 2160 @30fps encoding or decoding + 3840 x 2160 @30fps encoding or decoding.
- Up to a bit rate of 200 Mbit/s for H265/H264 encoding output.
- Supports JPEG Encoding and Decoding:
 - Baseline profile.
 - Resolution up to 16Mpixels.
- CBR, VBR, AVBR, FixQp and QpMap bit rate control modes supported.

Host Interfaces

- Transfer rate for AP SPI master up to 66 MHz using the BIF-SPI slave interface.
- Transfer mode for AP eMMC Host up to 8-wire HS200 mode (192 MB/s max) using the BIF-SD device interface.
- BIF-SPI and BIF-SD host interfaces used by Application Processor (AP) to access the X3M DDR, SRAM, and module registers for data exchange and control.
- USB 3.0 Host/Device dual-role SuperSpeed interface.

Network Interface

- One Gigabit Ethernet Interface:
 - The gigabit Ethernet is compliant with the following standards:
 - IEEE 1588-2008 for precision networked clock synchronization.
 - IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic.
 - IEEE 802.1Qbv-2015, 802.1Qbu-2016, and 802.1AS-Rev D5.0 for Time-Sensitive Networking (TSN).
 - RMII and RGMII interface for external Ethernet PHY.
 - 100Mbps half-duplexing or full-duplexing.
 - 1000Mbps full-duplexing.
 - TCP/UDP offload supported to reduce CPU loading.

Power Management

- Flexible clock switching, scaling and gating control.
- DVFS support for CPU and BPU.
- BPU0 and BPU1 shutting down respectively.
- Supports chip-level sleep mode for maximum power saving, only Always-On (AO) power domain active in sleep mode.
- Supports DDR IO retention in sleep mode, with DRAM in self-refresh state.

Peripheral Interfaces

- 4x UART:
 - 2-wire UART0/2/3.
 - 4-wire UART1 with hardware flow control.
 - Baud rate up to 921600 bps.
- 3x SPI:
 - Supports both master and slave modes.



- Up to 48 MHz.
- 2x I2S:
 - Supports both master and slave modes.
 - Half duplex for each, configured as RX or TX.
 - RX supporting 1/2/4/8/16-channel audio input.
 - TX supporting 1/2-channel audio output.
 - Supports 8/16/32/44.1/48/64 KHz sample rate.
 - Sample rates of I2S0 and I2S1 can be different.
- 6x I2C, only in master mode, up to 400Kbps.
- 9x PWM.
- 1x Lite PWM.
- 1x QSPI:
 - Only in master mode.
 - 1/2/4-wire mode, up to 83 MHz.
 - Mainly used to connect off-chip SPI NOR/NAND Flash.
- 3x SDIOs for SDHC3.0/SDIO3.0/eMMC5.0 Host Controller:
 - SD0 with 8-bit data bus. 1.8 V SDIO only.
 - SD1 with 4-bit data bus. Supports 3.3 V/1.8 V SDIO signaling.
 - SD2 with 4-bit data bus. Supports 3.3 V/1.8 V SDIO signaling.
 - Up to HS200 mode.
- All digital IOs can function as GPIO and can be selected as interrupt sources or wakeup sources, triggered by positive, negative, or both edges.
- Supports one channel low speed Lite-ADC:
 - 8-bit precision.
 - 1000SPS sampling rate.
 - Supports input voltage range: 0~1.0V.

Others

- Uses 24 MHz crystal oscillator as clock source.
- 32 KHz RTC clock input for low-power clock in sleep mode.
- Embedded PLLs providing clocks for all modules.
- 8 timers.
- Watchdog timer that triggers the entire chip reset in case of system crash.
- RTC timer that keeps running during sleep mode and can act as a wakeup source.
- Embedded EFUSE as chip ID.
- Embedded temperature sensor monitoring chip environment.
- DMAC gathering/scattering data within memories, such as DDR and SRAM.
- 64 KB on-chip SRAM shared by CPU, BIF-SPI, BIF-SD, and DMAC.



1.4 Application Scenarios

The X3M is highly-integrated System-on-Chip (SoC) that provides powerful intelligent perception capabilities and controls peripheral devices to accomplish specific tasks for different kinds of AIoT applications like Smart IP Camera, Human-Machine Interface devices, Interactive Robots, etc.

1.4.1 SoC as AP

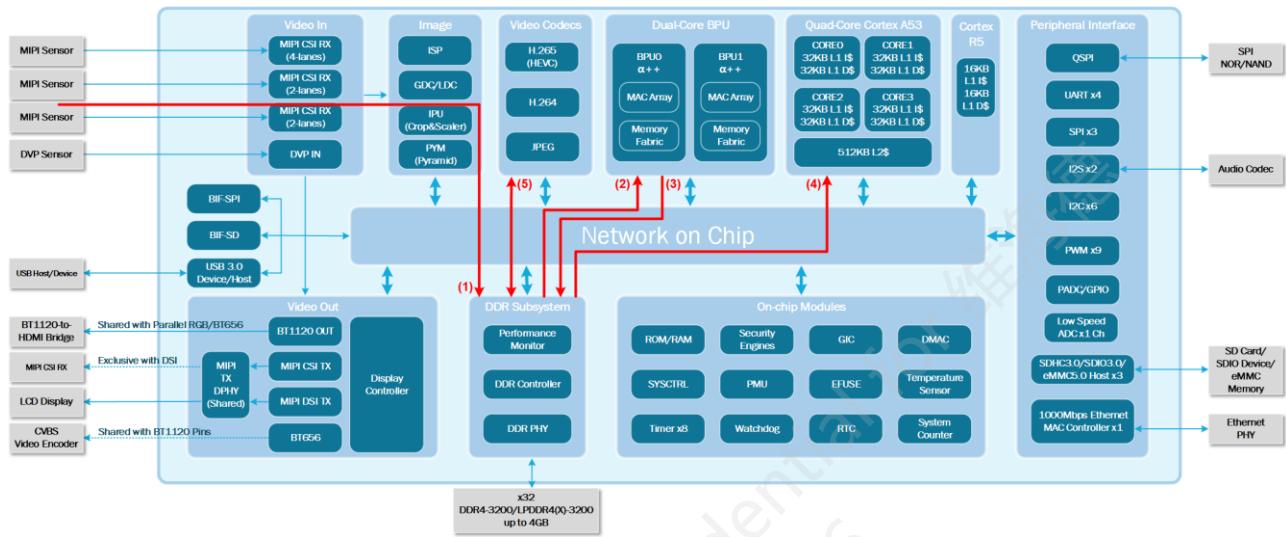


Figure 1-2 Standalone as AP with Mono Camera

In this scenario, a mono camera (the MIPI or DVP but not both) is connected to the X3M directly. The data paths are detailed as follows:

1. The input video stream is received through the MIPI CSI RX or DVP IN, then processed by ISP, IPU, and PYM, and finally stored into the DDR in YUV420 semi-planar format.
2. The BPU reads the images from the DDR and runs neural networks.
3. The BPU finally writes the analysis results into the DDR.
4. The CPU can implement further functions based on the intelligent analysis results.
5. The VPU (video codecs) encodes the input video in DDR and writes the stream to DDR.

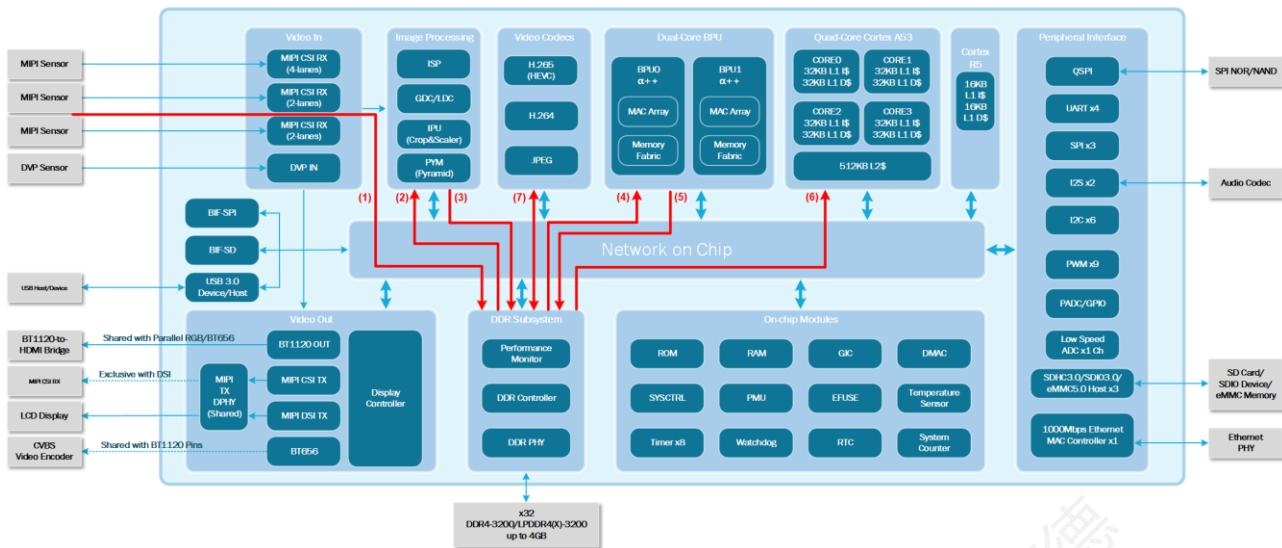


Figure 1-3 Standalone as AP with Multiple Cameras

In this scenario, an external sensor hub is required, which is used to connect the multiple cameras. The multi-camera input scenario datapath is as follows:

1. The multi-channels input video streams from sensor hub are received through the MIPI CSI RX, and SIF stores the multi-channels input video into DDR.
2. SIF reads the multi-channels video to ISP for image processing.
3. PIU processes the video streams processed by ISP and store the processed video into DDR.
4. The PYM reads the original images from the DDR to generate multi-layer pyramid images and then writes back (offline mode).
5. The BPU reads the original and pyramid images from the DDR and runs neural networks. The BPU finally writes the analysis results into the DDR.
6. The CPU can implement further functions based on the intelligent analysis results.
7. The VPU encodes the input video in DDR and writes the encoded streams to DDR.

1.5 Boot Mode

When power-up or wake-up from sleep mode, CPU starts executing the boot flow. The boot process can be divided into two stages, 1st boot and 2nd boot, which is introduced in the following sections.

1.5.1 1st Boot Mode

After the reset signal is released, CPU fetches its first instruction and starts the 1st boot stage. 1st boot mode includes on-chip ROM boot.



The procedure of the 1st boot stage is as follows:

1. Initialize the CPU itself and set up the running environment.
2. Switch the CPU and internal bus to higher frequency to speed up.
3. Initialize the necessary modules and peripherals.
4. Scan UART0 RX for the keyword "x2dbg" for 50 ms. If "x2dbg" detected, force to start booting from UART-XMODEM.
5. Obtain the selected 2nd boot mode from strap pins.
6. Load the 512INFO and 2nd boot firmware to on-chip SRAM.
7. Jump to SRAM and execute the 2nd boot firmware.

1.5.2 2nd Boot Mode

There are seven 2nd boot modes, including eMMC boot, SPI NAND boot, SPI NOR boot, USB boot, AP BIF-SPI boot, and UART-XMODEM boot. 1st boot program obtains the selected 2nd boot mode from strap pins and loads 512INFO and 2nd boot firmware from off-chip storage devices (like eMMC, SPI NAND or SPI NOR) or from communication interfaces (like BIF-SPI, USB or UART). Since the 2nd boot firmware is loaded from outside, it is programmable to minimize risks.

The procedure of the 2nd boot stage is as follows:

1. Start to run the 2nd boot firmware in on-chip SRAM.
2. Obtain the current boot reason from the PMU register.
3. Perform any of the following:
 - For the power-on boot, initialize the DDR Controller, DDR PHY and off-chip DRAM, execute the DDR data training, load the OS kernel image to DDR and run the firmware in DDR.
 - For the wake-up boot, restore the DDR Controller and DDR PHY parameters, exit from the DRAM self-refresh state, obtain the PC pointer held in the PMU register, and run the firmware in DDR.

1.5.3 Strap Pin Definitions

The X3M selects BT1120_OUT_CLK and BT1120_OUT_DAT[15:0] as strap pins. The strap pins are set to GPIO input mode at reset (RSTN = 0). When RSTN is released, the logic state of the strap pins will be latched into PADC registers, held stable until the reset signal RSTN becomes active again. During the reset the logic state of the strap pin chooses boot branches and options, as shown in [Table 1-1](#).

Please note that all these strap pins have built-in pull-down resistors in IO circuits, with default logic state of 0. If logic 1 is desired, connect stronger pull-up resistors on board. These pull-down/up resistors will not have impact on normal functions.

Table 1-1 Strap Pin Definition

Strap Pin	Share Pin	Default	Function
2NDBOOT_SEL	BT1120_OUT_DAT [2:0]	000	<p>2NDBOOT_SEL:</p> <p>000: 2nd BOOT from EMMC.</p> <p>001: 2nd BOOT from SPI FLASH(SPI NAND FLASH).</p> <p>010: 2nd BOOT from AP BIFSPI.</p> <p>011: 2nd BOOT from UART XMODEM.</p> <p>100: 2nd BOOT from USB, NORMAL BOOT.</p> <p>101: 2nd BOOT from SPI FLASH(SPI NOR FLASH).</p> <p>110: 2nd BOOT from USB with PROGRAMABLE BOOT.</p> <p>111: Reserved.</p> <p>Note:</p> <p>100 or 110 (USB BOOT or USB PROGRAM) will detect USB ID pin (GPIO[65], SD0_WPROT).</p> <p>0 (low): X3M is USB host, perform USB host operation</p> <p>1 (high): X3M is USB device, and boot from UART</p>
DEVICE_MODE	BT1120_OUT_DAT [3]	0	<p>If 2NDBOOT = EMMC:</p> <p>0= Uses negative-edge drive, positive-edge capture.</p> <p>1= Uses positive-edge drive, positive-edge capture.</p> <p>If 2NDBOOT=SPI NAND FLASH:</p> <p>0=2KB Page Size.</p> <p>1=4KB Page Size.</p> <p>If 2NDBOOT=SPI NOR FLASH:</p> <p>0=32bit address mode.</p> <p>1=24bit address mode.</p> <p>If 2NDBOOT=AP-BIFSPI/UART-XMODEM:</p> <p>0/1 = N/A.</p>
FASTBOOT_SEL	BT1120_OUT_DAT [5:4]	00	<p>Switches CPU clock frequency and internal bus clock frequency:</p> <p>00: cpu_clk=1.2G, ace_aclk=sys_noc_aclk=600M, sys_ap_aclk=400M, sys_pclk=cx_dbgclk=sif_mclk=300M.</p> <p>01: cpu_clk=600M, ace_aclk=sys_noc_aclk=300M, sys_ap_aclk=300M, sys_pclk=cx_dbgclk=sif_mclk=150M.</p> <p>10: cpu_clk=300M, ace_aclk=sys_noc_aclk=300M, sys_ap_aclk=300M,</p>

Strap Pin	Share Pin	Default	Function
			sys_pclk=cx_dbgclk=sif_mclk=150M. 11: No clock switch to high frequency (USB can't operate in this mode, USB needs sys_noc_aclk to run @60MHz or higher). cpu_clk=24M, ace_aclk=sys_noc_aclk=12M, sys_pclk=4.8MHz, sys_ap_aclk=cx_dbgclk=sif_mclk=8M.
UART_BAUD_RATE	BT1120_OUT_DAT [6]	0	UART0 baud rate for debug print and XMODEM transfer: 0: 921600bps. 1: 115200bps.
Reserved	BT1120_OUT_DAT [7]	0	Reserved
FORCE_LOAD_FLASH	BT1120_OUT_DAT [8]	0	When Warm boot: 0: Load SPL from SRAM. 1: Load SPL from flash/emmc/uart/bifspi/usb.
SPI_FLASH_RESET	BT1120_OUT_DAT [9]	0	If 2NDBOOT=SPI FLASH: 0: No reset. 1: Initiates a reset before accessing SPI NAND/NOR Flash.
DISABLE_WDOG	BT1120_OUT_DAT [10]	0	0: Enables Watchdog for clock switching, resets the entire chip when program runaway occurs. 1: Disables WatchDog.
SPI_NAND_RDI	BT1120_OUT_DAT [11]	0	If 2NDBOOT = SPI NAND: 0: Read ID command has dummy byte. 1: Read ID command has no dummy byte.
NAND_2PLANES	BT1120_OUT_DAT [12]	0	If 2NDBOOT = SPI NAND: 0: SPI NAND has only one plane and no plane select in 03H command. 1: SPI NAND has 2 planes and the plane select in 03H command.
Reserved	BT1120_OUT_DAT [13]	0	Reserved.
SKIP_CHECKSUM	BT1120_OUT_DAT [14]	0	Whether validate checksum: 0: Validates the checksum. 1: Ignores checksum (easy for debug).
SKIP_USB_FLESYS	BT1120_OUT_DAT [15]	0	0: USB pen drive with file system (FAT32). 1: USB pen drive without file system.

1.6 Memory Map

Table 1-2, Table 1-3 and Table 1-4 detail the memory map of the chip.

Table 1-2 Memory Map

Region	Start Address	End Address	Size
DDR	0x0000_0000	0x7FFF_FFFF	2 GB (Low)
	0x10000_0000	0x17FFF_FFFF	2 GB (High)
SRAM	0x8000_0000	0x8000_FFFF	64 KB
VIO_RAM	0x8020_0000	0x803F_FFFF	2 MB
IMI_RAM	0x8040_0000	0x8047_FFFF	512 KB
Reserved	0x8048_0000	0x8FFF_FFFF	-
GIC	0x9000_0000	0x9000_FFFF	64 KB
Reserved	0x9001_0000	0x9FFF_FFFF	-
APB Registers	0xA000_0000	0xAF00_FFFF	256 MB
QSPI Registers	0xB000_0000	0xB0FF_FFFF	16 MB
QSPI XIP	0xB100_0000	0xB1FF_FFFF	16 MB
USB	0xB200_0000	0xB20F_FFFF	1 MB
SPAcc	0xB210_0000	0xB210_FFFF	64 KB
Reserved	0xB211_0000	0xB2FF_FFFF	-
VIO_ISP	0xB300_0000	0xB303_FFFF	256 KB
Reserved	0xB304_0000	0xFFFFE_FFFF	-
ROM	0xFFFFE_0000	0xFFFF_FFFF	128 KB

Table 1-3 Memory Visibility

Region		Visibility							
		CPU	R5	BPU	BIFSPI	BIFSD	DMAC	USB(M)	SPAcc(M)
DDR	0~2G	✓	✓	✓	✓	✓	✓	✓	✓
	2~4G	✓	x	x	✓*	x	x	✓	x
SRAM		✓	✓	x	✓	✓	✓	✓	x
VIO_RAM		✓	✓	✓	✓	✓	✓	✓	✓
IMI_RAM		✓	✓	x	✓	x	✓	x	x
GIC		✓	✓	x	x	x	x	x	x
APB Registers		✓	✓	x	✓	✓	x	x	x



Region	Visibility							
	CPU	R5	BPU	BIFSPI	BIFSD	DMAC	USB(M)	SPAcc(M)
QSPI Registers	✓	✓	X	✓	✓	✓	✓	X
QSPI XIP	✓	✓	X	✓	✓	✓	✓	X
USB(S)	✓	✓	X	✓	✓	X	X	X
SPAcc(S)	✓	X	X	✓	X	X	X	X
VIO_ISP	✓	✓	X	✓	X	✓	X	X
ROM	✓	X	X	X	X	X	X	X

* BIFSPI/DMAC/SPAcc access higher 2G range of DDR via remap register setting.

Table 1-4 APB Register Map

Subsystem	Module	Register Space	Size
CPU Subsystem	CoreSight ROM Table	0xA000_0xxx	4 KB
	Cortex A53 Debug APB	0xA040_0000 ~ 0xA07F_FFFF	4 MB
	CXTSGEN	0xA080_xxxx	64 KB
	CXTPIU	0xA081_xxxx	64 KB
	CXCTI	0xA083_xxxx	64 KB
	CXATBREPLICATOR	0xA084_xxxx	64 KB
	CXATBFUNNEL	0xA085_xxxx	64 KB
	CXETB	0xA086_xxxx	64 KB
	Cortex R5 Debug APB	0xA09x_xxxx	1 MB
	SYSCTRL	0xA100_0xxx	4 KB
	Normal EFUSE	0xA100_1xxx	4 KB
	Timer Macro 0 with WatchDog	0xA100_2xxx	4 KB
	Timer Macro 1	0xA100_3xxx	4 KB
	Timer Macro 2	0xA100_4xxx	4 KB
	DMAC	0xA100_5xxx	4 KB
	BIFSPI	0xA100_6xxx	4 KB
	BIFSD	0xA100_7xxx	4 KB
	SPINLOCK	0xA100_Axxx	4 KB
	IPI	0xA100_Bxxx	4 KB
	DMAC_ISP	0xA100_Dxxx	4 KB



Subsystem	Module	Register Space	Size
	USB_PHY	0xA101_0000 ~ 0xA101_7FFF	32 KB
DDR Subsystem	DDR PHY	0xA200_0000 ~ 0xA2CF_FFFF	13 MB
	DDR Controller	0xA2D0_xxxx	64 KB
	Performance Monitor	0xA2D1_0xxx	4 KB
	DDRIO TEST CTRL	0xA2D2_0xxx	4 KB
BPU Subsystem	BPU0	0xA300_0xxx	4 KB
	BPU1	0xA300_1xxx	4 KB
VIO Subsystem	IPS	0xA400_0xxx	4 KB
	SIF	0xA400_1xxx	4 KB
	GDC_0	0xA401_xxxx	64 KB
	GDC_1	0xA402_xxxx	64 KB
	LDC	0xA403_0xxx	4 KB
	DWE_0	0xA403_4xxx	4 KB
	DWE_1	0xA403_5xxx	4 KB
	IPU	0xA404_0xxx	4 KB
	PYRAMID	0xA404_2xxx	4 KB
	VIO	0xA430_0xxx	4 KB
	IAR	0xA430_1xxx	4 KB
	MIPI CSI Host0	0xA435_0000 - 0xA435_07FF	2 KB
	MIPI CSI Host1	0xA435_1000 - 0xA435_17FF	2 KB
	MIPI CSI Host2	0xA435_0800 - 0xA435_0FFF	2 KB
	MIPI CSI Host3	0xA435_1800 - 0xA435_1FFF	2 KB
	MIPI CSI Device	0xA435_4xxx	4 KB
	MIPI DSI Host	0xA435_5xxx	4 KB
PERI Subsystem	UART0	0xA500_0xxx	4 KB
	UART1	0xA500_1xxx	4 KB
	UART2	0xA500_2xxx	4 KB
	UART3	0xA500_3xxx	4 KB
	SPI0	0xA500_4xxx	4 KB
	SPI1	0xA500_5xxx	4 KB
	SPI2	0xA500_6xxx	4 KB
	I2S0	0xA500_7xxx	4 KB



Subsystem	Module	Register Space	Size
I2C Subsystem	I2S1	0xA500_8xxx	4 KB
	I2C0	0xA500_9xxx	4 KB
	I2C1	0xA500_Axxx	4 KB
	I2C2	0xA500_Bxxx	4 KB
	I2C3	0xA500_Cxxx	4 KB
	PWM Macro 0	0xA500_Dxxx	4 KB
	PWM Macro 1	0xA500_Exxx	4 KB
	PWM Macro 2	0xA500_Fxxx	4 KB
	SD0	0xA501_0xxx	4 KB
	SD1	0xA501_1xxx	4 KB
	SD2	0xA501_2xxx	4 KB
	EMAC Host Controller	0xA501_4000 ~ 0xA501_5FFF	8 KB
	I2C4	0xA501_6xxx	4 KB
	I2C5	0xA501_7xxx	4 KB
	LPWM	0xA501_8xxx	4 KB
PMU Subsystem	PMU Controller	0xA600_0xxx	4 KB
	System Counter	0xA600_1xxx	4 KB
	RTC	0xA600_2xxx	4 KB
	PADC(GPIO)	0xA600_3xxx	4 KB
	PIN	0xA600_4xxx	4 KB
	SEC_REG	0xA600_8xxx	4 KB
NoC	APB Timeout Monitor	0xA700_0xxx	4 KB
VSP Subsystem	VPU	0xA800_xxxx	64 KB
	JPG	0xA801_xxxx	64 KB

1.7 Ordering Information

The production part numbers will be available from Horizon Robotics sales representative.



2 Hardware

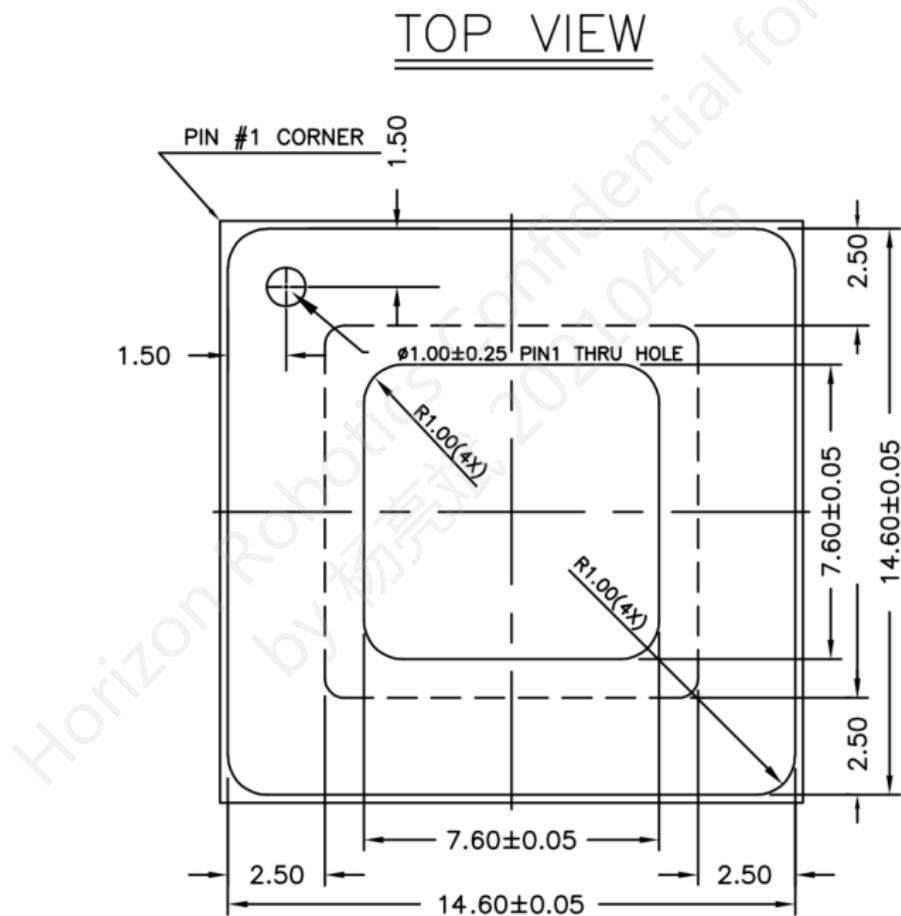
This chapter describes the hardware information in the following topics:

- [Package and Ball Map on page 32.](#)
- [Pin Description on page 45.](#)
- [Electrical Specifications on page 75.](#)
- [Interface Timings on page 90.](#)

2.1 Package and Ball Map

2.1.1 Package

The X3M uses the flip-chip BGA (FCBGA) package with 483 balls, 0.65 mm pitch and 15 mm x 15 mm size. [Figure 2-1](#) shows the Package Outline Dimensions (POD) of the X3M FCBGA483.



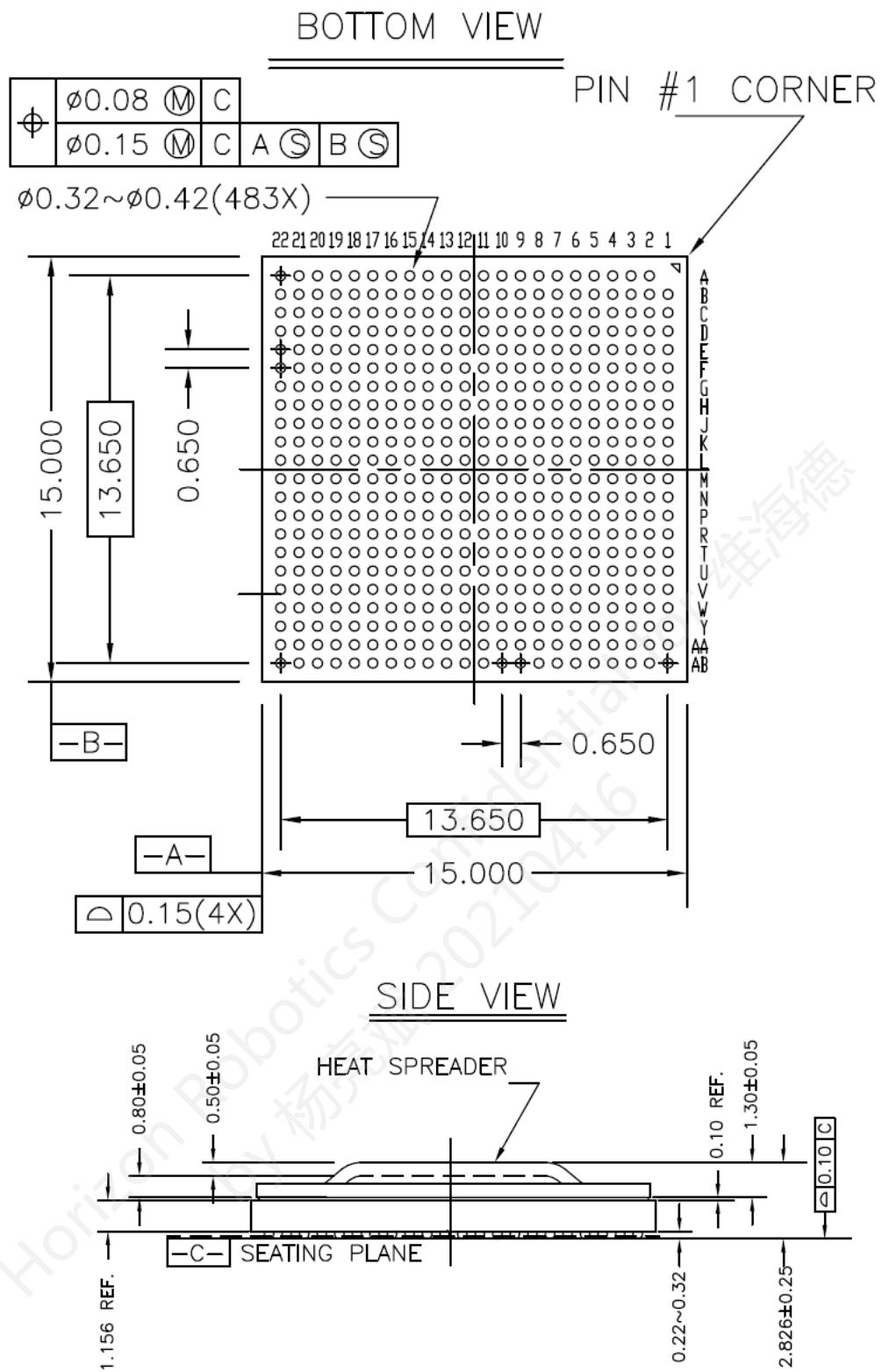


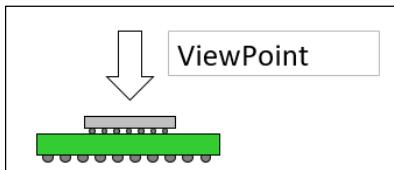
Figure 2-1 X3M FCBGA483 Package Outline

2.1.2 Ball Map

The FCBGA483 uses 483 (22 x 22) ball BGA with 12 blanks. Figure 2-2 to Figure 2-6



show the ball map for the X3M.



Index	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22			
A	NA 0_OUT _DATA7	BT112 0_OUT _DATA9	BT112 0_OUT _DATA1	BT112 0_OUT _DATA1	SD2_C ND	SD2_C LK	SD1_C ND	SD0_D ATA1	SD0_C ATA8	SD0_D ATA7	SD0_D ATA_S TRB	RGN1J _RX_C LK	RGN1J _TX_E N	VSS	BP_D1	BP_D9	BP_D0	VSS		A					
B	BT112 0_OUT _DATA8	BT112 0_OUT _DATA8	BT112 0_OUT _DATA1	BT112 0_OUT _DATA1	SD2_D ATA0	SD2_D ATA1	VSS	SD1_C LK	SD0_C ATA5	SD0_D ATA3	SD0_D ET_N	RGN1J _RXD0	RGN1J _TXD0	VSS	BP_D2	BP_D1 0	BP_D3	BP_D4		B					
C	BT112 0_OUT _DATA2	BT112 0_OUT _DATA5	BT112 0_OUT _DATA1	BT112 0_OUT _DATA1	SD2_D ATA3	SD2_D ATA2	SD1_D ATA1	SD1_D ATA2	VSS	SD0_D ATA4	SD0_H PROT	VSS	EPHY_C CLK	RGN1J _RXD01	RGN1J _RXD2	VSS	BP_D8	BP_D7	BP_D1 3	BP_D8	BP_D5	C			
D	BT112 0_OUT _DATA4	BT112 0_OUT _DATA1	BT112 0_OUT _DATA5	BT112 0_OUT _DATA7	BT112 0_VDD DDPST PST33	SD2_V 18	SD1_D ATA0	SD1_D ATA3	SD0_D ATA0	SD0_1 _VDDP ST18	SD0_D ATA2	ND10	MDCK	RGN1J _RXD3	RGN1J _RXD_Y	VSS	BP_D1 2	VSS	BP_D1 4	BP_D2 0	VSS	D			
E	B1FSD _GND _DATA0	B1FSD _DATA5	B1FSD _DATA7	B1FSD _DATA1	0_V DDPST 18	BT112 0_VDD DDPST PST33	VSS	SD1_V DDPST 18	SD1_V DDPST 33	SD0_V DDPST 33	SD0_V DDPST ST18	VDD_A 0	VDD_A 0	RGN1J _VDD DPST1 33	RGN1J _VDD DPST1 2	VSS	BP_D1 7	BP_D2 1	BP_D2 2	BP_D1 8	BP_A2	E			
F	B1FSD _CLK _DATA4	VSS	B1FSD _DATA3	B1FSD _DATA8	B1FSD _DATA0	B1FSD _VDD PST18	B1FSD _VDD PST18	SD2_V SD2_V 33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	BP_D1 9	BP_D1 8	VSS	BP_A1	BP_A0	F			
G	B1FSD _DATA2	B1FSD _DATA3	B1FSP _1_RST _N	B1FSP _1_VDD _1_CSN	B1FSP _1_VDD _1_CSN	B1FSP _1_VDD PST33	VSS	VSS	VSS	VDD_C NN1	VDD_C NN1	VDD_C NN1	VDD_C NN1	VSS	VSS	VSS	VSS	BP_D1 5	BP_A3	BP_A9	BP_A8	G			
H	B1FSD _RSTN _SDA	I2C3_SDA 1_N1S 0	B1FSP _1_NOS 1	I2C0_T33	I2C0_T33	VSS	VDD_C ORE_P D	VDD_C ORE_P D	VSS	VDD_C NN1	VDD_C NN1	VDD_C NN1	VDD_C NN1	VSS	VDD_D DR	VDDQ_DR	BP_A7	BP_A8	BP_A1 1	BP_A12		H			
J	VSS	I2C3_SCL K	SENSO R3_NC	I2C0_SDA LK	I2C0_SDA T18	VSS	VDD_C ORE_P D	VDD_C ORE_P D	VSS	VDD_C NN1	VDD_C NN1	VDD_C NN1	VDD_C NN1	VSS	VDD_D DR	VDDQ_DR	VSS	BP_A1 0	BP_A1 7	BP_A18		J			
K	RX0 _DATA	VSS	SENSO R2_NC	I2C2_SCL LK	I2C2_VDDPS T18	VSS	VSS	VDD_C ORE_P D	VDD_C ORE_P D	VDD_C ORE_P D	VDD_C ORE_P D	VDD_C ORE_P D	VDD_C ORE_P D	VSS	VDD_D DR	VDDQ_DR	BP_A1 4	BP_A1 3	BP_A5	BP_A4		K			
L	RX0 _DATA	RX0 _DATA	VSS	JTG_T DI	I2C2_SDA 33	VSS	VSS	VDD_C PU	VSS	VDD_C ORE_P D	VDD_C ORE_P D	VDD_C ORE_P D	VDD_C ORE_P D	VSS	VDD_D DR	VDDQ_DR	BP_VR EF	BP_A3 8	BP_A1 5	BP_NEN RESET_L		L			
M	RX0 _LKP	RX0 _DATA	VSS	JTG_T MS	JTG_T CK	JTG_T DO	VSS	VDD_C PU	VDD_C PU	VDD_C PU	VSS	VSS	VDD_C ORE_P D	VDD_C ORE_P D	VSS	VDD_D DR	VDDQ_DR	VSS	BP_ZN BP_A3 7	BP_ALE RT_N		M			
N	RX2_C LKP	RX0_C LKN	VSS	JTG_T RSTN	JTG_Y DDPST 33	VSS	VDD_C PU	VDD_C PU	VSS	VSS	VSS	VSS	VDD_C ORE_P D	VDD_C ORE_P D	VSS	VDD_D DR	VDDQ_DR	BP_A2 7	BP_A3 4	BP_A2 5	BP_A24		N		
P	RX2_D ATAP0	RX2_C LKN	VPH_N JP1	RX_RE XT	JTG_Y DDPST 18	VSS	VDD_C PU	VDD_C PU	VSS	VDD_C NN0	VDD_C NN0	VDD_C NN0	VDD_C NN0	VDD_C NN0	VDD_D DR	VDDQ_DR	VSS	BP_A3 0	BP_A2 0	BP_A2 0	BP_A21		P		
R	RX2_D ATAP0	RX2_D ATAM1	ATB_N JP1	TX_RE XT	VSS	VSS	VSS	VSS	VSS	VDD_C NN0	VDD_C NN0	VDD_C NN0	VDD_C NN0	VDD_C NN0	VDD_D DR	VDDQ_DR	BP_A2 6	BP_A3 3	BP_A3 1	BP_A32		R			
T	VSS	RX2_D ATAN0	VSS	VP_NJ P1	VSS	VSS	SYS_V DDPST	SYS_V DDPST	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ARNPL_L_VDD PST	VAA	VSS	BP_D2 8	BP_A2 2	BP_A2 9	BP_A28		T	
U	TX_CL KN	VSS	RX1_D ATAP1	RX1_D ATAN1	VSS	VSS	SYS_V DDPST	SYS_V DDPST	UART1 _RTSM	UART1 _CTSN	EFUSE _VDD	PVT_N DDA_T AVDD	VSS	VSS	ARNPL_L_VDD REF	ARNPL_L_VDD HV	VSS	BP_D2 5	BP_D2 4	VSS	BP_A3 5	BP_A38		U	
V	TX_DA TAN0	TX_CL KP	RX1_D ATAP0	RX1_D ATAN0	I2S1_NCLK	SENO_R0_NG LK	SENO_R1_NG LK	I2C1_SCL	I2C1_SDA	UART1 _TXD	PVT_A N_101	PVT_A N_100	VSS	VSS	VSS	VSS	BP_D2 6	BP_D3 3	BP_D4 4	BP_D2 7	BP_A23		V		
W	TX_DA TAN1	TX_DA LKP	RX1_C LKN	RX1_C LKN	I2S1_SD10	I2S0_NCLK	I2S0_LRCM	QSPJ_CSM1	QSPJ_HOLD 103	QSPJ_V JN_L0	PVT_V JN_L0	PVT_V JN_H	RESRE_F	VSS	VSS	VSS	BP_D3 1	VSS	BP_D2 9	BP_D3 2	VSS		W		
Y	TX_DA TAN2	TX_DA TAP1	NC	NC	SP10_CSN	I2S1_LRCK	I2S0_BCLK	I2S0_SD10	QSPJ_WP _102	QSPJ_V SLCK	EN_VD D_CNN 2	RSTN	VPH	NC	VSS	VP	VSS	BP_D4 4	BP_D3 8	BP_D3 0	BP_D3 7	BP_D38		Y	
AA	TX_DA TAN3	TX_DA TAP2	RX3_D ATAP1	RX3_D ATAN1	SP10_SCLK	X2A_W KUPIN N	X2A_J ROUT N	UART0 _RXD	QSPJ_N 101	EN_VD D_CNN 0	TEST NODE	ID	REF_P AD_CL K_N	DN	TX_P	RX_P	VSS	BP_D3 9	BP_D4 8	BP_D4 0	BP_D41		AA		
AB	VSS	TX_DA TAP3	RX3_D ATAP0	RX3_D ATAN0	SP10_N N10	MDT_R STOUT N	UART0 _TXD	QSPJ_N 100	X1_32_K	XO_24_N	XJ_24_N	VDD_U SB	REF_P AD_CL K_P	DP	TX_N	RX_N	VSS	BP_D4 3	BP_D4 5	BP_D4 2	VSS		AB		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22			

Figure 2-2 X3M FCBGA483 Ball Map



		Index	1	2	3	4	5	6	7	8	9	10	11
A		NA	BT1120_OUT_D_AT7	BT1120_OUT_D_AT9	BT1120_OUT_D_AT12	BT1120_OUT_D_AT15	SD2_CM_D	SD2_CL_K	SD1_CM_D	SD0_DA_TA1	SD0_CM_D	SD0_DA_TA6	
B		BT1120_OUT_D_AT3	BT1120_OUT_D_AT6	BT1120_OUT_D_AT8	BT1120_OUT_D_AT11	BT1120_OUT_D_AT14	SD2_DA_TA0	SD2_DA_TA1	VSS	SD1_CL_K	SD0_CL_K	SD0_DA_TA5	
C		BT1120_OUT_D_AT2	BT1120_OUT_D_AT5	BT1120_OUT_C_LK	BT1120_OUT_D_AT10	BT1120_OUT_D_AT13	SD2_DA_TA3	SD2_DA_TA2	SD1_DA_TA1	SD1_DA_TA2	VSS	SD0_DA_TA4	
D		BT1120_OUT_D_AT4	BT1120_OUT_D_AT1	BT1120_OUT_D_AT0	VSS	BT1120_2_VDD_PST18	BT1120_2_VDD_PST18	SD2_VD_TA0	SD1_DA_TA3	SD1_DA_TA0	SD0_DA_TA0	SD0_1_VDDPST_18	
E		BIFSD_CMD	BIFSD_DATA0	BIFSD_DATA5	BIFSD_DATA7	BT1120_0_VDD_PST18	BT1120_1_VDD_PST18	VSS	SD1_VD_DPST18	SD1_VD_DPST33	SD0_VD_DPST33	SD0_0_VDDPST_18	
F		BIFSD_CLK	BIFSD_DATA4	VSS	BIFSD DATA6	BIFSD0_VDDPS_T18	BIFSD1_VDDPS_T18	BIFSD2_VDDPS_T18	VSS	VSS	VSS	VSS	
G		BIFSD_DATA2	BIFSD_DATA3	BIFSPI_RSTN	BIFSPI_DATA1	BIFSPI_CS_N	BIFSPI_CS_N	BIFSPI_VDDPS_T33	VSS	VSS	VSS	VDD_CN_NT	
H		BIFSD_RSTN	I2C3_S_DA	BIFSPI_SCLK	BIFSPI_MISO	BIFSPI_MOSI	I2C0_V_DDPST3_3	VSS	VDD_CO_RE_PD	VDD_CO_RE_PD	VDD_CO_RE_PD	VDD_CO_NT	
J		VSS	I2C3_S_CL	SENSOR_3_MCLK	I2C0_S_CL	I2C0_S_DA	I2C0_V_DDPST1_8	VSS	VDD_CO_RE_PD	VDD_CO_RE_PD	VDD_CO_RE_PD	VSS	
K		RX0_D_ATAPI	VSS	SENSOR_2_MCLK	I2C2_S_CL	I2C2_V_DDPST3_3	I2C2_V_DDPST1_8	VSS	VDD_CO_RE_PD	VDD_CO_RE_PD	VDD_CO_RE_PD	VDD_CO_RE_PD	
L		RX0_D_ATAN1	RX0_D_ATAN1	VSS	JTG_TD_I	I2C2_S_DA	VSS	VSS	VDD_CO_U	VSS	VDD_CO_RE_PD	VDD_CO_RE_PD	

Figure 2-3 X3M FCBGA483 Ball Map (Top-Left Part)

12	13	14	15	16	17	18	19	20	21	22		
SD0_DA_TA7	SD0_DA_TA_STR_B	RGMII_RX_CLK	RGMII_TX01	RGMII_TX_CLK	RGMII_TX_EN	VSS	BP_D1	BP_D9	BP_D0	VSS	A	
SD0_DA_TA3	SD0_DE_T_N	RGMII_RXD0	RGMII_RXD0	RGMII_RXD2	RGMII_RXD3	VSS	BP_D2	BP_D10	BP_D3	BP_D4	B	
SD0_WP_ROT	VSS	EPHY_C_LK	RGMII_RXD1	RGMII_RXD2	VSS	BP_D8	BP_D7	BP_D13	BP_D6	BP_D5	C	
SD0_DA_TA2	MDIO	MDCK	RGMII_RXD3	RGMII_RX_DV	VSS	BP_D12	VSS	BP_D14	BP_D20	VSS	D	
VDD_AO	VDD_AO	RGMII_0_VDDPST33	RGMII_0_VDDPST33	RGMII_1_VDDPST18	RGMII_1_VDDPST18	VSS	BP_D17	BP_D21	BP_D22	BP_D16	BP_A2	E
VSS	VSS	VSS	VSS	VSS	VSS	BP_D19	BP_D18	VSS	BP_A1	BP_A0	F	
VDD_CN_NT	VDD_CN_NT	VDD_CN_NT	VSS	VSS	VSS	VSS	BP_D15	BP_A3	BP_A9	BP_A8	G	
VDD_CN_NT	VDD_CN_NT	VDD_CN_NT	VSS	VDD_DD_R	VSS	VDDQ_DR	BP_A7	BP_A6	BP_A11	BP_A12	H	
VSS	VSS	VSS	VSS	VDD_DD_R	VSS	VDDQ_DR	VSS	BP_A10	BP_A17	BP_A16	J	
VDD_CO_RE_PD	VDD_CO_RE_PD	VDD_CO_RE_PD	VSS	VDD_DD_R	VSS	VDDQ_DR	BP_A14	BP_A13	BP_A5	BP_A4	K	
VDD_CO_RE_PD	VDD_CO_RE_PD	VDD_CO_RE_PD	VSS	VDD_DD_R	VSS	VDDQLP	BP_VREF	BP_A38	BP_A15	BP_MEMRE_SET_L	L	

Figure 2-4 X3M FCBGA483 Ball Map (Top-Right Part)



M	RX0_C_LKP	RX0_D_ATAN_0	JTG_TM_S	JTG_TC_K	JTG_TD_O	VSS	VDD_C_P_U	VDD_C_P_U	VDD_C_P_U	VSS	VSS		
N	RX2_CL_KP	RX0_C_LKN	VSS	JTG_TR_STN	JTG_VD_DPST33	VSS	VDD_C_P_U	VDD_C_P_U	VSS	VSS	VSS		
P	RX2_DA_TAP1	RX2_CL_KN	VPH_MI_PI	RX_REX_T	JTG_VD_DPST18	VSS	VDD_C_P_U	VDD_C_P_U	VSS	VDD_C_N_0	VDD_C_N_0		
R	RX2_DA_TAPO	RX2_DA_TAN1	ATB_MI_PI	TX_REX_T	VSS	VSS	VSS	VSS	VSS	VDD_C_N_0	VDD_C_N_0		
T	VSS	RX2_DA_TANO	VSS	VP_MIP_I	VSS	VSS	SYS_VD_DPST	SYS_VD_DPST	VSS	VSS	VSS		
U	TX_CLK_N	VSS	RX1_DA_TAP1	RX1_DA_TAN1	VSS	VSS	SYS_VD_DPST	SYS_VD_DPST	UART1_RTTSN	UART1_CTSN	EFUSE_VDD		
V	TX_DAT_AN0	TX_CLK_P	RX1_DA_TAPO	RX1_DA_TAN0	I2S1_M_CLK	SENSOR_1_MCLK	SENSOR_0_MCLK	I2C1_S_CLK	I2C1_S_DA	UART1_RXD	UART1_TXD		
W	TX_DAT_AN1	TX_DAT_AP0	RX1_CLK_KP	RX1_CLK_KN	I2S1_S_DIO	I2S1_B_CLK	I2S0_M_CLK	I2S0_L_CLK	QSPI_C_SN1	QSPI_H_OLD_IO_3	QSPI_C_SN		
Y	TX_DAT_AN2	TX_DAT_AP1	NC	NC	SPI0_C_SN	I2S1_L_CLK	I2S0_B_CLK	I2S0_S_DIO	QSPI_W_P_IO2	QSPI_S_CLK	EN_VDD_CNN1		
AA	TX_DAT_AN3	TX_DAT_AP2	RX3_DA_TAP1	RX3_DA_TAN1	SPI0_S_CLK	X2A_WK_UPIN_N	X2A_IR_QOUT_N	UART0_RXD	QSPI_M_ISO_IO_1	EN_VDD_CORE	EN_VDD_CNN0		
AB	VSS	TX_DAT_AP3	RX3_DA_TAPO	RX3_DA_TAN0	SPI0_M_ISO	SPI0_M_WDT_RS	TOUT_N	UART0_RXD	QSPI_M_OSI_IO_0	XI_32K	XO_24M		
			1	2	3	4	5	6	7	8	9	10	11

Figure 2-5 X3M FCBGA483 Ball Map (Bottom-Left Part)

VDD_C_ORE_P_D	VDD_C_ORE_P_D	VSS	VDD_D_DR	VSS	VDDOL_P	VSS	BP_ZN	BP_A3_7	BP_ALE_RT_N	M		
VSS	VDD_C_ORE_P_D	VSS	VDD_D_DR	VSS	VDDOL_DR	BP_A2_7	BP_A3_4	BP_A2_5	BP_A24	N		
VDD_C_ORE_P_D	VDD_C_ORE_P_D	VSS	VDD_D_DR	VSS	VDDOL_DR	VSS	BP_A3_0	BP_A2_0	BP_A21	P		
VDD_C_ORE_P_D	VSS	VSS	VDD_D_DR	VSS	VDDOL_DR	BP_A2_8	BP_A3_3	BP_A3_1	BP_A32	R		
VSS	VSS	VSS	ARNPL_L_VDD_PST	VAA	VSS	BP_D2_8	BP_A2_2	BP_A2_9	BP_A28	T		
VSS	VSS	ARNPL_L_VDD_HV	ARNPL_L_VDD_REF	VSS	BP_D2_5	BP_D2_4	VSS	BP_A3_5	BP_A38	U		
PVT_A_N_100	VSS	VSS	VSS	VSS	BP_D2_3	BP_D3_3	BP_D3_4	BP_D2_7	BP_A23	V		
PVT_Y_IN_H0	RESREF	VSS	VSS	VSS	BP_D3_1	VSS	BP_D2_9	BP_D3_2	VSS	W		
VPH	NC	VSS	VP	VSS	BP_D4_4	BP_D3_8	BP_D3_0	BP_D3_7	BP_D38	Y		
ID	REF_P_AD_CL_K_N	DN	TX_P	RX_P	VSS	BP_D3_9	BP_D4_6	BP_D4_0	BP_D41	AA		
VDD_U_SB	REF_P_AD_CL_K_P	DP	TX_N	RX_N	VSS	BP_D4_3	BP_D4_5	BP_D4_2	VSS	AB		
		13	14	15	16	17	18	19	20	21	22	

Figure 2-6 X3M FCBGA483 Ball Map (Bottom-Right Part)



2.1.3 Pin List

Table 2-1 lists the pins alphabetically by ball number.

Table 2-1 Pin List

No.	Name	No.	Name
A1	NA	B1	BT1120_OUT_DAT3
A2	BT1120_OUT_DAT7	B2	BT1120_OUT_DAT6
A3	BT1120_OUT_DAT9	B3	BT1120_OUT_DAT8
A4	BT1120_OUT_DAT12	B4	BT1120_OUT_DAT11
A5	BT1120_OUT_DAT15	B5	BT1120_OUT_DAT14
A6	SD2_CMD	B6	SD2_DATA0
A7	SD2_CLK	B7	SD2_DATA1
A8	SD1_CMD	B8	VSS
A9	SD0_DATA1	B9	SD1_CLK
A10	SD0_CMD	B10	SD0_CLK
A11	SD0_DATA6	B11	SD0_DATA5
A12	SD0_DATA7	B12	SD0_DATA3
A13	SD0_DATA_STRB	B13	SD0_DET_N
A14	RGMII_RX_CLK	B14	RGMII_RXD0
A15	RGMII_TXD1	B15	RGMII_TXD0
A16	RGMII_TX_CLK	B16	RGMII_TXD2
A17	RGMII_TX_EN	B17	RGMII_TXD3
A18	VSS	B18	VSS
A19	BP_D1	B19	BP_D2
A20	BP_D9	B20	BP_D10
A21	BP_D0	B21	BP_D3
A22	VSS	B22	BP_D4
C1	BT1120_OUT_DAT2	D1	BT1120_OUT_DAT4
C2	BT1120_OUT_DAT5	D2	BT1120_OUT_DAT1
C3	BT1120_OUT_CLK	D3	BT1120_OUT_DAT0



No.	Name	No.	Name
C4	BT1120_OUT_DAT10	D4	VSS
C5	BT1120_OUT_DAT13	D5	BT1120_2_VDDPST18
C6	SD2_DATA3	D6	BT1120_VDDPST33
C7	SD2_DATA2	D7	SD2_VDDPST18
C8	SD1_DATA1	D8	SD1_DATA0
C9	SD1_DATA2	D9	SD1_DATA3
C10	VSS	D10	SD0_DATA0
C11	SD0_DATA4	D11	SD0_1_VDDPST18
C12	SD0_WPROT	D12	SD0_DATA2
C13	VSS	D13	MDIO
C14	EPHY_CLK	D14	MDCK
C15	RGMII_RXD1	D15	RGMII_RXD3
C16	RGMII_RXD2	D16	RGMII_RX_DV
C17	VSS	D17	VSS
C18	BP_D8	D18	BP_D12
C19	BP_D7	D19	VSS
C20	BP_D13	D20	BP_D14
C21	BP_D6	D21	BP_D20
C22	BP_D5	D22	VSS
E1	BIFSD_CMD	F1	BIFSD_CLK
E2	BIFSD_DATA0	F2	BIFSD_DATA4
E3	BIFSD_DATA5	F3	VSS
E4	BIFSD_DATA7	F4	BIFSD_DATA6
E5	BT1120_0_VDDPST18	F5	BIFSD0_VDDPST18
E6	BT1120_1_VDDPST18	F6	BIFSD1_VDDPST18
E7	VSS	F7	BIFSD_VDDPST33
E8	SD1_VDDPST18	F8	SD2_VDDPST33
E9	SD1_VDDPST33	F9	VSS



No.	Name	No.	Name
E10	SD0_VDDPST33	F10	VSS
E11	SD0_0_VDDPST18	F11	VSS
E12	VDD_AO	F12	VSS
E13	VDD_AO	F13	VSS
E14	RGMII_VDDPST33	F14	VSS
E15	RGMII_0_VDDPST18	F15	VSS
E16	RGMII_1_VDDPST18	F16	VSS
E17	VSS	F17	VSS
E18	BP_D17	F18	BP_D19
E19	BP_D21	F19	BP_D18
E20	BP_D22	F20	VSS
E21	BP_D16	F21	BP_A1
E22	BP_A2	F22	BP_A0
G1	BIFSD_DATA2	H1	BIFSD_RSTN
G2	BIFSD_DATA3	H2	I2C3_SDA
G3	BIFSD_DATA1	H3	BIFSPI_SCLK
G4	BIFSPI_RSTN	H4	BIFSPI_MISO
G5	BIFSPI_CSN	H5	BIFSPI_MOSI
G6	BIFSPI_VDDPST33	H6	I2C0_VDDPST33
G7	BIFSPI_VDDPST18	H7	VSS
G8	VSS	H8	VDD_CORE_PD
G9	VSS	H9	VDD_CORE_PD
G10	VSS	H10	VSS
G11	VDD_CNN1	H11	VDD_CNN1
G12	VDD_CNN1	H12	VDD_CNN1
G13	VDD_CNN1	H13	VDD_CNN1
G14	VDD_CNN1	H14	VDD_CNN1
G15	VSS	H15	VSS



No.	Name	No.	Name
G16	VSS	H16	VDD_DDR
G17	VSS	H17	VSS
G18	VSS	H18	VDDQ_DDR
G19	BP_D15	H19	BP_A7
G20	BP_A3	H20	BP_A6
G21	BP_A9	H21	BP_A11
G22	BP_A8	H22	BP_A12
J1	VSS	K1	RX0_DATAP1
J2	I2C3_SCL	K2	VSS
J3	SENSOR3_MCLK	K3	SENSOR2_MCLK
J4	I2C0_SCL	K4	I2C2_SCL
J5	I2C0_SDA	K5	I2C2_VDDPST33
J6	I2C0_VDDPST18	K6	I2C2_VDDPST18
J7	VSS	K7	VSS
J8	VDD_CORE_PD	K8	VSS
J9	VDD_CORE_PD	K9	VDD_CORE_PD
J10	VDD_CORE_PD	K10	VDD_CORE_PD
J11	VSS	K11	VDD_CORE_PD
J12	VSS	K12	VDD_CORE_PD
J13	VSS	K13	VDD_CORE_PD
J14	VSS	K14	VSS
J15	VSS	K15	VSS
J16	VDD_DDR	K16	VDD_DDR
J17	VSS	K17	VSS
J18	VDDQ_DDR	K18	VDDQ_DDR
J19	VSS	K19	BP_A14
J20	BP_A10	K20	BP_A13
J21	BP_A17	K21	BP_A5



No.	Name	No.	Name
J22	BP_A16	K22	BP_A4
L1	RX0_DATAP0	M1	RX0_CLKP
L2	RX0_DATAN1	M2	RX0_DATAN0
L3	VSS	M3	JTG_TMS
L4	JTG_TDI	M4	JTG_TCK
L5	I2C2_SDA	M5	JTG_TDO
L6	VSS	M6	VSS
L7	VSS	M7	VDD_CPU
L8	VDD_CPU	M8	VDD_CPU
L9	VSS	M9	VDD_CPU
L10	VDD_CORE_PD	M10	VSS
L11	VDD_CORE_PD	M11	VSS
L12	VDD_CORE_PD	M12	VDD_CORE_PD
L13	VDD_CORE_PD	M13	VDD_CORE_PD
L14	VDD_CORE_PD	M14	VDD_CORE_PD
L15	VSS	M15	VSS
L16	VDD_DDR	M16	VDD_DDR
L17	VSS	M17	VSS
L18	VDDQLP	M18	VDDQLP
L19	BP_VREF	M19	VSS
L20	BP_A38	M20	BP_ZN
L21	BP_A15	M21	BP_A37
L22	BP_MEMRESET_L	M22	BP_ALERT_N
N1	RX2_CLKP	P1	RX2_DATAP1
N2	RX0_CLKN	P2	RX2_CLKN
N3	VSS	P3	VPH_MIPI
N4	JTG_TRSTN	P4	RX_RECT
N5	JTG_VDDPST33	P5	JTG_VDDPST18



No.	Name	No.	Name
N6	VSS	P6	VSS
N7	VDD_CPU	P7	VDD_CPU
N8	VDD_CPU	P8	VDD_CPU
N9	VSS	P9	VSS
N10	VSS	P10	VDD_CNN0
N11	VSS	P11	VDD_CNN0
N12	VSS	P12	VDD_CNN0
N13	VSS	P13	VDD_CNN0
N14	VDD_CORE_PD	P14	VDD_CORE_PD
N15	VSS	P15	VSS
N16	VDD_DDR	P16	VDD_DDR
N17	VSS	P17	VSS
N18	VDDQ_DDR	P18	VDDQ_DDR
N19	BP_A27	P19	VSS
N20	BP_A34	P20	BP_A30
N21	BP_A25	P21	BP_A20
N22	BP_A24	P22	BP_A21
R1	RX2_DATAP0	T1	VSS
R2	RX2_DATAN1	T2	RX2_DATAN0
R3	ATB_MIPI	T3	VSS
R4	TX_REXT	T4	VP_MIPI
R5	VSS	T5	VSS
R6	VSS	T6	VSS
R7	VSS	T7	SYS_VDDPST
R8	VSS	T8	SYS_VDDPST
R9	VSS	T9	VSS
R10	VDD_CNN0	T10	VSS
R11	VDD_CNN0	T11	VSS



No.	Name	No.	Name
R12	VDD_CNN0	T12	VSS
R13	VDD_CNN0	T13	VSS
R14	VSS	T14	VSS
R15	VSS	T15	VSS
R16	VDD_DDR	T16	ARMPLL_VDDPST
R17	VSS	T17	VAA
R18	VDDQ_DDR	T18	VSS
R19	BP_A26	T19	BP_D28
R20	BP_A33	T20	BP_A22
R21	BP_A31	T21	BP_A29
R22	BP_A32	T22	BP_A28
U1	TX_CLKN	V1	TX_DATAN0
U2	VSS	V2	TX_CLKP
U3	RX1_DATAP1	V3	RX1_DATAP0
U4	RX1_DATAN1	V4	RX1_DATAN0
U5	VSS	V5	I2S1_MCLK
U6	VSS	V6	SENSOR1_MCLK
U7	SYS_VDDPST	V7	SENSOR0_MCLK
U8	SYS_VDDPST	V8	I2C1_SCL
U9	UART1_RTSN	V9	I2C1_SDA
U10	UART1_CTSN	V10	UART1_RXD
U11	EFUSE_VDD	V11	UART1_TXD
U12	PVT_VDDA_TAVDD	V12	PVT_AN_IO1
U13	VSS	V13	PVT_AN_IO0
U14	VSS	V14	VSS
U15	ARMPLL_VDDHV	V15	VSS
U16	ARMPLL_VDDREF	V16	VSS
U17	VSS	V17	VSS



No.	Name	No.	Name
U18	BP_D25	V18	BP_D26
U19	BP_D24	V19	BP_D33
U20	VSS	V20	BP_D34
U21	BP_A35	V21	BP_D27
U22	BP_A36	V22	BP_A23
W1	TX_DATAN1	Y1	TX_DATAN2
W2	TX_DATAP0	Y2	TX_DATAP1
W3	RX1_CLKP	Y3	NC
W4	RX1_CLKN	Y4	NC
W5	I2S1_SDIO	Y5	SPI0_CSN
W6	I2S1_BCLK	Y6	I2S1_LRCK
W7	I2S0_MCLK	Y7	I2S0_BCLK
W8	I2S0_LRCK	Y8	I2S0_SDIO
W9	QSPI_CSN1	Y9	QSPI_WP_IO2
W10	QSPI_HOLD_IO3	Y10	QSPI_SCLK
W11	QSPI_CSN	Y11	EN_VDD_CNN1
W12	PVT_VIN_LO	Y12	RSTN
W13	PVT_VIN_HI	Y13	VPH
W14	RESREF	Y14	NC
W15	VSS	Y15	VSS
W16	VSS	Y16	VP
W17	VSS	Y17	VSS
W18	BP_D31	Y18	BP_D44
W19	VSS	Y19	BP_D38
W20	BP_D29	Y20	BP_D30
W21	BP_D32	Y21	BP_D37
W22	VSS	Y22	BP_D36
AA1	TX_DATAN3	AB1	VSS



No.	Name	No.	Name
AA2	TX_DATAP2	AB2	TX_DATAP3
AA3	RX3_DATAP1	AB3	RX3_DATAP0
AA4	RX3_DATAN1	AB4	RX3_DATAN0
AA5	SPI0_SCLK	AB5	SPI0_MISO
AA6	X2A_WKUPIN_N	AB6	SPI0_MOSI
AA7	X2A_IRQOUT_N	AB7	WDT_RSTOUT_N
AA8	UART0_RXD	AB8	UART0_TXD
AA9	QSPI_MISO_IO1	AB9	QSPI_MOSI_IO0
AA10	EN_VDD_CORE	AB10	XI_32K
AA11	EN_VDD_CNN0	AB11	XO_24M
AA12	TEST_MODE	AB12	XI_24M
AA13	ID	AB13	VDD_USB
AA14	REF_PAD_CLK_M	AB14	REF_PAD_CLK_P
AA15	DM	AB15	DP
AA16	TX_P	AB16	TX_M
AA17	RX_P	AB17	RX_M
AA18	VSS	AB18	VSS
AA19	BP_D39	AB19	BP_D43
AA20	BP_D46	AB20	BP_D45
AA21	BP_D40	AB21	BP_D42
AA22	BP_D41	AB22	VSS

(1) NC_* means balls still exist but not connected.

(2) NA means balls are removed.

2.2 Pin Description

Table 2-2 lists the terms used for describing pin functions and features.

Table 2-2 Pin Symbol Description

Abbreviation	Description
I	Digital input



Abbreviation	Description
O	Digital output
IO	Digital input/output, controlled by software or function module
AI	Analog input
AO	Analog output
AIO	Analog input/output
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground
PD	With internal pull-down resistor
PU	With internal pull-up resistor
S	With Schmitt trigger feature
R	With output slew rate control feature

2.2.1 Power/Ground Pins

Table 2-3 Power/Ground Pin List

Pin Name	Number	Ball	Description
Digital Core Power			
VDD_AO	2	E12, E13	Always On domain core power 0.8 V ± 5%
VDD_CORE_PD	20	H8, H9, J8, J9, J10, K9, K10, K11, K12, K13, L10, L11, L12, L13, L14, M12, M13, M14, N14, P14	Shutdown domain core power 0.8 V ± 5%
VDD_CPU	8	L8, M7, M8, M9, N7, N8, P7, P8	Cortex A53 core power 1.2 GHz @ operating voltage 0.8 V ± 5% 1.5 GHz @ operating voltage 1 V ± 5%
VDD_DDR	8	H16, J16, K16 L16, M16, N16, P16, R16	DDR subsystem core power 3200 MT/s @ operating voltage 0.8 V + 5%, - 3%
VDD_CNN0	8	P10, P11	BPU0 core power

Pin Name	Number	Ball	Description
		P12, P13 R10, R11 R12, R13	1 GHz @ operating voltage 0.82 V ± 5% 1.2 GHz @ operating voltage 1V ± 5%
VDD_CNN1	8	G11, G12 G13, G14 H11, H12 H13, H14	BPU1 core power 1 GHz @ operating voltage 0.82 V ± 5% 1.2 GHz @ operating voltage 1V ± 5%
Digital IO Power			
SYS_VDDPST	4	T7, T8, U7, U8	General digital IO power
JTG_VDDPST33	1	N5	JTAG digital IO power
BIFSD_VDDPST33	1	F7	BIFSD digital IO power
BIFSPI_VDDPST33	1	G6	BIFSPI digital IO power
RGMII_VDDPST33	1	E14	RGMII digital IO power
BT1120_VDDPST33	1	D6	BT1120 OUT digital IO power
SD0_VDDPST33	1	E10	SD0 digital IO power
SD1_VDDPST33	1	E9	SD1 digital IO power
SD2_VDDPST33	1	F8	SD2 digital IO power
I2C0_VDDPST33	1	H6	I2C0/SENSOR2_MCLK/SENSOR3_MCLK digital IO power
I2C2_VDDPST33	1	K5	I2C/I3C digital IO power
VDDQ_DDR	6	H18, J18 K18, N18 P18, R18	DDR digital IO power
VDDQLP	2	L18, M18	DDR digital IO power
Analog Power			
ARMPPLL_VDDPST	1	T16	PLL digital supply voltage
ARMPPLL_VDDREF	1	U16	PLL digital supply voltage
ARMPPLL_VDDHV	1	U15	PLL analog supply voltage
VAA	1	T17	DDR PHY internal PLL analog power
VP_MIPI	1	T4	MIPI TX&RX PHY analog power
VPH_MIPI	1	P3	MIPI TX&RX PHY analog power
PVT_VDDA_TAVDD	1	U12	PVT sensor analog power
EFUSE_VDD	1	U11	EFUSE programming power



Pin Name	Number	Ball	Description	
VDD_USB	1	AB13	USB PHY power	
VP	1	Y16	USB PHY analog and digital low-voltage supply	
VPH	1	Y13	USB high-voltage supply for SuperSpeed operation	
Ground				
VSS	116	refer to ball map	Digital ground	

2.2.2 Digital Pins

2.2.2.1 Digital Pin List

Table 2-4 Digital Pin List

Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
Common					
TEST_MODE	AA12	I	PD	-	SYS_VDDPST
RSTN	Y12	I	PU/S	-	
XI_24M	AB12	CIN	CIN	-	
XO_24M	AB11	COUT	COUT	-	
XI_32K	AB10	CIN	S	-	
EN_VDD_CORE	AA10	IO	-	Config	
EN_VDD_CNN0	AA11	IO	-	Config	
EN_VDD_CNN1	Y11	IO	-	Config	
JTAG					
JTG_TCK	M4	IO	PD/S	Config	JTG_VDDPST33
JTG_TRSTN	N4	IO	PD/S	Config	
JTG_TMS	M3	IO	PU	Config	
JTG_TDI	L4	IO	PU	Config	
JTG_TDO	M5	IO	PU	Config	
BIFSPI					
BIFSPI_SCLK	H3	IO	PD/S	Config	BIFSPI_VDDPST33
BIFSPI_CSN	G5	IO	PU/S	Config	
BIFSPI_MOSI	H5	IO	PU	Config	



Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
BIFSPI_MISO	H4	IO	PU	Config	
BIFSPI_RSTN	G4	IO	PU/S	Config	
BIFSD					
BIFSD_CLK	F1	IO	PD/S	Config	BIFSD_VDDPST33
BIFSD_CMD	E1	IO	PU	Config	
BIFSD_DATA0	E2	IO	PU	Config	
BIFSD_DATA1	G3	IO	PU	Config	
BIFSD_DATA2	G1	IO	PU	Config	
BIFSD_DATA3	G2	IO	PU	Config	
BIFSD_DATA4	F2	IO	PU	Config	
BIFSD_DATA5	E3	IO	PU	Config	
BIFSD_DATA6	F4	IO	PU	Config	
BIFSD_DATA7	E4	IO	PU	Config	
BIFSD_RSTN	H1	IO	PU/S	Config	
QSPI					
QSPI_CSN	W11	IO	PU	Config	SYS_VDDPST
QSPI_CSN1	W9	IO	PU	Config	
QSPI_SCLK	Y10	IO	PU	Config	
QSPI_MOSI_IO0	AB9	IO	PU	Config	
QSPI_MISO_IO1	AA9	IO	PU	Config	
QSPI_WP_IO2	Y9	IO	PU	Config	
QSPI_HOLD_IO3	W10	IO	PU	Config	
EMAC					
EPHY_CLK	C14	IO	PD	Config	SYS_VDDPST
MDCK	D14	IO	PU	Config	
MDIO	D13	IO	PU	Config	
RGMII_RX_CLK	A14	IO	PD/S	Config	RGMII_VDDPST33
RGMII_RXD0	B14	IO	PD	Config	
RGMII_RXD1	C15	IO	PD	Config	
RGMII_RXD2	C16	IO	PD	Config	
RGMII_RXD3	D15	IO	PD	Config	
RGMII_RX_DV	D16	IO	PD	Config	



Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
RGMII_TX_CLK	A16	IO	PD	Config	
RGMII_TXD0	B15	IO	PD	Config	
RGMII_TXD1	A15	IO	PD	Config	
RGMII_TXD2	B16	IO	PD	Config	
RGMII_TXD3	B17	IO	PD	Config	
RGMII_TX_EN	A17	IO	PD	Config	
SD0					
SD0_CLK	B10	IO	PD	Config	SD0_VDDPST33
SD0_CMD	A10	IO	PU	Config	
SD0_DATA0	D10	IO	PU/S	Config	
SD0_DATA1	A9	IO	PU/S	Config	
SD0_DATA2	D12	IO	PU/S	Config	
SD0_DATA3	B12	IO	PU/S	Config	
SD0_DATA4	C11	IO	PU/S	Config	
SD0_DATA5	B11	IO	PU/S	Config	
SD0_DATA6	A11	IO	PU/S	Config	
SD0_DATA7	A12	IO	PU/S	Config	
SD0_DATA_STRB	A13	IO	PD/S	Config	
SD0_DET_N	B13	IO	PU/S	Config	SYS_VDDPST
SD0_WPROT	C12	IO	PD/S	Config	
SD1					
SD1_CLK	B9	IO	PD	Config	SD1_VDDPST33
SD1_CMD	A8	IO	PU	Config	
SD1_DATA0	D8	IO	PU/S	Config	
SD1_DATA1	C8	IO	PU/S	Config	
SD1_DATA2	C9	IO	PU/S	Config	
SD1_DATA3	D9	IO	PU/S	Config	
SD2					
SD2_CLK	A7	IO	PD	Config	SD2_VDDPST33
SD2_CMD	A6	IO	PU	Config	
SD2_DATA0	B6	IO	PU/S	Config	
SD2_DATA1	B7	IO	PU/S	Config	



Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
SD2_DATA2	C7	IO	PU/S	Config	
SD2_DATA3	C6	IO	PU/S	Config	
BT1120 OUT					
BT1120_OUT_CLK	C3	IO	PD/S	Config	BT1120_VDDPST33
BT1120_OUT_DAT0	D3	IO	PD	Config	
BT1120_OUT_DAT1	D2	IO	PD	Config	
BT1120_OUT_DAT2	C1	IO	PD	Config	
BT1120_OUT_DAT3	B1	IO	PD	Config	
BT1120_OUT_DAT4	D1	IO	PD	Config	
BT1120_OUT_DAT5	C2	IO	PD	Config	
BT1120_OUT_DAT6	B2	IO	PD	Config	
BT1120_OUT_DAT7	A2	IO	PD	Config	
BT1120_OUT_DAT8	B3	IO	PD	Config	
BT1120_OUT_DAT9	A3	IO	PD	Config	
BT1120_OUT_DAT10	C4	IO	PD	Config	
BT1120_OUT_DAT11	B4	IO	PD	Config	
BT1120_OUT_DAT12	A4	IO	PD	Config	
BT1120_OUT_DAT13	C5	IO	PD	Config	
BT1120_OUT_DAT14	B5	IO	PD	Config	
BT1120_OUT_DAT15	A5	IO	PD	Config	
UART0					
UART0_TXD	AB8	IO	PU	Config	SYS_VDDPST
UART0_RXD	AA8	IO	PU	Config	
UART1					
UART1_TXD	V11	IO	PU	Config	SYS_VDDPST
UART1_RXD	V10	IO	PU	Config	
UART1_RTSN	U9	IO	PU	Config	
UART1_CTSN	U10	IO	PU	Config	
SPI0					
SPI0_CSN	Y5	IO	PU	Config	SYS_VDDPST
SPI0_SCLK	AA5	IO	PU	Config	
SPI0_MOSI	AB6	IO	PU	Config	



Pin Name	Ball	I/O Type	Attribute	Drive	IO Power Domain
SPI0_MISO	AB5	IO	PU	Config	
I2S0					
I2S0_MCLK	W7	IO	PD	Config	SYS_VDDPST
I2S0_BCLK	Y7	IO	PD	Config	
I2S0_LRCK	W8	IO	PD	Config	
I2S0_SDIO	Y8	IO	PD	Config	
I2S1					
I2S1_MCLK	V5	IO	PD	Config	SYS_VDDPST
I2S1_BCLK	W6	IO	PD	Config	
I2S1_LRCK	Y6	IO	PD	Config	
I2S1_SDIO	W5	IO	PD	Config	
I2C0					
I2C0_SCL	J4	IO	PU	Config	I2C0_VDDPST33
I2C0_SDA	J5	IO	PU	Config	
I2C1					
I2C1_SCL	V8	IO	PU	Config	SYS_VDDPST
I2C1_SDA	V9	IO	PU	Config	
I2C2 / I2C3					
I2C2_SCL	K4	IO	PU	Config	I2C2_VDDPST
I2C2_SDA	L5	IO	PU	Config	
I2C3_SCL	J2	IO	PU	Config	
I2C3_SDA	H2	IO	PU	Config	
MISC					
SENSOR2_MCLK	K3	IO	PD	Config	I2C0_VDDPST33
SENSOR3_MCLK	J3	IO	PD	Config	
SENSOR0_MCLK	V7	IO	PD	Config	SYS_VDDPST
SENSOR1_MCLK	V6	IO	PD	Config	
WDT_RSTOUT_N	AB7	IO	PU	Config	
X2_WKUPIN_N	AA6	IO	PU/S	Config	
X2_IRQOUT_N	AA7	IO	PU	Config	

- (1) The PU/S attribute means having both features.
- (2) Some power pins and analog pins are included for clear grouping.

2.2.2.2 Digital Pin Multiplexing

The X3M SoC has a lot of functionalities but a limited number of pins. Even though a single pin can only perform one function at a time, they can be configured internally to perform different functions. [Table 2-5](#) details the pin multiplexing configuration for each pin.

Table 2-5 Digital Pin Multiplexing

Pin Name	Mux	Functions	Default Dir	Dir	Description
TEST_MODE	NA	TEST_MODE	I	I	Chip mode selection: 0 = Function mode 1 = Test mode for ATE
RSTN	NA	RSTN	I	I	Chip global reset, low active
XI_24M	NA	XI_24M	I	I	24 M crystal input
XO_24M	NA	XO_24M	O	O	24 M crystal output
XI_32K	NA	XI_32K	I	I	32 K external input
EN_VDD_COR_E	0	EN_VDD_CORE	O	O	Output control to enable/disable shutdown domain powers, default
	3	GPIO0[0]/GPIO[0]	-	IO	GPIO
EN_VDD_CNN0	0	EN_VDD_CNN0	O	O	Output control to enable/disable VDD_CNN0 power supply, default
	3	GPIO0[1]/GPIO[1]	-	IO	GPIO
EN_VDD_CNN1	0	EN_VDD_CNN1	O	O	Output control to enable/disable VDD_CNN1 power supply, default
	3	GPIO0[2]/GPIO[2]	-	IO	GPIO
JTG_TCK	0	JTG_TCK	I	I	JTAG or SWD clock input, default
	1	SPI1_SCLK	-	O	SPI1 master clock output
	3	GPIO0[3]/GPIO[3]	-	IO	GPIO
JTG_TRSTN	0	JTG_TRSTN	I	I	JTAG reset input, low active, default
	2	PWM0	-	O	PWM0 waveform output
	3	GPIO0[4]/GPIO[4]	-	IO	GPIO
JTG_TMS	0	JTG_TMS	I	IO	JTAG mode selection or SWD data input or output, default
	1	SPI1_CSN	-	O	SPI1 master chip select output
	3	GPIO0[5]/GPIO[5]	-	IO	GPIO



Pin Name	Mux	Functions	Default Dir	Dir	Description
JTG_TDI	0	JTG_TDI	I	I	JTAG data input, default
	1	SPI1_MOSI	-	O	SPI1 master data output
	3	GPIO0[6]/GPIO[6]	-	IO	GPIO
JTG_TDO	0	JTG_TDO	O	O	JTAG data output, default
	1	SPI1_MISO	-	I	SPI1 master data input
	3	GPIO0[7]/GPIO[7]	-	IO	GPIO
BIFSPI_CSN	0	BIFSPI_CSN	I	I	BIFSPI slave chip select input, default
	3	GPIO1[11]/GPIO[27]	-	IO	GPIO
BIFSPI_SCLK	0	BIFSPI_SCLK	I	I	BIFSPI slave clock input, default
	3	GPIO1[12]/GPIO[28]	-	IO	GPIO
BIFSPI_MOSI	0	BIFSPI_MOSI	I	I	BIFSPI slave data input, default
	3	GPIO1[13]/GPIO[29]	-	IO	GPIO
BIFSPI_MISO	0	BIFSPI_MISO	O	O	BIFSPI slave data output, default
	3	GPIO1[14]/GPIO[30]	-	IO	GPIO
BIFSPI_RSTN	0	BIFSPI_RSTN	I	I	BIFSPI slave reset input, default
	3	GPIO1[15]/GPIO[31]	-	IO	GPIO
BIFSD_CLK	0	BIFSD_CLK	I	I	BIFSD device clock input, default
	2	RGB_VSYNC	-	O	RGB interface VSYNC output
	3	GPIO1[4]/GPIO[20]	-	IO	GPIO
BIFSD_CMD	0	BIFSD_CMD	I	IO	BIFSD device command input and response output, default
	2	RGB_HSYNC	-	O	RGB interface HSYNC output
	3	GPIO1[5]/GPIO[21]	-	IO	GPIO
BIFSD_DATA0	0	BIFSD_DATA0	I	IO	BIFSD device data input or output, default
	1	PWM1	-	O	PWM1 waveform output



Pin Name	Mux	Functions	Default Dir	Dir	Description
	2	RGB_DAT16	-	O	RGB interface data output
	3	GPIO1[6]/GPIO[2 2]	-	IO	GPIO
BIFSD_DATA1	0	BIFSD_DATA1	I	IO	BIFSD device data input or output, default
	1	PWM2	-	O	PWM2 waveform output
	2	RGB_DAT17	-	O	RGB interface data output
	3	GPIO1[7]/GPIO[2 3]	-	IO	GPIO
BIFSD_DATA2	0	BIFSD_DATA2	I	IO	BIFSD device data input or output, default
	1	PWM3	-	O	PWM3 waveform output
	2	RGB_DAT18	-	O	RGB interface data output
	3	GPIO1[8]/GPIO[2 4]	-	IO	GPIO
BIFSD_DATA3	0	BIFSD_DATA3	I	IO	BIFSD device data input or output, default
	1	PWM4	-	O	PWM4 waveform output
	2	RGB_DAT19	-	O	RGB interface data output
	3	GPIO1[9]/GPIO[2 5]	-	IO	GPIO
BIFSD_DATA4	0	BIFSD_DATA4	I	IO	BIFSD device data input or output, default
	1	LPWM0	-	I	Lite PWM0 output
	2	RGB_DAT20	-	O	RGB interface DE output
	3	GPIO7[4]/GPIO[1 16]	-	IO	GPIO
BIFSD_DATA5	0	BIFSD_DATA5	I	IO	BIFSD device data input or output, default
	1	LPWM1	-	O	Lite PWM1 output
	2	RGB_DAT21	-	O	RGB interface data output
	3	GPIO7[5]/GPIO[1 17]	-	IO	GPIO
BIFSD_DATA6	0	BIFSD_DATA6	I	IO	BIFSD device data input or output, default



Pin Name	Mux	Functions	Default Dir	Dir	Description
	1	LPWM2	-	O	Lite PWM2 output
	2	RGB_DAT22	-	O	RGB interface data output
	3	GPIO7[6]/GPIO[18]	-	IO	GPIO
BIFSD_DATA7	0	BIFSD_DATA7	I	IO	BIFSD device data input or output, default
	1	LPWM3	-	O	Lite PWM3 output
	2	RGB_DAT23	-	O	RGB interface data output
	3	GPIO7[7]/GPIO[19]	-	IO	GPIO
BIFSD_RSTN	0	BIFSD_RSTN	I	I	BIFSD device reset input, default
	1	PPS_TRIGGER_IN	-	I	PPS trigger input
	2	RGB_DE	-	O	RGB interface DE output
	3	GPIO1[10]/GPIO[26]	-	IO	GPIO
QSPI_CS_N	0	QSPI_CS_N	O	O	QSPI master chip select output, default
	3	GPIO2[0]/GPIO[32]	-	IO	GPIO
QSPI_CS_N1	0	QSPI_CS_N1	O	O	QSPI master chip select output 1, default
	1	SPI0_CS_N1	-	O	SPI0 master chip select output 1
	3	GPIO7[8]/GPIO[120]	-	IO	GPIO
QSPI_SCLK	0	QSPI_SCLK	O	O	QSPI master clock output, default
	3	GPIO2[1]/GPIO[33]	-	IO	GPIO
QSPI_MOSI_IO_0	0	QSPI_MOSI_IO0	O	IO	QSPI master data output or data input or output in dual/quad-wire mode, default
	3	GPIO2[2]/GPIO[34]	-	IO	GPIO
QSPI_MISO_IO_1	0	QSPI_MISO_IO1	I	IO	QSPI master data input or data input or output in dual/quad-wire mode, default



Pin Name	Mux	Functions	Default Dir	Dir	Description
	3	GPIO2[3]/GPIO[35]	-	IO	GPIO
QSPI_WP_IO2	0	QSPI_WP_IO2	O	IO	QSPI write protect output control or data input or output in quad-wire mode, default
	3	GPIO2[4]/GPIO[36]	-	IO	GPIO
QSPI_HOLD_IO3	0	QSPI_HOLD_IO3	O	IO	QSPI hold output control or data input or output in quad-wire mode, default
	3	GPIO2[5]/GPIO[37]	-	IO	GPIO
EPHY_CLK	0	EPHY_CLK	-	O	25MHz clock output to external EPHY
	3	GPIO2[6]/GPIO[38]	I	IO	GPIO, default
MDCK	0	MDCK	-	O	MDIO I/F clock output to EPHY
	3	GPIO2[7]/GPIO[39]	I	IO	GPIO, default
MDIO	0	MDIO	-	IO	MDIO I/F data input or output with EPHY
	3	GPIO2[8]/GPIO[40]	I	IO	GPIO, default
RGMII_RX_CLK	0	RGMII_RX_CLK	-	I	RGMII RX clock input from EPHY
	3	GPIO2[9]/GPIO[41]	I	IO	GPIO, default
RGMII_RXD0	0	RGMII_RXD0	-	I	RGMII RX data from EPHY
	3	GPIO2[10]/GPIO[42]	I	IO	GPIO, default
RGMII_RXD1	0	RGMII_RXD1	-	I	RGMII RX data from EPHY
	3	GPIO2[11]/GPIO[43]	I	IO	GPIO, default
RGMII_RXD2	0	RGMII_RXD2	-	I	RGMII RX data from EPHY
	3	GPIO2[12]/GPIO[44]	I	IO	GPIO, default
RGMII_RXD3	0	RGMII_RXD3	-	I	RGMII RX data from EPHY



Pin Name	Mux	Functions	Default Dir	Dir	Description
	3	GPIO2[13]/GPIO[45]	I	IO	GPIO, default
RGMII_RX_DV	0	RGMII_RX_DV	-	I	RGMII RX data valid from EPHY
	3	GPIO2[14]/GPIO[46]	I	IO	GPIO, default
RGMII_TX_CLK	0	RGMII_TX_CLK	-	O	RGMII TX clock output to EPHY
	3	GPIO2[15]/GPIO[47]	I	IO	GPIO, default
RGMII_TXD0	0	RGMII_TXD0	-	O	RGMII TX data to EPHY
	3	GPIO3[0]/GPIO[48]	I	IO	GPIO, default
RGMII_TXD1	0	RGMII_TXD1	-	O	RGMII TX data to EPHY
	3	GPIO3[1]/GPIO[49]	I	IO	GPIO, default
RGMII_TXD2	0	RGMII_TXD2	-	O	RGMII TX data to EPHY
	3	GPIO3[2]/GPIO[50]	I	IO	GPIO, default
RGMII_TXD3	0	RGMII_TXD3	-	O	RGMII TX data to EPHY
	3	GPIO3[3]/GPIO[51]	I	IO	GPIO, default
RGMII_TX_EN	0	RGMII_TX_EN	-	O	RGMII TX data enable to EPHY
	3	GPIO3[4]/GPIO[52]	I	IO	GPIO, default
SD0_CLK	0	SD0_CLK	-	O	SD0 host clock output
	3	GPIO3[5]/GPIO[53]	I	IO	GPIO, default
SD0_CMD	0	SD0_CMD	-	IO	SD0 host command output and response input
	3	GPIO3[6]/GPIO[54]	I	IO	GPIO, default
SD0_DATA0	0	SD0_DATA0	-	IO	SD0 host data input or output
	3	GPIO3[7]/GPIO[55]	I	IO	GPIO, default
SD0_DATA1	0	SD0_DATA1	-	IO	SD0 host data input or output
	3	GPIO3[8]/GPIO[5]	I	IO	GPIO, default



Pin Name	Mux	Functions	Default Dir	Dir	Description
		6]			
SD0_DATA2	0	SD0_DATA2	-	IO	SD0 host data input or output
	3	GPIO3[9]/GPIO[57]	I	IO	GPIO, default
SD0_DATA3	0	SD0_DATA3	-	IO	SD0 host data input or output
	3	GPIO3[10]/GPIO[58]	I	IO	GPIO, default
SD0_DATA4	0	SD0_DATA4	-	IO	SD0 host data input or output
	3	GPIO3[11]/GPIO[59]	I	IO	GPIO, default
SD0_DATA5	0	SD0_DATA5	-	IO	SD0 host data input or output
	3	GPIO3[12]/GPIO[60]	I	IO	GPIO, default
SD0_DATA6	0	SD0_DATA6	-	IO	SD0 host data input or output
	3	GPIO3[13]/GPIO[61]	I	IO	GPIO, default
SD0_DATA7	0	SD0_DATA7	-	IO	SD0 host data input or output
	3	GPIO3[14]/GPIO[62]	I	IO	GPIO, default
SD0_DATA_ST RB	0	SD0_DATA_STR B	-	I	SD0 host data strobe input
	3	GPIO3[15]/GPIO[63]	I	IO	GPIO, default
SD0_DET_N	0	SD0_DET_N	-	I	SD0 host card detection input
	3	GPIO4[0]/GPIO[64]	I	IO	GPIO, default
SD0_WPROT	0	SD0_WPROT	-	I	SD0 host write protection input
	3	GPIO4[1]/GPIO[65]	I	IO	GPIO, default
SD1_CLK	0	SD1_CLK	-	O	SD1 host clock output
	3	GPIO4[2]/GPIO[66]	I	IO	GPIO, default
SD1_CMD	0	SD1_CMD	-	IO	SD1 host command output and response input
	3	GPIO4[3]/GPIO[6]	I	IO	GPIO, default

Pin Name	Mux	Functions	Default Dir	Dir	Description
		7]			
SD1_DATA0	0	SD1_DATA0	-	IO	SD1 host data input or output
	3	GPIO4[4]/GPIO[6 8]	I	IO	GPIO, default
SD1_DATA1	0	SD1_DATA1	-	IO	SD1 host data input or output
	3	GPIO4[5]/GPIO[6 9]	I	IO	GPIO, default
SD1_DATA2	0	SD1_DATA2	-	IO	SD1 host data input or output
	3	GPIO4[6]/GPIO[7 0]	I	IO	GPIO, default
SD1_DATA3	0	SD1_DATA3	-	IO	SD1 host data input or output
	3	GPIO4[7]/GPIO[7 1]	I	IO	GPIO, default
SD2_CLK	0	SD2_CLK	-	O	SD2 host clock output
	3	GPIO4[8]/GPIO[7 2]	I	IO	GPIO, default
SD2_CMD	0	SD2_CMD	-	IO	SD2 host command output and response input
	3	GPIO4[9]/GPIO[7 3]	I	IO	GPIO, default
SD2_DATA0	0	SD2_DATA0	-	IO	SD2 host data input or output
	3	GPIO4[10]/GPIO[74]	I	IO	GPIO, default
SD2_DATA1	0	SD2_DATA1	-	IO	SD2 host data input or output
	3	GPIO4[11]/GPIO[75]	I	IO	GPIO, default
SD2_DATA2	0	SD2_DATA2	-	IO	SD2 host data input or output
	3	GPIO4[12]/GPIO[76]	I	IO	GPIO, default
SD2_DATA3	0	SD2_DATA3	-	IO	SD2 host data input or output
	3	GPIO4[13]/GPIO[77]	I	IO	GPIO, default
BT1120_OUT_C_LK	0	BT1120_OUT_CLK / BT656_OUT_CLK	-	O	BT1120 output clock or BT656 output clock



Pin Name	Mux	Functions	Default Dir	Dir	Description
	1	DVP_IN_PCLK	-	I	DVP input clock
	2	RGB_CLK / TRACE_CLK	-	O	RGB interface output clock or CoreSight trace clock output or debug monitor clock output
	3	GPIO4[14]/GPIO[78]	I	IO	GPIO, default
BT1120_OUT_D AT0	0	BT1120_OUT_DA T0 / BT656_DAT0	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_VSYNC	-	I	DVP input vsync
	2	RGB_DAT0 / TRACE_DATA0	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO4[15]/GPIO[79]	I	IO	GPIO, default
BT1120_OUT_D AT1	0	BT1120_OUT_DA T1 / BT656_DAT1	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_HSYNC	-	I	DVP input hsync
	2	RGB_DAT1 / TRACE_DATA1	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[0]/GPIO[80]	I	IO	GPIO, default
BT1120_OUT_D AT2	0	BT1120_OUT_DA T2 / BT656_DAT2	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA0	-	I	DVP input data
	2	RGB_DAT2 / TRACE_DATA2	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[1]/GPIO[81]	I	IO	GPIO, default
BT1120_OUT_D AT3	0	BT1120_OUT_DA T3 / BT656_DAT3	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA1	-	I	DVP input data
	2	RGB_DAT3 / TRACE_DATA3	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output



Pin Name	Mux	Functions	Default Dir	Dir	Description
	3	GPIO5[2]/GPIO[8 2]	I	IO	GPIO, default
BT1120_OUT_D AT4	0	BT1120_OUT_DA T4 / BT656_DAT4	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA2	-	I	DVP input data
	2	RGB_DAT4 / TRACE_DATA4	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[3]/GPIO[8 3]	I	IO	GPIO, default
BT1120_OUT_D AT5	0	BT1120_OUT_DA T5 / BT656_DAT5	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA3	-	I	DVP input data
	2	RGB_DAT5 / TRACE_DATA5	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[4]/GPIO[8 4]	I	IO	GPIO, default
BT1120_OUT_D AT6	0	BT1120_OUT_DA T6 / BT656_DAT6	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA4	-	I	DVP input data
	2	RGB_DAT6 / TRACE_DATA6	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[5]/GPIO[8 5]	I	IO	GPIO, default
BT1120_OUT_D AT7	0	BT1120_OUT_DA T7 / BT656_DAT7	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA5	-	I	DVP input data
	2	RGB_DAT7 / TRACE_DATA7	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[6]/GPIO[8 6]	I	IO	GPIO, default
BT1120_OUT_D AT8	0	BT1120_OUT_DA T8 / BT656_DAT8	-	O	BT1120 output data or BT656 output data



Pin Name	Mux	Functions	Default Dir	Dir	Description
	1	DVP_IN_DATA6	-	I	DVP input data
	2	RGB_DAT8 / TRACE_DATA8	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[7]/GPIO[8 7]	I	IO	GPIO, default
BT1120_OUT_D AT9	0	BT1120_OUT_DA T9 / BT656_DAT9	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA7	-	I	DVP input data
	2	RGB_DAT9 / TRACE_DATA9	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[8]/GPIO[8 8]	I	IO	GPIO, default
BT1120_OUT_D AT10	0	BT1120_OUT_DA T10 / BT656_DAT9	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA8	-	I	DVP input data
	2	RGB_DAT10 / TRACE_DATA10	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[9]/GPIO[8 9]	I	IO	GPIO, default
BT1120_OUT_D AT11	0	BT1120_OUT_DA T11 / BT656_DAT11	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA9	-	I	DVP input data
	2	RGB_DAT11 / TRACE_DATA11	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[10]/GPIO[90]	I	IO	GPIO, default
BT1120_OUT_D AT12	0	BT1120_OUT_DA T12 / BT656_DAT12	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA10	-	I	DVP input data



Pin Name	Mux	Functions	Default Dir	Dir	Description
	2	RGB_DAT12 / TRACE_DATA12	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[11]/GPIO[91]	I	IO	GPIO, default
BT1120_OUT_D AT13	0	BT1120_OUT_DA T13 / BT656_DAT13	-	O	BT1120 output data or BT656 output data
	1	DVP_IN_DATA11	-	I	DVP input data
	2	RGB_DAT13 / TRACE_DATA13	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[12]/GPIO[92]	I	IO	GPIO, default
BT1120_OUT_D AT14	0	BT1120_OUT_DA T14 / BT656_DAT14	-	O	BT1120 output data or BT656 output data
	2	RGB_DAT14 / TRACE_DATA14	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[13]/GPIO[93]	I	IO	GPIO, default
BT1120_OUT_D AT15	0	BT1120_OUT_DA T15 / BT656_DAT15	-	O	BT1120 output data or BT656 output data
	2	RGB_DAT15 / TRACE_DATA15	-	O	RGB interface output data or CoreSight trace data output or debug monitor data output
	3	GPIO5[14]/GPIO[94]	I	IO	GPIO, default
UART0_TXD	0	UART0_TXD	O	O	UART0 TX data output, default
	3	GPIO5[15]/GPIO[95]	-	IO	GPIO
UART0_RXD	0	UART0_RXD	I	I	UART0 RX data input, default
	3	GPIO6[0]/GPIO[96]	-	IO	GPIO
UART1_TXD	0	UART1_TXD	-	O	UART1 TX data output



Pin Name	Mux	Functions	Default Dir	Dir	Description
	3	GPIO6[1]/GPIO[9 7]	I	IO	GPIO, default
UART1_RXD	0	UART1_RXD	-	I	UART1 RX data input
	3	GPIO6[2]/GPIO[9 8]	I	IO	GPIO, default
UART1_RTSN	0	UART1_RTSN	-	O	UART1 RTS output, low active
	1	UART2_TXD	-	O	UART2 TX data output
	3	GPIO6[3]/GPIO[9 9]	I	IO	GPIO, default
UART1_CTSN	0	UART1_CTSN	-	I	UART1 CTS input, low active
	1	UART2_RXD	-	I	UART2 RX data input
	3	GPIO6[4]/GPIO[1 00]	I	IO	GPIO, default
SPI0_CSN	0	SPI0_CSN	-	O	SPI0 master chip select output
	1	I2C4_SDA	-	IO	I2C4 master data input or output
	3	GPIO1[0]/GPIO[1 6]	I	IO	GPIO, default
SPI0_SCLK	0	SPI0_SCLK	-	O	SPI0 master clock output
	1	I2C4_SCL	-	O	I2C4 master clock output
	3	GPIO1[1]/GPIO[1 7]	I	IO	GPIO, default
SPI0_MOSI	0	SPI0_MOSI	-	O	SPI0 master data output
	1	I2C5_SDA	-	O	I2C5 master data input or output
	2	PWM5	-	O	PWM5 output
	3	GPIO1[2]/GPIO[1 8]	I	IO	GPIO, default
SPI0_MISO	0	SPI0_MISO	-	I	SPI0 master data input
	1	I2C5_SCL	-	I	I2C5 master clock output
	2	PWM6	-	O	PWM6 output
	3	GPIO1[3]/GPIO[1 9]	I	IO	GPIO, default
I2S0_MCLK	0	I2S0_MCLK	-	IO	I2S0 master/slave clock output
	3	GPIO6[5]/GPIO[1 01]	I	IO	GPIO, default



Pin Name	Mux	Functions	Default Dir	Dir	Description
I2S0_BCLK	0	I2S0_BCLK	-	IO	I2S0 master bit clock output I2S0 slave bit clock input
	3	GPIO6[6]/GPIO[102]	I	IO	GPIO, default
I2S0_LRCK	0	I2S0_LRCK	-	IO	I2S0 master left/right select output I2S0 slave left/right select input
	3	GPIO6[7]/GPIO[103]	I	IO	GPIO, default
I2S0_SDIO	0	I2S0_SDIO	-	IO	I2S0 master/slave data input or output
	3	GPIO6[8]/GPIO[104]	I	IO	GPIO, default
I2S1_MCLK	0	I2S1_MCLK	-	IO	I2S1 master clock output I2S1 slave clock input
	3	GPIO6[9]/GPIO[105]	I	IO	GPIO, default
I2S1_BCLK	0	I2S1_BCLK	-	IO	I2S1 master bit clock output I2S1 slave bit clock input
	3	GPIO6[10]/GPIO[106]	I	IO	GPIO, default
I2S1_LRCK	0	I2S1_LRCK	-	IO	I2S1 master left/right select output I2S1 slave left/right select input
	3	GPIO6[11]/GPIO[107]	I	IO	GPIO, default
I2S1_SDIO	0	I2S1_SDIO	-	IO	I2S1 master/slave data input or output
	3	GPIO6[12]/GPIO[108]	I	IO	GPIO, default
I2C0_SCL	0	I2C0_SCL	-	O	I2C0 master clock output
	3	GPIO0[8]/GPIO[8]	I	IO	GPIO, default
I2C0_SDA	0	I2C0_SDA	-	IO	I2C0 master data input or output
	3	GPIO0[9]/GPIO[9]	I	IO	GPIO, default
I2C1_SCL	0	I2C1_SCL	-	O	I2C1 master clock output
	3	GPIO0[10]/GPIO[10]	I	IO	GPIO, default



Pin Name	Mux	Functions	Default Dir	Dir	Description
I2C1_SDA	0	I2C1_SDA	-	IO	I2C1 master data input or output
	3	GPIO0[11]/GPIO[11]	I	IO	GPIO, default
I2C2_SCL	0	I2C2_SCL	-	O	I2C2 master clock output
	1	SPI2_MOSI	-	I/O	SPI2 master data output
	2	PWM7	-	O	PWM7 output
	3	GPIO0[12]/GPIO[12]	I	IO	GPIO, default
I2C2_SDA	0	I2C2_SDA	-	IO	I2C2 master data input or output
	1	SPI2_MISO	-	IO	SPI2 master data input
	2	PWM8	-	O	PWM8 output
	3	GPIO0[13]/GPIO[13]	I	IO	GPIO, default
I2C3_SCL	0	I2C3_SCL	-	O	I2C3 master clock output
	1	SPI2_SCLK	-	I/O	SPI2 master clock output
	3	GPIO0[14]/GPIO[14]	I	IO	GPIO, default
I2C3_SDA	0	I2C3_SDA	-	IO	I2C3 master data input or output
	1	SPI2_CSN	-	O	SPI2 master chip select output
	3	GPIO0[15]/GPIO[15]	I	IO	GPIO, default
SENSOR0_MC_LK	0	SENSOR0_MCLK	-	O	Master clock output to sensor0
	1	TEST_CLKOUT	-	O	Test clock output divided from PLL
	3	GPIO6[13]/GPIO[109]	I	IO	GPIO, default
SENSOR1_MC_LK	0	SENSOR1_MCLK	-	O	Master clock output to sensor1
	3	GPIO6[14]/GPIO[110]	I	IO	GPIO, default
SENSOR2_MC_LK	0	SENSOR2_MCLK	-	O	Master clock output to sensor2
	1	UART3_TXD	-	O	UART3 TX data output
	3	GPIO6[15]/GPIO[111]	I	IO	GPIO, default
SENSOR3_MC_LK	0	SENSOR3_MCLK	-	O	Master clock output to sensor3
	1	UART3_RXD	-	I	UART3 RX data input



Pin Name	Mux	Functions	Default Dir	Dir	Description
	3	GPIO7[0]/GPIO[12]	I	IO	GPIO, default
WDT_RSTOUT_N	0	WDT_RSTOUT_N	O	O	Watchdog reset output, low active, default
	2	TRACE_CTL	-	O	CoreSight trace control output
	3	GPIO7[1]/GPIO[13]	-	IO	GPIO
X2_WKUPIN_N	0	X2_WKUPIN_N	-	I	Wake up input, low active
	3	GPIO7[2]/GPIO[14]	I	IO	GPIO, default
X2_IRQOUT_N	0	X2_IRQOUT_N	-	O	Interrupt output to AP
	3	GPIO7[3]/GPIO[15]	I	IO	GPIO, default
BP_MEMRESE_T_L	NA	BP_MEMRESET_L	-	O	Output to reset DRAM, low active
BP_VREF	NA	BP_VREF	I	AI	Reference voltage input
BP_ZN	NA	BP_ZN	O	AIO	Connected to calibration resistor on PCB (240 ohm ± 1%)
A[0]_CKE0A	NA	A[0]_CKE0A	O	O	CKE for channel A
A[2]_CS0A	NA	A[2]_CS0A	O	O	CS for channel A
A[4]_CLKA_T	NA	A[4]_CLKA_T	O	AO	Differential clock for channel A
A[5]_CLKA_C	NA	A[5]_CLKA_C	O	AO	Differential clock for channel A
A[8]_CA0A	NA	A[8]_CA0A	O	O	CA for channel A
A[9]_CA1A	NA	A[9]_CA1A	O	O	CA for channel A
A[10]_CA2A	NA	A[10]_CA2A	O	O	CA for channel A
A[11]_CA3A	NA	A[11]_CA3A	O	O	CA for channel A
A[12]_CA4A	NA	A[12]_CA4A	O	O	CA for channel A
A[13]_CA5A	NA	A[13]_CA5A	O	O	CA for channel A
A[20]_CKE0B	NA	A[20]_CKE0B	O	O	CKE for channel B
A[23]_CS0B	NA	A[23]_CS0B	O	O	CS for channel B
A[24]_CLKB_T	NA	A[24]_CLKB_T	O	AO	Differential clock for channel B
A[25]_CLKB_C	NA	A[25]_CLKB_C	O	AO	Differential clock for channel B
A[28]_CA0B	NA	A[28]_CA0B	O	O	CA for channel B

Pin Name	Mux	Functions	Default Dir	Dir	Description
A[29]_CA1B	NA	A[29]_CA1B	O	O	CA for channel B
A[30]_CA2B	NA	A[30]_CA2B	O	O	CA for channel B
A[31]_CA3B	NA	A[31]_CA3B	O	O	CA for channel B
A[32]_CA4B	NA	A[32]_CA4B	O	O	CA for channel B
A[33]_CA5B	NA	A[33]_CA5B	O	O	CA for channel B
D[0]_DQ0	NA	D[0]_DQ0	O	IO	DQ for byte lane 0
D[1]_DQ1	NA	D[1]_DQ1	O	IO	DQ for byte lane 0
D[2]_DQ2	NA	D[2]_DQ2	O	IO	DQ for byte lane 0
D[3]_DQ3	NA	D[3]_DQ3	O	IO	DQ for byte lane 0
D[4]_DQ4	NA	D[4]_DQ4	O	IO	DQ for byte lane 0
D[5]_DQ5	NA	D[5]_DQ5	O	IO	DQ for byte lane 0
D[6]_DQ6	NA	D[6]_DQ6	O	IO	DQ for byte lane 0
D[7]_DQ7	NA	D[7]_DQ7	O	IO	DQ for byte lane 0
D[8]_DM0	NA	D[8]_DM0	O	IO	DM for byte lane 0
D[9]_DQS0_T	NA	D[9]_DQS0_T	O	AIO	Differential DQS for byte lane 0
D[10]_DQS0_C	NA	D[10]_DQS0_C	O	AIO	Differential DQS for byte lane 0
D[12]_DQ8	NA	D[12]_DQ8	O	IO	DQ for byte lane 1
D[13]_DQ9	NA	D[13]_DQ9	O	IO	DQ for byte lane 1
D[14]_DQ10	NA	D[14]_DQ10	O	IO	DQ for byte lane 1
D[15]_DQ11	NA	D[15]_DQ11	O	IO	DQ for byte lane 1
D[16]_DQ12	NA	D[16]_DQ12	O	IO	DQ for byte lane 1
D[17]_DQ13	NA	D[17]_DQ13	O	IO	DQ for byte lane 1
D[18]_DQ14	NA	D[18]_DQ14	O	IO	DQ for byte lane 1
D[19]_DQ15	NA	D[19]_DQ15	O	IO	DQ for byte lane 1
D[20]_DM1	NA	D[20]_DM1	O	IO	DM for byte lane 1
D[21]_DQS1_T	NA	D[21]_DQS1_T	O	AIO	Differential DQS for byte lane 1
D[22]_DQS1_C	NA	D[22]_DQS1_C	O	AIO	Differential DQS for byte lane 1
D[24]_DQ16	NA	D[24]_DQ16	O	IO	DQ for byte lane 2
D[25]_DQ17	NA	D[25]_DQ17	O	IO	DQ for byte lane 2
D[26]_DQ18	NA	D[26]_DQ18	O	IO	DQ for byte lane 2
D[27]_DQ19	NA	D[27]_DQ19	O	IO	DQ for byte lane 2
D[28]_DQ20	NA	D[28]_DQ20	O	IO	DQ for byte lane 2



Pin Name	Mux	Functions	Default Dir	Dir	Description
D[29]_DQ21	NA	D[29]_DQ21	O	IO	DQ for byte lane 2
D[30]_DQ22	NA	D[30]_DQ22	O	IO	DQ for byte lane 2
D[31]_DQ23	NA	D[31]_DQ23	O	IO	DQ for byte lane 2
D[32]_DM2	NA	D[32]_DM2	O	IO	DM for byte lane 2
D[33]_DQS2_T	NA	D[33]_DQS2_T	O	AIO	Differential DQS for byte lane 2
D[34]_DQS2_C	NA	D[34]_DQS2_C	O	AIO	Differential DQS for byte lane 2
D[36]_DQ24	NA	D[36]_DQ24	O	IO	DQ for byte lane 3
D[37]_DQ25	NA	D[37]_DQ25	O	IO	DQ for byte lane 3
D[38]_DQ26	NA	D[38]_DQ26	O	IO	DQ for byte lane 3
D[39]_DQ27	NA	D[39]_DQ27	O	IO	DQ for byte lane 3
D[40]_DQ28	NA	D[40]_DQ28	O	IO	DQ for byte lane 3
D[41]_DQ29	NA	D[41]_DQ29	O	IO	DQ for byte lane 3
D[42]_DQ30	NA	D[42]_DQ30	O	IO	DQ for byte lane 3
D[43]_DQ31	NA	D[43]_DQ31	O	IO	DQ for byte lane 3
D[44]_DM3	NA	D[44]_DM3	O	IO	DM for byte lane 3
D[45]_DQS3_T	NA	D[45]_DQS3_T	O	AIO	Differential DQS for byte lane 3
D[46]_DQS3_C	NA	D[46]_DQS3_C	O	AIO	Differential DQS for byte lane 3

- (1) Mux = NA means no function mux for this pin.
- (2) Mux = 0/1/2/3 means this pin function can be configured by PIN registers. The value is the function selection. Only listed values are legal.
- (3) If GPIO is the default function, it is in input state.
- (4) Almost all general digital pins have GPIO functions. They are organized in GPIO groups and can also be numbered in a flattened form, which are illustrated in this table.

2.2.3 Analog Pins

Table 2-6 Analog Pin List

Pin Name	Ball	Type	Description
MIPI CSI Host RX			
RX0_CLKP	M1	AI	MIPI RX0 clock lane
RX0_CLKN	N2	AI	MIPI RX0 clock lane
RX0_DATAP0	L1	AI	MIPI RX0 data lane 0
RX0_DATAN0	M2	AI	MIPI RX0 data lane 0
RX0_DATAP1	K1	AI	MIPI RX0 data lane 1



Pin Name	Ball	Type	Description
RX0_DATAN1	L2	AI	MIPI RX0 data lane 1
RX1_CLKP	W3	AI	MIPI RX1 clock lane
RX1_CLKN	W4	AI	MIPI RX1 clock lane
RX1_DATAP0	V3	AI	MIPI RX1 data lane 0
RX1_DATAN0	V4	AI	MIPI RX1 data lane 0
RX1_DATAP1	U3	AI	MIPI RX1 data lane 1
RX1_DATAN1	U4	AI	MIPI RX1 data lane 1
RX2_CLKP	N1	AI	MIPI RX2 clock lane
RX2_CLKN	P2	AI	MIPI RX2 clock lane
RX2_DATAP0	R1	AI	MIPI RX2 data lane 0
RX2_DATAN0	T2	AI	MIPI RX2 data lane 0
RX2_DATAP1	P1	AI	MIPI RX2 data lane 1
RX2_DATAN1	R2	AI	MIPI RX2 data lane 1
RX3_DATAP0	AB3	AI	MIPI RX3 data lane 0
RX3_DATAN0	AB4	AI	MIPI RX3 data lane 0
RX3_DATAP1	AA3	AI	MIPI RX3 data lane 1
RX3_DATAN1	AA4	AI	MIPI RX3 data lane 1
RX_REXT	P4	AIO	Connected to calibration resistor on PCB (200 ohm ± 1%)
MIPI CSI Device TX			
TX_CLKP	V2	AO	MIPI TX clock lane
TX_CLKN	U1	AO	MIPI TX clock lane
TX_DATAP0	W2	AO	MIPI TX data lane 0
TX_DATAN0	V1	AO	MIPI TX data lane 0
TX_DATAP1	Y2	AO	MIPI TX data lane 1
TX_DATAN1	W1	AO	MIPI TX data lane 1
TX_DATAP2	AA2	AO	MIPI TX data lane 2
TX_DATAN2	Y1	AO	MIPI TX data lane 2
TX_DATAP3	AB2	AO	MIPI TX data lane 3
TX_DATAN3	AA1	AO	MIPI TX data lane 3
TX_REXT	R4	AIO	Connected to calibration resistor on PCB (200 ohm ± 1%)



Pin Name	Ball	Type	Description
MIPI Analog Test			
ATB_MIPI	R3	AO	MIPI TX&RX PHY analog test output
USB			
TX_P	AA16	AO	USB3 tx data line
TX_M	AB16	AO	USB3 tx data line
RX_P	AA17	AI	USB3 rx data line
RX_M	AB17	AI	USB3 rx data line
DP	AB15	AIO	USB2 data line
DM	AA15	AIO	USB2 data line
ID	AA13	AIO	USB mini-receptacle identifier
RESREF	W14	AIO	External reference resistor
DDR			
BP_MEMRESET_L	L22	AO	DRAM reset
BP_ALERT_N	M22	AIO	DDR4 alert
BP_VREF	L19	AIO	Voltage reference for receivers and analog test point for debug
BP_ZN	M20	AO	Calibration external reference resistor
BP_A0	F22	AIO	DRAM address and command bits
BP_A1	F21	AIO	DRAM address and command bits
BP_A2	E22	AIO	DRAM address and command bits
BP_A3	G20	AIO	DRAM address and command bits
BP_A4	K22	AIO	DRAM address and command bits
BP_A5	K21	AIO	DRAM address and command bits
BP_A6	H20	AIO	DRAM address and command bits
BP_A7	H19	AIO	DRAM address and command bits
BP_A8	G22	AIO	DRAM address and command bits
BP_A9	G21	AIO	DRAM address and command bits
BP_A10	J20	AIO	DRAM address and command bits
BP_A11	H21	AIO	DRAM address and command bits
BP_A12	H22	AIO	DRAM address and command bits
BP_A13	K20	AIO	DRAM address and command bits
BP_A14	K19	AIO	DRAM address and command bits



Pin Name	Ball	Type	Description
BP_A15	L21	AIO	DRAM address and command bits
BP_A16	J22	AIO	DRAM address and command bits
BP_A17	J21	AIO	DRAM address and command bits
BP_A20	P21	AIO	DRAM address and command bits
BP_A21	P22	AIO	DRAM address and command bits
BP_A22	T20	AIO	DRAM address and command bits
BP_A23	V22	AIO	DRAM address and command bits
BP_A24	N22	AIO	DRAM address and command bits
BP_A25	N21	AIO	DRAM address and command bits
BP_A26	R19	AIO	DRAM address and command bits
BP_A27	N19	AIO	DRAM address and command bits
BP_A28	T22	AIO	DRAM address and command bits
BP_A29	T21	AIO	DRAM address and command bits
BP_A30	P20	AIO	DRAM address and command bits
BP_A31	R21	AIO	DRAM address and command bits
BP_A32	R22	AIO	DRAM address and command bits
BP_A33	R20	AIO	DRAM address and command bits
BP_A34	N20	AIO	DRAM address and command bits
BP_A35	U21	AIO	DRAM address and command bits
BP_A36	U22	AIO	DRAM address and command bits
BP_A37	M21	AIO	DRAM address and command bits
BP_A38	L20	AIO	DRAM address and command bits
BP_D0	A21	AIO	DRAM data bits and strobes
BP_D1	A19	AIO	DRAM data bits and strobes
BP_D2	B19	AIO	DRAM data bits and strobes
BP_D3	B21	AIO	DRAM data bits and strobes
BP_D4	B22	AIO	DRAM data bits and strobes
BP_D5	C22	AIO	DRAM data bits and strobes
BP_D6	C21	AIO	DRAM data bits and strobes
BP_D7	C19	AIO	DRAM data bits and strobes
BP_D8	C18	AIO	DRAM data bits and strobes
BP_D9	A20	AIO	DRAM data bits and strobes



Pin Name	Ball	Type	Description
BP_D10	B20	AIO	DRAM data bits and strobes
BP_D12	D18	AIO	DRAM data bits and strobes
BP_D13	C20	AIO	DRAM data bits and strobes
BP_D14	D20	AIO	DRAM data bits and strobes
BP_D15	G19	AIO	DRAM data bits and strobes
BP_D16	E21	AIO	DRAM data bits and strobes
BP_D17	E18	AIO	DRAM data bits and strobes
BP_D18	F19	AIO	DRAM data bits and strobes
BP_D19	F18	AIO	DRAM data bits and strobes
BP_D20	D21	AIO	DRAM data bits and strobes
BP_D21	E19	AIO	DRAM data bits and strobes
BP_D22	E20	AIO	DRAM data bits and strobes
BP_D24	U19	AIO	DRAM data bits and strobes
BP_D25	U18	AIO	DRAM data bits and strobes
BP_D26	V18	AIO	DRAM data bits and strobes
BP_D27	V21	AIO	DRAM data bits and strobes
BP_D28	T19	AIO	DRAM data bits and strobes
BP_D29	W20	AIO	DRAM data bits and strobes
BP_D30	Y20	AIO	DRAM data bits and strobes
BP_D31	W18	AIO	DRAM data bits and strobes
BP_D32	W21	AIO	DRAM data bits and strobes
BP_D33	V19	AIO	DRAM data bits and strobes
BP_D34	V20	AIO	DRAM data bits and strobes
BP_D36	Y22	AIO	DRAM data bits and strobes
BP_D37	Y21	AIO	DRAM data bits and strobes
BP_D38	Y19	AIO	DRAM data bits and strobes
BP_D39	AA19	AIO	DRAM data bits and strobes
BP_D40	AA21	AIO	DRAM data bits and strobes
BP_D41	AA22	AIO	DRAM data bits and strobes
BP_D42	AB21	AIO	DRAM data bits and strobes
BP_D43	AB19	AIO	DRAM data bits and strobes
BP_D44	Y18	AIO	DRAM data bits and strobes

Pin Name	Ball	Type	Description
BP_D45	AB20	AIO	DRAM data bits and strobes
BP_D46	AA20	AIO	DRAM data bits and strobes

2.3 Electrical Specifications

2.3.1 Recommended Operating Conditions

Table 2-7 summarizes the recommended operating conditions for the power supply under normal voltage.

Table 2-7 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
Digital Core Power					
VDD_AO	Always On domain core power	0.76	0.8	0.84	V
VDD_CORE_PD	Shut down domain core power	0.76	0.8	0.84	V
VDD_CPU	CPU core power @1.2GHz	0.76	0.8	0.84	V
	CPU core power @1.5GHz	0.95	1	1.05	V
VDD_DDR	DDR Controller & PHY core power @ 3200MT/s	0.776	0.8	0.84	V
VDD_CNN0	CNN0 core power @1.0GHz	0.78	0.82	0.86	V
	CNN0 core power @1.2GHz	0.95	1	1.05	V
VDD_CNN1	CNN1 core power @1.0GHz	0.78	0.82	0.86	V
	CNN1 core power @1.2GHz	0.95	1	1.05	V
VRIP_VDD_DDR	DDR core power supply rail ripple: DDR4 mode	-2.5	-	2.5	%VDD_DDR
VRIP_VDD_DDR	DDR core power supply rail ripple: LPDDR4 mode	-2.0	-	-2.0	%VDD_DDR
Digital IO Power					
SYS_VDDPST	SYS IO domain power	1.71	1.8	1.89	V
BIFSD_VDDPST33	BIFSD IO domain power:3.3V Mode	3.135	3.3	3.465	V
	BIFSD IO domain power:1.8V Mode	1.71	1.8	1.89	V
BIFSPI_VDDPST33	BIFSPI IO domain power:3.3V Mode	3.135	3.3	3.465	V
	BIFSPI IO domain power:1.8V	1.71	1.8	1.89	V

Symbol	Description	Min	Typ	Max	Unit
	Mode				
BT1120_VDDPST33	BT1120 IO domain power, 3.3V Mode	3.135	3.3	3.465	V
	BT1120 IO domain power: 1.8V Mode	1.71	1.8	1.89	V
SD0_VDDPST33	SD0 IO domain power:1.8V Mode	1.71	1.8	1.89	V
SD1_VDDPST33	SD1 IO domain power:3.3V mode	3.135	3.3	3.465	V
	SD1 IO domain power:1.8V mode	1.71	1.8	1.89	V
SD2_VDDPST33	SD2 IO domain power:3.3V mode	3.135	3.3	3.465	V
	SD2 IO domain power:1.8V mode	1.71	1.8	1.89	V
RGMII_VDDPST33	RGMII IO domain power:3.3V mode	3.135	3.3	3.465	V
	RGMII IO domain power:1.8V mode	1.71	1.8	1.89	V
VDDQ_DDR	LPDDR4 IO domain power	1.067	1.1	1.133	V
	LPDDR4X IO domain power	1.067	1.1	1.133	V
	DDR4 IO domain power	1.164	1.2	1.236	V
VRIP_VDDQ_DDR	DDR IO domain power rail ripple: DDR4	-5.0	-	5.0	%VDDQ_DR
VRIP_VDDQ_DDR	DDR IO domain power rail ripple: LPDDR4	-2.5	-	2.5	%VDDQ_DR
VDDQLP	LPDDR4X IO domain power Note: When not in LPDDR4x mode, the VDDQLP supply pin should be tied to the VDDQ_DDR supply	0.582	0.6	0.63	V
VRIP_VDDQLP	LPDDR4X IO domain power rail ripple Note: In other DDR modes, the VDDQ_DDR ripple spec applies to VDDQLP.	-5.0	-	5.0	%VDDQLP
JTG_VDDPST33	JTAG IO domain power:3.3V mode	3.135	3.3	3.465	V
	JTAG IO domain power:1.8V mode	1.71	1.8	1.89	V
I2C0_VDDPST33	I2C0 IO domain power:3.3V mode	3.135	3.3	3.465	V
	I2C0 IO domain power:1.8V mode	1.71	1.8	1.89	V
I2C2_VDDPST33	I2C2 IO domain power:3.3V mode	3.135	3.3	3.465	V
	I2C2 IO domain power:1.8V mode	1.71	1.8	1.89	V



Symbol	Description	Min	Typ	Max	Unit
Analog Power					
VDDA_PLL_MAIN	SYS PLL analog power	0.76	0.8	0.84	V
VDDA_PLL_DDR	DDR PLL analog power	1.62	1.8	1.98	V
VRIP_PLL_DDR	DDR PLL analog power rail ripple	-2.5	-	2.5	%VDDA_PLL_DDR
VDD_USB	USB PHY power	0.76	0.8	0.84	V
VP	USB PHY analog and digital low-voltage supply	0.76	0.8	0.84	V
VPH	USB high-voltage supply for SuperSpeed operation	3.135	3.3	3.465	V
VP_MIPI	MIPI HOST/DEV PHY analog power	0.76	0.8	0.84	V
VPH_MIPI	MIPI HOST/DEV PHY analog power	1.71	1.8	1.89	V
PVT_VDDA_TAVDD	Temperature sensor analog power	1.71	1.8	1.89	V
EFUSE_VDD	EFUSE program analog power	1.71	1.8	1.89	V
ARMPPLL_VDDPST	PLL digital supply power	0.76	0.8	0.84	V
ARMPPLL_VDDHV	PLL analog supply voltage	1.71	1.8	1.89	V
ARMPPLL_VDDREF	PLL digital supply voltage	0.76	0.8	0.84	V
VAA	DDR PHY internal PLL analog power	1.746	1.8	1.89	V
Ground					
VSS	Common Ground	-	0	-	V
GD_VIO	MIPI HOST/DEV PHY analog ground	-	0	-	V
Others					
BIFSD0_VDDPST18	It is required to implement 0.5uF~1uF capacitor on BIFSD0_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x BIFSD_VDDPST33), In 1.8V mode (~BIFSD_VDDPST33)			V
BIFSD1_VDDPST18	It is required to implement 0.5uF~1uF capacitor on BIFSD1_VDDPST18 pin on PCB to stabilize the output voltage of the	In 3.3V mode (~0.5 x BIFSD_VDDPST33), In 1.8V mode (~BIFSD_VDDPST33)			V



Symbol	Description	Min	Typ	Max	Unit
	internal LDO. Don't connect power to it				
BIFSPI_VDDPST18	It is required to implement 0.5uF~1uF capacitor on BIFSPI_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x BIFSPI_VDDPST33), In 1.8V mode (~BIFSPI_VDDPST33)			V
BT1120_0_VDDPS18	It is required to implement 0.5uF~1uF capacitor on BT1120_0_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x BT1120_VDDPST33), In 1.8V mode (~BT1120_VDDPST33)			V
BT1120_1_VDDPS18	It is required to implement 0.5uF~1uF capacitor on BT1120_1_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x BT1120_VDDPST33), In 1.8V mode (~BT1120_VDDPST33)			V
BT1120_2_VDDPS18	It is required to implement 0.5uF~1uF capacitor on BT1120_2_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x BT1120_VDDPST33), In 1.8V mode (~BT1120_VDDPST33)			V
SD0_0_VDDPST18	It is required to implement 0.5uF~1uF capacitor on SD0_0_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x SD0_VDDPST33), In 1.8V mode (~SD0_VDDPST33)			V
SD0_1_VDDPST18	It is required to implement 0.5uF~1uF capacitor on SD0_1_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x SD0_VDDPST33), In 1.8V mode (~SD0_VDDPST33)			V
SD1_VDDPST18	It is required to implement 0.5uF~1uF capacitor on SD1_VDDPST18 pin on PCB to	In 3.3V mode (~0.5 x SD1_VDDPST33),			V



Symbol	Description	Min	Typ	Max	Unit
	stabilize the output voltage of the internal LDO. Don't connect power to it	In 1.8V mode (~SD1_VDDPST33)			
SD2_VDDPST18	It is required to implement 0.5uF~1uF capacitor on SD2_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x SD2_VDDPST33), In 1.8V mode (~SD2_VDDPST33)			V
RGMII_0_VDDPST18	It is required to implement 0.5uF~1uF capacitor on RGMII_0_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x RGMII_VDDPST33), In 1.8V mode (~RGMII_VDDPST33)			V
RGMII_1_VDDPST18	It is required to implement 0.5uF~1uF capacitor on RGMII_1_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x RGMII_VDDPST33), In 1.8V mode (~RGMII_VDDPST33)			V
JTG_VDDPST18	It is required to implement 0.5uF~1uF capacitor on JTG_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x JTG_VDDPST33), In 1.8V mode (~JTG_VDDPST33)			V
I2C0_VDDPST18	It is required to implement 0.5uF~1uF capacitor on VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x I2C0_VDDPST33), In 1.8V mode (~I2C0_VDDPST33)			V
I2C2_VDDPST18	It is required to implement 0.5uF~1uF capacitor on I2C2_VDDPST18 pin on PCB to stabilize the output voltage of the internal LDO. Don't connect power to it	In 3.3V mode (~0.5 x I2C2_VDDPST33), In 1.8V mode (~I2C2_VDDPST33)			V



2.3.2 Power Consumption

2.3.3 Temperature and Thermal Resistance

Note

- The thermal resistance is provided in compliance with the JEDEC JESD51 series of standards. The actual system design and environment may be different.
 - For details about θ_{JA} , see the JEDEC Standard No.51-2.
 - For details about θ_{JB} , see the JEDEC Standard No.51-8.
 - For details about θ_{JC} , see the following standards:
 - MIL-STD-883 1012.1 Thermal characteristics.
 - SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages.
- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.

Caution

- Under no condition can the chip junction temperature exceed the destructive junction temperature in [Table 2-8](#). If the chip junction temperature exceeds the destructive junction temperature, the chip may be physically damaged.
- Under normal working conditions, the chip junction temperature should be less than or equal to the maximum junction temperature for Long-Term working in [Table 2-8](#).

[Table 2-8](#) lists the junction temperature requirements of the X3M.

Table 2-8 Junction Temperature Requirements

Symbol	Description	Min	Typ	Max	Unit
TA	Temperature ambient	-25		85	°C
TJ	Junction temperature for working			105	°C

[Table 2-9](#) lists the thermal resistance parameters of the X3M.

Table 2-9 Thermal Resistance Parameters

Symbol	Description	Min	Typ	Max	Unit
θ_{JA}	Junction-to-ambient thermal resistance		13.71		°C/W
θ_{JB}	Junction-to-board thermal resistance		3.72		°C/W



θ_{JC}	Junction-to-case thermal resistance		1.16		°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		13.71		°C/W

2.3.4 Electrostatic Discharge (ESD) Ratings

Table 2-10 summarizes the ESD ratings of the X3M.

Table 2-10 ESD Ratings

Symbol	Description	Value	Unit
HBM	Human-Body model (HBM)	2000	V
CDM	Charged-device model (CDM)	400	V

2.3.5 Power On/Off Sequence

For the power-up and power-down sequence details, see [3.3.4 Power Sequence](#).

2.3.6 Digital General IO Electrical Parameters

Table 2-11 summarizes the digital general IO electrical characteristics.

Table 2-11 Digital General IO Electrical Parameters

Symbol	Description	Drive Strength	Min	Typ	Max	Unit
VDDIO	Interface voltage	-	1.71	1.8	1.89	V
VIL	Input Low Voltage	-	-0.3		0.35*VDDIO	V
VIH	Input High Voltage	-	0.65*VDDIO		1.89	V
VT	Threshold Point	-	0.82	0.89	0.97	V
VT+	Schmitt Trigger Low to High Threshold Point	-	0.96	1.03	1.1	V
VT-	Schmitt Trigger High to Low Threshold Point	-	0.64	0.75	0.86	V
VTPU	Threshold Point with Pull-up Resistor Enabled	-	0.81	0.88	0.97	V
VTPD	Threshold Point with Pull-down Resistor Enabled	-	0.82	0.89	0.98	V
VTPU+	Schmitt Trigger Low to High Threshold Point	-	0.95	1.02	1.09	V



Symbol	Description	Drive Strength	Min	Typ	Max	Unit
	High Threshold Point with Pull-up Resistor Enabled					
V _{TPU} -	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	0.63	0.75	0.85	V
V _{TPD} +	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	0.96	1.05	1.11	V
V _{TPD} -	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	0.65	0.76	0.86	V
I _l	Input Leakage Current @ V _i =1.8V or 0V	-	-	-	±10μ	A
I _{OZ}	Tri-state Output Leakage Current @ V _o =1.8V or 0V	-	-	-	±10μ	A
R _{SPU}	Strong Pull-up Resistor	-	-	-	-	Ω
R _{PU}	Pull-up Resistor	-	60k	89k	137k	Ω
R _{PD}	Pull-down Resistor	-	61k	104k	196k	Ω
V _{OL}	Output Low Voltage	-	-	-	0.45	V
V _{OH}	Output High Voltage	-	1.35	-	-	V
I _{OL}	Low Level Output Current @ V _{OL} (max)	04	5.5	9.2	13.0	mA
		08	11.1	18.2	25.6	mA
		12	16.5	27.0	37.7	mA
		16	21.9	35.6	49.4	mA
I _{OH}	High Level Output Current @ V _{OH} (min)	04	6.6	9.6	13.2	mA
		08	13.1	19.1	26.2	mA
		12	19.5	28.5	39.0	mA
		16	25.9	37.9	51.8	mA

2.3.7 24M OSC IO Electrical Parameters

Table 2-12 lists the 24M oscillator (OSC) IO electrical parameters.



Table 2-12 24M OSC IO Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Freq	Frequency	-	24	-	MHz
Duty	Duty cycle	40	50	60	%
ESR	Crystal maximum ESR	-	-	40	Ω

2.3.8 32K Input Electrical Parameters

Table 2-13 lists the 32K input electrical parameters.

Table 2-13 32K Input Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Freq	Frequency	-	32768	-	Hz
Duty	Duty cycle	40	50	60	%

2.3.9 SDIO Electrical Parameters

Table 2-14 summarize the SD special IO electrical characteristics (1.8V).

Table 2-14 SDIO Electrical Parameters (1.8V)

Symbol	Description	Drive Strength (DS2,DS1,DS0)	Min	Typ	Max	Unit
VDDIO	Interface voltage	-	1.71	1.8	1.89	V
VIL	Input Low Voltage	-	-0.3	-	0.58	V
VIH	Input High Voltage	-	1.27	-	1.98	V
VT	Threshold Point	-	0.85	0.95	1.08	V
VT+	Schmitt Trigger Low to High Threshold Point	-	0.97	1.06	1.17	V
VT-	Schmitt Trigger High to Low Threshold Point	-	0.7	0.82	0.94	V
VTPU	Threshold Point with Pull-up Resistor Enabled	-	0.85	0.95	1.07	V
VTPD	Threshold Point with Pull-down Resistor Enabled	-	0.86	0.96	1.09	V
VTPU+	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	0.97	1.06	1.16	V



Symbol	Description	Drive Strength (DS2,DS1,DS0)	Min	Typ	Max	Unit
VTPU-	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	0.69	0.81	0.93	V
VTPD+	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	0.98	1.07	1.18	V
VTPD-	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	0.7	0.82	0.95	V
I _I	Input Leakage Current @ V _I =1.8V or 0V	-	-	-	±10µ	A
I _{OZ}	Tri-state Output Leakage Current @ V _O =1.8V or 0V	-	-	-	±10µ	A
R _{PU}	Pull-up Resistor	-	33k	59k	90k	Ω
R _{PD}	Pull-down Resistor	-	34k	61k	95k	Ω
V _{OL}	Output Low Voltage	-	-	-	0.45	V
V _{OH}	Output High Voltage	-	1.4	-	-	V
I _{OL}	Low Level Output Current @ V _{OL(max)}	000	4.5	7.7	11.3	mA
		001	6.7	11.4	16.7	mA
		010	9.0	15.2	22.1	mA
		011	11.2	18.8	27.3	mA
		100	13.4	22.6	32.7	mA
		101	15.6	26.2	37.8	mA
		110	17.7	29.7	42.8	mA
		111	19.9	33.2	47.7	mA
I _{OH}	High Level Output Current @ V _{OH(min)}	000	2.6	6.3	11.9	mA
		001	3.8	9.4	17.7	mA
		010	5.1	12.6	23.7	mA
		011	6.4	15.7	29.4	mA
		100	7.6	18.8	35.2	mA
		101	8.9	21.8	40.9	mA



Symbol	Description	Drive Strength (DS2,DS1,DS0)	Min	Typ	Max	Unit
		110	10.1	24.9	46.6	mA
		111	11.4	27.9	52.2	mA

Table 2-15 summarizes the SD special IO electrical characteristics (3V).

Table 2-15 SDIO Electrical Parameters (3.3V)

Symbol	Description	Drive Strength (DS2,DS1,DS0)	Min	Typ	Max	Unit
VDDIO	Interface voltage	-	3.135	3.3	3.465	V
V _{IL}	Input Low Voltage	-	-0.3	-	0.25*VDDI O	V
V _{IH}	Input High Voltage	-	0.625*VDDIO	-	3.465	V
V _T	Threshold Point	-	0.76	0.94	1.24	V
V _{T+}	Schmitt Trigger Low to High Threshold Point	-	0.94	1.09	1.36	V
V _{T-}	Schmitt Trigger High to Low Threshold Point	-	0.68	0.89	1.2	V
V _{TPU}	Threshold Point with Pull-up Resistor Enabled	-	0.74	0.92	1.22	V
V _{TPD}	Threshold Point with Pull-down Resistor Enabled	-	0.76	0.95	1.25	V
V _{TPU+}	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled	-	0.93	1.07	1.34	V
V _{TPU-}	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled	-	0.66	0.88	1.18	V
V _{TPD+}	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled	-	0.95	1.1	1.38	V
V _{TPD-}	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled	-	0.68	0.9	1.22	V



Symbol	Description	Drive Strength (DS2,DS1,DS0)	Min	Typ	Max	Unit
	Enabled					
I _l	Input Leakage Current @ V _I =3.3V or 0V	-	-	-	±10μ	A
I _{OZ}	Tri-state Output Leakage Current @ V _O =3.3V or 0V	-	-	-	±10μ	A
R _{PU}	Pull-up Resistor	-	33k	59k	91k	Ω
R _{PD}	Pull-down Resistor	-	34k	61k	108k	Ω
V _{OL}	Output Low Voltage	-	-	-	0.125*VDDI _O	V
V _{OH}	Output High Voltage		0.75*VDDIO	-	-	V
I _{OL}	Low Level Output Current @V _{OL} (max)	000	2.8	5.4	9.8	mA
		001	4.1	8.0	14.6	mA
		010	5.5	10.7	19.4	mA
		011	6.8	13.2	23.9	mA
		100	8.2	15.9	28.7	mA
		101	9.6	18.4	33.2	mA
		110	10.9	20.9	37.6	mA
		111	12.2	23.4	42.0	mA
I _{OH}	High Level Output Current @V _{OH} (min)	000	4.4	7.6	13.5	mA
		001	6.6	11.4	20.2	mA
		010	8.8	15.2	26.9	mA
		011	10.9	18.9	33.5	mA
		100	13.1	22.6	40.1	mA
		101	15.2	26.3	46.7	mA
		110	17.4	30.1	53.3	mA
		111	19.6	33.7	59.7	mA

2.3.10 DDR Electrical Parameters

Table 2-16 summarizes the DDR IO DC/AC electrical characteristics in LPDDR4 mode.



Table 2-16 LPDDR4 Mode DDR DC/AC Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
Vref	Reference voltage	-	Variable	-	V
VrefDC-err	DC reference voltage error	-0.75%	-	0.75%	VDDQ_DDR
VrefAC-err	AC reference voltage error	-0.25%	-	0.25%	VDDQ_DDR
IIZ	Vref input leakage current	-	-	50	uA
IIZ	BP_DAT input leakage current	-	-	50	uA
VIH-DC	Input high voltage for BP_DAT*	Vref + 0.020	-	-	V
VIL-DC	Input low voltage for BP_DAT*	-	-	Vref - 0.020	V
VIH-ACHS	High-speed input high voltage for BP_DAT*(logic 1)	Vref + 0.070	-	Vref + 0.440	V
VIL-ACHS	High-speed input low voltage for BP_DAT*(logic 0)	Vref - 0.440 or 0	-	Vref - 0.070	V
VID-DC	Differential input voltage for abs(DQS_t - DQS_c)	0.100	-	-	V
VOH-DC	Output high voltage	0.8*VDDQ_DR	-	-	V
VOL-DC	Output low voltage	-	-	0.2*VDDQ_DDR	V
RTT	On-die termination (ODT) programmable resistances	-	open, 120, 60, 40	-	Ω
ROnPu	Output driver pull-up impedance: DQ, DQS outputs	-	120, 60, 40	-	Ω
ROnPd	Output driver pull-down impedance: DQ, DQS outputs	-	120, 60, 40	-	Ω
ROnPu	Output driver pull-up impedance: address, command, CLK outputs	-	120, 60, 40	-	Ω
ROnPd	Output driver pull-down impedance: address, command, CLK outputs	-	120, 60, 40	-	Ω
ROnPu	Output driver pull-up impedance: BP_MEMRESET_L	-	24~40	-	Ω
ROnPd	Output driver pull-down impedance: BP_MEMRESET_L	-	24~40	-	Ω

2.3.11 MIPI CSI RX Electrical Parameters

Table 2-17 summarizes the MIPI CSI high-speed receiver (RX) electrical characteristics.



Table 2-17 MIPI CSI RX Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
V _{PIN}	Pin signal voltage range	-50	-	1350	mV
I _{LEAK}	Pin leakage current	-10	-	10	uA
V _{GND SH}	Ground shift	-50	-	50	mV
V _{OH(absmax)}	Maximum transient output voltage level	-0.15	-	1.45	V
t _{VOH(absmax)}	Maximum transient time above V _{OH(absmax)}	-	-	20	ns
V _{IDTH}	Differential input high voltage threshold	-	-	70 ⁽²⁾	mV
		-	-	40 ⁽³⁾	mV
V _{IDTL}	Differential input low voltage threshold	-70 ⁽²⁾	-	-	mV
		-40 ⁽³⁾	-	-	mV
V _{IHHS}	Single ended input high voltage	-	-	460 ⁽⁴⁾	mV
V _{ILHS}	Single ended input low voltage	-40 ⁽⁴⁾	-	-	mV
V _{CMRXDC} ⁽⁵⁾	Input common mode voltage	70	-	330	mV
Z _{ID}	Differential input impedance	80	100	125	Ω

(1) For D-PHY spec 1.1 compatibility mode (≤ 1.5 Gbps).

(2) In case of High-speed deskew calibration (> 1.5 Gbps).

(3) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(4) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

2.3.12 MIPI CSI TX Electrical Parameters

Table 2-18 summarizes the MIPI CSI high-speed transmitter (TX) electrical characteristics.

Table 2-18 MIPI CSI TX Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
V _I	Input signal voltage range	-50	-	1350	mV
I _{LEAK} ⁽¹⁾	Input leakage current	-10	-	10	uA
V _{GND SH}	Ground shift	-50	-	50	mV
V _{OH(absmax)}	Maximum transient output voltage level	-0.15	-	1.45	V



Symbol	Description	Min	Typ	Max	Unit
tVOH(absmax)	Maximum transient time above $V_{OH}(absmax)$	-	-	20	ns
VOD ⁽²⁾	HS transmit differential output voltage magnitude	100	200	225	mV
$\Delta VOD ^{(2)}$	Change in differential output voltage magnitude between logic states	-	-	14	mV
VCM _{TX} ⁽²⁾	Steady-state common mode output voltage	150	200	250	mV
$\Delta V_{CMTX}(1,0)$ ⁽²⁾	Changes in steady-state common mode output voltage between logic states	-	-	5	mV
V _{OHH} ⁽²⁾	HS output high voltage	-	-	360	mV
Z _{os}	Single ended output impedance	40	50	62.5	Ω
ΔZ_{os}	Single ended output impedance mismatch	-	-	10	%

(1) $V_{GNDH(min)} \leq VI \leq V_{GNDH(max)} + V_{OH}(absmax)$, lane module in LP receive mode.

(2) Under the conditions $80\Omega \leq R_L \leq 125\Omega$.

2.3.13 USB Electrical Parameters

Table 2-19 summarizes the USB transmitter (TX) electrical characteristics.

Table 2-20 summarizes the USB Receiver (RX) electrical characteristics.

Table 2-19 USB TX Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
UI	Unit Interval	199.94	-	200.06	ps
V _{TX-DFF-PP}	Differential p-p Tx voltage swing	0.8	1	1.2	V
V _{TX-DFF-PP-LOW}	Low-Power Differential p-p Tx voltage swing	0.4	-	1.2	V
V _{TX-DE-RATIO}	Tx de-emphasis	3.0		4.0	dB
R _{TX-RCV-DETECT}	DC differential impedance	72	-	120	Ω
V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection	-	-	0.6	V
C _{AC-COUPLING}	AC Coupling Capacitor	75	-	265	nF



Symbol	Description	Min	Typ	Max	Unit
tCDR_SLEW_MAX	Maximum skew rate	-	10	-	ms/s
V _{TX-CM-IDLE-DELTA}	Transmitter idle common-mode voltage change	-600	-	+600	mv

Table 2-20 USB RX Electrical Parameters

Symbol	Description	Min	Typ	Max	Unit
UI	Unit Interval	199.94	-	200.06	ps
R _{RX-DC}	Receiver DC common-mode impedance	18	-	30	Ω
R _{RX-DIFF-DC}	DC differential impedance	72	-	120	Ω
Z _{RX-HIGH-IMP-DC-POS}	DC Input CM Input Impedance for V>0 during Reset or power down	10k	-	-	Ω
V _{RX-LFPS-DET-DIFFp-p}	LFPS Detect Threshold	100	-	300	mV
C _{RX-AC-COUPLING}	AC Coupling Capacitor	297	-	363	nF
T _{DISCHARGE}	Discharge Time	-	-	250	ms

2.4 Interface Timings

2.4.1 DDR Interface Timings

2.4.1.1 LPDDR4 Clock AC Timings

Table 2-21 lists the LPDDR4 clock AC timing parameters.

Table 2-21 LPDDR4 Clock AC Timing Parameters

Parameter	Symbol	3200		Unit
		Min	Max	
Average clock period	tCK(avg)	0.625	100	ns
Average High pulse width	tCH(avg)	0.46	0.54	tCK(avg)
Average Low pulse width	tCL(avg)	0.46	0.54	tCK(avg)
Absolute High clock pulse width	tCH(abs)	0.43	0.57	tCK(avg)



Parameter	Symbol	3200		Unit
		Min	Max	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	tCK(avg)
Clock period jitter	tJIT(per)	-40	40	ps
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	80	ps

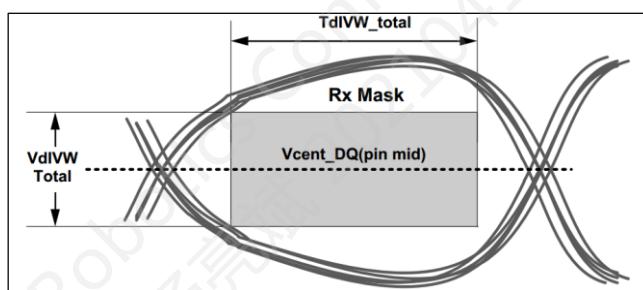
2.4.1.2 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are VdIVW and TdIVW.

The DQ input receiver mask for voltage and timing is shown in [Figure 2-7](#) is applied per pin. The total mask (VdIVW_total, TdIVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property and is not the valid data-eye.

Vcent_DQ(pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component.



[Figure 2-7 LPDDR4 DQ Receiver Mask](#)

[Figure 2-8](#) illustrates the DQ to DQS tDQS2DQ and tDQ2DQ timings at the DRAM pins referenced from the internal latch for the LPDDR4.

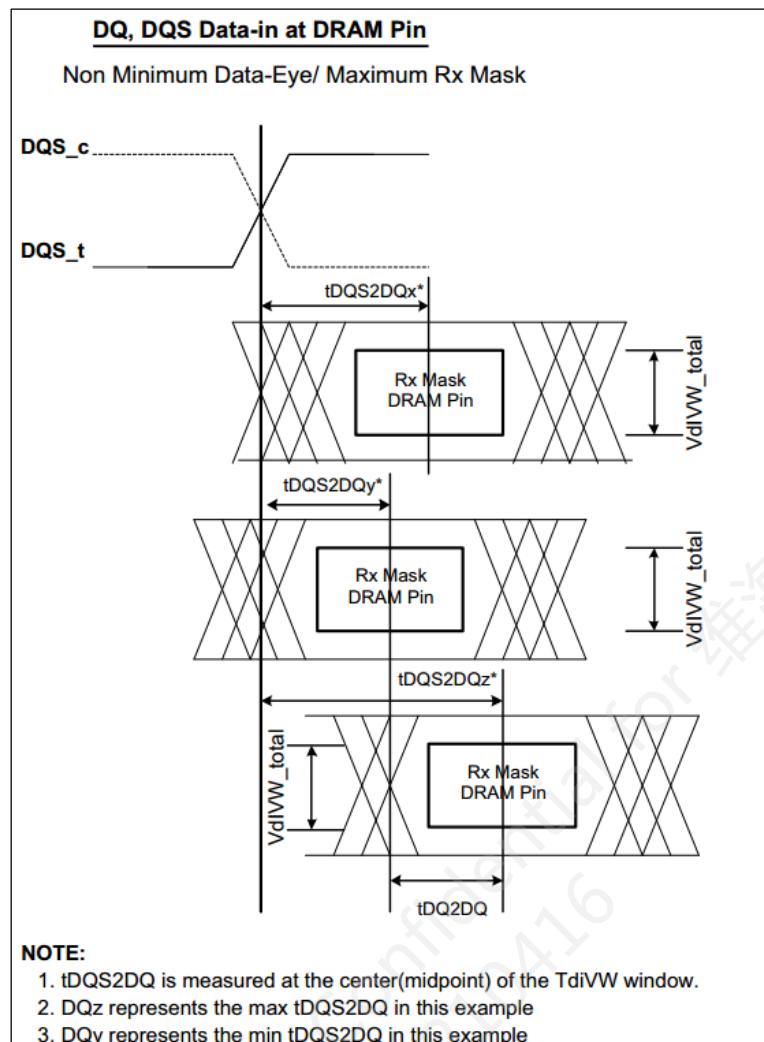


Figure 2-8 LPDDR4 DQ to DQS tDQS2DQ and tDQ2DQ Timings

Table 2-22 lists the write timing parameters of dqs_out relative to dq_out for the LPDDR4.

Table 2-22 LPDDR4 Write Timing Parameters of dqs_out Relative to dq_out

Parameter	Symbol	3200		Unit
		Min	Max	
Rx Mask voltage - p-p total	VdIVW_total	-	140	mV
Rx timing window total (At VdIVW voltage levels)	TdIVW_total	-	0.25	UI
DQ to DQS offset	tDQS2DQ	200	800	Ps
DQ to DQ offset	tDQ2DQ	-	30	ps



Write Timings of dqs_out Relative to CK

Figure 2-9 illustrates the write timing of dqs_out relative to CK for the LPDDR4.

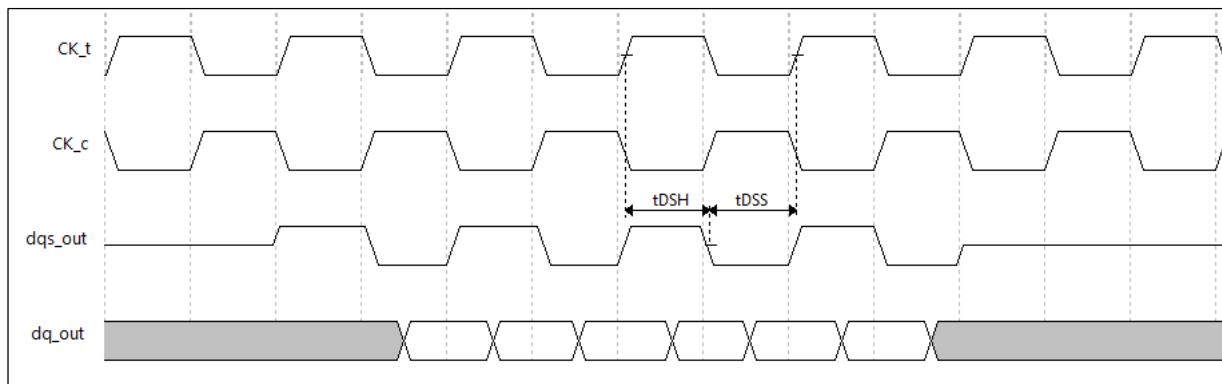


Figure 2-9 LPDDR4 Write Timing of dqs_out Relative to CK

Table 2-23 lists the write timing parameters of dqs_out Relative to CK for the LPDDR4.

Table 2-23 LPDDR4 Write Timing Parameters of dqs_out Relative to CK

Parameter	Symbol	3200		Unit
		Min	Max	
DQS falling edge to CK setup time	tDSS	0.2	-	tCK(avg)
DQS falling edge hold time from CK	tDSH	0.2	-	tCK(avg)

Write Timings of CMD/ADDR Relative to CK

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in Figure 2-10. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in Figure 2-10 is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to successfully capture a valid input signal; it is not the valid data-eye.

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component.

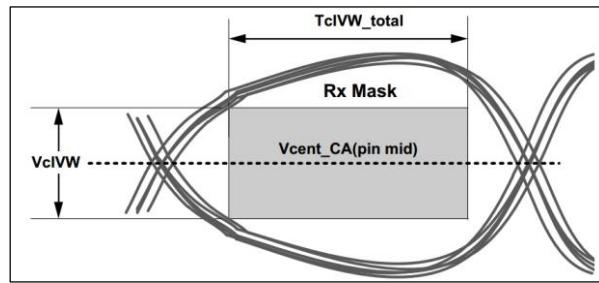


Figure 2-10 LPDDR4 CA Receiver Mask

Figure 2-11 illustrates the write timings of CMD/ADDR relative to CK for the LPDDR4.

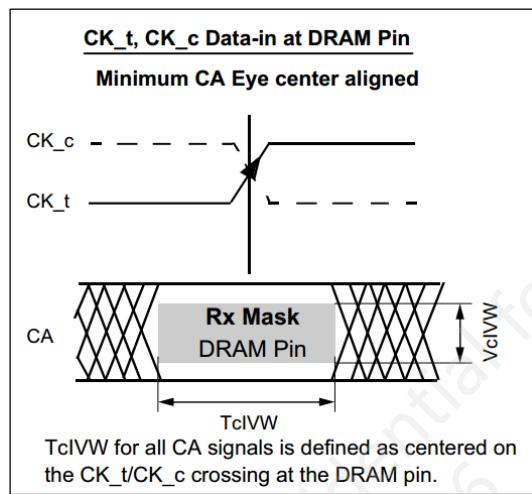


Figure 2-11 LPDDR4 CA Timings at the DRAM Pin

Table 2-24 lists LPDDR4 write timing parameters of CA Relative to CK for the LPDDR4.

Table 2-24 LPDDR4 Write Timing Parameters of CA Relative to CK

Parameter	Symbol	3200		Unit
		Min	Max	
Rx Mask voltage - p-p	VcIVW	-	155	mV
Rx timing window	TcIVW	-	0.3	UI

2.4.1.3 Read Timings

Read Timings of CMD/ADDR Relative to CK

The read timings of CMD/ADDR relative to CK are the same as [Write Timings of CMD/ADDR Relative to CK](#).

Read Timings of dqs_in Relative to dq_in

[Figure 2-12](#) illustrates the data read timing definitions tQH and tDQSQ across all DQ signals per DQS group for the LPDDR4.

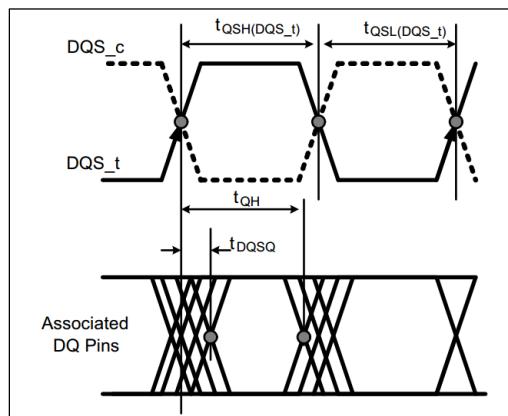


Figure 2-12 LPDDR4 Read Timing Definitions t_{QH} and t_{DQSQ}

Figure 2-13 illustrates the data read timing t_{QW} valid window defined per DQ signal for the LPDDR4.

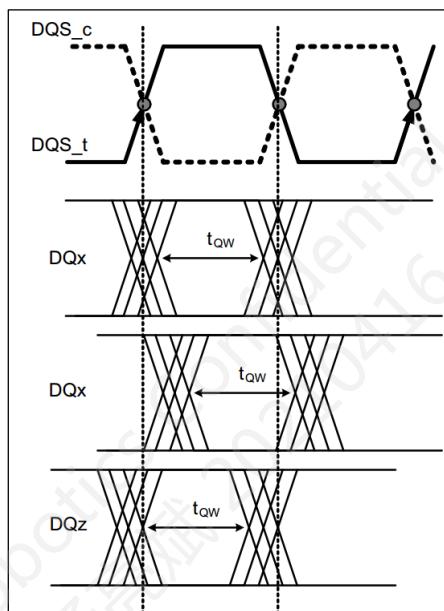


Figure 2-13 LPDDR4 Read Timing t_{QW} Valid Window per DQ Signal

Table 2-25 describes LPDDR4 Read Timing parameters of dqs_in Relative to dq_in.

Table 2-25 LPDDR4 Read Timing Parameters of dqs_in Relative to dq_in

Parameter	Symbol	3200		Unit
		Min	Max	
DQS_t, DQS_c to DQ Skew total, per group, per access	t_{DQSQ}	-	0.18	UI
DQ output hold time total from DQS_t,	t_{QH}	$\min(t_{QSH}, t_{QL})$	-	UI



Parameter	Symbol	3200		Unit
		Min	Max	
DQS_c (DBI-Disabled)				
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	min(tQSH_DBI, tQSL_DBI)	-	UI
DQ output window time total, per pin	tQW_total	0.7	-	UI
DQS, DQS# differential output low time (DBI- Disabled)	tQSL	tCL(abs) - 0.05	-	tCK(avg)
DQS, DQS# differential output high time (DBI- Disabled)	tQSH	tCH(abs) - 0.05	-	tCK(avg)
DQS, DQS# differential output low time (DBI- Enabled)	tQSL_DBI	tCL(abs) - 0.045	-	tCK(avg)
DQS, DQS# differential output high time (DBI- Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCK(avg)

2.4.2 MIPI CSI Host RX Timings

Table 2-26 and Table 2-27 list the MIPI CSI host RX timing parameters.

Table 2-26 Timing parameters of MIPI CSI RX HS Line Drivers

Parameter	Symbol	Min	Typ	Max	Unit
Maximum Serial Data rate (forward direction)	-	80	-	2500	Mbps
DDR CLK frequency	FDDRCLK	40	-	1250	MHz
DDR CLK duty cycle	tCDC	-	50%	-	-
DDR CLK/DATA Jitter	-	-	75	-	ps
UI instantaneous	UI _{INST}	0.5	-	12.5	ns

Table 2-27 Timing parameters of MIPI CSI RX Clock

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock Setup Time (RX)	T _{SETUP(RX)}	0.15	-	-	UI



Parameter	Symbol	Min	Typ	Max	Unit
Below 1Gbps					
Data to Clock Setup Time (RX) Below 1.5Gbps Above 1Gbps	T _{SETUP(RX)}	0.20	-	-	UI
Data to Clock Hold Time (RX) Below 1Gbps	T _{HOLD(RX)}	0.15	-	-	UI
Data to Clock HOLD Time (RX) Below 1.5Gbps Above 1Gbps	T _{HOLD(RX)}	0.20	-	-	UI
Static Data to Clock Skew (Channel) Above 1.5Gbps and below 2.5Gbps	t _{SKEW(TLIS)}	-0.10	-	0.10	UI
Channel Static Data to Clock Skew (Channel) Above 1.5Gbps and below 2.5Gbps	t _{SKEW(CH)}	-0.20	-	0.20	UI

2.4.3 MIPI CSI Device TX Timings

Table 2-28 and Table 2-29 list the MIPI CSI device TX timing parameters.

Table 2-28 MIPI TX Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Maximum Serial Data rate (forward direction)	-	80	-	2500	Mbps
DDR CLK frequency	F _{DDRCLK}	40	-	1250	MHz
DDR CLK duty cycle	t _{cDC}	-	50%	-	-
DDR CLK/DATA Jitter	-	-	75	-	ps
UI instantaneous	UI _{INST}	0.5	-	12.5	ns

Table 2-29 Timing parameters of MIPI CSI TX HS Line Drivers

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock Skew Below 1Gbps	t _{SKEW(TLIS)}	-0.20	-	0.20	UI
Data to Clock Skew Above 1Gbps and below 1.5Gbps	t _{SKEW(TLIS)}	-0.10	-	0.10	UI
Data to Clock Skew Below 1Gbps	t _{SKEW(TX)}	-0.15	-	0.15	UI
Data to Clock Skew	t _{SKEW(TX)}	-0.20	-	0.20	UI



Parameter	Symbol	Min	Typ	Max	Unit
Above 1Gbps and below 1.5Gbps					
Static Data to Clock Skew (TX)	tSKEW(TX)	-0.20	-	0.20	UI
Above 1.5Gbps and below 2.5Gbps					
Static Data to Clock Skew (Channel)	tSKEW(TLIS)	-0.10	-	0.10	UI
Above 1.5Gbps and below 2.5Gbps					
Dynamic Data to Clock Skew (TX)	tSKEW(TX)	-0.15	-	0.15	UI
Above 1.5Gbps and below 2.5Gbps					
Channel ISI	ISI	-	-	20	UI
Above 1.5Gbps and below 2.5Gbps					

2.4.4 SD/SDIO/eMMC Interface Timing

Figure 2-14 illustrates the single-edge data input and output timings of the SD/SDIO/eMMC interface.

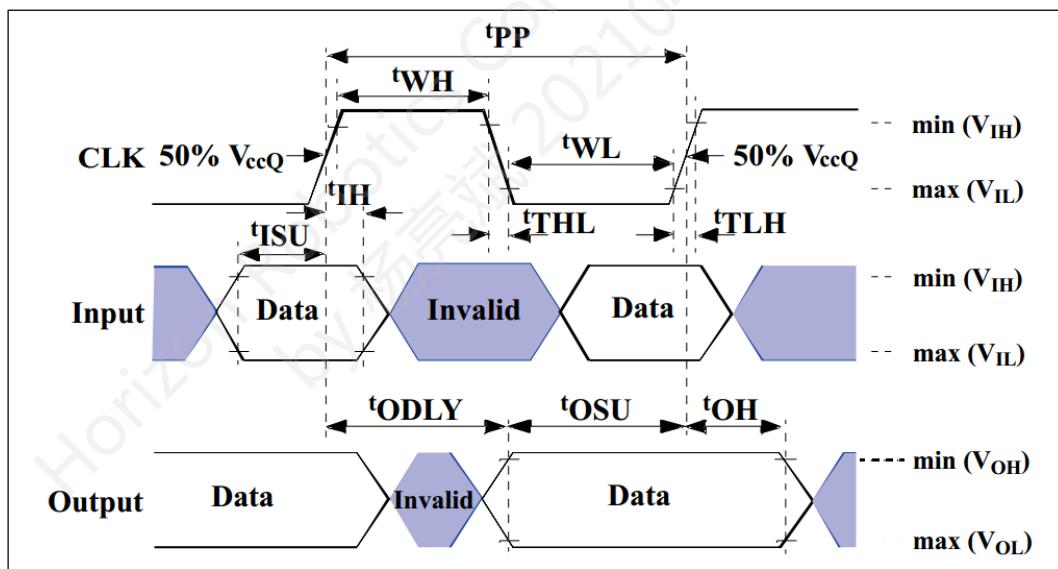


Figure 2-14 Single-edge Data Input and Output Timing Diagram

Table 2-30 lists the timing parameters of the SD/SDIO/eMMC interface.



Table 2-30 SD/SDIO/eMMC Timing Parameters

Speed Mode	Maximum Frequency (MHz)/Cycle (ns)		Minimum Hold Time	Minimum Setup Time	Maximum Output Delay of the Card	High Level Duration of the Card Clock
MMC_HS200	192MHz	5.21ns	0.8ns	1.4ns	10.66ns	(0.45~0.55) clock cycle
MMC_HS	48MHz	20.83ns	3.0ns	3.0ns	13.7ns	
SD_SDR104	192MHz	5.21ns	0.8ns	1.4ns	10.66ns	
SD_SDR50	96MHz	10.42ns	0.8ns	3.0ns	7.5ns	
SD_SDR25	48MHz	20.83ns	2.0ns	6.0ns	14ns	
SD_SDR12	24MHz	41.67ns	5.0ns	5.0ns	14ns	
SD_HS	48MHz	20.83ns	2.0ns	6.0ns	14ns	
SD_DS	24MHz	41.67ns	5.0ns	5.0ns	14ns	
Identification mode	400KHz	2.5 μ s	5.0ns	5.0ns	50ns	

2.4.5 BIFSD Interface Timing

The single-edge data input and output timings of the BIFSD interface is identical to the SD/SDIO/eMMC interface, as shown in [Figure 2-14](#).

[Table 2-31](#) lists the timing parameters of the BIFSD interface.

Table 2-31 BIFSD Timing Parameters

Speed Mode	Maximum Frequency (MHz)/Cycle (ns)		Minimum Hold Time	Minimum Setup Time	Maximum Output Delay of J3	High Level Duration of the Card Clock
MMC_HS200	200MHz	5ns	0.8ns	1.4ns	10ns	(0.45~0.55) clock cycle
MMC_HS	50MHz	20ns	3.0ns	3.0ns	13.7ns	
Identification mode	400KHz	2.5 μ s	5.0ns	5.0ns	50ns	

2.4.6 BIFSPI Interface Timing

[Figure 2-15](#) illustrates the BIFSPI slave timing with CPOL = 0 and CPHA = 0.

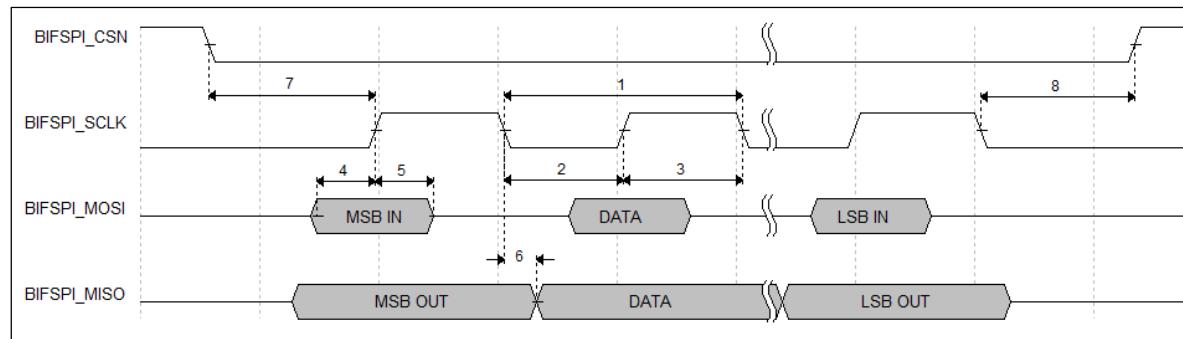


Figure 2-15 BIFSPI Slave Timing Diagram

Table 2-32 lists the BIFSPI slave timing parameters.

Table 2-32 BIFSPI Slave Timing Parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, BIFSPI_SCLK	T _c	15.2	-	-	ns
2	Pulse duration, BIFSPI_SCLK low	T _l	-	T _c /2	-	ns
3	Pulse duration, BIFSPI_SCLK high	T _h	-	T _c /2	-	ns
4	Setup time, BIFSPI_MOSI (input) valid before BIFSPI_SCLK (output) rising edge	T _{su}	T _c /2 - 2.5	-	-	ns
5	Hold time, BIFSPI_MOSI (input) valid after BIFSPI_SCLK (output) rising edge	T _{hd}	0	-	-	ns
6	Delay time, BIFSPI_SCLK (output) falling edge to BIFSPI_MISO (output) transition	T _d	0 - T _c /2	-	T _c /2 - 2	ns
7	Delay time, BIFSPI_CSN (output) falling edge to first BIFSPI_SCLK (output) rising edge	T _d (CS-SCK)	T _c /2	-	-	ns
8	Delay time, BIFSPI_SCLK (output) falling edge to BIFSPI_CSN (output) rising edge	T _d (SCK-CS)	1 T _c	-	-	ns

2.4.7 QSPI Interface Timing

Figure 2-16 illustrates the QSPI master timing with CPOL = 0 and CPHA = 0.

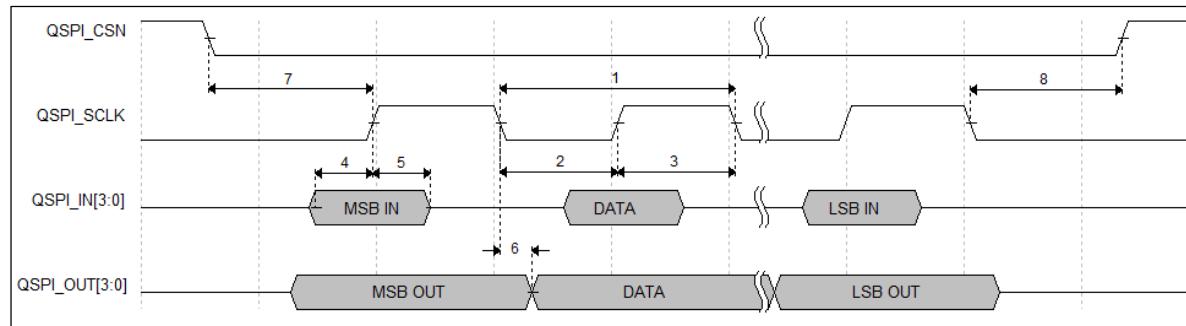


Figure 2-16 QSPI Master Timing (CPOL = 0, CPHA = 0) Diagram

Table 2-33 lists the QSPI timing parameters.

Table 2-33 QSPI Timing Parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, QSPI_SCLK	T _c	8	-	-	ns
2	Pulse duration, QSPI_SCLK low	T _l	-	T _c /2	-	ns
3	Pulse duration, QSPI_SCLK high	T _h	-	T _c /2	-	ns
4	Setup time, QSPI_MISO (input) valid before QSPI_SCLK (output) rising edge	T _{su}	T _c /2 - 2.3	-	-	ns
5	Hold time, QSPI_MISO (input) valid after QSPI_SCLK (output) rising edge	T _{hd}	0	-	-	ns
6	Delay time, QSPI_SCLK (output) falling edge to QSPI_MOSI (output) transition	T _d	0 - T _c /2	-	T _c /2 - 2	ns
7	Delay time, QSPI_CS (output) falling edge to first QSPI_SCLK (output) rising edge	T _d (CS - SCK)	T _c /2	-	-	ns
8	Delay time, QSPI_SCLK (output) falling edge to QSPI_CS (output) rising edge	T _d (SCK-CS)	1 T _c	-	-	ns

2.4.8 SPI Interface Timing

Figure 2-17 illustrates the SPI master timing diagram with CPOL = 0 and CPHA = 0.

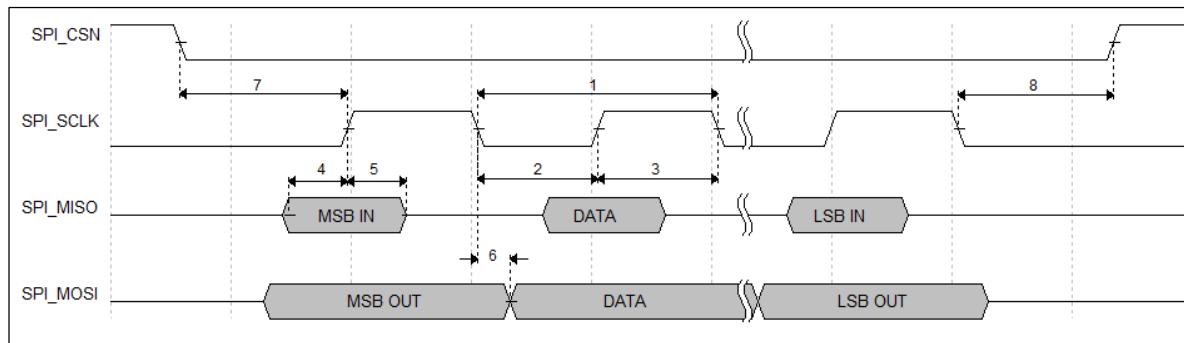


Figure 2-17 SPI Master Timing (CPOL = 0, CPHA = 0) Diagram

Table 2-34 lists the SPI timing parameters.

Table 2-34 SPI Timing Parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit
1	Cycle time, SPI_SCLK	T _c	21.3	-	-	ns
2	Pulse duration, SPI_SCLK low	T _l	-	T _c /2	-	ns
3	Pulse duration, SPI_SCLK high	T _h	-	T _c /2	-	ns
4	Setup time, SPI_MISO (input) valid before SPI_SCLK (output) rising edge	T _{su}	T _c /2 - 4	-	-	ns
5	Hold time, SPI_MISO (input) valid after SPI_SCLK (output) rising edge	T _{hd}	0	-	-	ns
6	Delay time, SPI_SCLK (output) falling edge to SPI_MOSI (output) transition	T _d	3 - T _c /2	-	T _c - 3.5	ns
7	Delay time, SPI_CS_N (output) falling edge to first SPI_SCLK (output) rising edge	T _{d(CS-CK)}	T _c /2	3.5 T _c	14.5 T _c	ns
8	Delay time, SPI_SCLK (output) falling edge to SPI_CS_N (output) rising edge	T _{d(CK-CS)}	1 T _c	4 T _c	15 T _c	ns

2.4.9 EMAC Interface Timing

Figure 2-18 illustrates the RGMII (1000 Mbps max) RX timing diagram.

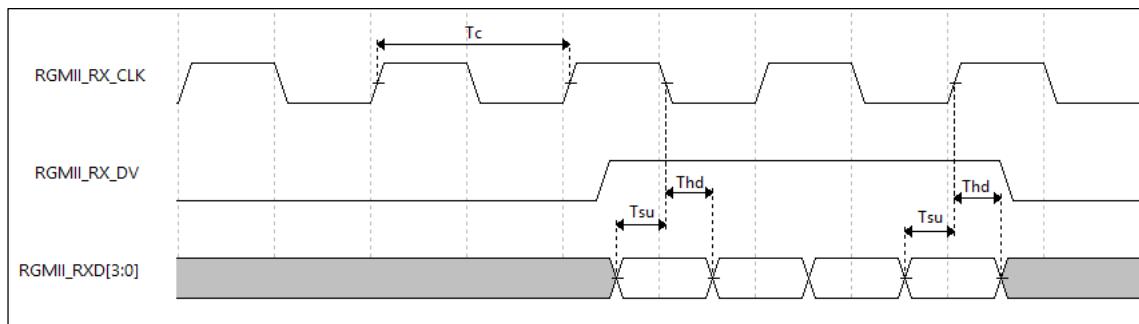


Figure 2-18 RGMII RX Timing Diagram

Figure 2-19 illustrates the RGMII (1000 Mbps max) TX timing diagram.

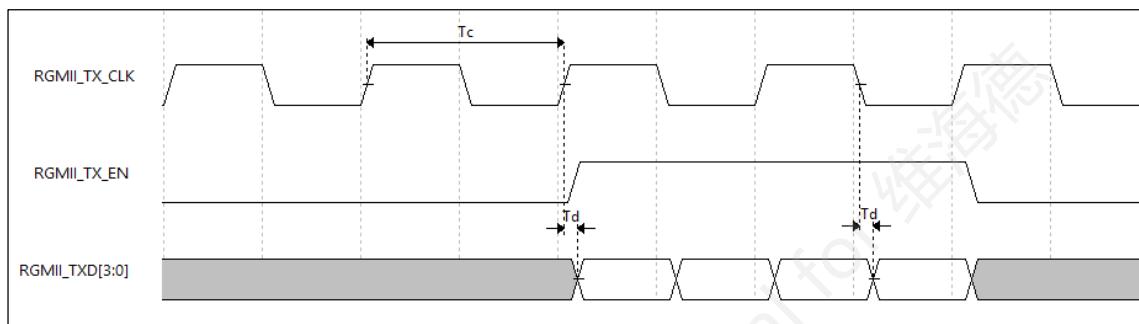


Figure 2-19 RGMII TX Timing Diagram

Table 2-35 lists the RGMII timing parameters.

Table 2-35 RGMII TX/RX Timing Parameters

Parameter	Symbol	Signal	Min	Max	Unit
RGMII clock cycle	T _c	RGMII_TX_CLK RGMII_RX_CLK	7.2	8.8	ns
RGMII signal setup time	T _{su} (RX)	RGMII_RX_DV RGMII_RXD[3:0]	1.2	-	ns
RGMII signal hold time	T _{hd} (RX)	RGMII_RX_DV RGMII_RXD[3:0]	1.2	-	ns
RGMII output signal delay	T _d (TX)	RGMII_TX_EN RGMII_TXD[3:0]	-0.5	0.5	ns

2.4.10 DVP IN Interface Timing

Figure 2-20 illustrates the DVP input interface timing diagram.

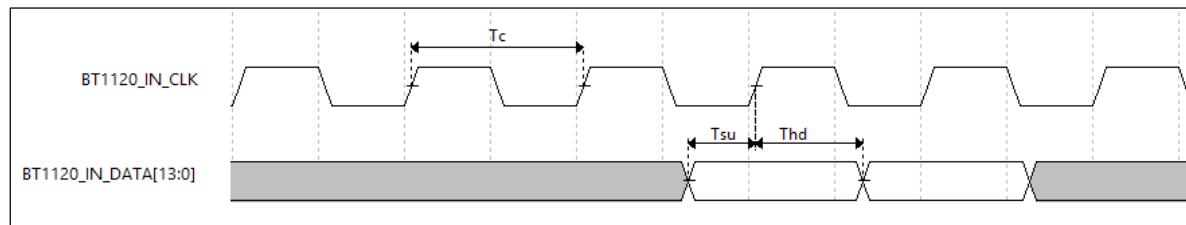


Figure 2-20 DVP Input Timing Diagram

Table 2-36 lists the timing parameters of the DVP input interface.

Table 2-36 DVP Input Timing Parameters

Parameter	Symbol	Signal	Min	Max	Unit
DVP IN clock cycle	T _c	BT1120_OUT_CLK	6.25	-	ns
DVP IN signal setup time	T _{su}	BT1120_OUT_DATA[13:0]	1.5	-	ns
DVP IN signal hold time	T _{hd}	BT1120_OUT_DATA[13:0]	1.5	-	ns

2.4.11 Parallel RGB OUT Interface Timing

Figure 2-21 illustrates the DVP output interface timing diagram.

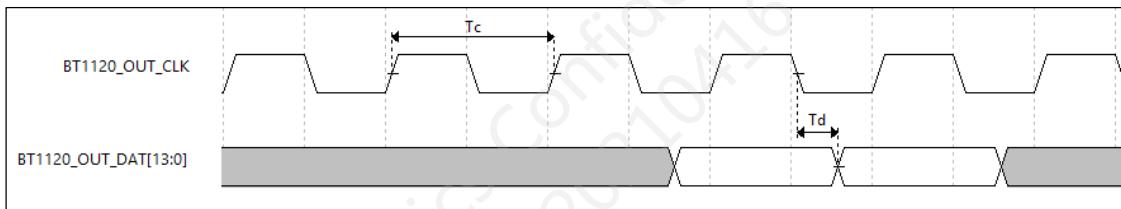


Figure 2-21 Parallel RGB Output Timing Diagram

Table 2-37 lists the timing parameters of the Parallel RGB output interface.

Table 2-37 Parallel RGB Output Timing Parameters

Parameter	Symbol	Signal	Min	Max	Unit
RGB888 OUT clock cycle	T _c	BT1120_OUT_CLK	6.12	-	ns
RGB888 OUT signal delay	T _d	BT1120_OUT_DAT[15:0]	1.1 - T _c /2	T _c /2 - 0.7	ns

2.4.12 BT1120 OUT Interface Timing

Figure 2-22 illustrates the BT1120 output interface timing diagram.

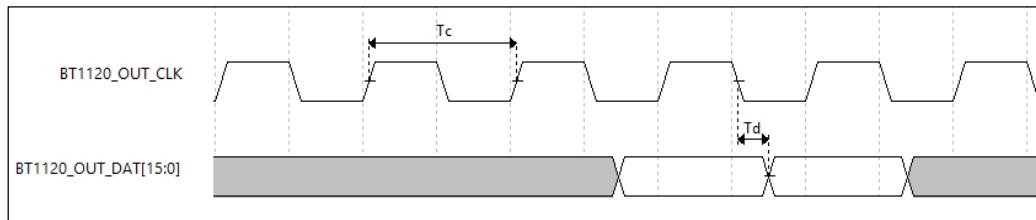


Figure 2-22 BT1120 Output Timing Diagram

Table 2-38 lists the timing parameters of the BT1120 output interface.

Table 2-38 BT1120 Output Timing Parameters

Parameter	Symbol	Signal	Min	Max	Unit
BT1120 OUT clock cycle	T _c	BT1120_OUT_CLK	6.12	-	ns
BT1120 OUT signal delay	T _d	BT1120_OUT_DAT[15:0]	1.1 - T _c /2	T _c /2 - 0.7	ns

2.4.13 I2S Interface Timing

Figure 2-23 illustrates the I2S slave mode input timing diagram.

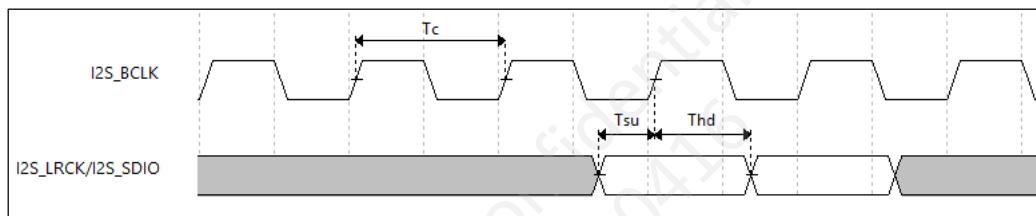


Figure 2-23 I2S Input Timing Diagram

Table 2-39 lists the I2S input timing parameters.

Table 2-39 I2S Input Timing Parameters

Parameter	Symbol	Signal	Min	Typ	Max	Unit
I2S clock cycle	T _c	I2S_BCLK	-	325.52	-	ns
I2S IN signal setup time	T _{su}	I2S_LRCK I2S_SDIO	T _c /2 - 10	-	-	ns
I2S IN signal hold time	T _{hd}	I2S_LRCK I2S_SDIO	T _c /2	-	-	ns

Figure 2-24 illustrates the I2S slave mode output timing diagram.

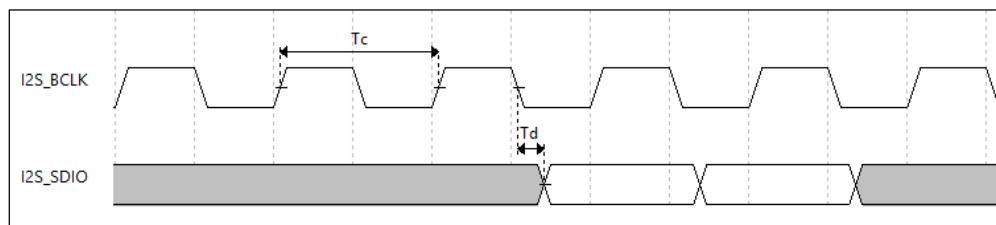


Figure 2-24 I2S Output Timing Diagram

Table 2-40 lists the I2S output timing parameters.

Table 2-40 I2S Output Timing Parameters

Parameter	Symbol	Signal	Min	Typ	Max	Unit
I2S clock cycle	Tc	I2S_BCLK	-	325.52	-	ns
I2S OUT signal delay	Td	I2S_SDIO	-Tc/2	-	Tc/2 - 11	ns

2.4.14 JTAG Interface Timing

Figure 2-25 illustrates the JTAG timing diagram.

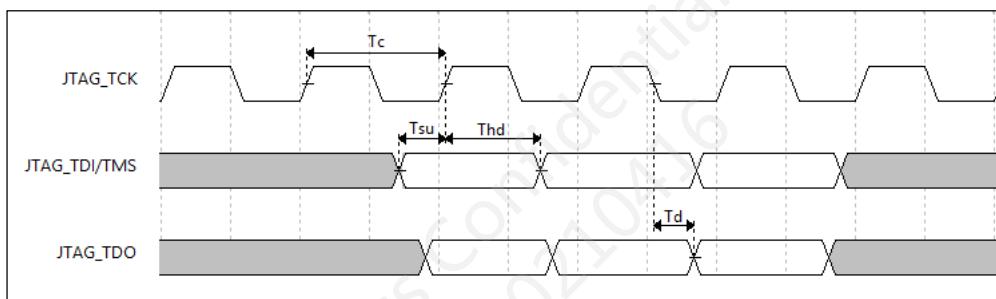


Figure 2-25 JTAG Timing Diagram

Table 2-41 lists the JTAG timing parameters.

Table 2-41 JTAG Timing Parameters

Parameter	Symbol	Signal	Min	Max	Unit
JTG_TCK clock cycle	Tc	JTG_TCK	50	-	ns
JTG_TDI/TMS signal setup time	Tsu	JTG_TDI, JTG_TMS	15	-	ns
JTG_TDI/TMS signal hold time	Thd	JTG_TDI, JTG_TMS	15	-	ns
JTG_TDO signal delay	Td	JTG_TDO	0	14	ns



3 System Architecture

This chapter describes the architecture for the system level clocks, reset control, power management and low-power mode, and interrupt system.

3.1 Clock Structure

3.1.1 Overview

The Clock Generator manages clock input, clock generation, and clock control in a uniform manner as follows:

- Manages and control clock inputs.
- Divides and controls clock frequencies.
- Generates working clocks for each module.

The Clock Generator generates clocks for all the chip blocks. It selects one of the system clock sources to supply the system clock, and also controls the system clock selection. A set of clock generation registers controls the clock dividers that are used for divided system and peripheral clock generation.

The device implements seven PLLs:

- ARMPPLL – For the quad-core Cortex-A53 processor.
- DDRPLL – For the DDR subsystem.
- VIOPLL – For the VIO subsystem.
- VIOPLL2 – For the Camera Sensor MCLK/IAR Display Pixel Clock
- CNNPLL – For the BPU subsystem.
- PERIPHPLL – For the PERI subsystem.
- SYSPPLL – For the CPU subsystem.

3.2 Reset Structure

3.2.1 Overview

The reset management module resets the entire chip and each functional module in a uniform manner as follows:

- Manages and controls power-on reset.
- Manages and controls watchdog reset.
- Manages and controls IO reset.
- Controls the software reset of each functional module.
- Synchronizes reset signals to the clock domain corresponding to each module.
- Generates reset signals of the functional modules in the chip.



3.2.2 Reset Control

Table 3-1 lists the types of reset signals that are categorized based on the reset ss.

Table 3-1 Types of Reset Signals

Type	Description
Global hard reset signal (RSTN)	Globally resets the entire chip.
Power-on reset (core_pd_rstb)	Globally resets almost the entire chip except the PMU subsystem.
Local reset signal (xx_rsten)	Separately resets each module of the chip, initiated by software.
Watchdog reset signal (wdt_rstb)	The same as power-on reset.

3.2.3 Reset Sources

Table 3-2 lists the destructive and functions reset sources of the device by module.

Table 3-2 Reset Source List

Module	Reset Sources			
	Power-on Reset	SW Reset	WDG Reset	IO Reset
PMU Subsystem				
PMU/PADC/RTC /SYSCNT	ao_rstb	-	-	RSTN
CPU Subsystem				
A53	core_pd_rstb	core_warmrstn[1:0]	wdt_rstb	-
Coresight	core_pd_rstb	dbg_pclk_rsten atb_atclk_rsten atb_tsclk_rsten armv8pil_clk_rsten ctxpiu_clkin_rsten	wdt_rstb	JTG_TRSTN
DMAC	core_pd_rstb	sys_dmac_rsten	wdt_rstb	-
BIFSPI	core_pd_rstb	sys_bifspi_rsten ⁽¹⁾ sys_bifspi_shreg_rsten	wdt_rstb	BIFSPI_RSTN ⁽¹⁾
BIFSD	core_pd_rstb	sys_bifsd_rsten ⁽²⁾	wdt_rstb	BIFSD_RSTN ⁽²⁾
ROMC	core_pd_rstb	sys_romc_rsten	wdt_rstb	-
SRAMC	core_pd_rstb	sys_sramc_rsten	wdt_rstb	-
GIC	core_pd_rstb	sys_gic_rsten	wdt_rstb	-



Module	Reset Sources			
	Power-on Reset	SW Reset	WDG Reset	IO Reset
QSPI	core_pd_rstb	sys_qspi_rsten	wdt_rstb	-
Timer0	core_pd_rstb	timer0_rsten	wdt_rstb	-
Timer1	core_pd_rstb	timer1_rsten	wdt_rstb	-
Timer2	core_pd_rstb	timer2_rsten	wdt_rstb	-
DDR Subsystem				
DDRC	core_pd_rstb	core_ddrc_rsten presetn_ctrl_rsten presetn_phy_rsten ddrc_port0_rsten ddrc_port1_rsten ddrc_port2_rsten ddrc_port3_rsten ddrc_port4_rsten ddrc_port5_rsten ddrc_port6_rsten ddrc_port7_rsten ddrc_port8_rsten	wdt_rstb	-
VIO Subsystem				
SIF	core_pd_rstb	sif_mclk_rsten dvp_pix_clk_rsten bt_pix_clk_rsten	wdt_rstb	-
MIPI	core_pd_rstb	mipi_ipi_clk_rsten mipi_cfg_clk_rsten	wdt_rstb	-
IAR	core_pd_rstb	iar_pix_clk_rsten	wdt_rstb	-
PYM	core_pd_rstb	pym_mclk_rsten	wdt_rstb	-
BPU Subsystem				
CNN0	core_pd_rstb	cnn0_rsten	wdt_rstb	-
CNN1	core_pd_rstb	cnn1_rsten	wdt_rstb	-
PERI Subsystem				
UART0	core_pd_rstb	uart0_rsten	wdt_rstb	-
UART1	core_pd_rstb	uart1_rsten	wdt_rstb	-
UART2	core_pd_rstb	uart2_rsten	wdt_rstb	-



Module	Reset Sources			
	Power-on Reset	SW Reset	WDG Reset	IO Reset
UART3	core_pd_rstb	uart3_rsten	wdt_rstb	-
SPI0	core_pd_rstb	spi0_rsten	wdt_rstb	-
SPI1	core_pd_rstb	spi1_rsten	wdt_rstb	-
SPI2	core_pd_rstb	spi2_rsten	wdt_rstb	-
PWM0	core_pd_rstb	pwm0_rsten	wdt_rstb	-
PWM1	core_pd_rstb	pwm1_rsten	wdt_rstb	-
PWM2	core_pd_rstb	pwm2_rsten	wdt_rstb	-
I2C0	core_pd_rstb	i2c0_rsten	wdt_rstb	-
I2C1	core_pd_rstb	i2c1_rsten	wdt_rstb	-
I2C2	core_pd_rstb	i2c2_rsten	wdt_rstb	-
I2C3	core_pd_rstb	i2c3_rsten	wdt_rstb	-
I2C4	core_pd_rstb	i2c4_rsten	wdt_rstb	-
I2C5	core_pd_rstb	i2c5_rsten	wdt_rstb	-
SD0	core_pd_rstb	sd0_rsten	wdt_rstb	-
SD1	core_pd_rstb	sd1_rsten	wdt_rstb	-
SD2	core_pd_rstb	sd2_rsten	wdt_rstb	-
ETH0	core_pd_rstb	eth0_rsten	wdt_rstb	-
I2S0	core_pd_rstb	i2s0_rsten	wdt_rstb	-
I2S1	core_pd_rstb	i2s1_rsten	wdt_rstb	-

- (1) Keep BIFSPI_RSTN high during system boot up. Otherwise, when BIFSPI_RSTN is asserted, the CPU will hang up when CPU accesses the BIFSPI shared register.
- (2) Keep BIFSD_RSTN high during system boot up, Otherwise, when BIFSD_RSTN is asserted, the CPU will hang up when CPU accesses the BIFSD shared register.

3.3 Power Management and Power Modes

3.3.1 Overview

The X3M includes a robust power management infrastructure that enables applications to select among various operational and low-power modes. In low-power mode, the power consumption of the chip is reduced effectively.

3.3.2 Power Domains

Figure 3-1 illustrates the separate power domains of the chip in more detail. The PMU



subsystem and digital IOs are in the always-on power domain, and other subsystems of the chip are in the main powered-down domains - voltage domain, power domain, or voltage + power domain. In sleep mode, other areas of the chip except the always-on power domain are powered off. At this time, the power consumption of the entire chip is the minimum.

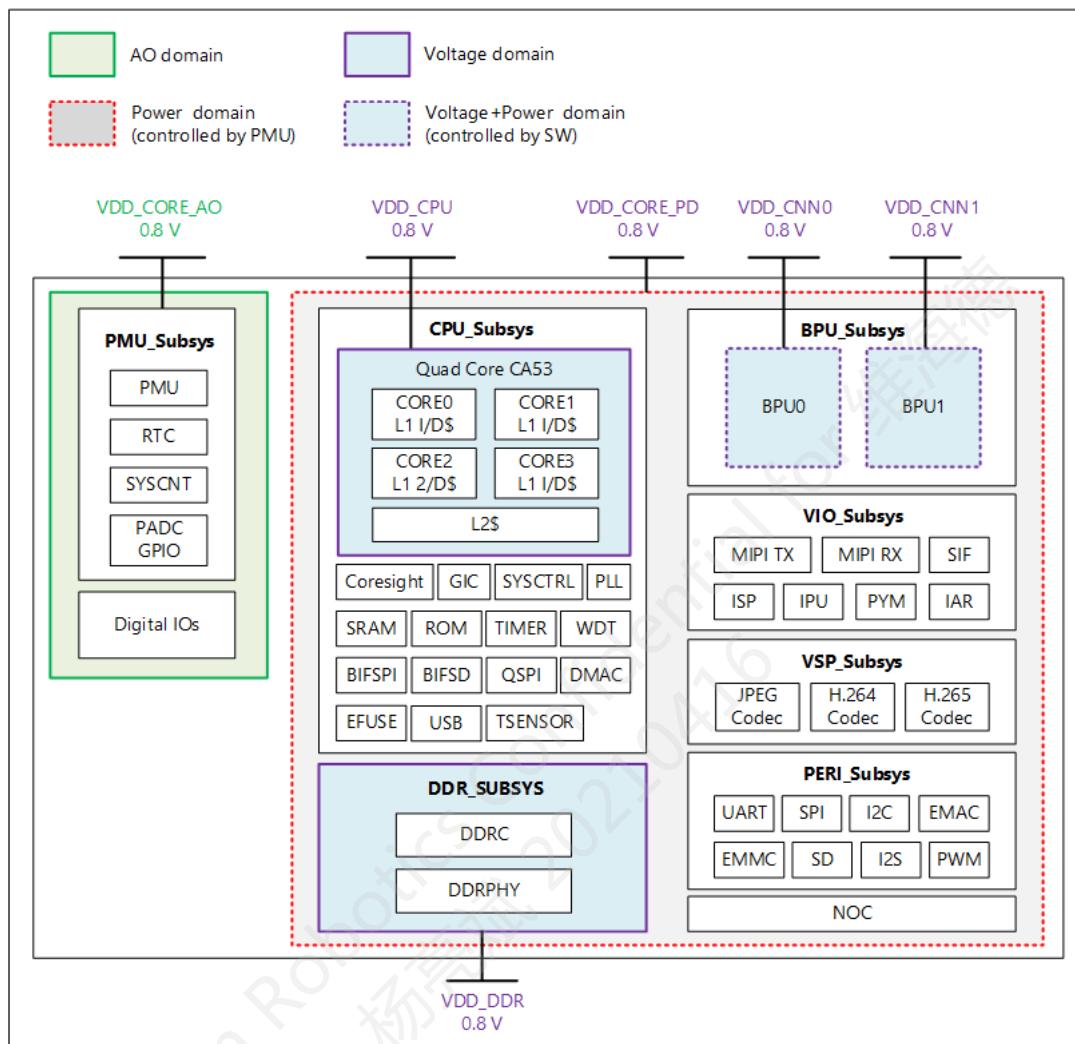


Figure 3-1 Power Domain Block Diagram

The Power Management Unit (PMU) Controller controls the power-on and power-off timings of the chip. It also controls the power supply to turn on or off the chip.

VDD_CPU, VDD_CNN0 and VDD_CNN1 voltage domains supports voltage and frequency scaling, which can run at different operating voltages depending on the performance as required in the scenarios. Furthermore, VDD_CNN0 and VDD_CNN1 can be powered up and down via software.

3.3.3 Power Groups

Figure 3-2 shows the division of power supply groups in more detail. The power



supplies are classified into group based on the power-up/power-down requirements.

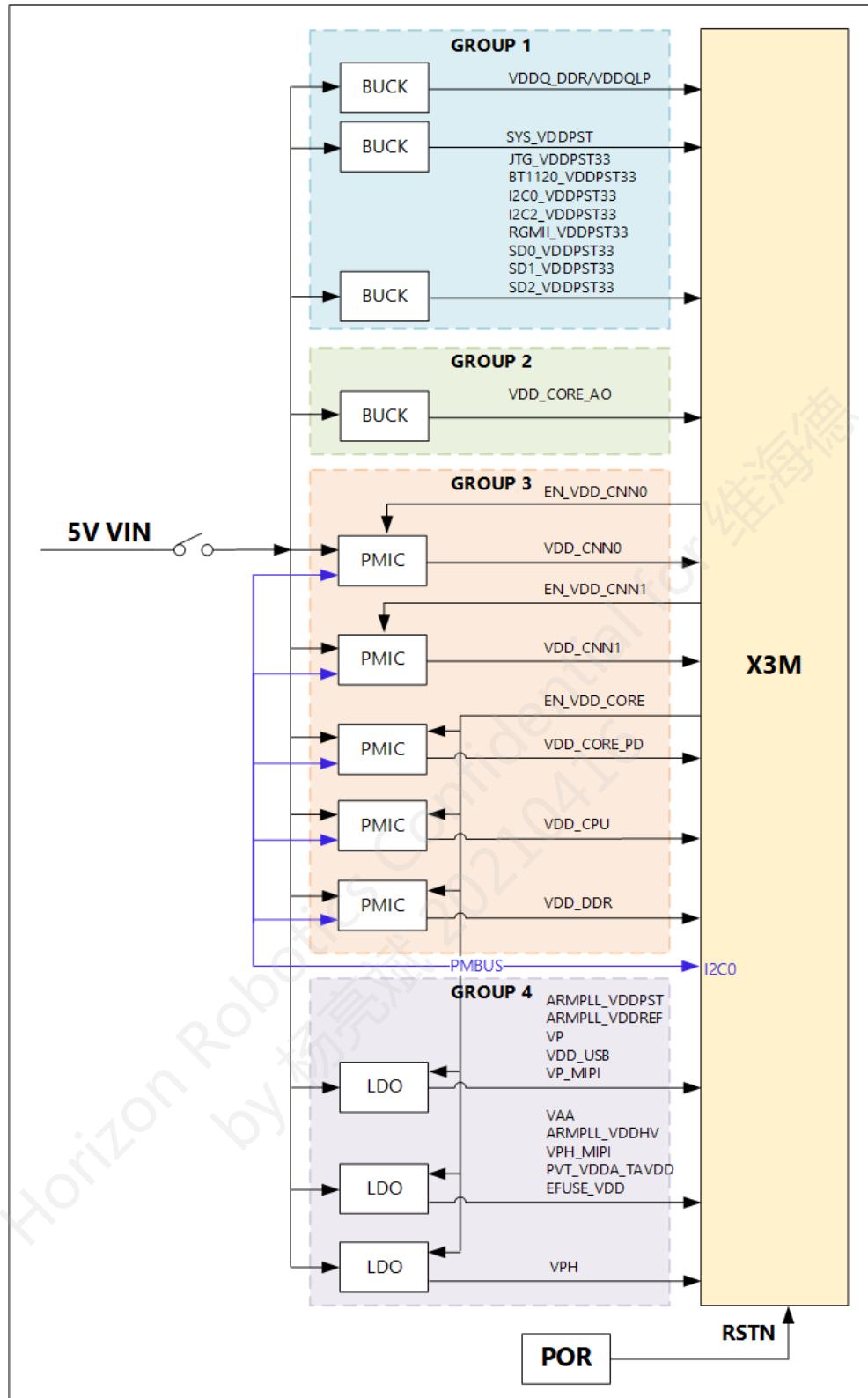


Figure 3-2 Power Group Tree

POR: internal power-on reset (POR) module.



RSTN: global hard reset signal.

EN_VDD_CNN0: powers up or powers down the VDD_CNN0 power supply via software.

EN_VDD_CNN1: powers up or powers down the VDD_CNN1 power supply via software.

EN_VDD_CORE: powers up or powers down the VDD_CORE_PD, VDD_CPU, VDD_DDR and the power group 4 power supplies simultaneously via PMU.

Table 3-3 lists the voltage, always-on and powered-down properties, and the maximum ramp rate for each power signal by power group.

Table 3-3 Power Groups

Power	Voltage	Property	Max Ramp Rate
Group 1			
SYS_VDDPST	1.8 V	Always-on	< 18 mV/us
SD0_VDDPST33	1.8 V	Always-on	
RGMII_VDDPST33	1.8 V/3.3 V	Always-on	
SD1_VDDPST33			
SD2_VDDPST33			
JTG_VDDPST33			
BIFSD_VDDPST33			
BIFSPI_VDDPST33			
BT1120_VDDPST33			
I2C0_VDDPST33			
I2C2_VDDPST33			
VDDQ_DDR	1.2 V (DDR4) 1.1 V (LPDDR4/4X)	Always-on	< 5 mV/us
VDDQLP	1.2 V (DDR4) 1.1 V (LPDDR4) 0.6 V (LPDDR4X)		
Group 2			
VDD_CORE_AO	0.8 V	Always-on	< 18 mV/us
Group 3			
VDD_CORE_PD	0.8 V	Powered-down	< 18 mV/us
VDD_CPU			
VDD_CNN0			
VDD_CNN1			
VDD_DDR			
Group 4			
ARMPPLL_VDDPST	0.8 V	Powered-down	-
ARMPPLL_VDDREF			



Power	Voltage	Property	Max Ramp Rate
ARMPPLL_VDDHV	1.8 V	Powered-down	-
VAA	1.8 V	Powered-down	< 5 mV/us
VDD_USB	0.8 V	Powered-down	< 100 mV/us
VP			
VP_MIPI			
VPH	3.3 V	Powered-down	< 18 mV/us
VPH_MIPI	1.8 V	Powered-down	
PVT_VDDA_TAVDD	1.8 V	Powered-down	< 60 mV/us
EFUSE_VDD	1.8 V	Powered-down	

3.3.4 Power Sequence

Power-Up Sequence

Figure 3-3 shows the timing diagram for the power-up sequence of the X3M.

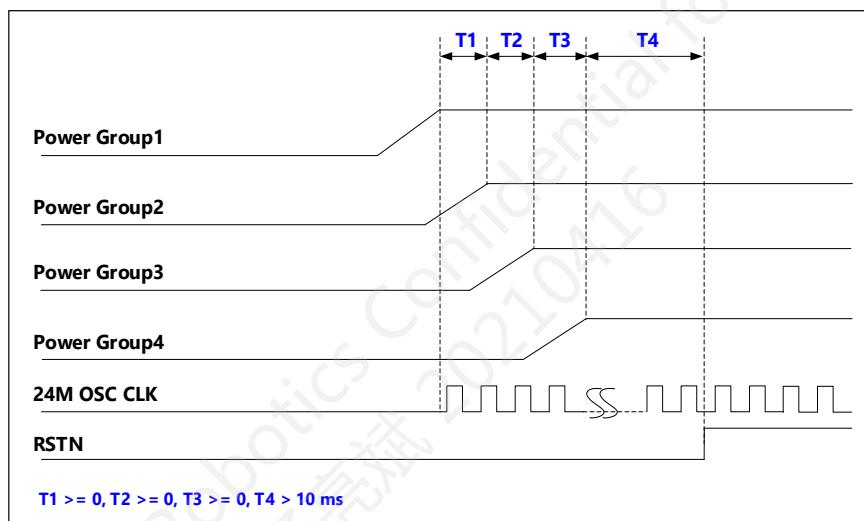


Figure 3-3 Power-Up Sequence

Power Group 2 must power up after Power Group 1 is up and stable. Power Group 3 must power up after Power Group 2 is up and stable. Power Group 4 must power up after Power Group 3 is up and stable. The RSTN is triggered to enter power-on mode after Power Group 4 is up more than 10 ms.

Delay between stages can vary. T1 is greater than or equal to 0. T2 is greater than or equal to 0. T3 is greater than or equal to 0. T4 must be greater than 10 ms.

Rise time within a group is flexible.

Power-Down Sequence

Figure 3-4 shows the timing diagram for the power-down sequence of the X3M.

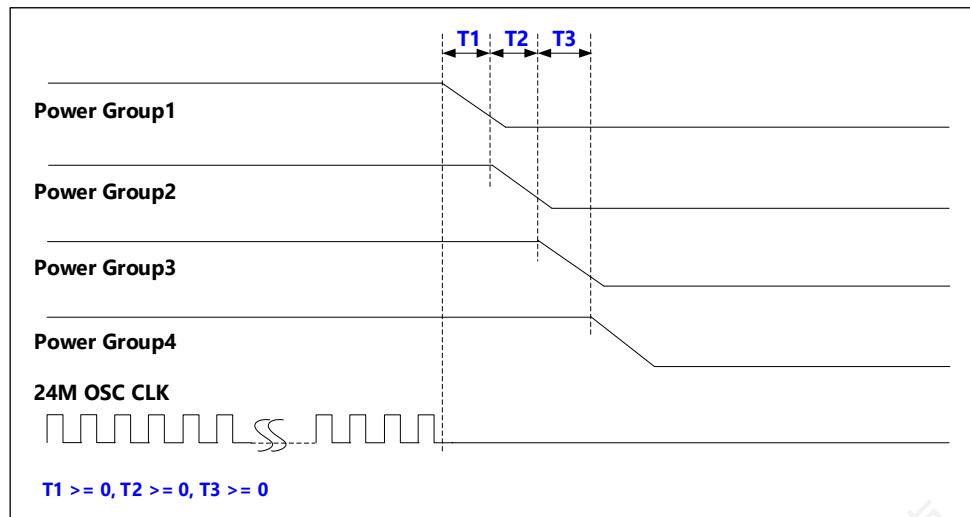


Figure 3-4 Power-Down Sequence

Power Group 2 must power down after Power Group 1 is down. Power Group 3 must power down after Power Group 2 is down. Power Group 4 must power down after Power Group 3 is down. Then the RSTN resets the entire chip.

Delay between stages can vary. T1 is greater than or equal to 0. T2 is greater than or equal to 0. T3 is greater than or equal to 0. T4 must be greater than 0.

Falling time within a group is flexible.

Enter Sleep Mode

Figure 3-5 shows the timing diagram for the enter sleep mode sequence of the X3M.

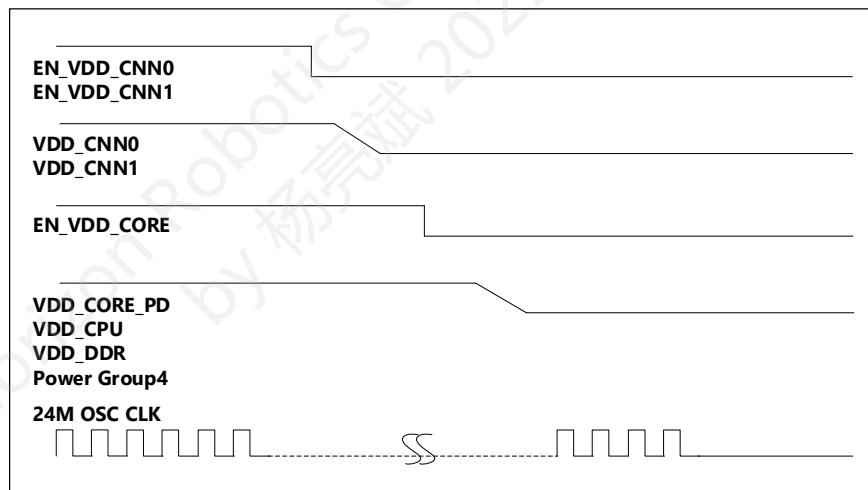


Figure 3-5 Enter Sleep Mode Sequence

Exit Sleep Mode

Figure 3-6 shows the timing diagram for the exit sleep mode sequence of the X3M.

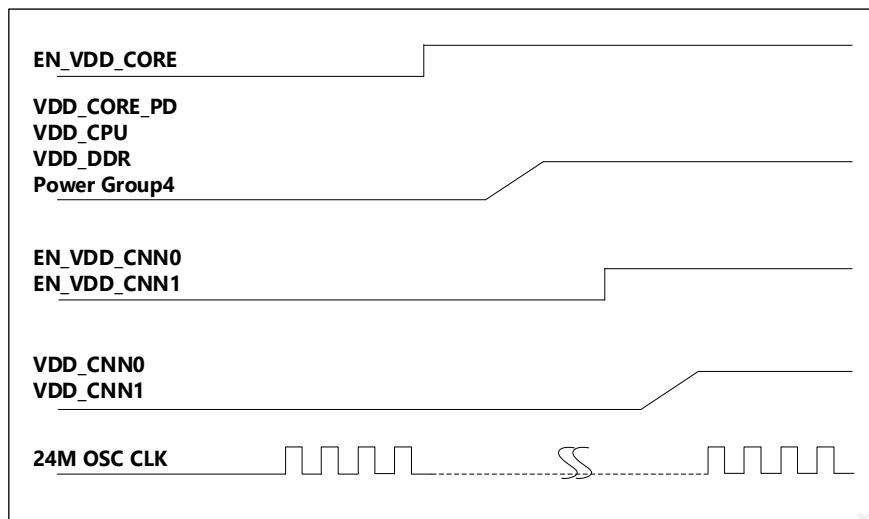


Figure 3-6 Exit Sleep Mode Sequence

3.3.5 Power Modes

The X3M power management supports the following power modes including:

- Normal Mode – This is the normal functional operating mode. In this mode, the CPU runs its normal operational mode.
- Sleep Mode – In this mode, almost the entire chip is powered down except for the always-on domain. The external DRAM enters self-refresh state so as to preserve the memory content. The chip can also wake up faster.
- Power Off – In this mode, the entire chip is powered down.

The power domains can be controlled independently to give different combinations of powered-up and powered-down domains. **Table 3-4** lists the powered-up and powered-down domain combinations for each power mode of operation.

Table 3-4 Power On/Off State for Power Mode

VDD_CORE_AO	Power Group 1	VDD_CORE_PD	VDD_CPU	VDD_DDR	VDD_CNN0	VDD_CNN1	Power Group 4
Power Off							
Off	Off	Off	Off	Off	Off	Off	Off
Sleep Mode							
On	On	Off	Off	Off	Off	Off	Off
Normal Mode							
On	On	On	On	On	On/Off	On/Off	On

(1) On = Block is powered up.

(2) Off = Block is powered down.



3.4 Interrupt Maps

This section describes the interrupt assignment details of the X3M.

3.4.1 SGI Interrupt Maps

Table 3-5 lists the detailed mapping between the IRQ number and the corresponding Software Generated Interrupt (SGI) source.

Table 3-5 SGI Interrupt Maps

IRQ ID	Interrupt Source
0	Software interrupt 1
1	Software interrupt 2
2	Software interrupt 3
3	Software interrupt 4
4	Software interrupt 5
5	Software interrupt 6
6	Software interrupt 7
7	Software interrupt 8
8	Software interrupt 9
9	Software interrupt 10
10	Software interrupt 11
11	Software interrupt 12
12	Software interrupt 13
13	Software interrupt 14
14	Software interrupt 15
15	Software interrupt 16

3.4.2 PPI Interrupt Maps

Table 3-6 lists the detailed mapping between the IRQ number and the corresponding Private Peripheral Interrupt (PPI) source.

Table 3-6 PPI Interrupt Maps

IRQ ID	Interrupt Source	Description
25	-	Virtual Maintenance IRQ, not used in the chip
26	CORE[n].nCNTHPIRQ	Hypervisor Physical Timer IRQ, low active
27	CORE[n].nCNTVIRQ	Virtual Timer IRQ, low active



IRQ ID	Interrupt Source	Description
28	-	Legacy FIQ, not used in the chip
29	CORE[n].nCNTPSIRQ	Secure Physical Timer IRQ, low active
30	CORE[n].nCNTPNSIRQ	Non-Secure Physical Timer IRQ, low active
31	-	Legacy IRQ, not used in the chip

3.4.3 SPI Interrupt Maps

Table 3-7 lists the detailed mapping between the IRQ number and the corresponding Shared Peripheral Interrupt (SPI) source.

Table 3-7 SPI Interrupt Maps

IRQ ID	Interrupt Source	Description
32	CORE[0].CTIIRQ	Edge triggered, rising edge active
33	CORE[1].CTIIRQ	
34	CORE[2].CTIIRQ	
35	CORE[3].CTIIRQ	
36	CORE[0].COMMIRQ	High active (The original CPU output is low active, and is inverted when connected for keeping consistent with SPI.)
37	CORE[1].COMMIRQ	
38	CORE[2].COMMIRQ	
39	CORE[3].COMMIRQ	
40	CORE[0].PMUIRQ	
41	CORE[1].PMUIRQ	
42	CORE[2].PMUIRQ	
43	CORE[3].PMUIRQ	
44	CPU.EXTERRIRQ	
45	timer0_irq0	High active
46	timer0_irq1	High active
47	timer0_irq2	High active
48	timer1_irq0	High active
49	timer1_irq1	High active
50	timer1_irq2	High active
51	timer2_irq0	High active
52	timer2_irq1	High active
53	timer2_irq2	High active
54	bifspi_irq	High active
55	bifsd_irq	High active



IRQ ID	Interrupt Source	Description
56	dmac_irq	High active
57	qspi_irq	High active
58	usb_irq	High active
59	ddrc_irq	High active
60	ddrphy_irq	High active
61	uart0_irq	High active
62	uart1_irq	High active
63	uart2_irq	High active
64	uart3_irq	High active
65	spi0_irq	High active
66	spi1_irq	High active
67	spi2_irq	High active
68	i2s0_irq	High active
69	i2s1_irq	High active
70	i2c0_irq	High active
71	i2c1_irq	High active
72	i2c2_irq	High active
73	i2c3_irq	High active
74	i2c4_irq	High active
75	i2c5_irq	High active
76	pwm0_irq	High active
77	pwm1_irq	High active
78	pwm2_irq	High active
79	sd0_irq	High active
80	sd1_irq	High active
81	sd2_irq	High active
82	eth0_ch_rx_irq	High active
83	eth0_ch_tx_irq	High active
84	eth0_irq	High active
85	rtc_irq	High active
86	padc_irq	High active
87	cnn0_irq	High active
88	cnn1_irq	High active
89	mipi_csi_host0_irq	High active



IRQ ID	Interrupt Source	Description
90	mipi_csi_host1_irq	High active
91	mipi_csi_host2_irq	High active
92	mipi_csi_host3_irq	High active
93	mipi_tx_host_irq	High active
94	mipi_tx_dev_irq	High active
95	Perf_monitor_irq	High active
96	pvt_irq	High active
97	apb_timeout_irq	High active
98	vpu_irq	High active
99	jpg_irq	High active
100	lpwm_irq	Rising edge trigger
101	iar_irq	High active
102	sif_irq	High active
103	isp0_irq	High active
104	isp1_irq	High active
105	dwe0_irq	High active
106	gdc0_irq	High active
107	ldc0_irq	High active
108	t2l0_irq	High active
109	dwe1_irq	High active
110	gdc1_irq	High active
111	ldc1_irq	High active
112	t2l1_irq	High active
113	ipu0_irq	High active
114	ipu1_irq	High active
115	pym_irq	High active
116	md_irq	High active
117	ips_irq	High active
118	aes_irq	High active
119	pka_irq	High active
120	dma_isp_irq	High active
121	ipi0_irq/pi1_irq	High active ipi0_irq is for CA53 gic ipi1_irq is for CR5 gic
122	sec_fw_irq	High active



IRQ ID	Interrupt Source	Description
123	trng_irq	High active
124	noc_perf_mon_intr	High active
125	ddr_ecc_irq	High active
126~127	Reserved	-



4 CPU Subsystem

4.1 Quad Core A53 CPU

4.1.1 Introduction

The X3M CPU subsystem is based on the low-power ARM® Cortex®-A53 processor that implements the ARMv8-A architecture. The Cortex-A53 processor has four cores, each with an L1 memory system and a single shared L2 cache.

The Cortex-A53 processor supports the Advanced SIMD and Scalar Floating-point instructions in the A64 instruction set, and the Advanced SIMD and VFP instructions in the A32 and T32 instruction sets.

The Cortex-A53 processor also supports Dynamic Voltage and Frequency Scaling (DVFS) for power saving.

4.1.1.1 Features

The quad core A53 CPU has the following key features:

- Quad-core ARM® Cortex®-A53 processor, with 32 KB/32 KB L1 I/D cache and 512 KB L2 cache.
- Supports FPU.
- Supports NEON SIMD.
- Separate VDD_CPU voltage domain, up to 1.2 GHz @ nominal VDD_CPU.
- Supports Dynamic Voltage and Frequency Scaling (DVFS).
- Supports warm reset for each core and the reboot address can be redirected by the software configurable register.

4.2 CoreSight Debug and Trace

4.2.1 Introduction

The debug and trace architecture in the X3M is based on ARM® CoreSight™ SoC-400 that provides a powerful, modular debug and trace infrastructure and tool chain. As multicore applications are more common-place, debug and trace solutions become critical to SoC designers and software developers. The CoreSight SoC-400 provides improved productivity for all parties involved in the design process.

The CoreSight SoC-400 is a comprehensive set of configurable debug & trace components, supporting many features to enable rapid and efficient debug. The debug components are accessible by the debugger via the DAP Controller based architecture. In addition, a group of debug registers is designed to support the self-host debugging.



The CoreSight SoC-400 is compliant with the following specifications:

- Version 2 of the ARM® CoreSight™ Architecture Specification.
- Version 3 of the ARM® AMBA® APB Protocol Specification.
- ARM® AMBA® 4 ATB Protocol Specification ATBv1.0 and ATBv1.1.
- ARM® Debug Interface Architecture Specification, ADIv5.0 to ADIv5.2.
- ARM® AMBA® Specification (Rev 2.0).
- ARM® AMBA® AXI and ACE Protocol Specification.
- IP-XACT version 1.4, defined by Accellera.
- IEEE 1149.1-2001 IEEE Standard Test Access Port and Boundary Scan Architecture (JTAG).

4.2.1.1 Features

The CoreSight debug and trace module has the following key features:

- Supports 5-pin JTAG and 2-pin SWD (Serial Wire Debug) interface to attach the external debugger.
- Supports both self-hosted debug/trace and external debugger debug/trace operations.
- Halts/resumes CPU cores by the external debugger.
- 4 KB on-chip Embedded Trace Buffer (ETB) that stores trace data.
- Supports cross triggering between CPU cores to halt/resume simultaneously.
- Controls CoreSight/CPU debug authority by the authentication register.
- System Counter that halts/resumes simultaneously with CPU debug entry/exit.

4.3 GIC Interrupt Controller

4.3.1 Introduction

The X3M integrates a GIC-400 that is a high-performance, area-optimized interrupt controller with an Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI) interface. It detects, manages, and distributes interrupts in the X3M SoC configurations. The GIC provides registers for managing the interrupt sources, interrupt behaviors, interrupt grouping and interrupt routing to one or more cores.

The GIC implements the following interrupt types:

- Software Generated Interrupts (SGIs).
- External Private Peripheral Interrupts (PPIs) for the processor.
- Internal PPIs for the processor

The Cortex-A53 processor implements the GIC CPU interface as described in the Generic Interrupt Controller (GICv2) architecture that supports:



- Two security states.
- Software-generated interrupts (SGIs).
- Message based interrupts.
- Interrupt masking and prioritization.
- Wakeup events in power-management environments.
- Configuring each interrupt as either Group 0 or Group 1.
 - Signaling Group 0 interrupts to the target processor using either the IRQ or the FIQ exception request.
 - Signaling Group 1 interrupts to the target processor using the IRQ exception request only.

4.3.1.1 Features

The GIC has the following key features:

- In cooperation with dual-core Cortex A53, interrupts can be:
 - Enabled or disabled.
 - Assigned to one of two groups, Group 0 (secure) or Group 1 (non-secure).
 - Prioritized.
 - Distributed to the target CPU core.
- Supports the following interrupt types:
 - 16 Software Generated Interrupts (SGIs).
 - 4 Private Peripheral Interrupts (PPIs) for each CPU core.
 - 95 Shared Peripheral Interrupts (SPIs).
- Supports physical interrupts IRQ and FIQ to CPU cores.

4.4 On-chip ROM

4.4.1 Introduction

The on-chip Read Only Memory (ROM) is used to store the program that boots the system after the system is powered on initially, which can be accessed by the CPU via the AXI bus.

The BOOTROM contains a 128 KB ROM block that supports 32-bit read/write operations.

The boot ROM supports the following boot devices:

- eMMC.
- Serial NAND/NOR flash.

4.4.1.1 Features

The on-chip ROM has the following key features:



- 128 KB on-chip ROM accessed by CPU for boot.
- Supports 32-bit read/write operations.

4.5 On-chip SRAM

4.5.1 Introduction

The on-chip static random access memory (SRAM) can be accessed by the CPU, BIFSPI, BIFSD and DMAC via the AXI bus.

AXI SRAM contains a 64 KB SRAM block, and supports 32-bit read/write operations.

4.5.1.1 Features

The on-chip SRAM has the following key features:

- 64 KB on-chip SRAM accessed by CPU, BIFSPI, BIFSD, and DMAC.
- Supports 32-bit read/write operations.

4.6 QSPI

4.6.1 Introduction

The Quad SPI (Quad Serial Peripheral Interface) is an advanced SPI serial NAND/NOR flash memory controller, which is used to provide access to external serial NAND/NOR flash memory devices.

The QSPI supports the traditional SPI as well as the dual-SPI mode which allows to communicate on two data lines. It uses up to six lines in quad mode: one line for chip select, one line for clock and four lines for data in and data out.

The QSPI work in master mode only. It is primarily intended for fast booting from the external QSPI flash. It also supports XIP mode that enables execution of code from the SPI NOR flash instead of the more traditional way of executing the code from memories such as DDR/SRAM.

4.6.1.1 Features

The QSPI module has the following key features:

- Supports Single/Dual/Quad SPI, master mode only.
- Supports batch/non-batch mode TX and RX.
- Configurable 1/2/4-byte data width to access 16-byte TX FIFO and 16-byte RX FIFO.
- Configurable frequency divider for QSPI_SCLK, up to 83 MHz.
- The NOR flash supporting 24-/32-bit address mode, while the NAND flash supporting 2/4 KB page size.



- Comprehensive status and interrupt reporting.

4.7 BIFSPI

4.7.1 Introduction

The BIFSPI module is used for data transfers between the Application Processor (AP) and the X3M, as well as access to DDR and other module registers. There are three BIFSPI datapaths as follows:

- The CP accesses the BIFSPI private configuration register and the registers shared by the AP and CP through the APB bus.
- The AP accesses the registers shared by the AP and the CP through the SPI bus.
- The AP accesses the DDR and other module registers through the BIFSPI converted to the AXI bus.

4.7.1.1 Features

The BIFSPI has the following key features:

- SPI slave interface with Horizon customized communication protocol
- SPI serial clock up to 66MHz.
- BIFSPI_RSTN input pin resets control logic except internal share registers, while SYSCTRL can reset both.
- Thirty-one 32-bit internal share registers exchanges information with AP, while SHARE_REG_31 indicating internal bus status is read-only.
- AP access address range is controllable to prevent illegal access.
- AP can access any of the following:
 - Internal share registers.
 - All on-chip module registers except BIFSPI itself.
 - Off-chip DDR and on-chip SRAM.
- Data package size: 4 bytes for registers, up to 4K bytes for DDR and SRAM.
- Supports parity check command for read/write operations.
- Interrupts reporting status and exceptions.

4.8 BIFSD

4.8.1 Introduction

The BIFSD interface converts the eMMC host access of the AP into the X3M internal bus access, supporting access to DDR, SRAM and internal registers. The BIFSD primarily serves as the datapath for read and write operations between the AP and the X3M, where the AP access is regarded as an eMMC Device. The clock frequency for each 4/8 data lines can be up to 200 MHz (HS200 Mode), therefore the BIFSD can provide up to



200 MB/s physical bandwidth for high speed data transfer.

The BIFSD complies fully with eMMC 4.3/4.4/4.41/4.5/4.51/5.0 specifications.

4.8.1.1 Features

The BIFSD has the following key features:

- Embedded MultiMediaCard (eMMC) device interface compliant with eMMC5.0 specification.
- AP can access off-chip DDR and on-chip SRAM through the BIFSD interface.
- Supports single/multiple block R/W access.
- Supports 1/4/8 data lines up to 200 MHz in HS200 mode.
- Some frequently used interrupts can be processed by the hardware engine instead of CPU.
- AP can reset the BIFSD interface using the BIFSD_RSTN input pin.
- Comprehensive status and interrupt reporting.

4.9 DMAC

4.9.1 Introduction

The X3M Direct Memory Access Controller (DMAC) is a module of the CPU subsystem that provides a high-performance and high-speed data transfer. The DMAC can also be used for memory to memory copying or moving of data within memory. The DMAC can offload expensive memory operations, such as large copies or scatter-gather operations, from the CPU to a dedicated DMA engine.

The X3M DMAC supports only one channel and can be triggered only by software request. The data transfer begins when the DMA channel is idle. With software mode, the CPU sends an initial instruction to begin transferring. When the transfer is done the DMAC generates an interrupt to the CPU core. The channel registers need to be configured carefully before each transmission.

4.9.1.1 Features

The DMAC has the following key features:

- Single channel DMA controller that only supports memory-to-memory data transfer including:
 - DDR → DDR.
 - DDR → SRAM.
 - SRAM → DDR.
 - SRAM → SRAM.
- Supports both normal mode and Linked List Item (LLI) mode.
- Burst length of internal AXI bus could be configured as 1/2/4/8/16.



- Source address, destination address, and transfer length must be aligned to a burst length of 8 bytes.
- Status and interrupt reporting.

4.10 SYSCTRL

4.10.1 Introduction

The X3M System Control (SYSCTRL) module is mainly designed for clock/reset generation and miscellaneous system control function. The SYSCTRL includes 7 PLLs to generate on-chip high speed clocks using a set of multiplexers, dividers and clock gates. It also controls the asynchronous resets for each functional module in the X3M power down domain.

The PLL is a frequency synthesizer optimized for low power digital clocking. It has wide input and output ranges along with best-in-class jitter performance with excellent supply noise immunity.

4.10.1.1 Features

The SYSCTRL module has the following key features:

- Integrates 1 high-accuracy low-noise fractional PLL for DDR subsystem and 6 integer PLLs for other on-chip clocks.
- Includes glitch-free clock multiplexers to switch clock sources dynamically.
- Instantiates clock dividers to generate target clock frequencies.
- Inserts clock gating cells to control clock on/off.
- CPU/BUS clock dynamic changes such as clock source switching, frequency ratio adjustment, and target frequency change.
- Software-readable clock on/off status.
- Software reset for all function modules.

4.11 Timer

4.11.1 Introduction

The X3M has 3 timer macro modules. Each macro module has 3 timers, for example, one 64-bit timer0, one 32-bit timer1, and one 32-bit timer2. However, timer2 of timer macro 0 is specially used as watchdog. Thus, the chip has a total of 8 general timers.

4.11.1.1 Features

The Timer module has the following key features:

- The X3M has 8 general timers and 1 watchdog, as shown in [Table 4-1](#).



Table 4-1 Timer Details

Timer Macro	Base Address	Timer	Description
Timer Macro 0	0xA100_2000	timer0	64-bit general timer
		timer1	32-bit general timer
		timer2	dedicated as watchdog
Timer Macro 1	0xA100_3000	timer0	64-bit general timer
		timer1	32-bit general timer
		timer2	32-bit general timer
Timer Macro 2	0xA100_4000	timer0	64-bit general timer
		timer1	32-bit general timer
		timer2	32-bit general timer

- Uses 1 MHz base clock that is divided from 24 MHz external oscillator directly
- Various timer operation modes as shown in [Table 4-2](#).

Table 4-2 Timer Operation Modes

Operation Mode	Description
One-time mode	Runs only once then stops.
Periodical mode	Runs periodically and generates an interrupt each time, until software stops it.
Continuous mode	Generates an interrupt at given target value, continues to count, until software stops it.

- Configurable period/target value.
- Generates interrupts depending on the operation mode when reaching the target value.
- Status registers for running status and current value.

4.12 Watchdog

4.12.1 Introduction

The Watchdog timer module is an independent timer for system use. It provides a safety feature to ensure that software is executing as planned and that the CPU is not stuck in an infinite loop or executing unintended code. If the watchdog module is not serviced (refreshed) within a certain period, it can generate a system reset to reboot the CPU.

Timer2 of timer macro 0 is used as watchdog in the X3M. Watchdog interrupt configuration registers (WDTGT and WDWAIT values) need to be set. When the counter reaches WDTGT, an interrupt is generated to restart the watchdog for another WDTGT



period. When the system doesn't respond to the interrupt request when timeout (WDWAIT) occurs and a watchdog reset will be applied to the chip. The reset operation is triggered by the watchdog timeout event but actually performed by the PMU Controller, which will reset the most part of the chip, except the PMU subsystem. Besides, the active-low reset signal will be sent out through the WDT_RSTOUT_N pin to reset certain peripherals on the board. The watchdog reset duration can be configured using SLEEP_PERIOD register of the PMU Controller. Afterwards, the chip recovers from this watchdog reset and reboots.

4.12.1.1 Features

The Watchdog module has the following key features:

- Two-stage counter including counting to WDTGT and WDWAIT.
- Configurable timeout interval
- Uses 1 MHz base clock that is divided from 24 MHz external oscillator directly.
- Resets the most part of the chip on watchdog timeout except PMU subsystem.
- The active-low reset signal WDT_RSTOUT_N resets peripherals on board.
- Programmable reset duration.
- Recovery from watchdog reset is the same as power-up boot.

4.13 EFUSE

4.13.1 Introduction

The X3M integrates a 2048-bits high density electrical fuse macro that is used for chip ID. The electrical fuse is a type of non-volatile memory fabricated in standard CMOS logic process, which provides reliable protection for discrete components or circuits by melting under current overload conditions.

The EFUSE macro is one-off written when the chip is in test mode. In normal mode, the operations are controlled via the APB interface by software.

4.13.1.1 Features

The EFUSE macro has the following key features:

- Double bit scheme to enhance reliability, providing 1024 logical bits from a 2048-bit physical EFUSE macro.
- Supports programming at ATE tester and in field.
- Reads all the 1024 logical bits to software registers at the same time after the module reset removal.



4.14 Temperature Sensor

4.14.1 Introduction

Due to continued device scaling and consequent addition of more components on-chip, which in-turn results in enhanced heat generation, chip temperature monitoring has become a critical issue for ensuring reliable operation.

The X3M integrates an on-chip temperature sensor that monitors and reports the chip junction temperature.

4.14.1.1 Features

The temperature sensor has the following key features:

- Temperature measurement range: -40 ~ 125°C for junction temperature measurement, with $\pm 5^\circ\text{C}$ absolute accuracy.
- 12-bit measurement result with 0.125°C resolution.
- Configurable conversion time (CT) and interrupt at the end of each conversion cycle.

4.15 USB

4.15.1 Introduction

The X3M supports either device or host mode separately, not simultaneously for USB application, totally compatible with *USB 3.0 Specification*.

When acted as device mode, support USB 3.0 SuperSpeed(5 Gbps), USB 2.0 high-speed (480 Mbps), full-speed (12 Mbps) data rate. When acted as host mode, support SuperSpeed, high-speed, full-speed and low-speed (1.5 Mbps) data rate, compatible with xHCI specification.

4.15.1.1 Features

The X3M USB 3.0 has the following key features:

- 5-Gbps SuperSpeed data transmission rate through 3-m USB cable.
- Robust PHY tolerates wide voltage, and temperature variations.
- Spread Spectrum clock (SSC) generation and absorption, Down-spread is programmable from -4,980 ppm through -4,003 ppm.
- Low-jitter PLL technology with excellent supply isolation.
- Internal DMA controller for both device and host mode.
- Dynamic FIFO memory allocation for endpoints.
- Software controlled standard USB commands (USB SETUP commands detected and forwarded to application for decoding).



- Low MIPS requirement – Driver involved only in setting up transfers and high-level error recovery.
- Descriptor caching and data pre-fetching used to meet system performance in high-latency system.



5 DDR Subsystem

The DDR memory subsystem including a DDR Controller, a PHY, IOs and an embedded performance monitor. The DDR subsystem implementations offer the highest performance and the highest quality with a small footprint and minimal power consumption.

5.1 DDR Controller and DDR PHY

5.1.1 Introduction

The X3M DDR Controller is an enhanced universal DDR memory controller that supports DDR4/LPDDR4/LPDDR4X x32 off-chip DRAM memories, which is configurable, high performance, and optimized. The DDR Controller is responsible for communication with the system through an AXI interface, DDR command generation, DDR command optimizations, and a read/write datapath.

The X3M DDR PHY is responsible for the timing adjustment. It uses special calibration and training mechanisms to ensure the signal integrity (SI) and power integrity (PI). The high-speed DDR PHY provides low latency and up to 3200 MT/s throughput.

5.1.1.1 Features

The DDR Controller and DDR PHY have the following key features:

- Supports x32 off-chip DDR4/LPDDR4/LPDDR4X DRAM.
- Supports up to 4 GB capacity.
- Separate VDD_DDR voltage domain for DDR Controller and DDR PHY.
- Supports DDR4 maximum speed up to DDR4-3200.
- Supports LPDDR4/LPDDR4X maximum speed up to LPDDR4-/LPDDR4X-3200.
- Embedded performance monitor measuring bandwidth, latency, and other metrics on internal bus and DDR Controller, used for debug and performance optimization.

5.2 Performance Monitor

5.2.1 Introduction

The DDR embedded performance monitor is responsible for measuring the bandwidth, latency, and other metrics on internal bus and inside the DDR Controller, which is used for debug and performance optimization.

5.2.1.1 Features

The DDR Performance Monitor has the following key features:



- Measures bandwidth, latency and other metrics on internal bus
- Investigates bandwidth, latency and other metrics inside the DDR controller.
- Used for debug and performance optimization.

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6 VIO Subsystem

The Video In/Out (VIO) Subsystem is mainly responsible for processing image input and output.

The input path includes a Sensor Interface (SIF) module, an Image Signal Processing (ISP) module and an Image Processing Unit (IPU) module. The SIF provides video interfaces of image input and image output, including the MIPI, and DVP interfaces. The ISP provides image processing for RAW images and converts RAW format image to YUV format image. The IPU provides resize functions such as Crop/Scaler/Pyramid. The image is finally converted to the YUV420SP NV12 format and will be written to the DDR, waiting for the BPU module to use.

The output path is that the IAR module reads the DDR, gets the image and outputs it to a Display System through the external interface such as MIPI DSI/CSI-2 DEVICE/BT1120/BT656/Parallel RGB. [Figure 6-1](#) shows the VIO block diagram.

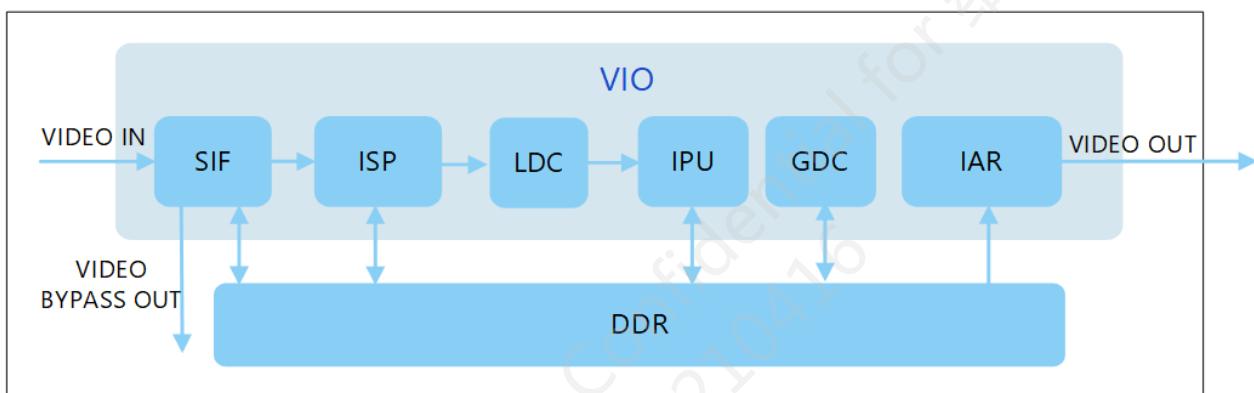


Figure 6-1 VIO Block Diagram

6.1 MIPI CSI Host

6.1.1 Introduction

The MIPI CSI Host implements the CSI-2 protocol on the host side. The CSI-2 link protocol specification is a part of communication protocols defined by MIPI Alliance standards intended for mobile system chip-to-chip communications. The CSI-2 specification is for the image application processor communication in cameras.

The MIPI CSI Host is designed to receive data from a CSI-2 compliant camera sensor. The MIPI CSI Host is designed to integrate with a MIPI D-PHY, which is configured to act as the physical layer.

6.1.1.1 Features

The MIPI CSI Host has the following key features:



- MIPI Rx Port 0(Rx1/3) 1/2/4 D-PHY RX data lanes and a clock lane.
- MIPI Rx Port 1(Rx0) 1/2 D-PHY RX data lanes and a clock lane.
- MIPI Rx Port 2(Rx2) 1/2 D-PHY RX data lanes and a clock lane
- Up to 2 Gbps per data lane.
- MIPI Rx1 and Rx3 support 4 virtual channels.
- MIPI Rx0 and Rx2 support 2 virtual channels.
- Supported image format:
 - YUV422 8-/10-bit.
 - RAW8/Raw10/Raw12/Raw14.
- Video input performance up to 4K@30fps.

6.2 SIF

6.2.1 Introduction

The Sensor Interface (SIF) module is an interface module between the external video and internal chip. The supported external interfaces are MIPI CSI-2 HOST and DVP, as shown in [Figure 6-2](#), the video goes into a Data MUX module through this external interface and then is transferred to the ISP/IPU. The Data Mux selects one of the three interface and transmits the data backwards. The SIF module transfers each interface from PCLK clock domain to MCLK clock domain.

When the X3M is used as a CP, the SIF module will directly bypass the video input to the AP using the MIPI CSI-2 DEVICE interface. The bypass datapath is detailed as follows:

MIPI HOST -> MIPI DEVICE. (If the MIPI HOST enables two virtual channels, then select one of the two channels and bypass the data to MIPI DEVICE.)

The SIF module supports Virtual Channel mode if the user requires more than one sensor datapath to come into the X3M. For the Virtual Channel mode, the image data comes into the X3M through the MIPI interface with two virtual channels. In this case, the SIF module transmits the data of two channels to the IPU module.

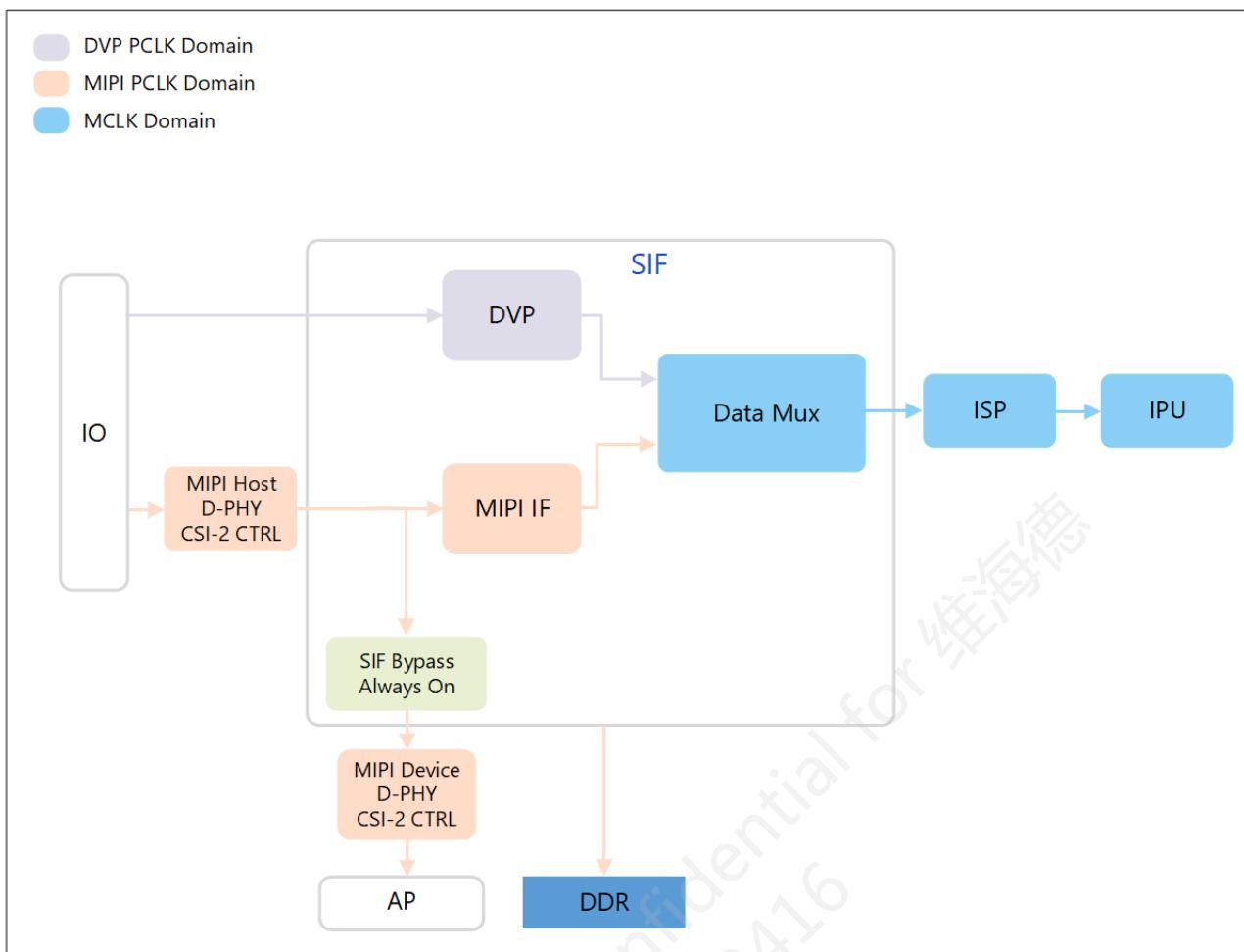


Figure 6-2 SIF Block Diagram

The basic requirements for Virtual Channel mode include:

- The size of the two images should be equal.
- The two images should be in YUV 422 format.

6.2.1.1 Features

The SIF module has the following key features:

- Supports the MIPI interface:
 - 1/2/4 Lane Data Lanes with transfer rate up to 2.0Gbps per Lane.
 - 8-/10-bit YUV 422, RAW 8-/10-/12-/14-bit format.
 - Supported frame rate: 4K@30fps, 1080P@60fps and 720P@120fps.
- Supports the DVP interface:
 - 12-bit data bus interface, up to 160 MHz.
 - 8-/10-bit YUV 422, RAW 8-/10-/12-/16-/20-bit format.
 - Supported input performance: 1080p@30fps and 720p@60fps.
- Supports the MIPI bypass to the AP:

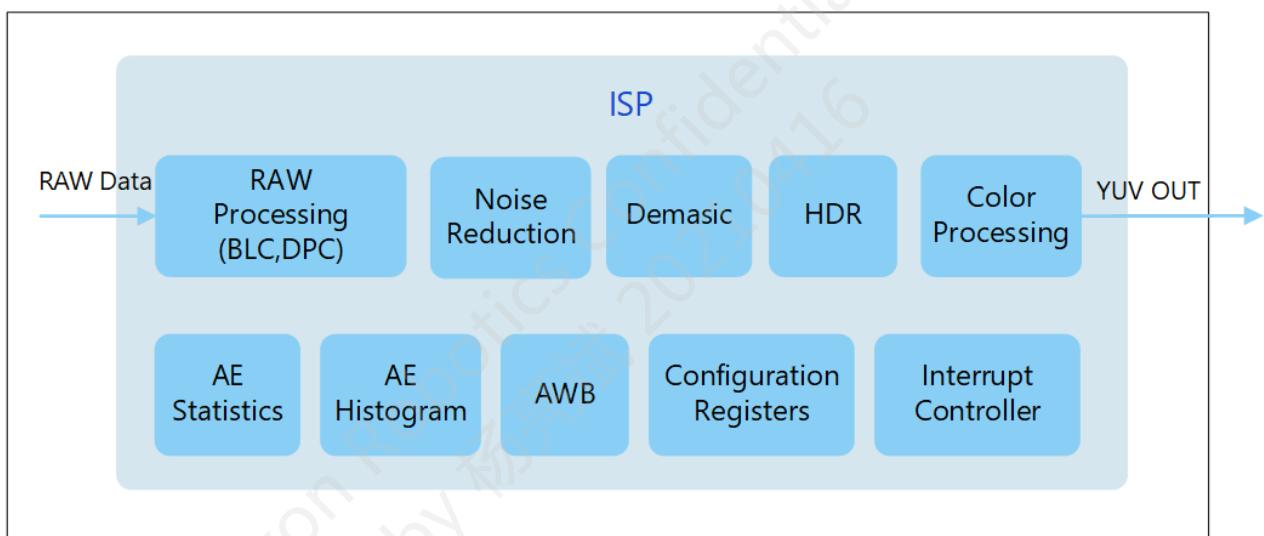


- Supports Frame_ID insertion functionality.
- Maximum resolution of input and output is 4096 x 2160.
- Supports Virtual Channel mode:
 - Virtual Channel mode – With MIPI the virtual channel enabled, the SIF will bypass the two virtual channel to IPU.
 - Supports 2 Channel Frame_ID insertion.
- The size of the two images should be equal.
- The two images should be in YUV 422 format.
- Supports motion detection of YUV and RAW formats.
- The output performance up to 4K@30fps or 1080p@60fps.

6.3 ISP

6.3.1 Introduction

The Image Signal Processing (ISP) module consists of several major algorithm modules: Raw Processing, Noise Reduction, HDR, AE, AWB, Demosaic and Color processing, as shown in [Figure 6-3](#).



[Figure 6-3 ISP Block Diagram](#)

6.3.1.1 Features

The ISP module has the following key features:

- Built-in Image Signal Processor (ISP) supporting RAW to YUV conversion.
- Supports High Dynamic Range (HDR) sensors:
 - Supports Digital Overlap (DOL) HDR sensor.
 - Supports linearized HDR sensors.
 - Supports native (on sensor) companded HDR sensors.



- Supports Auto-Exposure, Auto-White balance, and Auto-Focus (3A) histogram statistics.
- Supports Lens Shading Correction.
- Supports Defect Pixel Correction (DPC).
- Supports Spatial Noise Reduction.
- Supports Temporal Noise Reduction (3DNR).
- Supports Color Noise Reduction.
- Supports purple fringing Correction.
- Supports Lens Distortion Correction (LDC).
- Supports Crop from input image.
- Supports 3D Color Look-up Table (LUT).
- Supports RGB sharpening and edge enhancement.
- Supports Gamma Correction.
- Lens GDC and Fisheye Correction.
- ISP tuning tool on the PC.
- Maximum resolution of the input image is 4096 x 2160.
- The maximum input performance supported: 4K@30fps and 1080p@60fps.

6.4 IPU

6.4.1 Introduction

The Image Process Unit (IPU) module processes the YUV image data from the sensor or image data from the ISP module, and writes the processed image data back to DDR for the BPU module to call for subsequent processing, as shown in [Figure 6-4](#). The IPU mainly includes Test Pattern Generator, Cropping module, Scaler module, OSD module and several other format conversion modules.

There are three DDR datapaths, two are connected to the output of the Cropping, the other is connected to the output of the Scaler, and either of them can be enabled or disabled. The IPU supports inserting the Frame_ID (timestamp) into image data before writing it to the DDR.

The IPU module supports three input datapaths:

1. LDC output following ISP in NV12 format.
2. DDR data from AXI read port in NV12 format.
3. DVP input (bypass ISP) in YUV422 format.
4. Test Pattern Generator input.

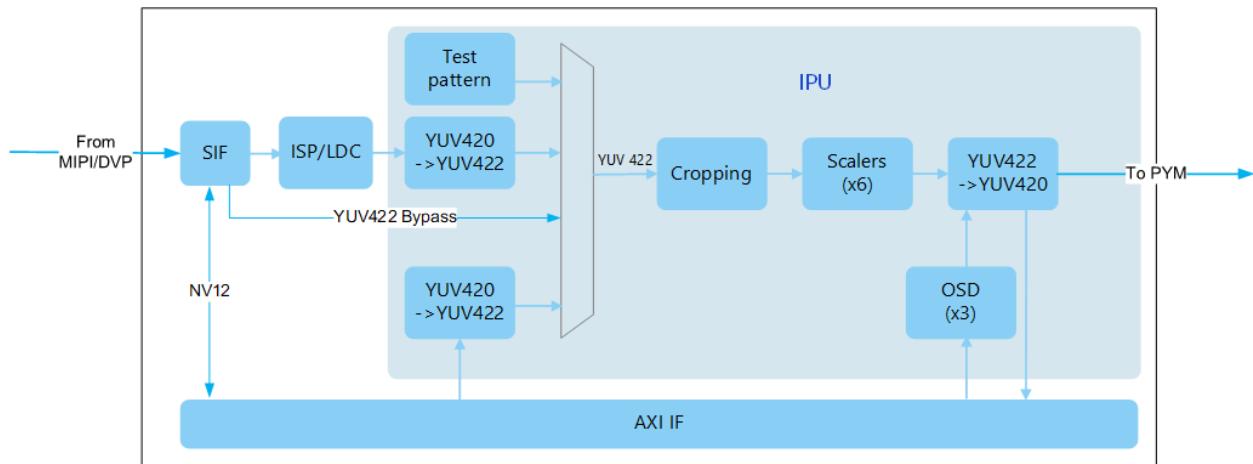


Figure 6-4 IPU Block Diagram

6.4.1.1 Features

The IPU module has the following key features:

- Supports the input image in YUV 444/YUV 422 format.
- Supports output Test Pattern Generator.
- Supports the Cropping processing:
 - The maximum resolution of the input image is 4096 x 2160.
 - The minimum resolution of the input image is 32 x 32.
 - The maximum resolution of the output image to DDR is 4096 x 4096.
- Output image to DDR, in YUV420SP NV12 format.
- Supports fetching and inserting the Frame_ID.
- Supports the Scaler processing:
 - Total 6 Scalers (1 for upscale and 5 for downscale).
 - The maximum resolution of the input image is 4096 x 2160.
 - The minimum resolution of the input image is 32 x 32.
 - The maximum resolution of the output image to DDR:
 - Up Scaler: 4096 x 4096.
 - Down Scaler 0/4: 1280 x 720.
 - Down Scaler 1/3: 1920 x 1080.
 - Down Scaler 2: 4096 x 4096.
 - The maximum resolution of the output image to Pyramid is 4096 x 4096.

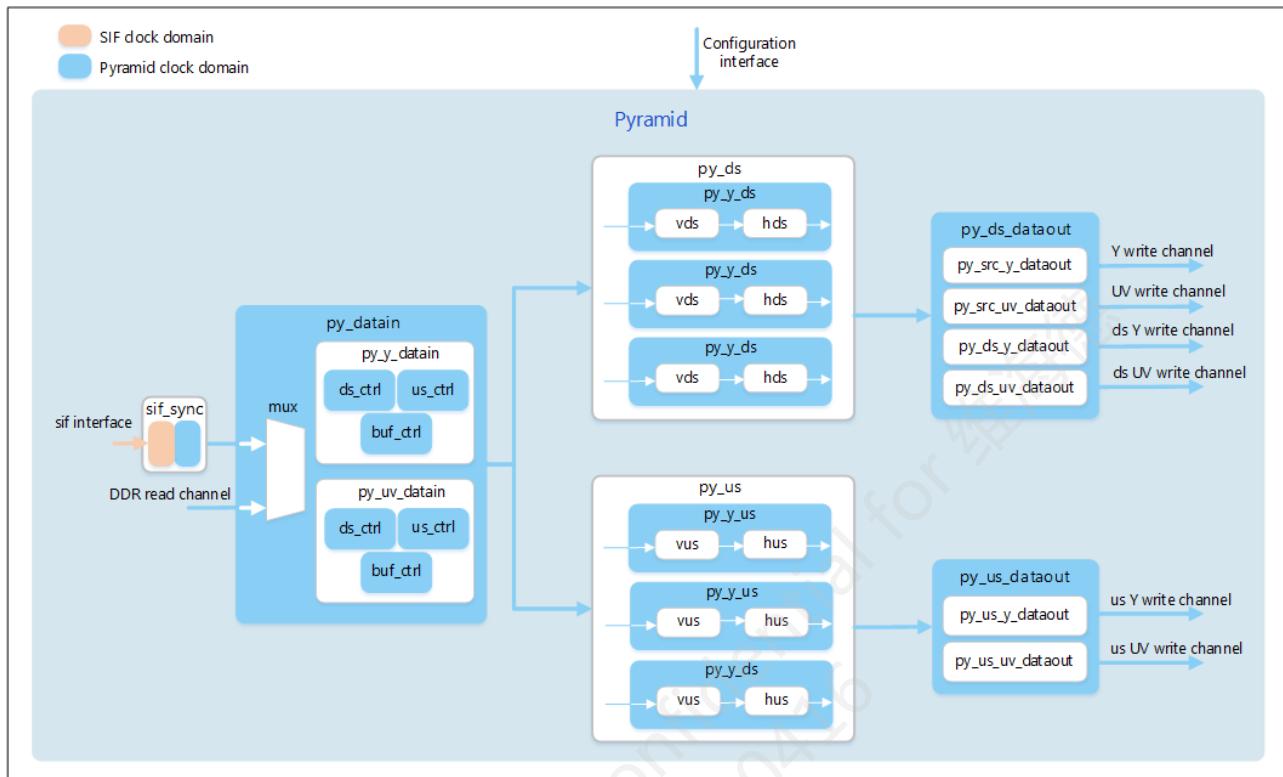
6.5 PYM

6.5.1 Introduction

The Pyramid (PYM) module is located in the IPU module of the X3M, and primarily



processes the YUV420 image data from the Scaler in IPU or directly from the DDR. The PYM supports downscaling or up-scaling processing based on a ROI (region of interest) of the original image. The size of the PYM output image is depending on the requirement of the BPU. The PYM output is written to DDR in YUV420 NV12 format. [Figure 6-5](#) shows the PYM diagram.



[Figure 6-5 PYM Block Diagram](#)

6.5.1.1 Features

The PYM module has the following key features:

- The maximum resolution of the input image is 4096 x 2160.
- The minimum resolution of the input image is 64 x 64.
- Supported video streaming performance: 1080p@30fps and 720p@60fps/30fps.
- Supports online/offline mode:
 - Input pyramid data from the Scaler in the IPU module in online mode.
 - Input pyramid data from the DDR in offline mode.
- Supports downscaling capabilities:
 - 0 ~ 23 layers in total, layer 0 as the original image. 6 base layers that have a fix one-dimensional scale ratio: 1/2, and 3 adjustable layers based on each base layer. The adjustable one-dimensional scale ratio: 1/2 ~ 1, compared to the Corresponding base layer.
 - Each downscaling layer enabled independently, the UV signals processing for each layer also enabled separately.



- Supports up to 23 ROI areas. Each layer independently selected for the ROI area and downscaling calculation based on the ROI selected.
- One-dimensional minimum reduction ratio: 1/64.
- The minimum resolution of output image is 48 x 32 (width x height).
- Supports up-scaling capabilities:
 - Six arbitrary ROI areas that are determined by the coordinates of the upper left corner and the width and height of the area. Even width and height.
 - The one-dimensional magnification ratio of the six ROI areas: 1.28, 1.6, 2, 2.56, 3.2, 4.
 - 6 ROI areas enabled independently.
- The maximum resolution of the output image is 4096 x 4096.

6.6 GDC

6.6.1 Introduction

GDC is a highly configurable Geometrical Distortion Correction engine, capable of performing up to four simultaneous geometric warp functions, each displayed in a sub-window, at video resolution up to 4K UHD. The GDC engine is suitable for video surveillance, fisheye correction, automotive reversing cameras, and panoramic correction and demo cameras.

The GDC module is a stand-alone engine, interfaced via AXI to integrate into a video pipeline, operating on YUV 4:2:0 data. The GDC module incorporates a controller which, once loaded with a transform “sequence”, enables the engine to run stand-alone, without the need of a powerful host processor. Updates to the sequence are only required on transform changes and PTZ adjustments.

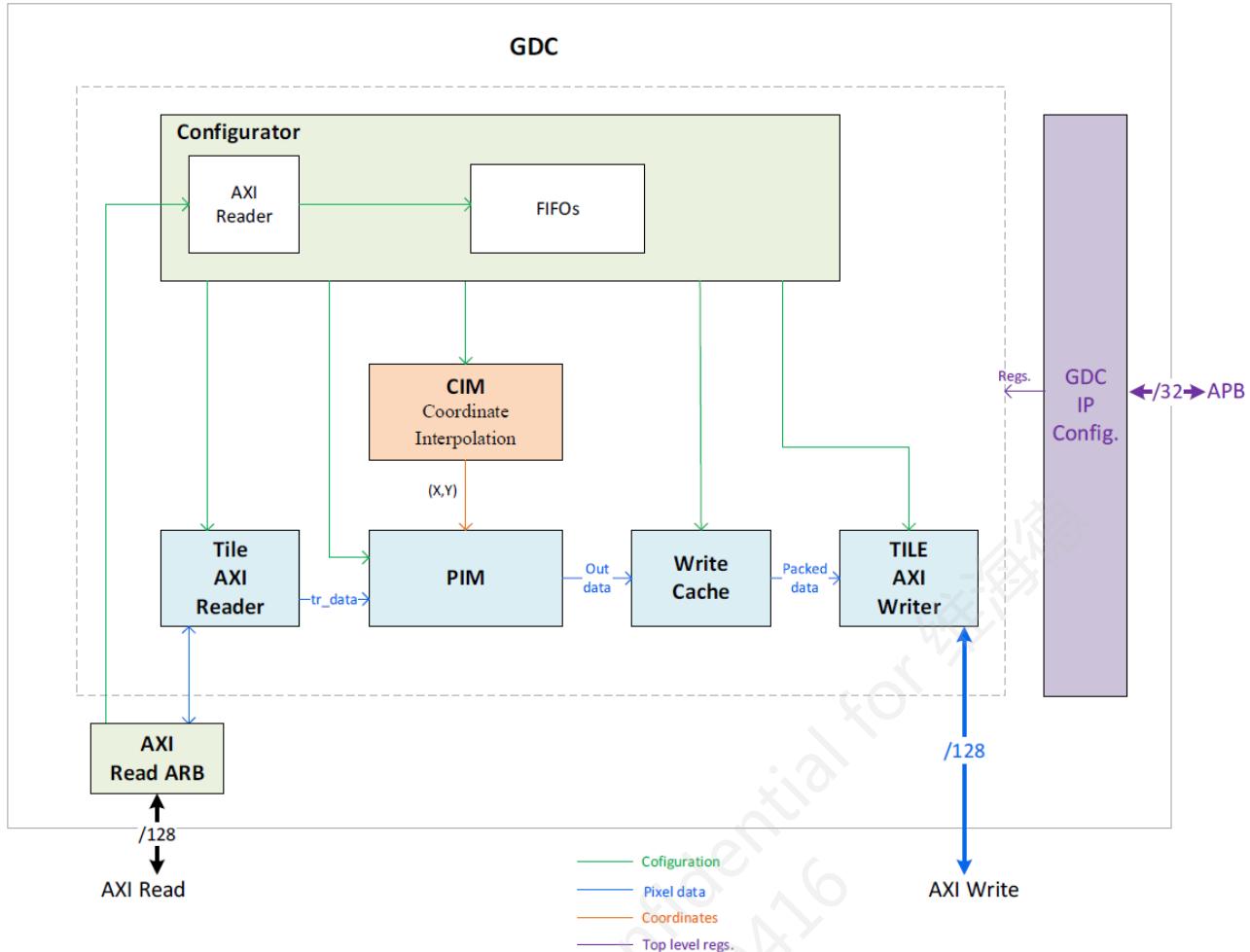
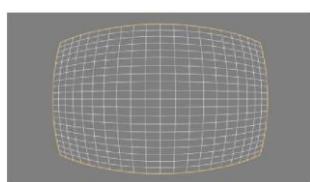


Figure 6-6 GDC Block Diagram

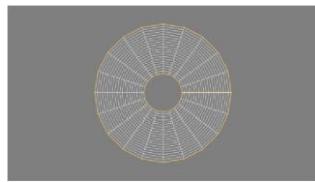
6.6.1.1 Features

The GDC module has the following key features:

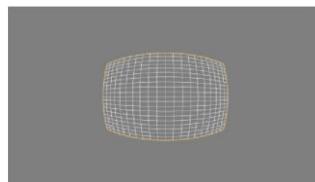
- Video mode:
YUV 4:2:0 SemiPlanar (NV12).
- Transformations:
 - Panoramic:



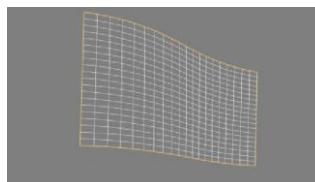
- Cylindrical:



- Arbitrary plane:



- Custom:



- Tile based processing:
 - Tiles are defined for input and output separately.
 - The GDC configuration generation tool divides output tiles and calculates the corresponding input side tiles.
 - Coefficients used for input tile to output tile transformation are pre-calculated and loaded to hardware through AXI read interface.
 - Supports only rectangular tiles.
 - Minimum supported tile size is 1x1 pixel. Maximum tile size would be whole the frame size.
- Multi-Window Output:
 - Output frame can be divided into sub-window up to a maximum of four, with a flexible choice of layouts.
 - Each sub-window can be configured with any available transform.

6.7 IAR

6.7.1 Introduction

The IAR module reads the image data and the detection results corresponding to the image from the system memory, and transmits the processed image data. The IAR reads the image data from up to four FBUFs (up to four display layers, two image layers and two UI layers), converts image data of various formats in the FBUF into a unified YUV 444 format, and blends image data of the four display layers using the Overlay & Alpha-Blending operation. Afterwards, it continues the image post-



processing including brightness adjustment, etc., and finally outputs the image data according to the MIPI DSI/CSI-2 DEVICE/BT1120/BT656/RGB888 interface timings.

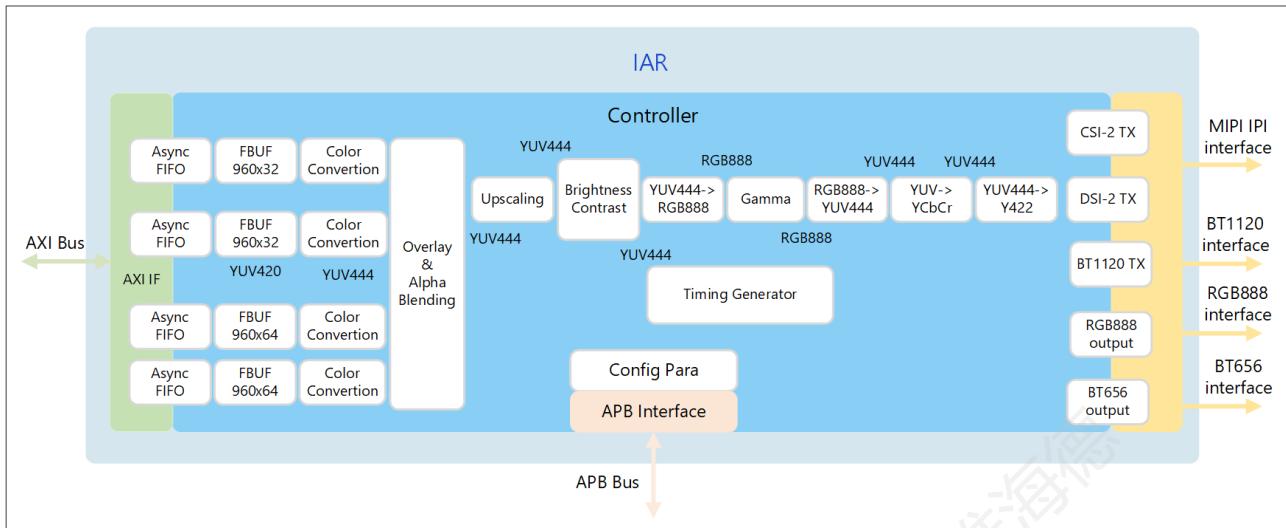


Figure 6-7 IAR Block Diagram

6.7.1.1 Features

The IAR module has the following key features:

- Supports display by the IAR through the BT1120 output interface in YUV 422 8-bit format, up to 1080P@60fps, and pixel rate up to 148.5MHz.
- Supports video stream output by the IAR through the MIPI CSI device interface in YUV 422 8-bit format, up to 1080P@30fps.
- Supports two-layer alpha blending on background, blending 1 video layer of YUV420SP format and 1 UI layer of ARGB8888/RGAB8888 format together.
- Programmable background color.
- Programmable layer size and top-left coordinate.
- Supports cropping capabilities from the top-left corner of an image when reading frame buffer from the DDR.
- Supports adjustments for brightness, contrast, saturation and hue.
- Supports gamma correction.

6.8 MIPI CSI Device

6.8.1 Introduction

The MIPI CSI Device implements the CSI-2 protocol on the device side. The CSI-2 link protocol specification is a part of communication protocols defined by MIP Alliance standards intended for mobile system chip-to-chip communications. The CSI-2 specification is for the image application processor communication in cameras.

The MIPI CSI Device is designed to send data to a CSI-2 compliant host. The MIPI CSI



Device is designed to integrate with a MIPI D-PHY, which is configured to act as the physical layer.

6.8.1.1 Features

The MIPI CSI Device has the following key features:

- 1/2/4 D-PHY TX data lanes and a clock lane.
- Up to 2 Gbps per lane.
- Supported image format:
 - YUV 422 8-/10-bit.
 - RAW8/Raw10/Raw12/Raw14/Raw16.
- Integrated Video Pattern Generator.
- Bit Error Rate (BER) pattern.
- Video output performance up to 4K2K@30fps.



7 BPU Subsystem

7.1 BPU

7.1.1 Introduction

The X3M is based on a dual-core Brain Processing Unit (BPU) that is a kind of heterogeneous multi-instruction multi-stream computing architecture. One of the core computing devices is a tensor calculation accelerator customized for Horizon neural networks, which can adjust the calculation mode according to the input data size in order to maximize the utilization efficiency of the multiplier array.

The BPU enables static memory sharing among multiple computing components to save memory resources. With best compiler optimization strategy, it can read and write DDR data and perform different type of operations in parallel.

7.1.1.1 Features

The BPU has the following key features:

- Dual-core BPU (BPU0 and BPU1), providing effective 5 TOPS computing power.
- Separate power domain for each core, VDD_CNN0 for BPU0, and VDD_CNN1 for BPU1, which can be shut off respectively.
- Up to 1GHz @ nominal VDD_CNN operating voltage.
- Supports Horizon customized neural networks, such as MobileNet V1, MobileNet V2, ResNet18, ResNet50, VGG, Faster-RCNN, UNet, etc.
- Supports [1,3,5,7] x [1,3,5,7] kernel for convolution, and stride = [1,2] for horizontal and vertical directions.



8 VSP Subsystem

8.1 VSP

8.1.1 Introduction

The X3M VSP subsystem integrates H.265 (HEVC), H.264, and JPEG codec for different kinds of video compression/decompression applications.

8.1.1.1 Features

- Supports H.265 (HEVC) Encoding and Decoding:
 - Main profile@L5.1.
 - Resolution up to 8Mpixels@30fps.
 - I/P/B Slices supported.
- Supports H.264 Encoding and Decoding:
 - Baseline/Main/High profiles@L5.1.
 - Resolution up to 8Mpixels@30fps.
 - H.264 Supports SVC-T Encoding.
- Supports JPEG Encoding and Decoding:
 - Baseline profile.
 - Resolution up to 16Mpixels.
- CBR, VBR, AVBR, FixQp and QpMap bit rate control modes supported:
 - ROI encoding with custom QP map.



8.1.1.2 VSP Block Diagram

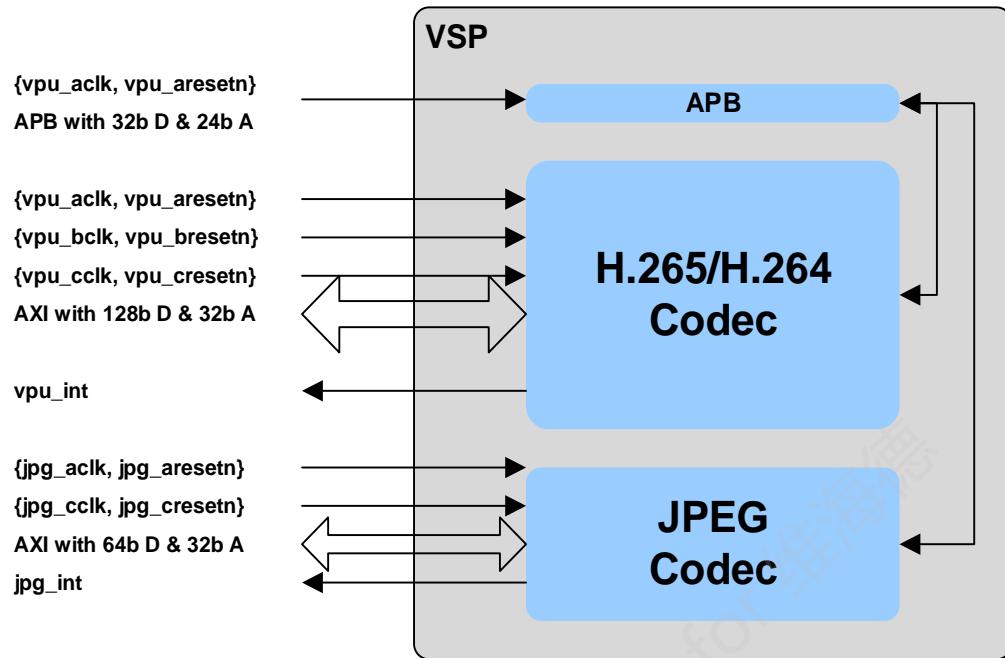


Figure 8-1 VSP Block Diagram and Interfaces



9 PERI Subsystem

9.1 UART

9.1.1 Introduction

The Universal Asynchronous Receiver/Transmitter (UART) module provides serial communication capabilities, which allows communication with external devices such as computers using a serial cable and RS232 protocol. This module implements all necessary functions associated with start-stop asynchronous communication. Serial data is transmitted and received at standard baud rates configured by the internal baud rate generator.

The X3M has 4 UART modules, UART0 to UART3. The UART1 is 4-wire version with hardware flow control, while the others are 2-wire version with TXD and RXD only. Some UART modules share pins with other modules. For multiplexing scheme details, see [2.2.2.2 Digital Pin Multiplexing](#).

9.1.1.1 Features

The UART module has the following main features:

- Full-duplex operation with TXD and RXD.
- Robust data reception with x16 over sampling and noise filtering.
- Configurable frame format:
 - Data bit: 7 or 8 bits.
 - Parity bit: none, even, or odd.
 - Stop bit: 1 or 2 bits.
- Programmable baud rate generator with integer and fraction divisors.
- Support standard baud rates including 19200, 38400, 57600, 115200, 230400, 460800, and 921600 (x 16 over sampling).
- UART1 has hardware flow control with RTSN and CTSN.
- Supports data transmission and reception by UART_RDR and UART_TDR registers.
- Supports data transmission and reception by embedded DMA Controller, with 64-byte TX FIFO and 64-byte RX FIFO.
- DMA supports RX FIFO flush operation on timeout condition for real-time applications.
- Comprehensive status and interrupt reporting.
- Supports software flow control capability by programmable XON/XOFF characters.



9.2 SPI

9.2.1 Introduction

The X3M Serial Peripheral Interface (SPI) Controller module consists of three SPI Controllers. The SPI is a master/slave synchronous serial bus. The SPI module implements both master and slave function, which is compliant with the SPI protocol.

The synchronous SPI protocol allows a master device to initiate serial data transfers with a slave device. A slave select signal (SSN) allows selection of an individual slave SPI device. The slave devices that are not selected do not interface with the SPI bus activities. The master controls the flow of communication by providing serial clock and slave select signals. The slave select signal is an optional active-low signal that enables the serial data input and output of the slave.

The SPI is a 4-wire bus:

- A clock signal named SCLK that is always driven by the master; all the SPI signals are synchronous to this clock signal.
- A slave select signal for each slave, SSN, used to select the slave the master communicates with.
- A data line from the master to the slaves, named MOSI (Master Out-Slave In).
- A data line from the slaves to the master, named MISO (Master In-Slave Out).

9.2.1.1 Features

The SPI module has the following key features:

- Full-duplex synchronous serial data transfer with MOSI and MISO, master mode only.
- Programmable SCLK frequency, polarity, and phase, up to 48MHz.
- Supports only one CSN signal, with programmable polarity.
- Supports 8-bit or 16-bit transfer mode, with programmable MSB or LSB first.
- Supports data transmission and reception by TX and RX registers.
- Supports data transmission and reception by embedded DMA controller, with 32-byte TX FIFO and 32-byte RX FIFO.
- DMA supporting RX FIFO flush operation on timeout condition for real-time applications.
- Comprehensive status and interrupt reporting.

9.3 I2S

9.3.1 Introduction

The X3M I2S module provides an easy way of sending/receiving the PCM audio over



the digital audio data serial interface. The data serial interface supports both I2S and DSP protocols. It includes two I2S/DSP receivers for audio recording and two transmitters for audio playback. The I2S/DSP receiver gets the audio data from external audio codec, converts it to 8- or 16-bit PCM data, and then sends the PCM data to the system memory through the AVDMA for further encoding. On the other hand, the I2S/DSP transmitter gets the audio data through the AVDMA to external audio codec for playback.

The I2S Serial Interface is a serial bus specification which is widely used to transfer digital audio data between devices. Generally speaking, the I2S is a stereo serial interface carrying left and right channel data. The I2S Interface consists of 3 wires: sclk (serial clock), ws (word select, also referred to as lrck), sd (serial data in/out). The device that provides sclk and ws is regarded as a master, while the device that accepts sclk and ws is identified as a slave.

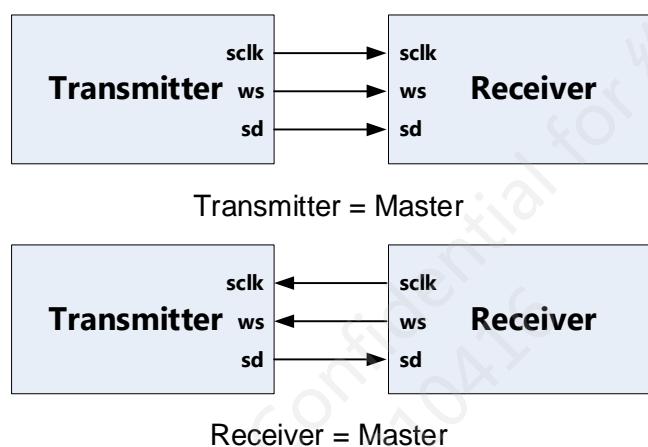


Figure 9-1 I2S Serial Interface

9.3.1.1 Features

The I2S module has the following key features:

- Supports Master/Slave mode.
- Half-duplex mode only, configured as RX or TX at a time.
- RX supporting 1/2/4/8/16-channel audio input
- TX supporting 1/2-channel audio output
- Supports 8-/16-bit sample accuracy
- Supports 8/16/32/44.1/48/64 KHz sample rate
- Supports I2S/DSP mode.
- Configurable LRCK polarity for I2S mode.
- Comprehensive status and interrupt reporting.



9.3.1.2 Standard I2S Bus

The standard I2S bus timing is as shown in [Figure 9-2](#). The master provides sclk, as well as drives lrck by sclk's negative edge. Both the master and slave drive sd using sclk's negative edge and capture sd using sclk's positive edge. The MSB of digital audio data is available on the 2nd capture edge of sclk following an lrck transition. The other bits up to the LSB are then shifted serially in order. When lrck is low, left channel data is transferred. When lrck is high, right channel data is transferred. The duty cycle of lrck should be 50%. Since a pair of left and right channel data makes up a stereo audio sample, the frequency of lrck represents the sampling rate. Depending on the word length of digital audio data and the frequency relationship between sclk and lrck, there may be unused sclk cycles after the LSB. For example, the word length of digital audio data is N, and $F_{sclk}/F_{lrck}/2 = N+2$. Thus, there are 2 unused sclk cycles between the LSB of left channel data and the MSB of right channel data, and vice versa. During these unused sclk cycles, sdout should be driven as zero and sdin should be ignored. Note that $F_{sclk}/F_{lrck}/2 = N$ is allowed, which is the critical configuration. Then, the LSB of left channel data is available in the 1st sclk cycle after an lrck rising transition, while the LSB of right channel data is available in the 1st sclk cycle after a lrck falling transition.

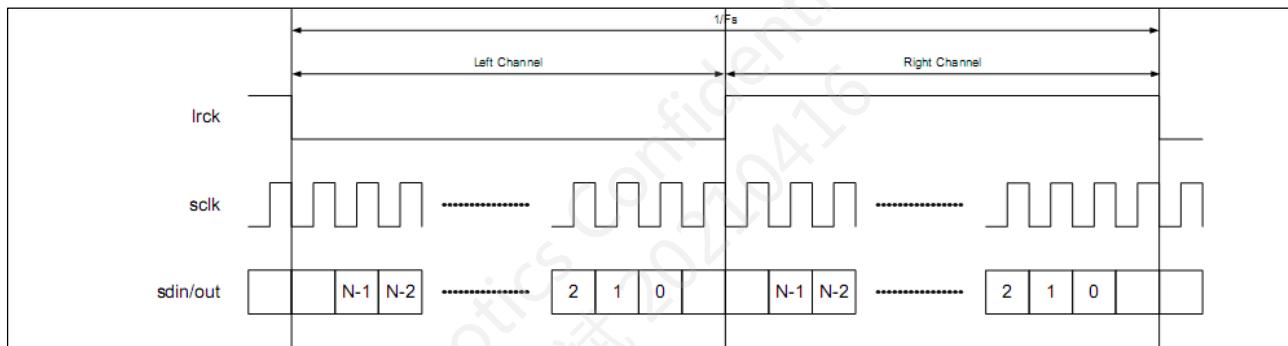


Figure 9-2 Standard I2S Bus Timing

9.3.1.3 Standard DSP Bus

The standard DSP bus timing is as shown in [Figure 9-3](#). Similar to I2S bus specification, the master provides sclk and drives lrck by sclk's falling edge. Both the master and slave drive sdout using sclk's falling edge and capture sdin using sclk's rising edge. The MSB of left channel data is available on the 2nd capturing edge of sclk following an lrck rising edge. The other bits up to the LSB are then shifted serially in order. Only left channel data is transferred. Right channel data is discarded by the transmitter or treated as zeros by the receiver. The frequency of lrck represents the sampling rate and the positive pulse of lrck may last one or more sclk cycles. Depending on the word length of digital audio data and the frequency relationship between sclk and lrck, there may be unused sclk cycles after the LSB. For example, the word length of digital audio data is N, and $F_{sclk}/F_{lrck} = N+4$. Thus, there are 4 unused sclk cycles between two



successive left channel datas. During these unused sclk cycles, sdout should be driven as zero and sdin should be ignored. Note that $F_{sclk}/F_{lrck} = N$ is allowed, which is the critical configuration. Then, the LSB of left channel data is available in the 1st sclk cycle after an lrck rising edge.

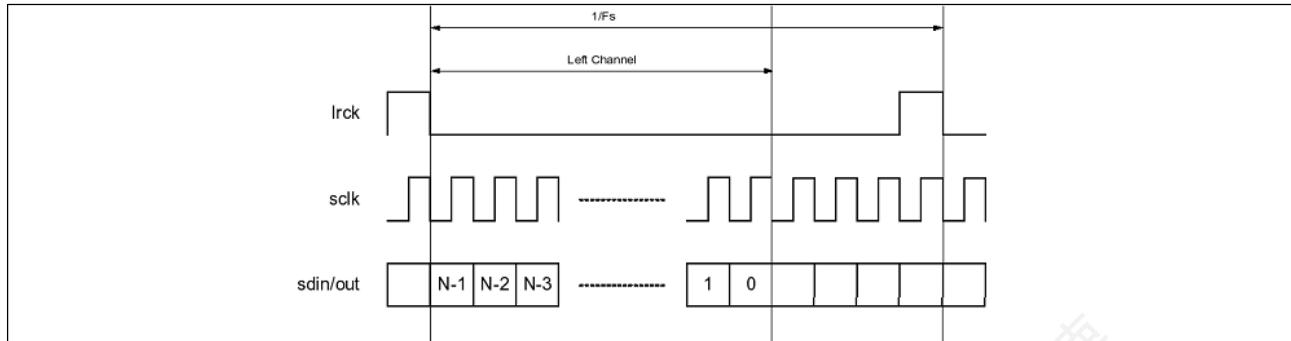


Figure 9-3 Standard DSP Bus Timing

9.3.1.4 Multi-channel I2S/DSP Bus

Even though the standard I2S and DSP format can have only 2 audio data on left channel and right channel, the Time Division Multiplex is a method of transmitting multi-channel audio via an I2S/DSP bus. [Figure 9-4](#) and [Figure 9-5](#) shows the digital serial audio data organization for multi-channel audio.

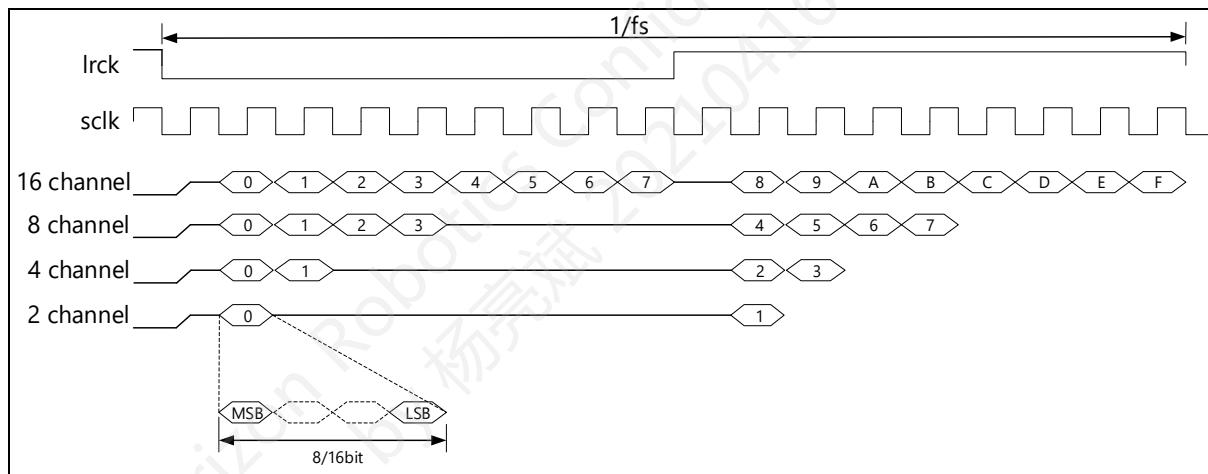


Figure 9-4 Multi-channel I2S Bus Timing

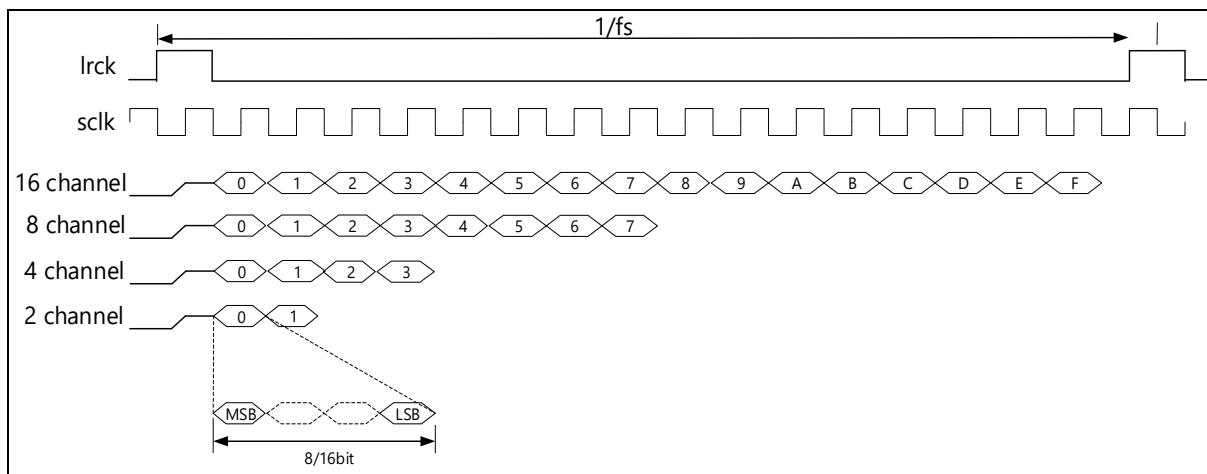


Figure 9-5 Multi-channel DSP Bus Timing

9.4 I2C

9.4.1 Introduction

I2C is a two-wire, bidirectional serial bus, which provides a simple and efficient method of data exchange between devices. It is most suitable for applications that require occasional communication over a short distance between many devices.

The X3M I2C Master Controller module has six separate I2C Master Controllers, each of which provides an interface between the internal Cortex-A53 processor and any external I2C bus compatible device that connects through the I2C serial bus. They use the same I2C Master Controller module.

9.4.1.1 Features

The I2C module has the following key features:

- Compliant with Philips I2C Bus Specification Version 2.1.
- Supports master mode only and used in a single-master multi-slave system.
- Supports standard mode (up to 100Kbps) and fast mode (up to 400Kbps).
- Supports 7- and 10-bit device addressing modes.
- Comprehensive status and interrupt reporting.

9.4.1.2 I2C Standard/Fast Mode

The I2C bus uses a serial data (SDA) and a serial clock (SCL) for data transfers. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a current-source or pull-up resistor, as shown in Figure 9-6. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. The number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF.

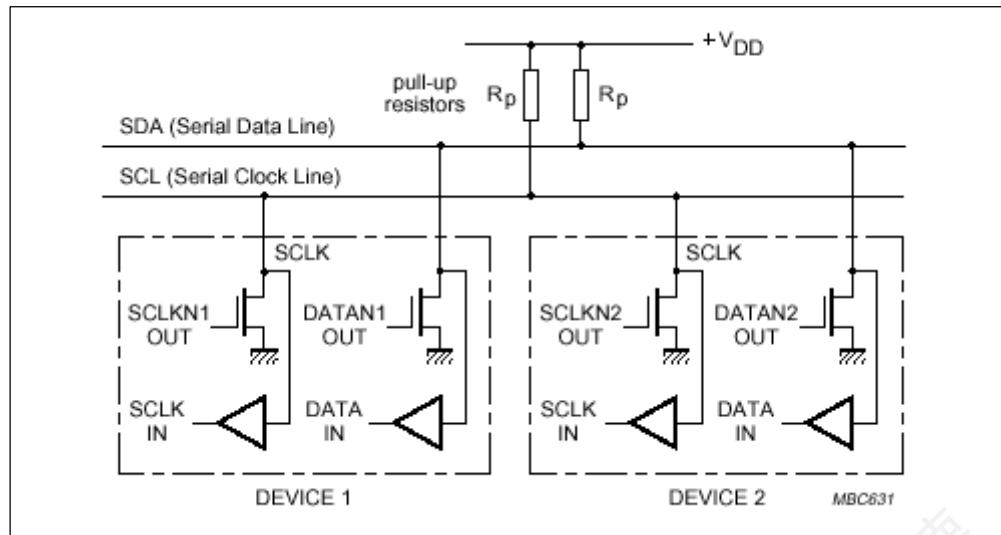


Figure 9-6 Connection of Stand/Fast Mode Devices to the I2C Bus

9.4.1.3 Data Transfer Format

Data is transferred between a master and a slave synchronously to SCL on the SDA line on a byte-to-byte basis. Each data byte is 8-bit long. The number of bytes can be transmitted first. An acknowledge bit follows each transferred byte. A transition on the SDA line while SCL is high is interpreted as control commands (START or STOP).

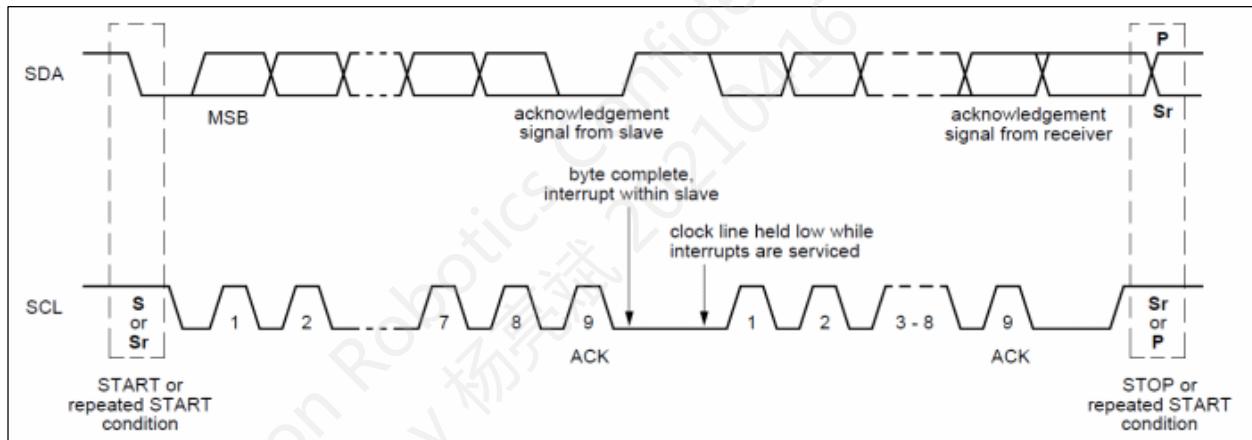


Figure 9-7 Data Transfer on the I2C Bus

9.5 PWM

9.5.1 Introduction

The Pulse-Width Modulation (PWM) module is used to generate square waves with variable pulse width and frequency. The frequency of output signal ranges from $\text{pwm_mclk}/4000$ to $\text{pwm_mclk}/2$, and the output pulse ratio ranges from 0/256 to 255/256. The average DC voltage of PWM wave can be used to drive various devices, such as LED and motor. The X3M has nine PWM outputs, each of which can be



controlled by software independently.

PWM (Pulse-Width Modulation) is widely used in motor speed control, LED brightness adjust, rectifier, audio output etc. For example, the LED brightness can be controlled by the high to low ratio of the PWM signals. If the PWM signal's frequency is fast enough, the human eyes can't detect the transition from on-to-off and off-to-on of the LED, what human get is only the average brightness. The same is true for the motors and so on. So we can use different pulse ratios and different pulse clocks to represent different information. The higher pulse ratio indicates brighter light and stronger shake of motor.

9.5.1.1 Features

The PWM module has the following key features:

- 3 PWM macro modules, each macro consisting of 3 PWM units, providing a total of 9 PWM units.
- Programmable PWM output frequency from $\text{pwm_mclk}/4000$ to $\text{pwm_mclk}/2$.
- Programmable PWM output pulse ratio from 0/256 to 255/256.
- Interrupt generated every $(\text{TIME_SLICE} * 1024)$ pwm_mclk cycles to notify CPU to change PWM settings.

9.6 Lite PWM

9.6.1 Introduction

The Lite PWM (LPWM) module is designed to work with the external Lidar device. This module is used to generate square waves with variable pulse width and frequency, which is synchronized to the pulse per second (PPS) trigger signal. The frequency of output signal ranges from 2K to 1Hz with 1MHz reference clock, and the output pulse width ranges from 0.01ms ~ 0.16ms. The X3M has up to four LPWM outputs, each of which can be controlled by software independently.

9.6.1.1 Features

The LPWM module has the following key features:

- APB internal bus interface.
- Supports up to 4 external channels.
- The pulse high width of the output waveform ranges from 0.01ms to 0.16ms.
- The frequency of the output waveform ranges from 25Hz to 50KHz.



9.7 SD/SDIO/eMMC Host Controller

9.7.1 Introduction

The eMMC/SD/SDIO Controller (referred to as MMC Controller) controls the read/write operations on the secure digital (SD) card and eMMC, and supports various extended devices based on the secure digital input/output (SDIO) protocol.

The X3M provides three MMC Host Controllers that support the eMMC/SD protocol. Typically, the MMC0 Controller controls the devices that comply with the protocol Multi Media Card (eMMC version 4.3/4.4/4.41/4.5/4.51/5.0), while the MMC1/MMC2 Controller controls the devices that comply with SD memory specification version 3.0 and SDIO specification version 3.0.

The MMC Controller supports SD 3.0 ultra-high speed (UHS-1), provides up to SDR104 mode. It supports up to HS200 mode in eMMC mode.

9.7.1.1 Features

The SD/SDIO/eMMC Host Controller has the following key features:

- Instantiates 3 SD/SDIO/eMMC Host Controllers:
 - SD0 supports up to 8-wire data bus, supports hot-plug detection.
 - SD1/SD2 supports up to 4-wire data bus.
- eMMC supporting up to HS200 mode, with transfer clock up to 192 MHz.
- SD/SDIO supporting up to SDR104 mode, with transfer clock up to 192 MHz.
- Supports phase tuning for drive clock and sample clock respectively by step of 22.5 degree.
- Uses SD special IO for 3.3 V to 1.8 V switching for SD1/SD2.
- Comprehensive interrupt and status reporting.

9.8 EMAC Host Controller

9.8.1 Introduction

The X3M integrates Ethernet Media Access Controllers (EMAC) and Physical layer (PHY) device Management Data Input/Output (MDIO) peripherals. The EMAC is used to transmit and receive data at 100/1000 Mbps over Ethernet connections in compliance with the IEEE 802.3-2008 specification. The MDIO controls PHY configuration and status monitoring.

The MAC operation is fully programmable and can be used in Network Interface Card, bridging, or switching applications. The core implements programmable embedded FIFOs that can provide buffering on the receive path for lossless flow control.

A unified DMA arbiter optimizes data transfer between and provides an enhanced



buffer descriptor programming model with IEEE 1588 functionality support. The programmable Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications.

9.8.1.1 Features

The EMAC Host Controller has the following key features:

- Full-duplex/Half-duplex Ethernet MAC Host Controller with RGMII/RMII PHY interface compliant with IEEE 802.3-2008 specification.
- 100/1000 Mbps data transfer rate by 25/125 MHz double data rate RGMII PHY interface.
- 100 Mbps data transfer rate by 50 MHz double data rate RMII PHY interface.
- 25 MHz EPHY_CLK output to external PHY as its reference clock.
- Automatic CRC and pad generation controllable on a per-packet basis.
- MDIO clause 22 and clause 45 master interface for external PHY configuration and management.
- Supports data transmission and reception by embedded DMA controller with 16K-byte TX FIFO and 16K-byte RX FIFO.
- Support for TCP Segmentation Offload (TSO) and UDP Fragmentation Offload (UFO).
- Supports Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in TX direction.
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o).
- Time sensitive networking features:
 - IEEE 802.1Qbv-2015, Enhancements to Scheduling Traffic.
 - IEEE802.1Qbu/802.3br, Frame preemption and Interspersing Express Traffic.
- Audio and video features:
 - Separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes.
 - Up to four queues on the Receive paths for AV traffic and seven queues on the Transmit path for AV traffic.
 - IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for Transmit channels.



10 PMU Subsystem

10.1 PMU Controller

10.1.1 Introduction

The X3M integrates a highly efficient and comprehensive power supply. A Power Management Unit (PMU) Controller allows the chip to be placed in low power mode for power saving.

The X3M PMU Controller is dedicated for managing and controlling the power of the entire chip. The chip going to sleep mode is triggered by software. It waits for the CA53 WFI event to start the sleep procedure, the main power down domain VDD_CORE_PD is turned off and only a small leakage power of Always ON domain VDD_CORE_AO is left. Then the chip will wake up when any wakeup source is triggered.

10.1.1.1 Features

The PMU Controller has the following key features:

- Supports separate power domains as follows:

Table 10-1 Power Domain Operation Modes

Power Domain	Normal Working Mode	Low Power Sleep Mode
VDD_CNN0	Controllable on/off	Off
VDD_CNN1	Controllable on/off	Off
VDD_CORE_AO	On	On
VDD_CORE_PD, VDD_CPU, VDD_DDR	On	Off

- The following voltage domains supports voltage and frequency scaling:
 - VDD_CPU domain running at 1.2 GHz @ nominal operating voltage.
 - VDD_DDR domain running at 800~3200 MT/s @ nominal operating voltage.
 - VDD_CNN0 and VDD_CNN1 domains running at 1GHz @ nominal operating voltage.
- Programmable sleep/wakeup flow and watchdog reset/reboot flow.
- Supports various wakeup sources for exiting low power sleep mode:
 - Timing counter within the PMU Controller.
 - RTC alarm event.
 - X2_WKUPIN_N input pin.
 - Any 4 GPIOs.
- WAKEUP_STATUS and WAKEUP_SOURCE read-only registers that indicate boot



- reasons
- Thirty-two 32-bit software registers storing information during sleep mode.

10.2 System Counter

10.2.1 Introduction

The CoreSight SoC-400 Timestamp Generator module provides a System Counter to the Cortex-A53 processor generic timer. The System Counter value is carried to the CPU with a synchronous binary encoded 64-bit bus, CNTVALUEB[63:0] and counts up (incrementing by one number) using a 24 MHz free running clock, which is used as a basis for the Generic Timer.

This System Counter measures the passing of time in real-time. It is used to generate the time reported by the Cortex-A53 processor that implements the Generic Timer specification. The time will not count backwards. The timestamp counter is 64-bit which is large enough to make overflow unlikely in normal usage models. However, if the counter does overflow, then it wraps around to zero, and a force synchronization event is issued through the timestamp interconnect.

The Cortex-A53 Generic Timer is compliant with the ARMv8-A architecture.

10.2.1.1 Features

The System Counter has the following key features:

- Started and stopped by software control.
- Software gets the current value through APB bus or from CPU CNTVALUEB input signal.
- Uses 24 MHz base clock directly from external 24 MHz crystal oscillator.
- Not affected by chip sleep mode, keep counting if still enabled, or keep its value if stopped by software before entering sleep mode.

10.3 RTC

10.3.1 Introduction

The Real-Time Clock (RTC) is a precise timer that can generate interrupts at intervals specified by the user. The RTC uses a 1024 Hz free running clock.

The basic purpose of the RTC is to maintain a calendar. It can also be used to wake up the chip from a sleep state.

The RTC unit can generate alarm interrupts at a particular time. It also supports ticks to interrupt the CPU at programmable periodic time intervals, such as once per minute or once per day.



10.3.1.1 Features

The RTC has the following key features:

- RTC calendar mode that provides seconds, minutes, hours, day of week, date, month, and year with leap year compensation.
- Binary-Coded Decimal (BCD) for calendar representation.
- Uses 1024 Hz base clock that is divided from external 32768 Hz crystal oscillator directly.
- Alarm interrupt occurring when the RTC calendar matches the target alarm time.
- Tick interrupt with configurable period.
- Alarm as a wake-up source that can bring the chip out of sleep mode.
- All functions not affected by chip sleep mode.

10.4 PADC/PIN

10.4.1 Introduction

The PIN Controller together with the IOMUX, enables the IC to share one PAD to several functional blocks. The sharing is done by multiplexing the PAD signals (input, output, output enable, etc). The PADC controller controls the SD0/SD1/SD2/I2C0/I2C2/I2C3/JTAG/BIFSPI/BIFSD/EMAC/BT1120 IO PAD voltage settings parameters.

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. The PADC controller controls the GPIO output data and direction of external I/O pads. There are total 121 digital IOs with GPIO function. The GPIO can generate individual interrupts/wakeup events from 121 GPIOs.

10.4.1.1 Features

The PADC/GPIO module has the following key features:

- Pinmux sharing one chip pin with up to 4 functions.
- GPIO function for 121 digital pins.
- Any 4 of the 121 GPIOs can be selected as interrupt/wakeup source, with configurable trigger edge and debounce time.
- PADC can control the registers to switch between 1.8 V and 3.3 V voltage modes for specified IOs
- All digital IO can set driving strength, enable PU/PD resistor, control output slew rate, and enable input Schmitt trigger feature.
- Software-triggered interrupt output X2A_IRQOUT_N with configurable pulse polarity and pulse width.



A. Appendix

A.1 Reflow Profile

制造站别/ Process	Reflow	
次数/ Times	3 times in succession	
峰值温度/ Peak temperature	245 °C max	
MSL	JEDEC Level3	

Temperature ↑

Time →

Supplier $T_p \leq T_c$

User $T_p \leq T_c$

T_c

$T_c - 5^\circ C$

T_p

T_L

T_{max}

T_{min}

Max. Ramp Up Rate = 3°C/s

Max. Ramp Down Rate = 6°C/s

Preheat Area

t_s

t

$T_c - 5^\circ C$

Time 25°C to Peak

预热/ Preheat	T_{smin} to T_{smax}	150 ~ 200 °C
	Time (ts) from (T_{smin} to T_{smax})	60 ~ 120 seconds
温度上升速度/ Ramp-up rate	T_L to T_p	3 °C/second max.
液化温度/ Liquidous temperature	T_L	217 °C
产品峰值温度/ Peak package body temperature	T_p	245 °C max.
产品使用温度/ Classification temperature (T_c)	$T_c - 5^\circ C$	240 °C max.
	Time (t_p)* within 5 °C	30 seconds max.
温度冷却速度/ Ramp-down rate	T_p to T_L	6 °C/second max.
达到最高温度的时间/ Time 25°C to peak temperature		8 minutes max.