**ADC**

VDD

C1
10u

IC1
ADS7886SDBVT

5VD

R5
10k

1 VDD
2 GND
3 VIN

CS 6
SDO 5
SCLK 4

CS
SDO
SCLK

GNDA

GNDA GNDD

Connect grounds at ADC

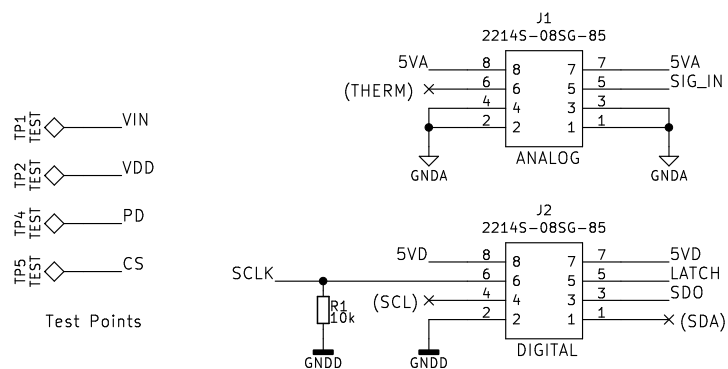Accepts 5V digital input
on 3.3V VDD

**POWER**

U1
LP5907MFX-3.3

5VA

1 IN      OUT 5      VDD
3 EN
2 GND

C2
10u

GNDA      GNDA
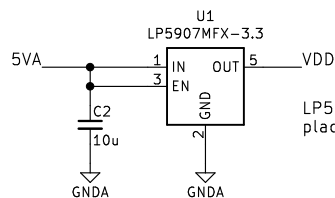
LP5907 allows output capacitors
placed far from LDO

Boring LDO internally set to 3.3V output.
(the LP5907 is pretty cool but the implementation is boring)

**ANALOG INPUT**

VDD

C3
10u

GNDA

SIG_IN

3 +
4 -
6 V+
2 V-
5 ENABLE
1

U2
OPA355NA

VDD

GNDA

D1
BAT_63-02V_H6327

2        1

PD

R2
TC33X-2-101E

1 CCW      CW 3
2 WIPER

VIN

C4
1n

R4
1M

GNDA

T=1ms
C0G/NP0 capacitor
recommended

Peak detect with adjustable Rs

**INTERFACE**

J1
2214S-08SG-85

5VA    8  | 8    7 |  7    5VA
(THERM) ×  6  | 6    5 |  5    SIG_IN
           4  | 4    3 |  3
           2  | 2    1 |  1

GNDA      ANALOG      GNDA

TP1 TEST ◇ — VIN
TP2 TEST ◇ — VDD
TP4 TEST ◇ — PD
TP5 TEST ◇ — CS

Test Points

J2
2214S-08SG-85

5VD    8  | 8    7 |  7    5VD
SCLK      6  | 6    5 |  5    LATCH
(SCL) ×   4  | 4    3 |  3    SDO
           2  | 2    1 |  1  × (SDA)

R1
10k

GNDD      GNDD

DIGITAL
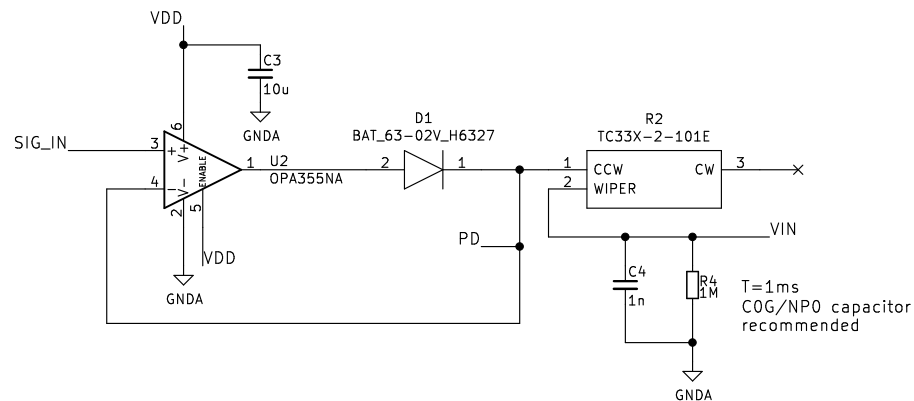
Connectors

Some spots around the board that might be
useful for debugging but hard to reach otherwise.

"Not connected" pins are I2C.

**CS TIMING**

5VD

C6
10u

GNDD

LATCH

R6
10k

GNDD

2 ⊳ 4

U3
74LVC1G14

GNDD

R3
100

CS

C5
1n

GNDD

Inverter accepts 3.3V input on 5VD.
Source/sink 32mA.

Fall time from 5V to 0.4V
becomes ≈250ns.

CS is delayed inverted latch.

Notes:
The ADC itself pulls 2mA.
The Pi has configurable pull up/down resistors. As a result, no output
resistors are included in this design.
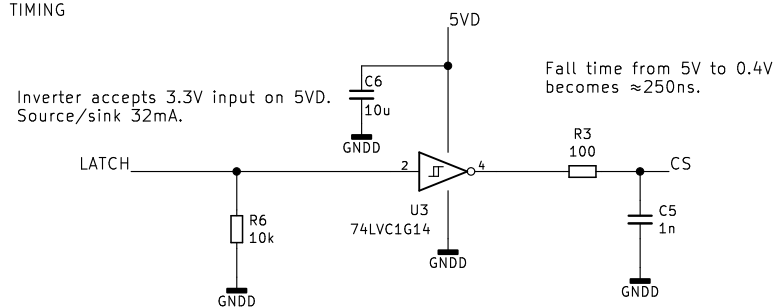Johnson noise equivalent to the LSB would be >1MΩ.