CS204 - Computer Architecture
Course Project Details
Phase 2

Phase 2: Code for a 5 step instruction execution.
Design and implement the function simulator 32bit RISCV ISA instructions.
Here, we would take the input from the .mc file (output of Phase 1) and pick one instruction at a time, using the value in PC (0x0). You will write a C/C++/Java/Python program. You would need to include structures for all the registers here - PC, IR, Register File, temporary registers (like RM, RY, etc), etc., five steps of instruction execution as functions. To give an overall idea, I am sharing a `.rar` file with you. It contains several files for a C like implementation. Reading the `.mc` file might be slightly different but the essence remains same.

All the instructions in the given in the input `.mc` file is executed as per the functional behavior of the instructions. Each instruction must go through the following steps:
Step 1: Fetch
Step 2: Decode
Step 3: Execute
Step 4: Memory Access
Step 5: Register Update or Writeback

Along with execution of instruction in steps, simulator should also provide messages what it is doing in each stage as an update in all the structures that would change. As part of the simulator, you should implement an additional instruction which exits the simulator, writes the data memory in `.mc` file before exiting. Further, introduce a variable "clock" that increments once for every instruction. Print the number of clock cycles at the end of each cycle.

You must test the software using assembly programs:
- Fibonacci Program
- Factorial Program
- Bubble Sort Program

The template implementation attached contains a README file, a design document, Makefile, and C code to start with. As part of your submission you are expected to submit the source code along with updated design document, README, input test files. Overall project evaluation will be on:
- Functional completeness
- Documentation completeness
- Testcase

Hope your Phase 1 is going smoothly. To start with Phase 2 right away, you can take a sample RISC-V machine code (may be from Venus) as `.mc` file. Remember that Phase 1 and Phase 2 need to be submitted by 15th March 2020 11.55PM and will be evaluated during 16th-22nd March 2020.

Revert if you have any questions.