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# Question Paper Code : 30138

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Electronics and Communication Engineering

EC 3352 — DIGITAL SYSTEMS DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the decimal number 431 to binary.

2. State DeMorgan's theorem.

3. What is an encoder?

4. State the difference between parity generator and parity checker.

5. How are the outputs of Mealy model and Moore model decided?

6. What is a universal shift register?

7. When does a race condition exist in an asynchronous sequential circuit?

8. What is the cause of an essential hazard?

9. Define noise margin.

10. List the types of ROMs with their expansion.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Simplify the Boolean function $(BC'+A'D)(AB'+CD')$ to a minimum number of literals. (6)

(b) Describe various types of hazards and the methods to eliminate hazards in combinational and sequential circuits. (13)

15. (a) (i) Draw and explain CMOS logic circuits. (7)

(ii) Explain a TTL gate with totem pole output. (6)

Or

(b) (i) Using 64 × 8 ROM chips with an enable input, construct a 512 × 8 ROM with 8 chips and a decoder. (7)

(ii) Draw a PLA circuit to implement the functions (6)

$F_1 = A'B + AC + A'BC'$

$F_2 = (AC + AB + BC)'$

PART C — (1 × 15 = 15 marks)

16. (a) Simplify the following Boolean function by using the tabulation method.

$F = \Sigma(0,1,2,8,10,11,14,15)$ (15)

Or

(b) A sequential circuit has two JK flip flops A and B and one input X. The circuit is described by the following flip flop input equations.

$J_A = x \qquad K_A = B$

$J_B = x \qquad K_B = A'$

(i) Derive the state equations A ($t$ + 1) and B ($t$ + 1) by substituting the input equations for the J and K variables. (8)

(ii) Draw the state diagram of the circuit. (7)