

Reg. No. : 

--	--	--	--	--	--	--	--	--	--

## Question Paper Code : 51011

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Fourth Semester

Electrical and Electronics Engineering

EE 3402 — LINEAR INTEGRATED CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the steps involved in the manufacturing process of an integrated circuit.
2. What is meant by parasitic capacitance?
3. Determine the output voltage  $V_o$  for the non-inverting amplifier circuit shown in Fig.1.

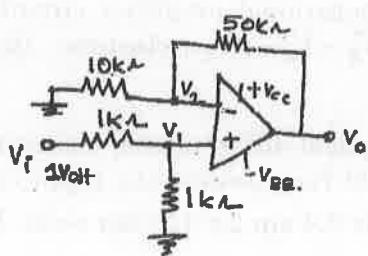


Fig. 1

4. Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to 1 KHz.
5. Draw the circuit of a triangular wave generator using a comparator and an integrator.
6. Interpret the minimum analog voltage be converted into a digital signal for a 4-bit ADC when  $V_{ref} = 5V$ .
7. Draw a circuit that produces a time delay of 3 ms using IC 555.

8. Define the lock range and capture the range of a PLL.
9. Compare linear mode power supply with switch mode power supply.
10. How is current boosting achieved using IC 723?

**PART B — (5 × 13 = 65 marks)**

11. (a) (i) Summarize the steps involved in the N-well process in CMOS processing technology. (7)
- (ii) Write short notes on
  - (1) Oxidation (2)
  - (2) Epitaxy (2)
  - (3) Deposition. (2)

Or

- (b) (i) Discuss the ion implantation diffusion and metallization in silicon semiconductor technology. (7)
  - (ii) Summarize the steps involved in the P-well process in CMOS processing technology. (6)
12. (a) (i) Derive the gain of the non-inverting amplifier using Opamp. (7)
  - (ii) Design an inverting amplifier with a gain of -5 and input resistance of  $10\text{ K}\Omega$ . (6)

Or

- (b) (i) Design an operational amplifier circuit to produce output voltage  $V_0 = 3V_1 + 4V_2 - V_3 - 2V_4$ . Assume the feedback resistance as  $20\text{ K}\Omega$ . (6)
  - (ii) Design a practical differentiator circuit to differentiate signals from 500Hz to 1000 Hz. Assume the input capacitance of  $0.1\ \mu\text{F}$ , if the input signal is  $0.4 \sin 2\pi (1000)t$  volts. Express the output voltage. (7)
13. (a) Design a second-order low-pass Butterworth filter with a cut-off frequency of 10 KHz and unity gain at low frequency. Also, determine the magnitude of the voltage transfer function in dB at 12 for the filter.

Or

- (b) Using Opamp, discuss in detail the circuit to implement a logarithmic amplifier. Also, Illustrate how two analog voltages are multiplied using log-antilog amplifiers.

14. (a) Explain the operation of PLL with a suitable diagram. Show how phase locked loop can be employed for FSK demodulation.

Or

- (b) Discuss the operation of the Voltage Controlled Oscillator with neat, functional diagram.

15. (a) Design a voltage regulator circuit to produce a constant voltage of 9V and discuss the voltage regulator circuit.

Or

- (b) Draw the functional block diagram of the IC 723 regulator and explain its current limiting feature and current fold-back characteristics.

PART C — (1 × 15 = 15 marks)

16. (a) Design an analog circuit to solve the following equation

$$\frac{d^2v}{dt^2} = 50 \frac{dv}{dt} + 200v - 20.$$

Or

- (b) Design a monostable multivibrator using an operational amplifier to generate a non-sinusoidal waveform with a time delay of 100 ms..
-