Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70090

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Third Semester

Electrical and Electronics Engineering

EE 3302 – DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare TTL and ECL logic families.
2. When is Quine McClusky method preferred for logic minimization?
3. Convert the given expression to the standard SOP form.

   $F(a,b,c) = \sum m(0,1,5,6,10,11,12,13,14,15)$
4. Convert $(1001)_2$ to its equivalent Excess-3 code.
5. Differentiate mealy circuits from moore circuits.
6. Compare synchronous circuits with asynchronous circuits.
7. Distinguish between PAL and PLA
8. What are critical and non critical races?
9. What are generics in VHDL?
10. List out the objects of VHDL.

PART B — (5 × 13 = 65 marks)

11. (a) Describe the working of a 2 input ECL NOR gate.

Or

(b) Explain the operation of 2 input CMOS NAND gate.

12. (a) Implement the sum output of full adder using

(i) 4×1 multiplexer

(ii) 2×1 multiplexer

Or

(b) Design a 3 bit comparator circuit and implement using logic gates.

13. (a) Design a 2 bit even parity generator using moore circuit and implement using D flip flops.

Or

(b) Design a synchronous mod 6 counter using T flip flops.

14. (a) An Asynchronous sequential circuit is described by the following excitation and output function.

$Y = x_1 x_2 + (x_1 + x_2)y$

$z = y$

(i) Draw the logic diagram of the circuit

(ii) Derive the transition table and output map

(iii) Describe the behaviour of the circuit

Or

(b) Give the PLA realization of the given function using a PLA with 3 inputs, 4 AND gates and 2 outputs.

$F_1(a,b,c) = \sum m(0,1,3,4)$

$F_2(a,b,c) = \sum m(1,2,3,4,5)$

15. (a) Write a VHDL code to realize a half adder using

(i) behavioral modeling

(ii) structural modeling

and distinguish between both.

Or

(b) Write a VHDL code to realize a

(i) 4×1 muiltiplexer

(ii) JK flipflop

PART C — (1 × 15 = 15 marks)

16. (a) Design a switching circuit that converts a 4 bit binary code into a 4 bit equivalent gray code and implement using ROM array.

Or

(b) A clocked sequential circuit is provided with a single input x and a single output z. Whenever the input produces a string of pulses 111 or 000, the circuit should produce an output of z=1. (Overlapping is allowed)

(i) Obtain the state diagram

(ii) Obtain the state table

(iii) Design the sequence detector using D flip flop.

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