Design and Simulate of 1001 Sequence detector Using eSim Tool

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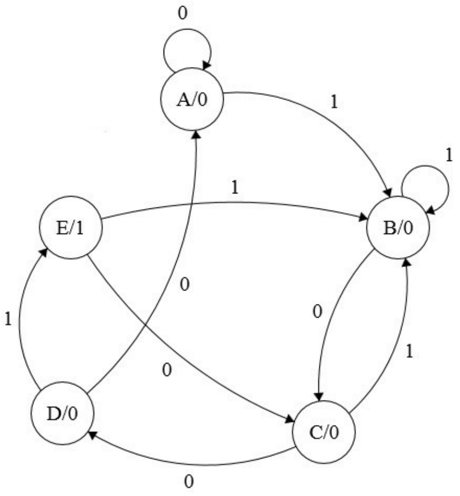
Abstract-sequence detector is a part of digital circuit which takes bit strings as input and gives output as 1 when the correct sequence has been detected. Sequence detector work on the principal of finite state machine.State machine are of two typeas mealy and moore machine .mealy machine is and FSM whose output depends on the present state as well as the present input where as moore machine only depends on only present input.

INTRODUCTION

In paper this post we are going to discuss the Verilog code of 1001 sequence detector. The sequence detector is of overlapping type. It means that the sequencer keep track of the previous sequences. Whenever the sequencer finds the incoming sequence matches with the 1001 sequence it gives the output 1.

As Moore machine is used mostly in all practical designs the Verilog code for 1001 sequence detector fsm is written in Moore fsm logic.

1001 Sequence Detector State Diagram is given below.



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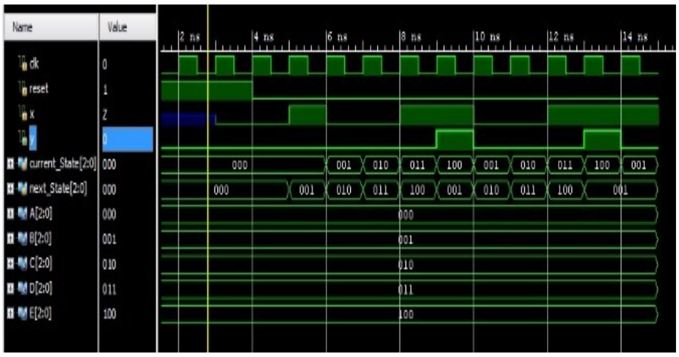
VERILOG CODE

```
module Moore machine
(
   input wire clk, reset,
   input wire  in ,
   output reg  out,
     reg[2:0] state_reg, state_next

);
parameter [2:0]     // for 5 states /// size_state = 2:0//
   s0 = 3'b000,
   s1 = 3'b001,
   s2 = 3'b010,
   s3 =  3'b011,
   s4 = 3'b100  ;
// state register : state_reg//
always @(posedge clk, posedge reset) begin
   if (reset) begin
      state_reg <= s0;
   end
   else begin
      state_reg <= state_next;
   end
end
 // This is the combinational part of the sequential design//

always @(in, state_reg) begin
   state_next = state_reg; // default state_next//
   case (state_reg)
      s0 : begin
         if (in == 1'b1) begin
            state_next = s1;
         end
         else begin // remain in current state//
            state_next = s0;
         end
      end
      s1 : begin
          if (in == 1'b1) begin
            state_next = s2;
         end
         else begin // remain in current state//
            state_next = s0;
         end
      end
      s2 : begin
         if (in == 1'b0) begin
            state_next = s3;
         end
         else begin // remain in current state//
            state_next = s2;
         end
      end
      s3 : begin
         if (in == 1'b1) b
```

OUTPUT



Reference

IMPLEMENTATION OF SEQUENCE DETECTOR USING REVERSIBLE LOGIC N Srinivasa Rao Dept. of ETE, BMS College of Engineering, Bengaluru, India,