Design and Simulate of 1001 Sequence detector Using eSim Tool

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Abstract-Sequence detector is a part of digital circuit which takes bit strings as input and gives output as 1 when the correct sequence has been detected. Sequence detector work on the principal of finite state machine.State machine are of two typeas mealy and moore machine .mealy machine is and FSM whose output depends on the present state as well as the present input where as moore machine only depends on only present input.

INTRODUCTION:

In paper this post we are going to discuss the Verilog code of 1001 sequence detector. The sequence detector is of overlapping type. It means that the sequencer keep track of the previous sequences. Whenever the sequencer finds the incoming sequence matches with the 1001 sequence it gives the output 1.

As Moore machine is used mostly in all practical designs the Verilog code for 1001 sequence detector fsm is written in Moore fsm logic.
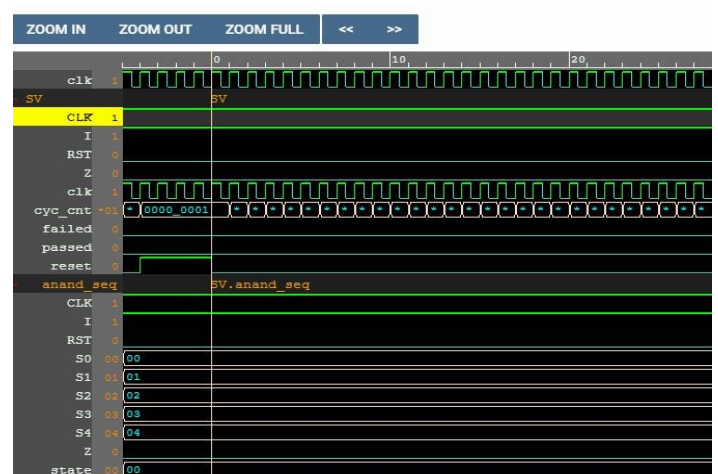
1001 Sequence Detector State Diagram is given below.

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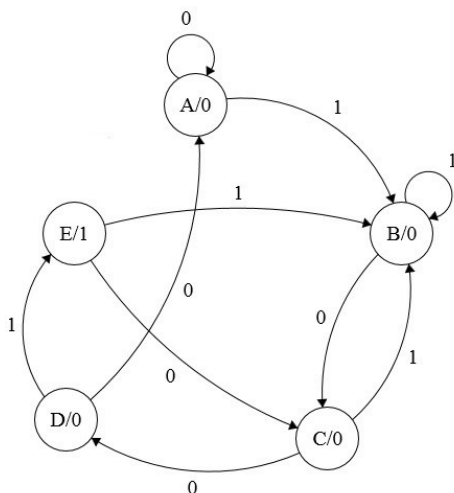
CIRCUIT DIAGRAM:
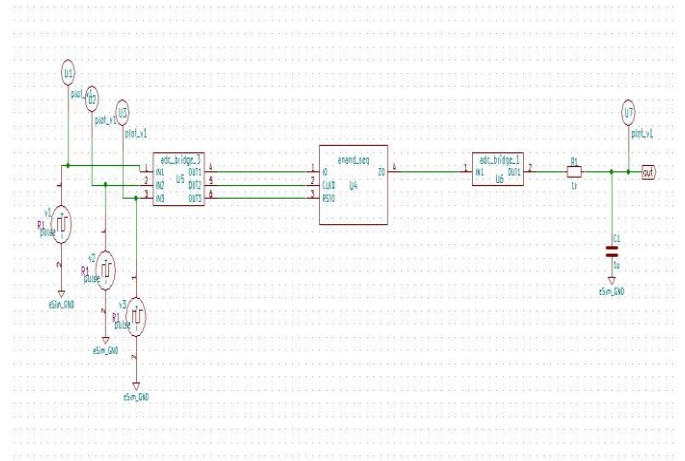
OUTPUT :

REFERENCE:

[1] Digital Design by Morris Mano.

[2] Minns, Peter D., and Ian Elliott. FSM-based digital design using Verilog HDL. John Wiley & Sons, 2008.