Silicon waveguides fabrication for integrated photonics-based quantum processor

Alok Anand
Electrical & Computer Engineering,
Carnegie Mellon University
Pittsburgh, USA
aloka@andrew.cmu.edu

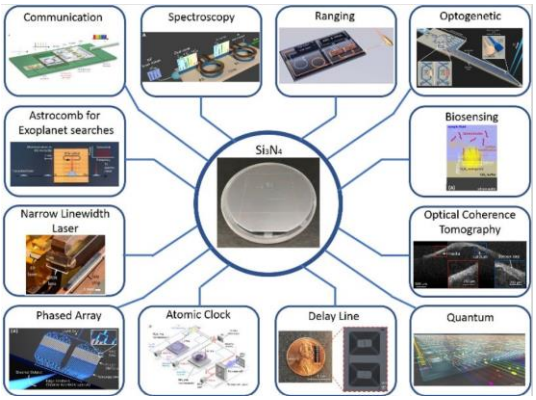
I. Introduction

Advancements in fabrication of Silicon photonics in recent years have led to enabling utilization in generation and detection of optical signals integrated on-chip. To achieve integrated Silicon photonics circuits, Silicon Nitride has promising characteristics with operation in sub-milliwatt optical pump power, high spectral brightness, and high photon purity. Fabrication of Silicon Nitride waveguides is performed in way like CMOS fabrication technology involving DUV stepper lithography, dry etching, and low-pressure chemical vapor deposition. Integrated Silicon Nitride micro-ring resonator is fabricated with cladding of silicon dioxide on lower side with top air cladding. In fabrication of resonators, core of the device is a high-Q Si_3N_4 micro-ring that needs critical parameters monitoring for silicon nitride film thickness, ring width and ring radius.
For silicon nitride (Si_3N_4) supporting a much wider bandgap, enabling operation across wavelengths from the near-ultraviolet to the mid-infrared, it leads to achieve high yield photonic micro-resonators for quantum processors, it is required to high quality silicon nitride waveguides for loss less circuit, along with generation of single photon delay lines and entanglement generation with CNOT gates. Integrated Silicon nitride photonics-based quantum gates fabrication will help to release bulk photonics integrated circuits in uniform and scalable form with different components like memories and detectors fabricated on to get a full integrated processor.

II. Background

With tremendous growth in silicon waveguides and ring resonator and its promising application in a wide range of its application in silicon communications, light detection and ranging, bio-sensing, atomic clock, and photonics quantum circuits. Silicon waveguides, particularly photonics utilize standard complementary metal-oxide semiconductor fabrication process to achieve high density, high yield with mass fabrication. In photonics application Silicon, Silicon Nitride and Silicon dioxide has wider applications with Silicon nitride-based waveguides with the promise of wide transparency range covering visible to mid-IR range.

Low propagation losses are crucial for on-chip optical waveguides in applications as nonlinear and quantum photonics, optical gyroscopes, and narrow linewidth lasers. Silicon nitride waveguide and resonator for photonic applications, employs standard CMOS fabrication technology with stepper lithography, dry etching, low pressure chemical vapor deposition.



III. Fabrication Process

Fabrication of silicon nitride waveguide is performed using subtractive processing and Damascene process. Subtractive process is an additive, robust and reproducible method for fabricating silicon nitride films directly deposited on the substrate and waveguides are then patterned in resist and followed by etching of surrounding silicon nitride film. Damascene process includes fabrication of waveguides with etching trenches in thermally oxidized silicon followed by filling silicon nitride in trenches. Damascene process includes CMOS fabrication technology of DUV stepper lithography, dry etching, low vapor deposition.

Fabrication process silicon nitride waveguides, determines critically function of optical device and material properties used in these films.

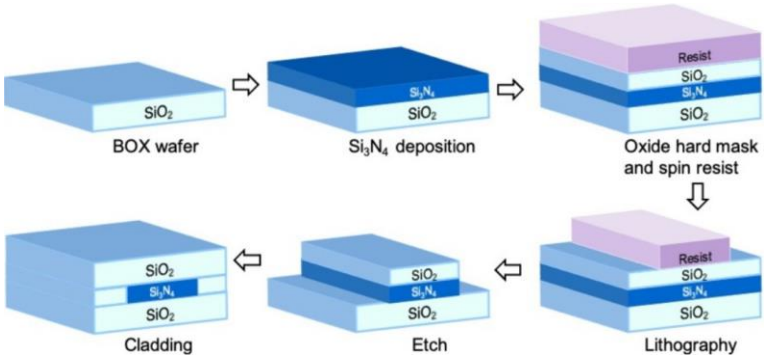


Figure 1. Steps involved in fabrication of Silicon nitride waveguides

(A) Oxidation: In fabrication of silicon nitride waveguide core-layer with cladding layer of Silicon dioxide on top and bottom layer, utilizes combination of dry and wet oxidation process at 1200 DegC that provides thick oxide layer of 2-4um of high quality.

(B) Deposition: Higher density film with lower roughness and optical loss is favored with multilayer deposition of silicon nitride waveguide performed using reactive gases ammonia and Di-chlorosilane at 800 Deg C form silicon nitride, hydrogen, and hydrochloric acid. Deposition of silicon nitride using LPCVD, is annealed in argon atmosphere at 1200 DegC derive out bonded hydrogen to improve quality of deposited films. Process is repeated to perform multilayer deposition process to achieve final deposition thickness.

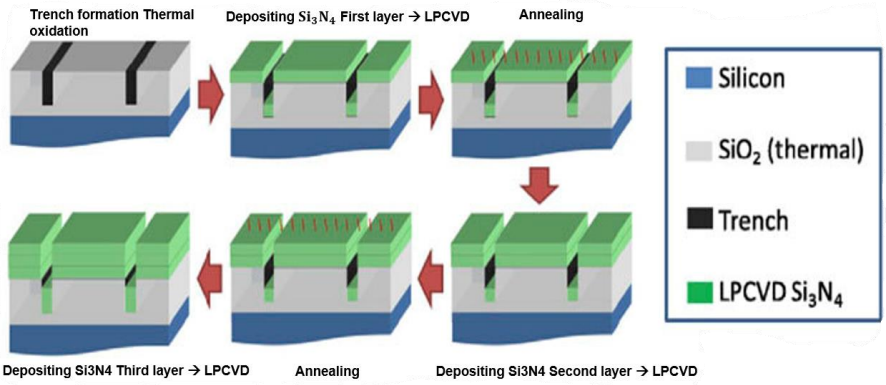


Figure 2. Multi-layer deposition of Silicon nitride waveguides

(C) Lithography: E-beam Lithography is performed accelerating voltage of 100 KV, with beam current adjusted to 100nA. Wafer is cleaned with RCA cleaned, with negative photo-resist coating, followed by prebake and lithography process to attain small feature size.
(D) Etching: After lithography process and resist development design pattern is transferred using etch pattern. In Silicon nitride etching is performed with mixture of trichloromethane at 47 sccm, oxygen at 23 sccm and nitrogen at 7 sccm that reduces polymer deposition on sidewalls. Oxygen flow is kept high to remove polymer formation as oxygen reacts with polymer to form carbon monoxide and carbon dioxide.
(E) Cladding: In the final fabrication process to obtain multilayer top cladding silicon nitride with deposition of thin, high quality oxide deposition with LPCVD that uses DCS and nitrous oxide to form high temperature silicon dioxide layer with two steps one from low quality oxide layer and high-quality oxide layer to provide thick cladding.

IV. Optimization of fabrication steps to achieve high quality waveguides

Quality factor is a measure of sharpness of resonance relative to its central frequency and represents stored energy of resonator. Quality factor is measured using laser scanning technique and measurement of photon lifetime by ring-down with rapid scanning of laser into resonance.

(A) Surface roughness on effect on waveguide and improvement of fabrication step
Surface roughness during etch process plays major role in loss limitations caused because of O-H bonds in SiO_2 and N-H and Si-H bonds in Si_3N_4. Side wall roughness is reduced with optimize etch recipe. Polymer formation is reduced in dry etch transfer process with higher oxygen flow that removes polymer residue to form carbon monoxide (CO) and carbon dioxide (CO_2).
Q is high and the mode is highly confined, extremely small defects or roughness can induce a visible splitting.
Normalized transmission spectra of waveguide fabricated using different processes reduces frequency splitting to achieve high Q.

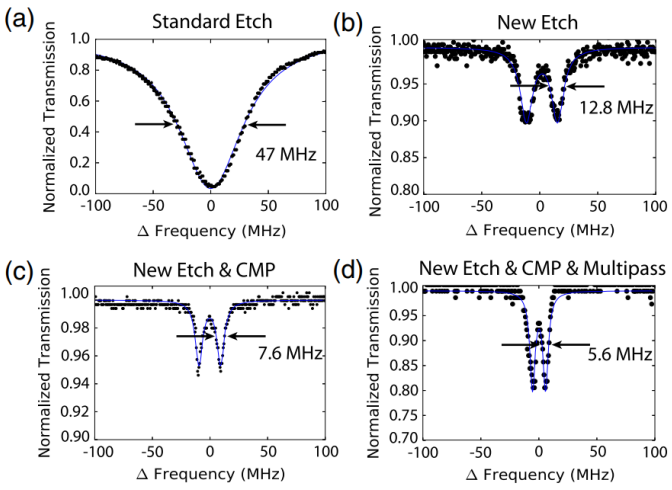


Figure 3. Frequency transmission from waveguide obtained with different fabrication step

(a) Device fabricated using the standard process, measured FWHM of 47 MHz
(b) Device fabricated using the optimized etch process optimized etch process but without CMP and without multi-pass lithography, but without our new surface smoothing technique and multi-pass lithography with a measured FWHM of 12.8 MHz
(c) Device fabricated using both optimized etch recipe and CMP but without multi-pass lithography, FWHM of 7.6 MHz
(d) Device fabricated with optimized etch recipe, surface smoothing technique, multi-pass lithography with a measured FWHM of 5.6 MHz

Oxygen reacts with photoresist, used in etching as mask to transfer patterns. To avoid this effect, higher oxygen flow is maintained to decrease the etching selectivity, degrading the ability to transfer patterns. For compensating this effect, a silicon dioxide hard mask instead of a photoresist to maintain the ability to transfer waveguide patterns along with eliminating polymer formation on the sidewalls with a higher oxygen flow. Nitrogen is also added to increase the nitride selectivity over oxide.

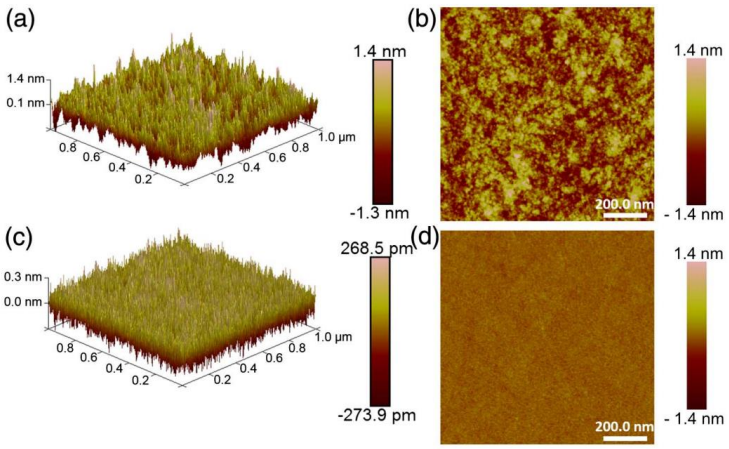
(B) Multi-pass lithography reduces the lithography induced roughness thickness.

Electron-beam (E-beam) lithography, employs extensive use of pattering optical waveguides, provides a line edge roughness, leads extra roughness to the sidewalls. During E-beam lithography, instability from beam current fluctuations, beam jitter, beam drift, stage position errors, and mechanical vibration generate statistical errors, resulting in line edge roughness in the patterns, adding roughness to the sidewalls.

To reduces the line edge roughness, employing multi-pass lithography consists of exposing same pattern multiple times at a lower current

Figure 4. AFM measurement of the top surface of Si_3N_4.

(a) 3D AFM scan of the top surface of Si_3N_4 before CMP with RMS roughness of 0.38 nm and correlation length of 29 nm.
(b) 2D image of the top surface of Si_3N_4 before CMP and scaled to −1.4 to 1.4 nm with RMS roughness of 0.38 nm and correlation length of 29 nm.
(c) 3D image of the top surface of Si_3N_4 after CMP with RMS roughness of 0.08 nm and correlation length of 8.76 nm.
(d) 2D image of the top surface of Si_3N_4 after CMP and scaled to −1.4 to 1.4 nm with RMS roughness of 0.08 nm and correlation length of 8.76 nm.



Reduction of top and bottom waveguide roughness to achieve high factor to utilize CMP chemical mechanical polishing (CMP) of Si_3N_4 after deposition. Root-mean-squared (RMS) roughness has decreased from 0.38 nm to 0.08 nm (AFM scans of different CMP Si_3N_4 films). CMP process of providing smooth surface, determined by roughness of CMP pad and slurry.

2D and 3D AFM measurements of Si_3N_4 surface roughness before and after CMP using different pads and slurries. CMP pad plays a more important role than slurry in reducing surface RMS, root mean squared (RMS) roughness can be decreased from 0.38 nm (before polishing) to 0.08 nm (after optimized polishing).

V. Conclusion

This report describes fabrication step of silicon nitride waveguides for photonics and different steps and the steps variation that affect the quality factor of waveguide resulting in high losses. Optimization of fabrication step in etch, lithography techniques that are utilized to minimize losses and achieve high quality waveguides. To minimize roughness of the waveguide interface with overall performance of the device.

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