Course code	Course Name	L-T-P-Credits	Year of Introduction
IC207	DESIGN OF LOGIC CIRCUITS	3-0-0-3	2016

Course Objectives

- To study various number systems and conversions
- To study Boolean Algebra
- To study combinational logic design and circuits
- To study various sequential components and circuits
- To study finite state machines
- To study the logic families.

Syllabus

Number system and codes - Boolean algebra and related theorems – Combinational logic and reduction using Algebraic Method and Karnaugh maps – Combinational circuits – Latches, Flip-Flops and registers – Asynchronous counters - Introduction to design of synchronous sequential circuits using Finite State Machines – Basic working of TTL NAND and CMOS inverter gates.

Expected Outcome

After the completion of the course, students should be able to

- Convert numbers represented in one system to other
- Simplify Boolean expressions
- Design and implement combinational circuits
- Design and implement sequential circuits
- Explain the working of TTL NAND and CMOS inverter gates

Text Books:

1. Charles H. Roth, Jr. Fundamentals of Logic Design, 5th edition, Thomson Books/Cole.
2. A. Anand Kumar, Fundamentals of Digital Circuits, PHI learning, 2/e, 2010, ISBN: 978-81-203-3679-7.

Reference Books:

1. Thomas L Floyd, Digital Fundamentals, Pearson, 10/e, 2011.
2. Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with VHDL Design, TMH
3. John F Wakerly, Digital Design- Principles and Practices(Third edition), Pearson
4. Taub and Schilling, Digital principles and applications, TMH
5. Mano M M, Digital Design, PHI.
6. R P Jain, Modern Digital Electronics, Tata Mc Graw Hill, 4/e, 2009.

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	Number systems: Binary, Octal, and Hexadecimal - Representation of negative numbers in binary - Binary arithmetic.	2	15%

	Binary codes: BCD & BCD addition, XS-3 & Gray Codes, Error detection and correction codes - Parity & Hamming codes.	2	
	Boolean algebra: Operations, Laws & Theorems, De Morgan's theorems - SOP & POS Boolean expressions and truth tables	2	
II	Applications of Boolean Algebra: Formation of switching functions from word statements, Minterm and Maxterm expansions, Incompletely specified functions.	3	**15%**
	Minimization Techniques: Algebraic, Karnaugh map (up to 6 variables) & Quine-McCluskey methods - Realization using basic gates and universal gates.	6	
FIRST INTERNAL EXAM			
III	Combinational Logic Circuits & Design: Adders & Subtractors – Types, Ripple carry & Carry look ahead adders, BCD adder.	3	**15%**
	Code converters – examples & Comparators. Multiplexers, Demultiplexers, Decoders & Encoders.	3	
IV	Sequential Logic circuits & Design: Latches – SR Latch. Flip-Flops – SR, JK, D & T Flip Flops – Level & Edge triggered flip flops – Synchronous & Asynchronous inputs - Conversion between flip flops. Master slave flip flops.	3	**15%**
	Shift Registers: SISO, SIPO, PISO, PIPO shift registers, Right & Left shifts, Bidirectional & Universal shift registers. Applications: Serial binary adder and binary multiplier circuits.	3	
SECOND INTERNAL EXAM			
V	Counters: Asynchronous counters- Up, Down and Up/ Down counter, Mod n counters.	4	**20%**
	Introduction to design of synchronous sequential circuits using Finite State Machines - Mealy & Moore types with single input-single out problems- Synchronous counter design	4	
	Shift register counters - Ring & Johnson counters.	1	
VI	Logic families: Introduction to different logic families, Standard logic levels - Current and voltage parameters - fan in and fan out - Propagation delay, noise consideration.	1	**20%**
	TTL: Basic working principle of a TTL NAND gate - Totem pole and Open collector gate output configurations - Tri-state logic - characteristics of a TTL NAND gate.	3	
	CMOS: Basic working principle of a CMOS inverter, Comparison of TTL & CMOS, Interfacing TTL & CMOS ICs.	2	
END SEMESTER EXAM			

QUESTION PAPER PATTERN:

Maximum Marks: 100 Exam Duration: 3 Hours

There shall be three parts for the question paper.

Part A includes Modules 1 & 2 and shall have three questions of fifteen marks out of which two are to be answered. There shall be subdivisions, limited to a maximum of 4, in each question.

Part B includes Modules 3 & 4 and shall have three questions of fifteen marks out of which two are to be answered. There shall be subdivisions, limited to a maximum of 4, in each question.

Part C includes Modules 5 & 6 and shall have three questions of twenty marks out of which two are to be answered. There shall be subdivisions, limited to a maximum of 4, in each question.

Note: Each part shall have questions uniformly covering both the modules in it.