Computer Architecture LAB
Assignment-5 Report

Discrete Event Simulator

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Contents

1 Previous Processor

Program	Number of instructions	Number of cycles	ThroughPut
Descending	305	507	0.6
Even - odd	12	20	0.6
Fibonacci	110	169	0.65
Palindrome	29	41	0.71
Prime or not	19	31	0.61

2 Current Processor

Program	Number of instructions	Number of cycles	ThroughPut
Descending	237	12217	0.019
Even - odd	7	329	0.021
Fibonacci	86	4245	0.02
Palindrome	22	1005	0.0218
Prime or not	12	605	0.0198

3 Conclusion

As we can see from the above tables, latency of each event has affected the throughput to a large extent. Also we can observe that the throughput of all the benchmark programs are close to 0.02 which is 1/memory_latency. This is happening because memory latency is very high compared to number of other events latency.