Computer Architecture Lab

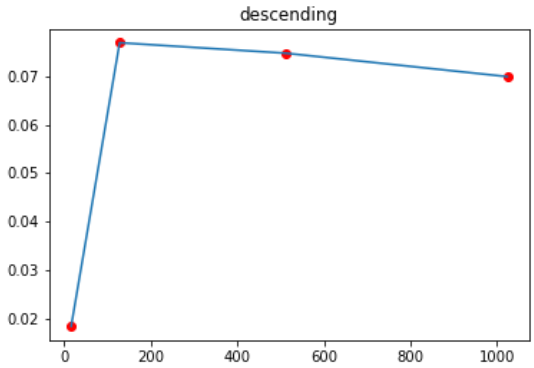
Assignment 6 - Implementation of L1 Cache

Anand Hegde - 200020007

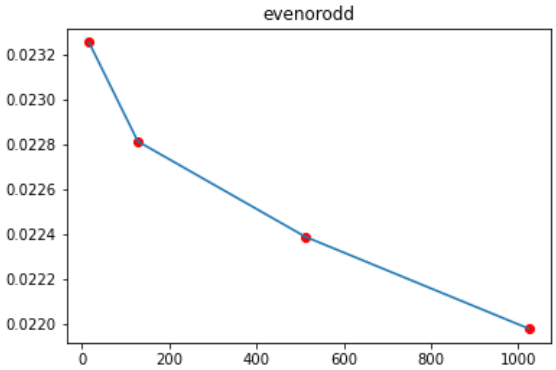
Arvind Kumar M - 200020008

IPC vs L1-i cache size

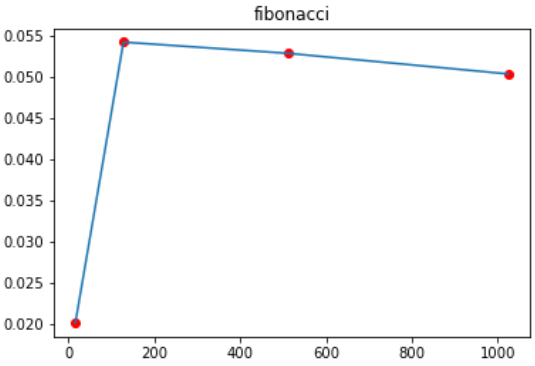
Descending



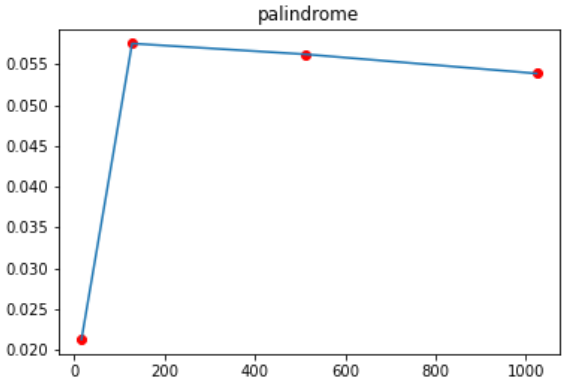
EvenOrOdd



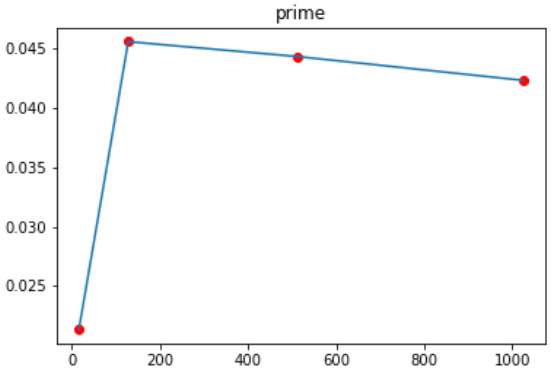
Fibonacci



Palindrome

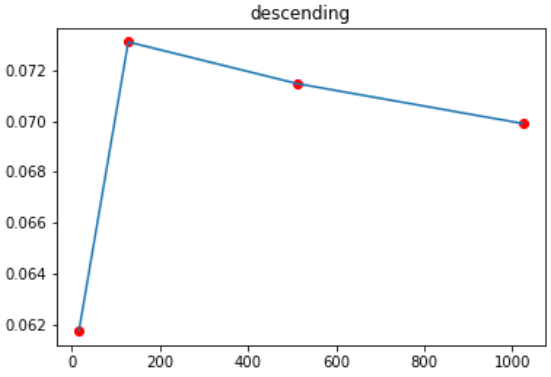


Prime

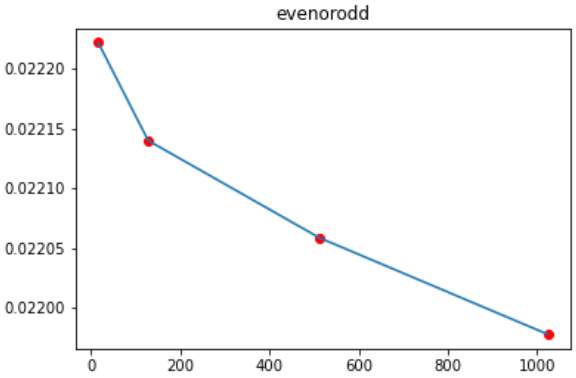


IPC vs L1-d cache size

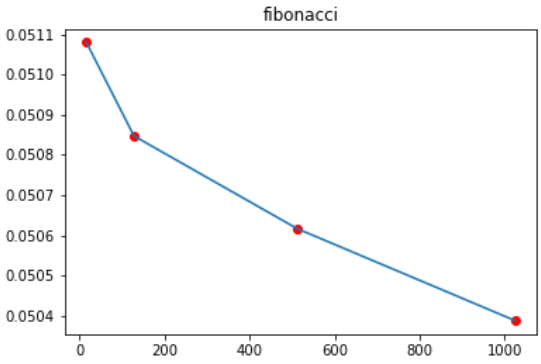
Descending



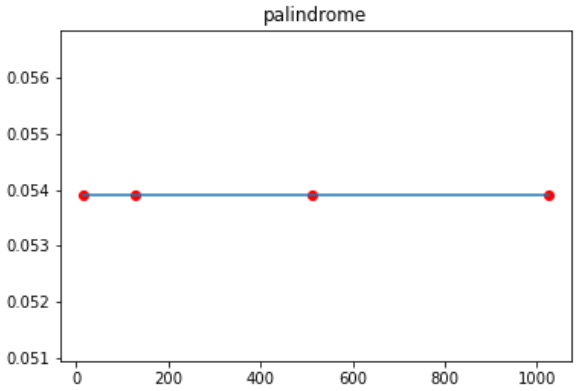
EvenOrOdd



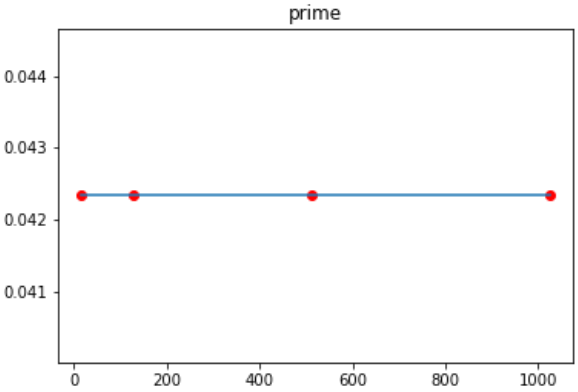
Fibonacci



Palindrome



Prime



Observation from plots

- In descending, prime, palindrome and fibonacci there is temporal locality of instructions fetched. So the IPC increases when L1-i cache size is increased from 16B to 128B.
- It is observed that 128B L1-i cache is optimal for both of them. As we increase the size further, the latency of cache increases which decreases the IPC.
- In the Even-odd program there is little temporal locality. So the graph has a negative slope which means IPC decreases.
- In the program descending, where we have to sort the given array. So there will be temporal locality which cannot fit inside 16B but they can be fitted in 128B so, the IPC increases when we increase the cache size to 128B but, again it decreases because of the penalty from the larger latency of larger caches.
- In the programs prime and palindrome have very data-memory access statements, so the slope is close to 0.

- In even odd and Fibonacci, we have data-access statements that can be fitted inside 16B. So, When we increase the cache size the penalty due to latency is hurting the performance.

Benchmark program for L1-i cache

Program to show performance improvement when L1-i cache size is increased from 16B to 128B keeping L1-d cache size as 128B.

ToyRisc Program

```
    .data
a:
    10
    .text
main:
    sub %x6, %x6, %x6
    addi %x6, 10, %x6
loop:
    addi %x9, 1, %x9
    addi %x9, 2, %x9
    addi %x9, 3, %x9
    addi %x9, 4, %x9
    addi %x9, 5, %x9
    addi %x9, 6, %x9
    subi %x6, 1, %x6
    bgt %x6, %x0, loop
    end
```

Comparison

Parameters\Cache size	16B	128B
No. of instructions	83	83
No. of Cycles	3777	755
IPC	0.021	0.109

Benchmark program for L1-d cache

Program to show performance improvement when L1-d cache size is increased from 16B to 128B keeping L1-i cache size as 128B.

ToyRisc Program

```
      .data
a:
      1
      2
      3
      4
      5
      6
      7
      .text
main:
      sub %x4, %x4, %x4
      sub %x3, %x3, %x3
      addi %x3, 10, %x3
for:
      load %x4, $a, %x4
      load %x4, $a, %x4
      load %x4, $a, %x4
      load %x4, $a, %x4
      load %x4, $a, %x4
      load %x4, $a, %x4
      load %x4, $a, %x4
      sub %x4, %x4, %x4
      subi %x3, 1, %x3
      bgt %x3, %x0, for
      end
```

Comparison

Parameters\Cache size	16B	128B
No. of instructions	104	104
No. of Cycles	3557	1107
IPC	0.029	0.093