VLSI Engineering Lab Assignment 2

(Deadline - March 16, 2020 at 1359 hrs)

Refer to the Baugh Wooley Multiplier discussed in the lab. Modify the architecture which has an additional control input t. When t = 0, the multiplier treats the real time inputs as unsigned numbers and functions as Braun's array multiplier. When t = 1, the multiplier treats the real time inputs as two's complement numbers and functions as the modified Baugh Wooley Multiplier. The most optimized array multiplier in terms of hardware shall fetch full credit. Include all the optimization that was discussed during the lab class.

Write the Verilog Code for the above m×n combined unsigned and two's complement array multiplier accepting two numbers A and B having 7 and 6 bits respectively (choose the multiplier and the multiplicand smartly), and the control signal t, with exhaustive simulation outputs. Instantiate the requisite number of half adders and full adders in the code along with other logic gates as deemed necessary.

Answer the following questions.

1) For an m × n multiplier with an m-bit multiplicand and n-bit multiplier accepting the additional control signal t, compute the following:
(i) The number of half adders and full adders required as a function of m and n
(ii) The computation time necessary to obtain the product bits in terms of the propagation delay of half adder (tHA) and full adder (tFA). You may ignore the propagation delay of the logic gates performing the logic operation to generate the partial products in your estimate and neglect interconnection delays.
a) Baugh Wooley Multiplier
b) Braun's Array Multiplier
c) Sign Magnitude Multiplier

2) Draw the modified array structure for multiplication of numbers with 3 and 5 bits respectively when you perform sign-magnitude multiplication for t = 1 and 2's complement multiplication for t = 0. Does the critical path differ for t = 0 as compared to t = 1?