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NAAC with 'A' Grade

EXAMINATIONS SEPTEMBER /OCTOBER 2020
SUPPLEMENTARY SEMESTER / GRADE IMPROVEMENT/ RE –REGISTERED CANDIDATES

Program	:	**B.E. : Computer Science and Engineering**	**Semester**	:	**IV**
Course Name	:	**Computer Organization and Architecture**	**Max. Marks**	:	**100**
Course Code	:	**CS45**	**Duration**	:	**3 Hrs**

Instructions to the Candidates:

- Answer any one full question from each unit.

UNIT- I

1.	a)	Explain connection between the Processor and the Memory.	CO1	(06)
	b)	Explain the concept of stack frame and frame pointer with an example.	CO1	(06)
	c)	Register R1 and R2 of a computer contains the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions: i) LOAD 20(R1),R5 ii) MOVE #5000,R5 iii) ADD –(R2),R5 iv) SUBTRACT (R1)+,R5	CO1	(08)
2.	a)	Explain Pipelining and Superscalar Operation.	CO1	(08)
	b)	Demonstrate the use of Indirect Addressing mode with an example.	CO1	(06)
	c)	Describe different formats of encoding machine instruction for different Addressing modes.	CO1	(06)

UNIT– II

3.	a)	Explain the working of a hardwired control unit with a diagram.	CO2	(06)
	b)	Multiply each of the following pairs of signed 2's complement numbers using booth algorithm and bit pairing of the multiplier (Assume A is the Multiplicand and B is the Multiplier) i) A=010111 B=110110 ii) A=110011 B=101100.	CO2	(08)
	c)	Write the sequence of control steps required for the single bus structure for the following instruction Add (R2),R1.	CO2	(06)
4.	a)	Draw and explain the multi-bus organization of a Processor.	CO2	(06)
	b)	Give an Algorithm for Restoring division method. Illustrate the working of the Algorithm for 8/3 and Represent $(1259.125)_{10}$ in IEEE floating point format.	CO2	(08)
	c)	Illustrate the working of CSA with 45 and 63 as the Multiplicand and Multiplier respectively.	CO2	(06)

UNIT- III

5.	a)	Explain with an example, different types of dependencies.	CO3	(06)
	b)	Explain with an example the Classic Five-Stage Pipeline for a RISC Processor.	CO3	(06)

	c)	Consider the unpipelined processor in the previous section. Assume that it has a 1 ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40%, respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline?	CO3	(08)
6.	a)	Discuss different types of data hazards with examples.	CO3	(10)
	b)	Justify the statement with respect to the pipeline technique: "If there are no stalls, the speedup is equal to the number of pipeline stages".	CO3	(05)
	c)	Explain Dynamic Branch Prediction and Branch-Prediction Buffers.	CO3	(05)

UNIT- IV

7.	a)	With a neat diagram describe centralized shared memory architecture.	CO4	(08)
	b)	Discuss Directory-Based Cache Coherence Protocols with an example	CO4	(06)
	c)	Differentiate between: i. Write-back and write-through cache. ii. Multicore and Multiprocessor Architectures.	CO4	(06)
8.	a)	With a neat diagram demonstrate write invalidate, cache coherence protocol for a private write-back cache showing the states and state transitions for each block in the cache.	CO4	(08)
	b)	Demonstrate different cache mapping techniques with examples.	CO4	(08)
	c)	With a neat diagram discuss different levels in the memory hierarchy.	CO4	(04)

UNIT- V

9.	a)	Explain Interrupt priority schemes.	CO5	(06)
	b)	Define bus arbitration? Explain the different variants of the bus arbitration.	CO5	(10)
	c)	Explain parallel input interface circuit.	CO5	(04)
10.	a)	Explain use of DMA controller in a computer system.	CO5	(06)
	b)	Differentiate between synchronous bus and Asynchronous bus.	CO5	(10)
	c)	Explain USB architecture and its key features.	CO5	(04)

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