Computer Organization and Architecture

Course Code: CS45 **Credits: 3:1:0**
Prerequisites: Basics of Computers **Contact Hours: 42+28**
Course Coordinator/s: Chandrika Prasad

Course Contents:

Unit 1

Functional units, bus structures, performance, **Overflow in integer arithmetic**: Numbers, Arithmetic operations and characters, Memory locations and addresses, Memory operations, instructions and **instruction sequencing**, addressing modes, Subroutines and use of stack frames, Encoding of machine instructions.

Unit 2

Arithmetic unit: Multiplication of two numbers, A signed operand multiplication, Booth algorithm, Bit pair recoding and CSA – integer division, IEEE standard for floating point numbers. **The Processor:** Processing unit: Fundamental concepts, Execution of complete instruction, Multiple bus organization, Hardwired control, Microprogrammed control. Only Definition

Unit 3

Instruction level parallelism: Introduction and challenges, **Data dependences and Hazards:** Data dependences, Name dependences, Control Dependences, Basic pipeline scheduling and loop unrolling, Pipelining: Introduction, A simple implementation of a RISC instruction set, The classic five-stage pipeline for a RISC processor, Basic performance issues in pipelining, **The major hurdle of pipelining-** pipeline hazards, Performance of pipeline stages, structural hazards, Data hazards, Branch hazards. (loop unrolling: Only Definition & Simple example)

Unit 4

Memory unit: Memory Hierarchy, Basics of Cache memory, Cache mapping techniques, **Multiprocessor Architecture:** Centralized shared-memory architecture, **Distributed memory architecture**, **Basic scheme for enforcing coherence**: Snooping coherence protocols, Basic implementation techniques, An example protocol, Directory based cache coherence protocols, An example Directory protocol. To be ignored

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Unit 5

Input Output Unit: Accessing I/O devices, **Interrupts**: Interrupt hardware, Enabling and disabling of interrupts, Handling multiple devices, Controlling device requests, exceptions, **Direct Memory Access** –Bus arbitration, Synchronous bus and asynchronous bus, parallel port and serial port.

Textbooks:

1. C Hamacher, Z Vranesic, S Zaky: Computer Organization, Tata McGraw Hill, 5th Edition, 2011.
2. John L Hennessy, David A Patterson: Computer Architecture A Quantitative Approach, Elsevier, 5th Edition 2012.

Reference Books:

1. David A. Patterson, John L. Hennessy: Computer Organization and Design, M.K Publishers, 4th edition, 2010
2. William Stallings, "Computer Organization and Architecture, Designing for Performance", 9e, Pearson, 2014.

List of Tutorial Exercises:

1. Demonstrating instruction execution stages using MarieSim Simulator.
2. Executing an ARM programs using ARMsim simulator.
3. Designing an ALU to perform various functions using Logisim simulator.
4. Implementing different multiplication algorithms using Logisim simulator.
5. Implementing pipeline technique using CPUOS simulator.
6. Executing MIPS programs using QtSpim simulator.
7. Designing memory system operations using Logisim simulator

Course Outcomes (COs):

1. Describe an overview of computer hardware and software which includes the basic functional units, interconnection, addressing techniques and instruction sequencing. (PO-1,3,5,10 PSO-1,2)
2. Appraise different algorithms used to perform fast multiplication, division and to represent floating point numbers in binary. (PO-1,2,3,4,5,10 PSO-1,2)
3. Examine basic processing unit and importance of pipelining to achieve instruction level parallelism. (PO-1,2,3,4,5,10 PSO-1,2)