Internal Assessment Question Paper – 2

M.S. Ramaiah Institute of Technology
(Autonomous Institute, Affiliated to VTU)
Department of CSE

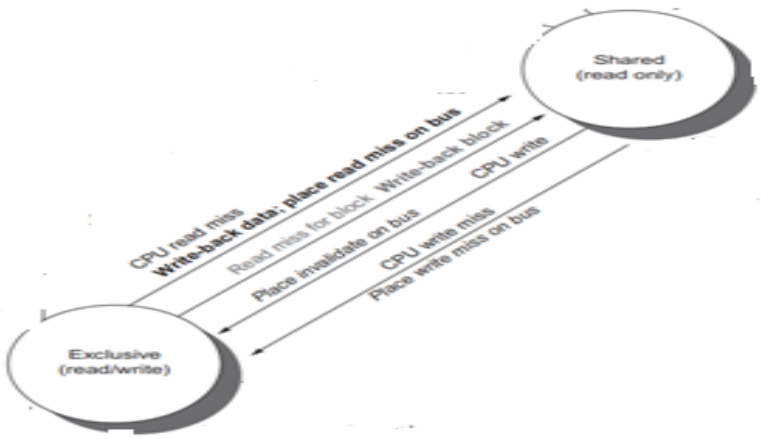
Programme: B.E | **Term: March to June 2021**
Course : Computer Organization and Architecture | **Course Code: CS45**
CIE: I | **Sem: IV** | **Section: A, B & C**
Max Marks: 30 | **Time: 1Hr** | **Portions for Test: L17-L39**
Date: 15/7/2021

Instructions to Candidates: Question 1 is compulsory. Answer any one question from 2 or 3.

Sl#	Question	Marks	Bloom's Level	CO Mapping
1	a) Describe Data dependence and Name Dependence with an example for each	5	Understand	CO3
	b) With a neat diagram explain the features and limitations of centralized memory architecture.	5	Understand	CO4
	c) Discuss how the system handles multiple interrupt-requests simultaneously.	5	Understand	CO5

2	a) Identify any hazards in the following code snippet and also provide the possible solutions for the identified hazard
	`DADD R1,R2,R3`
	`DSUB R4,R1,R5`
	`AND R6,R1,R7`
	`OR R8,R1,R9`
	`XOR R10,R1,R11`
		5	Apply	CO3

	b) Consider a cache block of 128 words and 16 words per block and 64K words of main memory, then show how the main memory address is divided when direct, associative and two-way set associative cache mappings are employed.	5	Apply	CO4
	c)Discuss the following types of Exceptions: i) Recovery from errors ii) Debugging iii) Privilege exception	5	Understand	CO5
	(OR)			
3	a) With a diagram, demonstrate branch hazards that occurs in pipeline technique and provide the solution for the same	5	Apply	CO3
	b) Assume the system has two cores C1 and C2 and employs three-state Snooping cache coherence protocol, identify the reasons for the state transition shown in the following diagram.	5	Apply	CO4

				
	c) Differentiate between **i) Write through and write back cache** **ii) Programmed I/O and Interrupt Initiated I/O**	**5**	**Understand**	**CO5**

CO3: Examine basic processing unit and importance of pipelining to achieve instruction level parallelism.
CO4: Illustrate cache memory mapping techniques, various memory architectures and protocols for cache coherence.
CO5: Explain the basics concepts of I/O, interrupts, direct memory access technique and types of busses.