Internal Assessment Question Paper – 1

Ramaiah Institute of Technology
(Autonomous Institute, Affiliated to VTU)
Department of CSE

Programme: B.E **Term: Feb to** June 2021
Course: Introduction to Microprocessor and Microcontroller **Course Code:** CS43
Date: **CIE:** I **Credits:** 3:0:0
Sem&Section: IV (A, B & C) Date: 10.06.2021
Max Marks: 30 **Time:** 1Hr **Portions for Test:**L1-L19

Instructions to Candidates: Mobiles, smart watches or any electronic gadgets are strictly banned.
Question 1 is compulsory. Answer any one question from 2 or 3.

Sl#	Question	Marks	Bloom's Level	CO Mapping
1	Enumerate and Explain the different ways of embedded programming	8M	L2	CO1
	b)i)List various Implementation features of Cortex M0 ? ii)What is result and NZCV status flag values when the following arithmetic operations are done. Justify your answer a) 0x70000000 +0x70000000 b) 0x00001234 - 0x00001000 c) 0x80000000 +0x80000000 d) 0x90000000 + 0x90000000	3+4=7M	L3	CO2
2	a)Explain the register transfer level design to determine exactly the control signals that are required to cause the datapath to carry out the full set of operations.also explain CortexM0 's Interrupt Vector Table.	9M	L2	CO1
	b) Discuss about the pipeline hazards in RISC. Also Compare Risc and Cisc Processors	3+3=6M	L2	CO1
3	a)Explain CMSIS organization ? various supporting files ? Describe the advantages of using CMSIS	8M	L2	CO2
	b) Explain the startup sequence of CortexM0? Explain the Program image?	7M	L2	CO2

Course Outcomes meant to be assessed by the IA Test-I:
1. Explain the architecture and organization of the Processors. (PO-2, 3, 4, PSO-1)
2. Design Operation Modes and States using special purpose registers. (PO-1,2, 3, 4,PSO-1)