AIM: To verify the following outputs using FPGA

1) Shift registers
2) Up/down counter

SOFTWARE USED: INTEL QUARTUS PRIME

THEORY :

SHIFT REGISTERS:

A shift register is a sequential logic circuit used to store and move binary data in a specific direction with each clock pulse. It consists of a series of flip-flops connected in a chain, where the output of one flip-flop becomes the input of the next. Depending on the configuration, data can be shifted left or right, and input/output can be either serial or parallel. Common types include SISO (Serial-In Serial-Out), SIPO (Serial-In Parallel-Out), PISO (Parallel-In Serial-Out), and PIPO (Parallel-In Parallel-Out). In FPGA verification, the shift register is tested first in simulation by applying known input patterns and observing the correct bit movement in waveforms. On hardware, the operation is validated by applying clock and data inputs using switches and observing the output on LEDs or via a logic analyzer. This confirms correct shifting direction, reset operation, and data storage functionality.

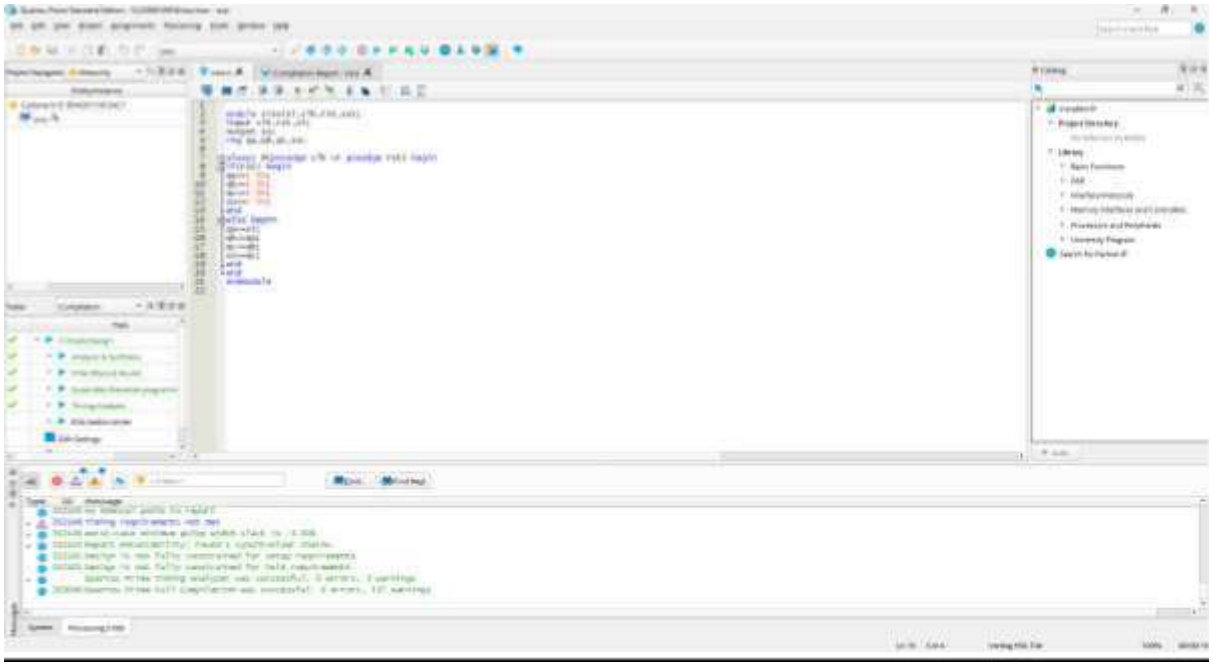
UP/DOWN COUNTER:

An up/down counter is a digital circuit that counts sequentially in increasing (up) or decreasing (down) order, based on a control signal. It can be implemented as a synchronous counter, where all flip-flops are triggered by the same clock, or as an asynchronous (ripple) counter, where the output of one flip-flop serves as the clock for the next. In up mode, the counter increments its value on each clock pulse, while in down mode, it decrements. Verification in FPGA involves simulating the counter to check for correct counting sequence, direction changes, and wrap-around behavior when limits are reached. In hardware testing, clock inputs are provided from the FPGA's internal clock or push buttons, and outputs are displayed on LEDs or 7-segment displays. This

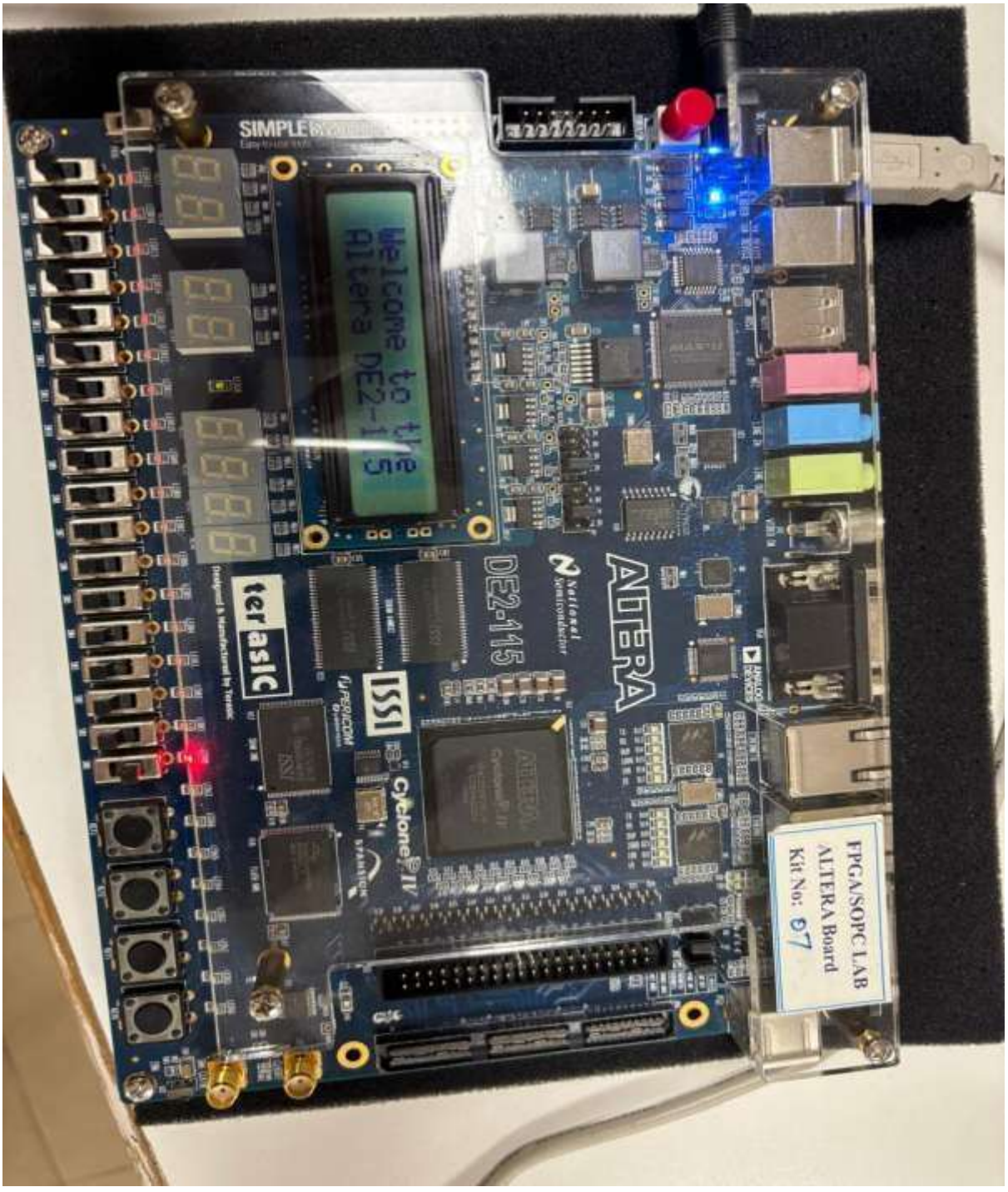
ensures that both up and down counting functions operate as expected under various test conditions.

VERILOG CODES :

1) SISO



OUTPUT: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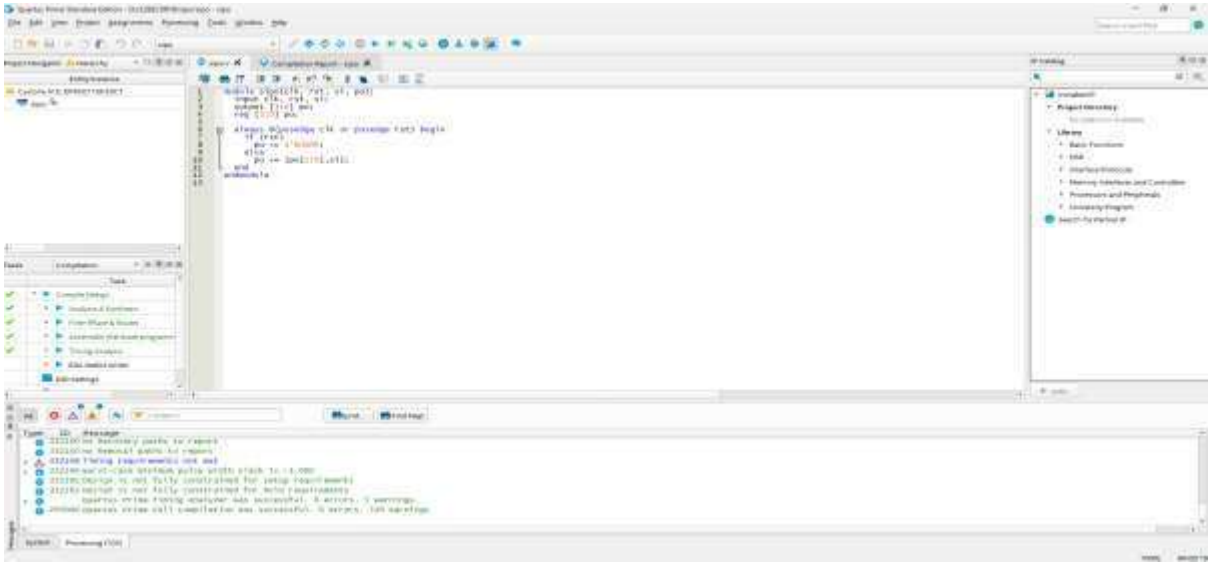
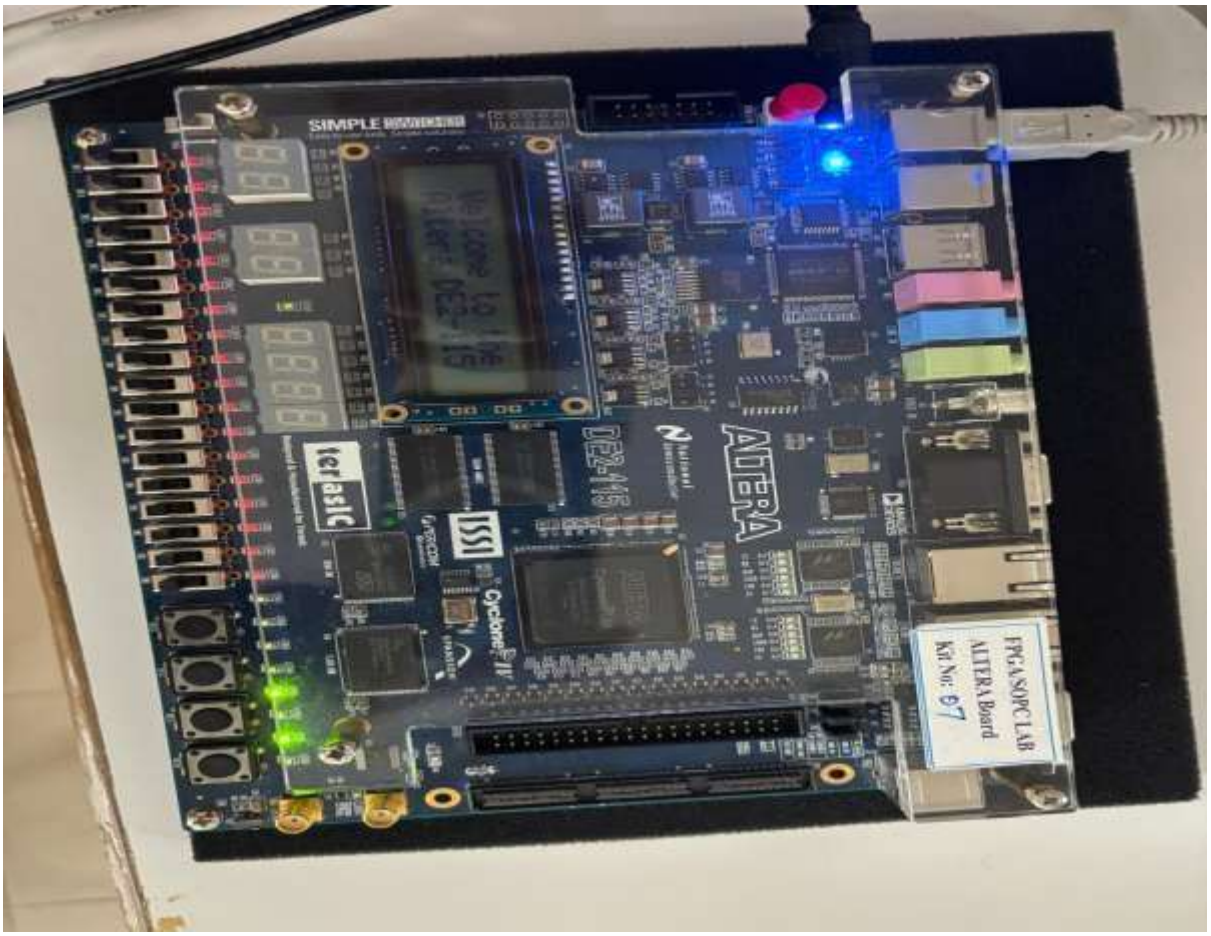
2) SIPO:



OUTPUT:

VERIFIED FOR INPUT- 1010



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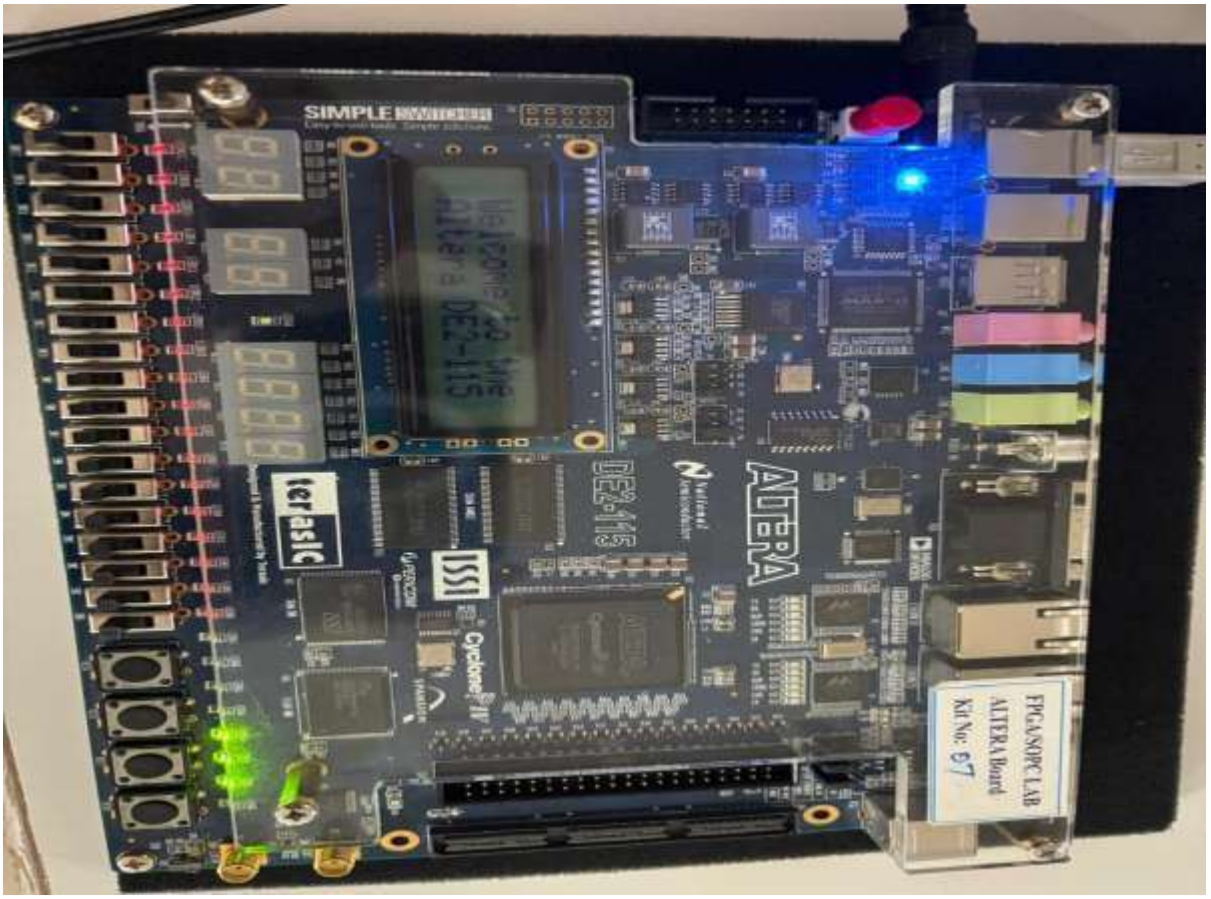

VERIFIED FOR INPUT- 1001

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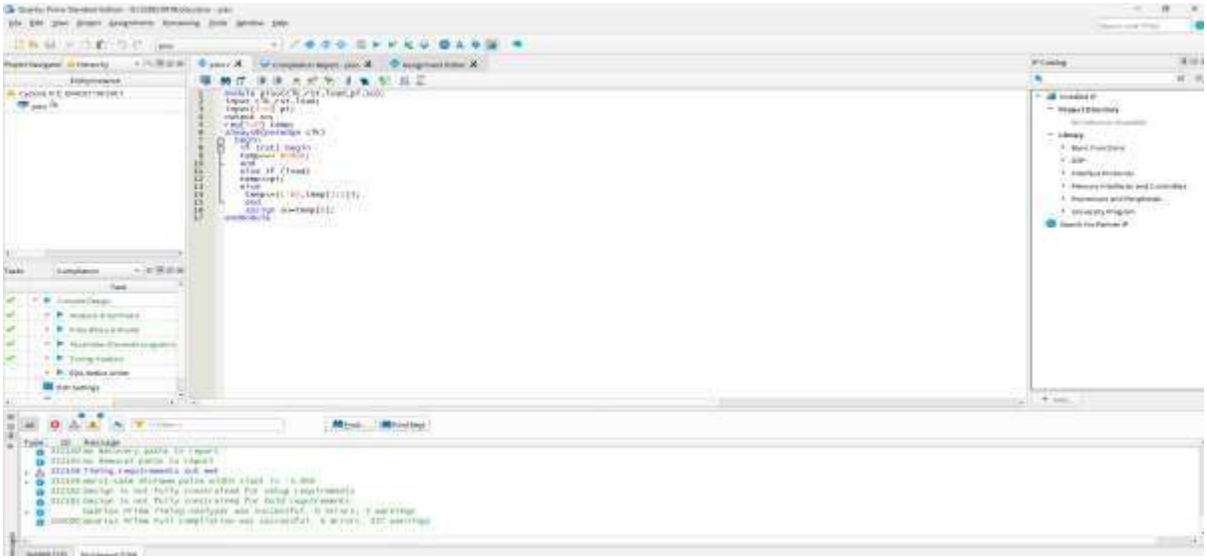
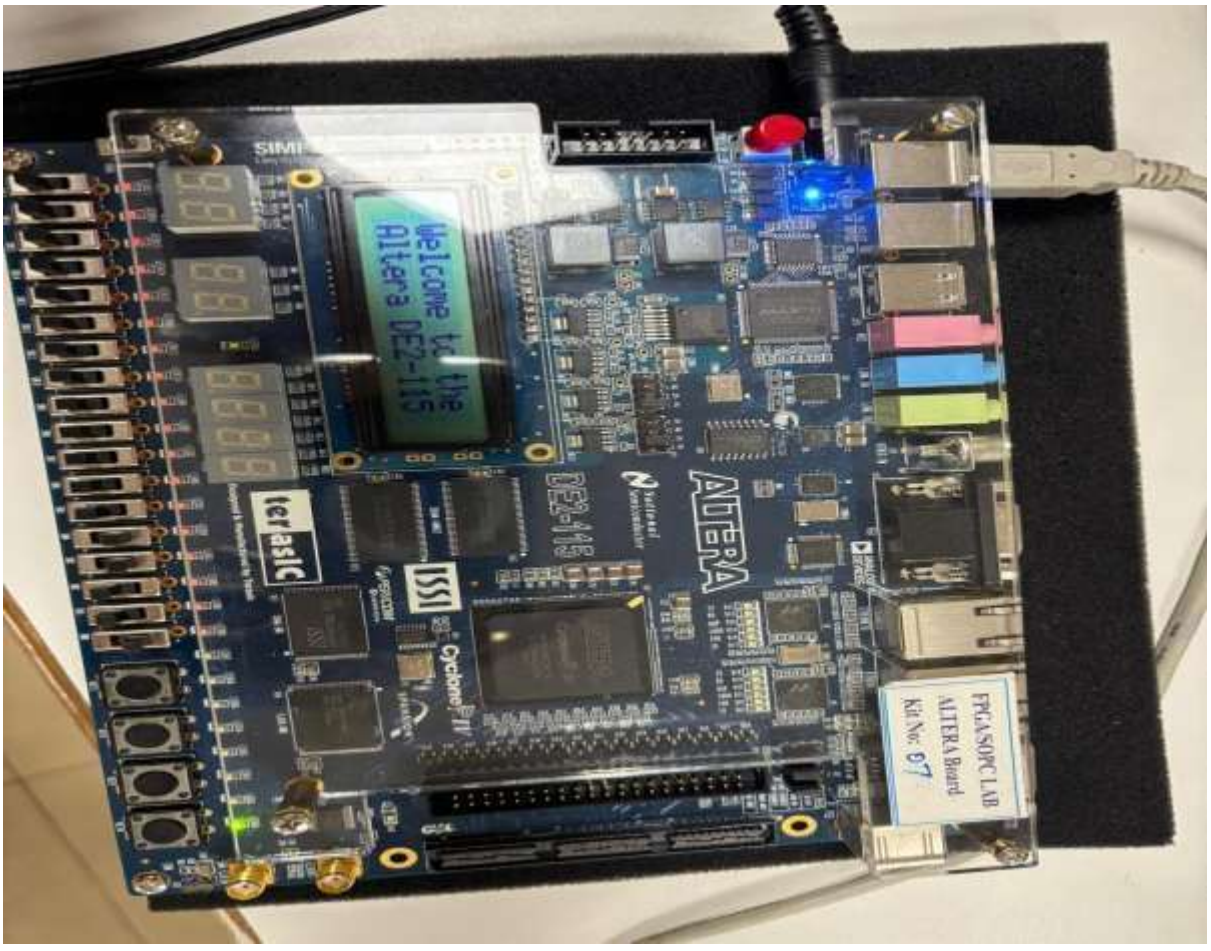


OUTPUT:

VERIFIED FOR INPUT-1001

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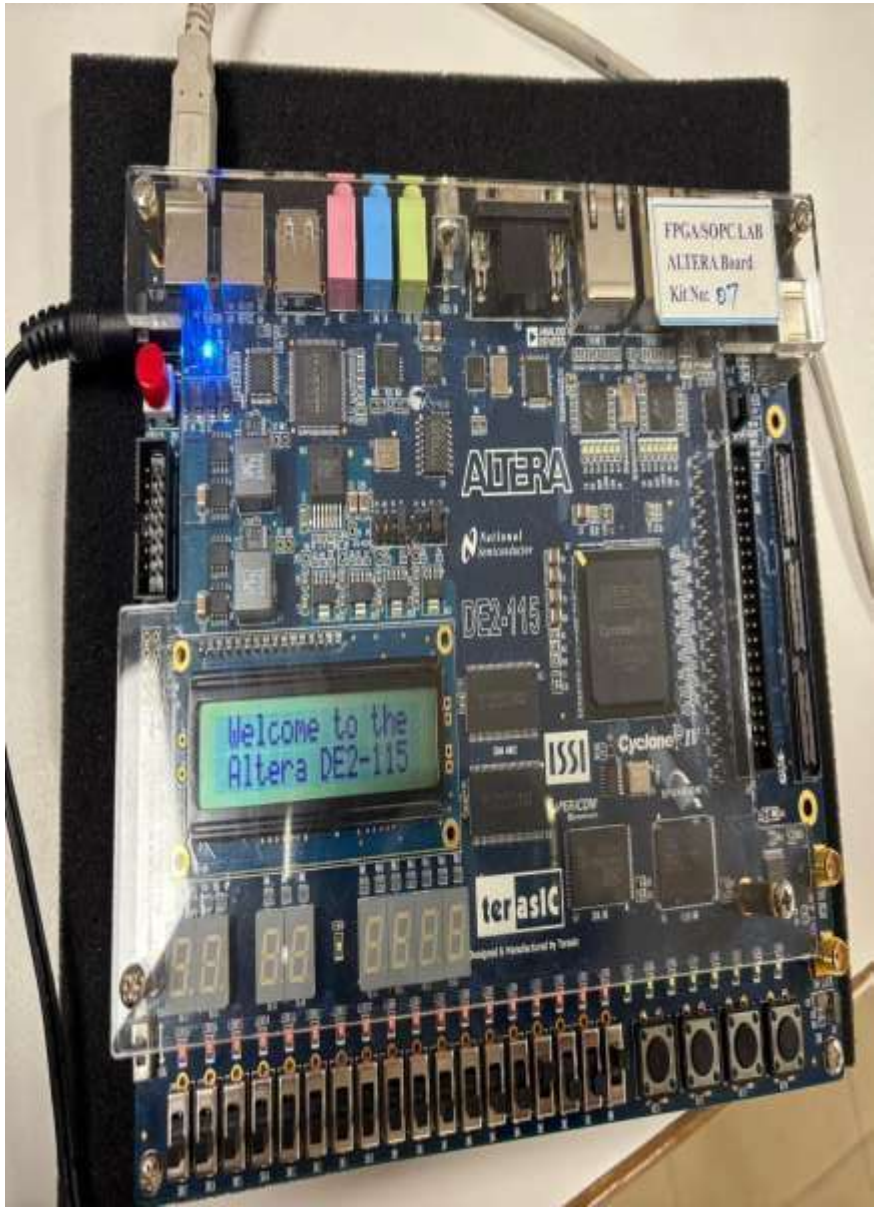
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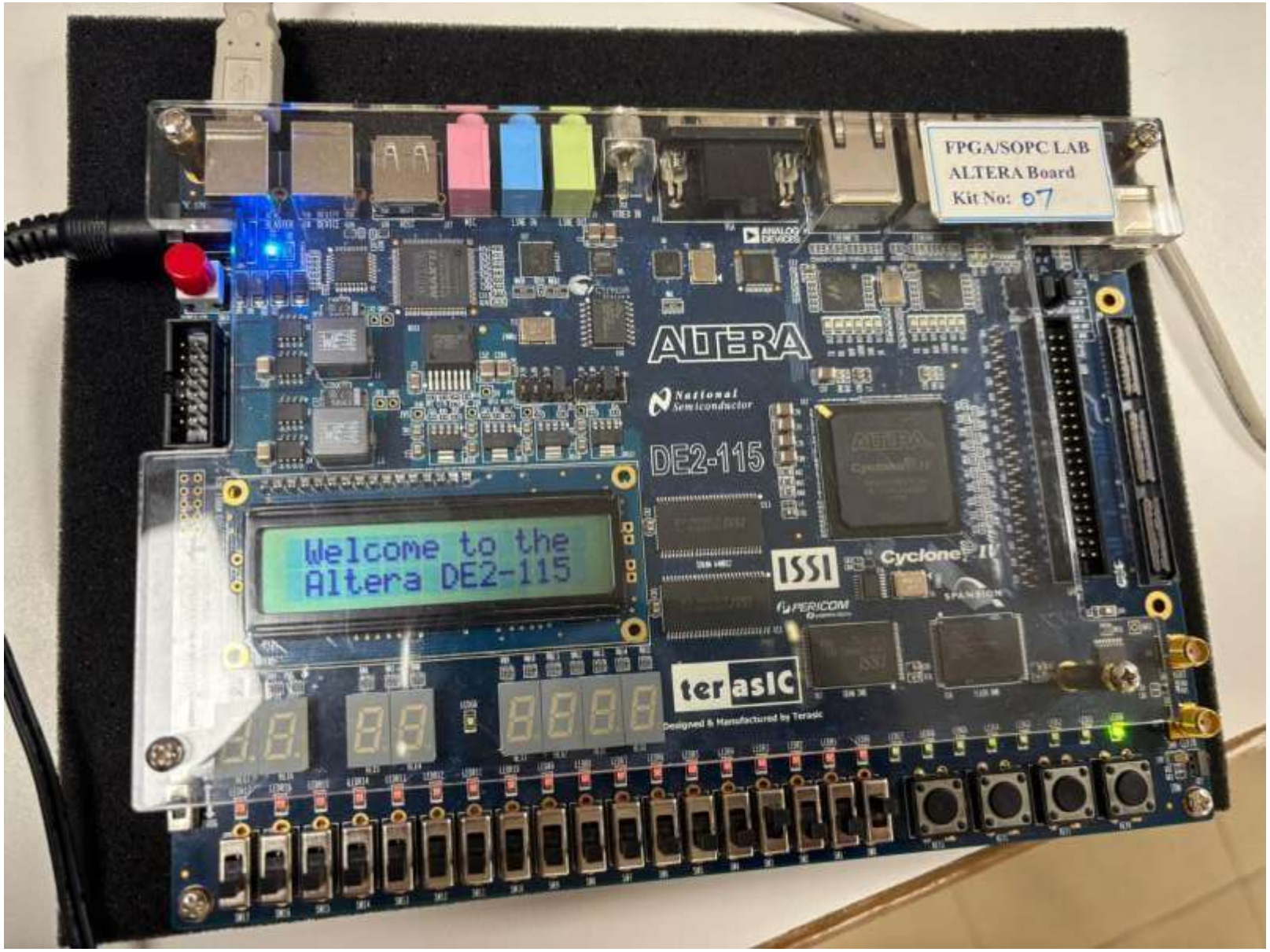
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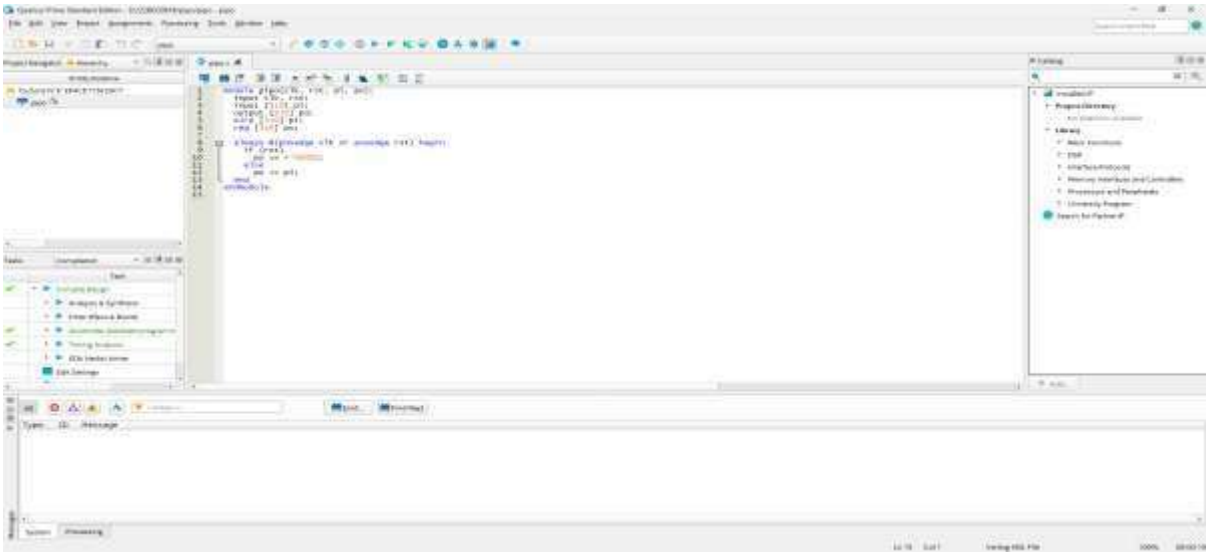
4) PIPO:



OUTPUT:

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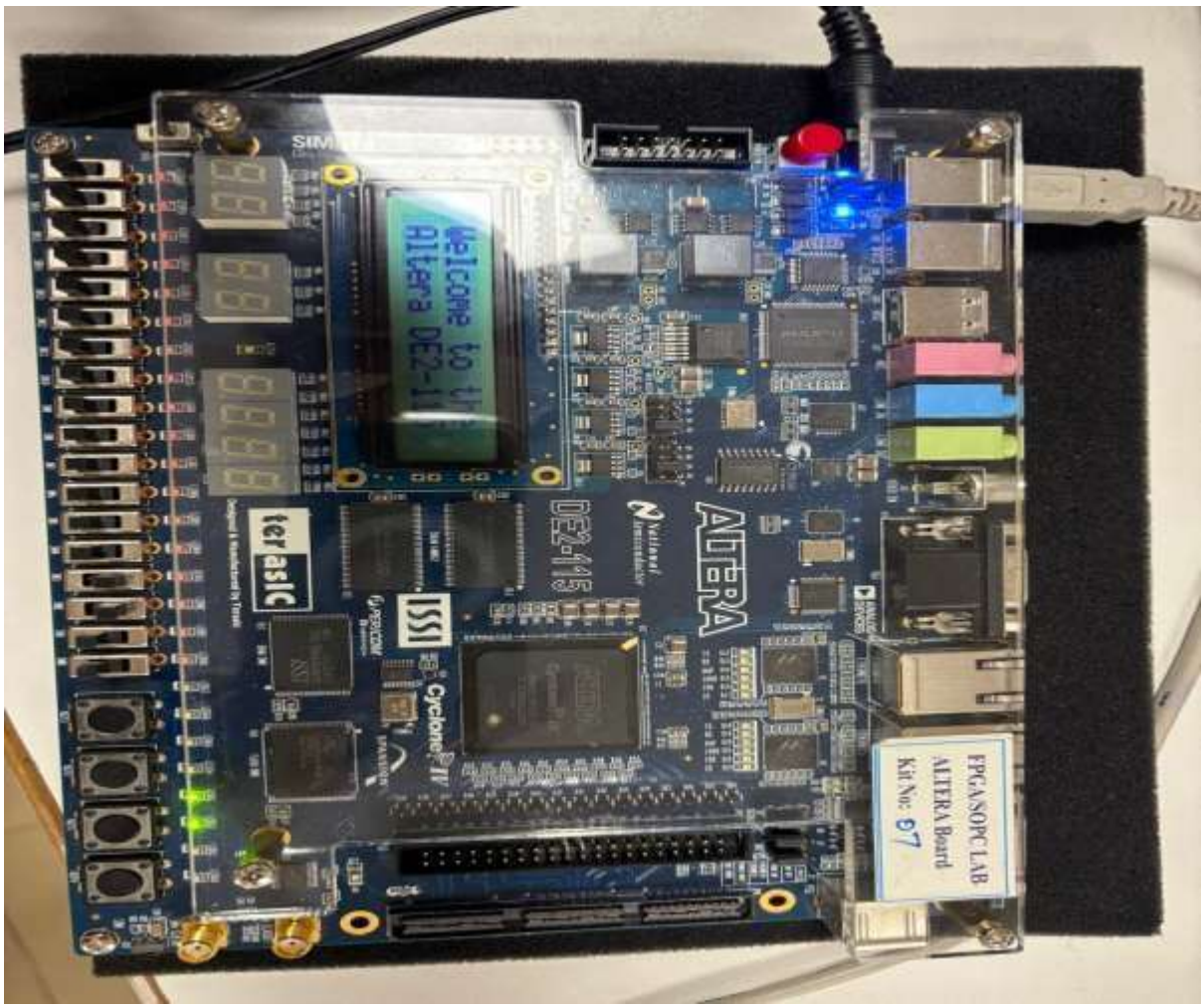

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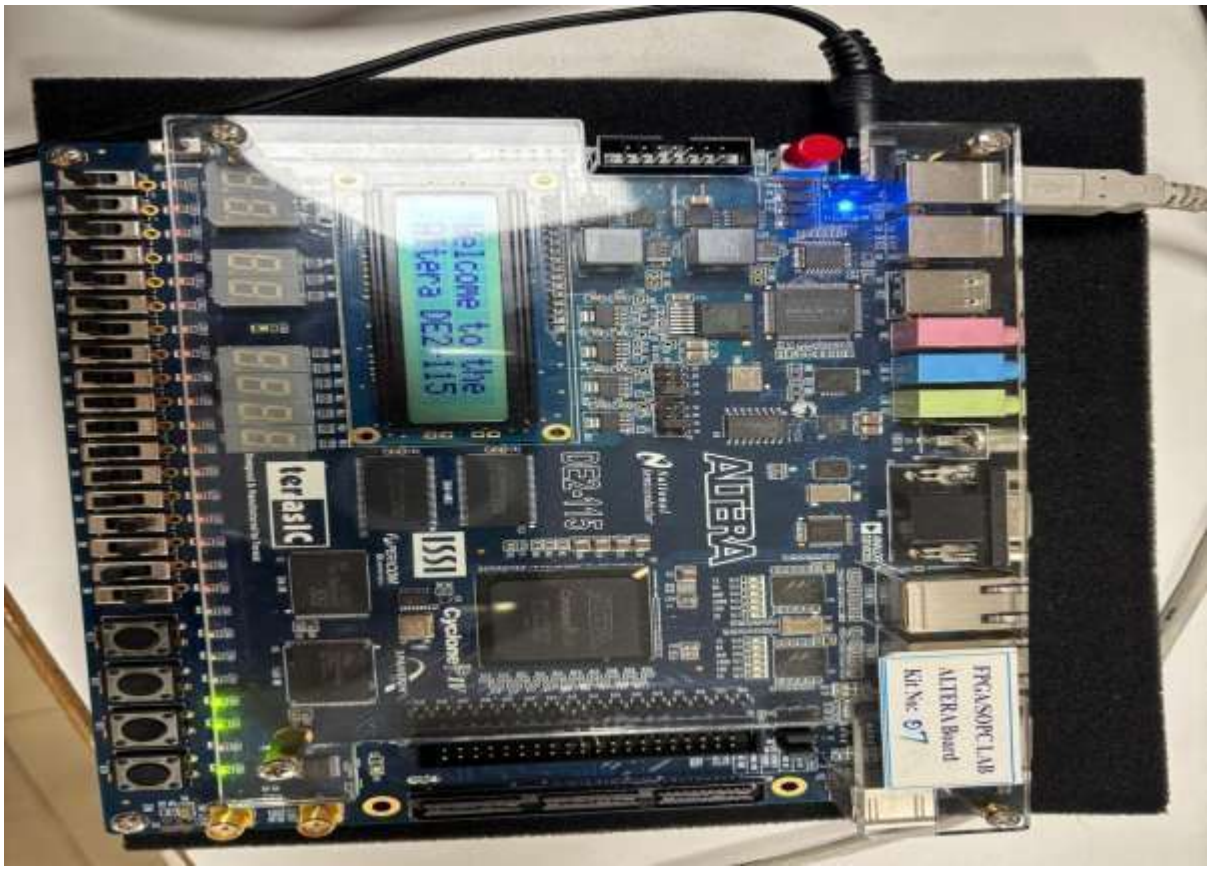

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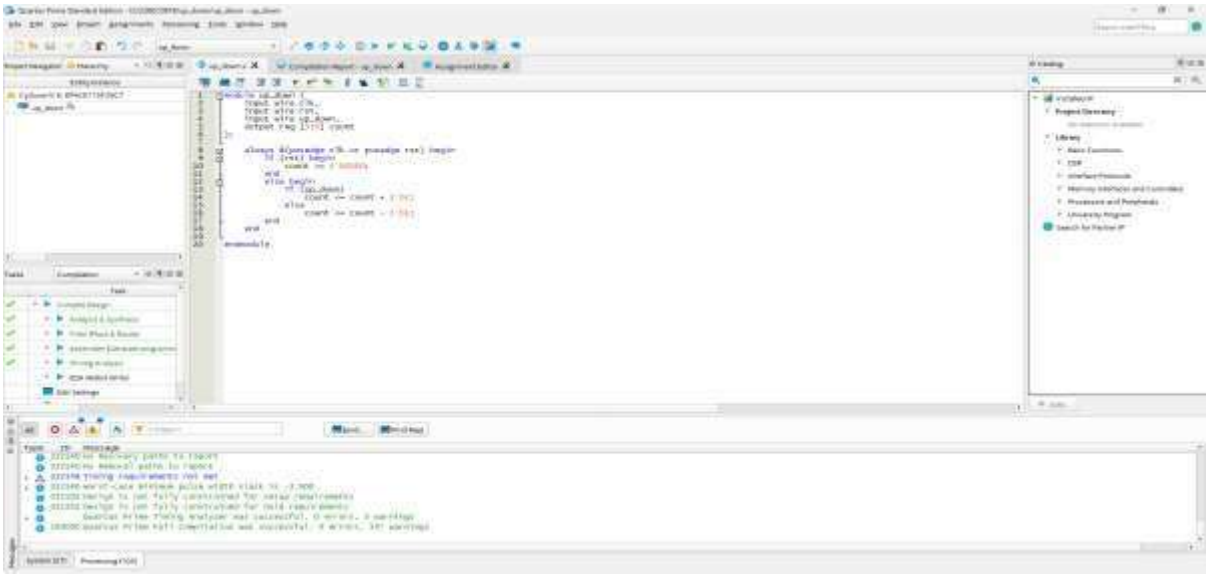
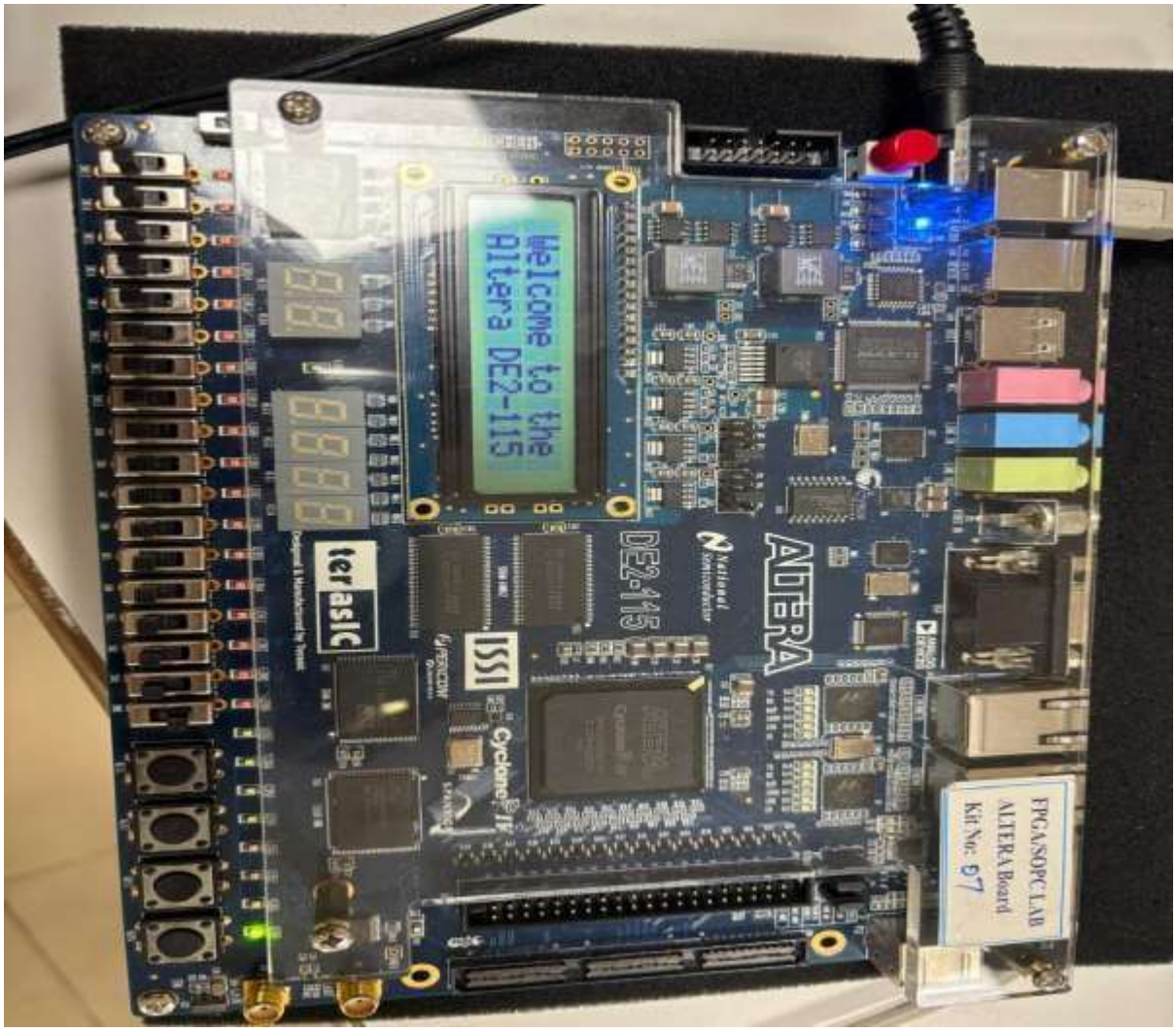
VERILOG CODE FOR UP/DOWN COUNTER:



OUTPUT FOR UP COUNTER:

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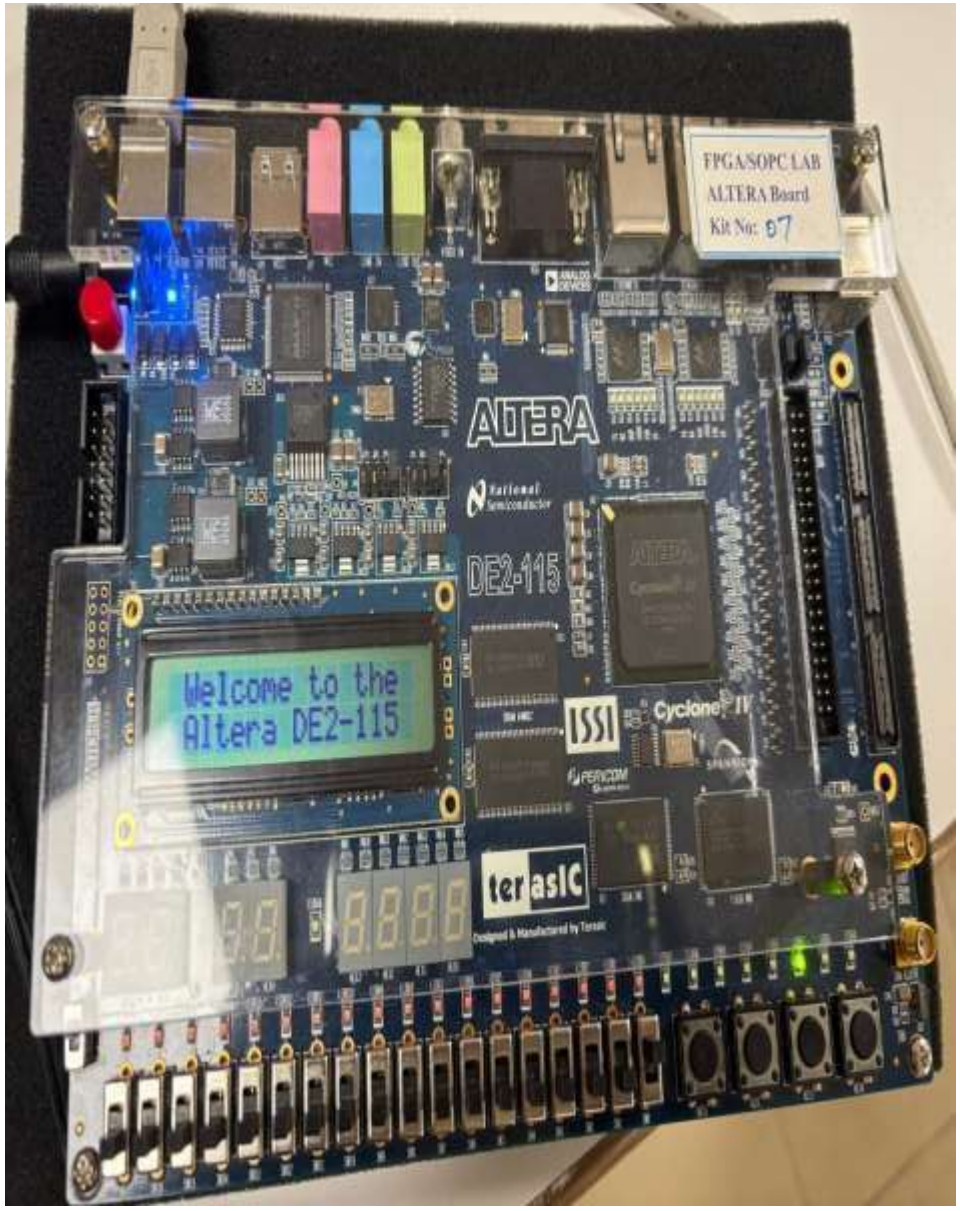
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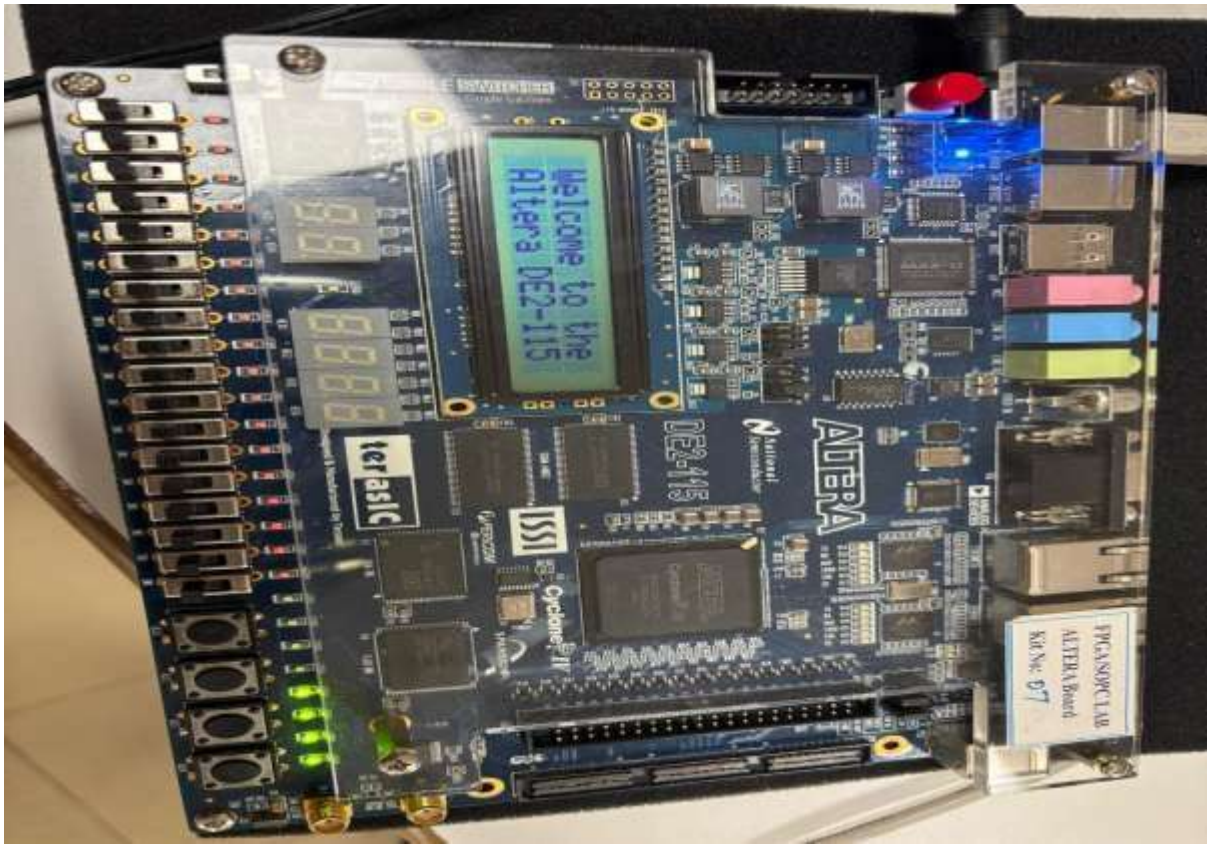
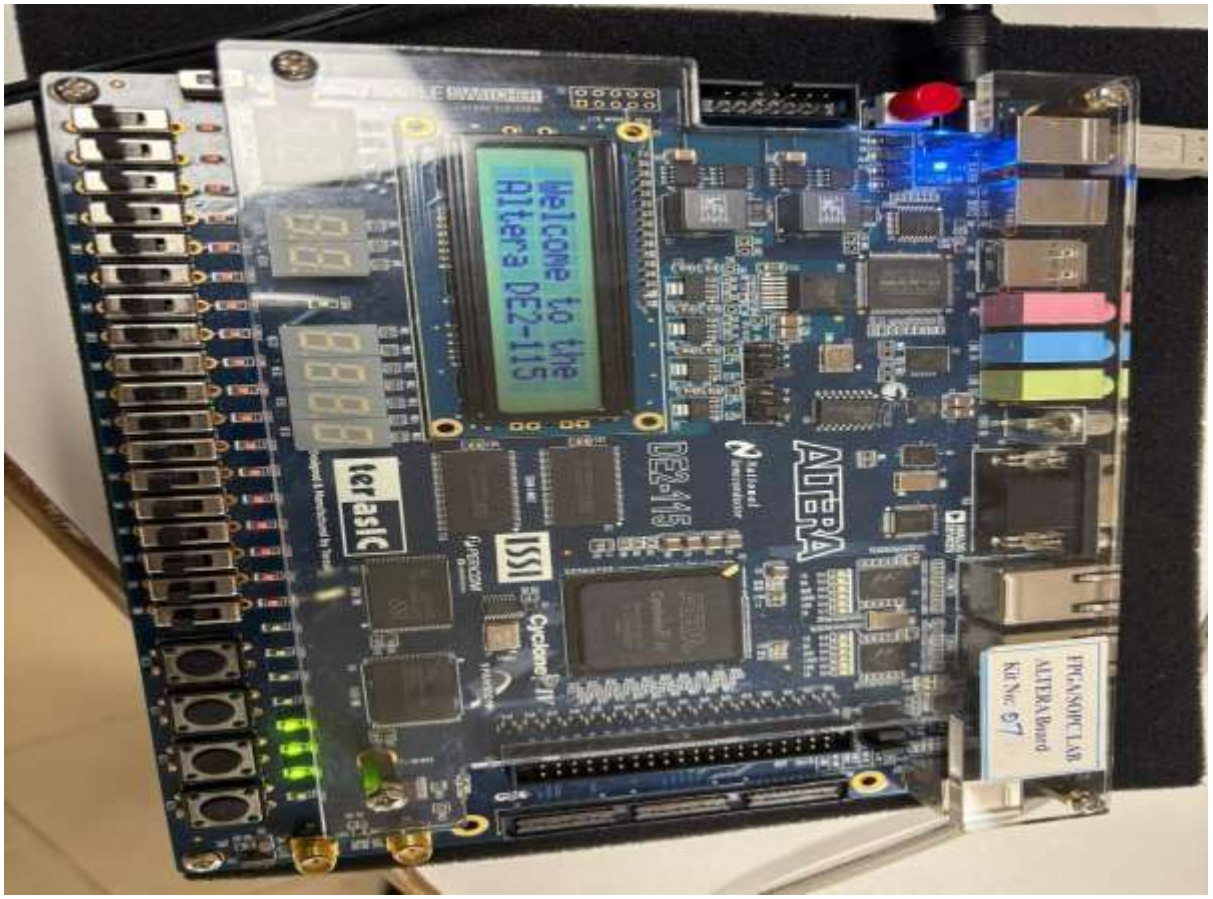
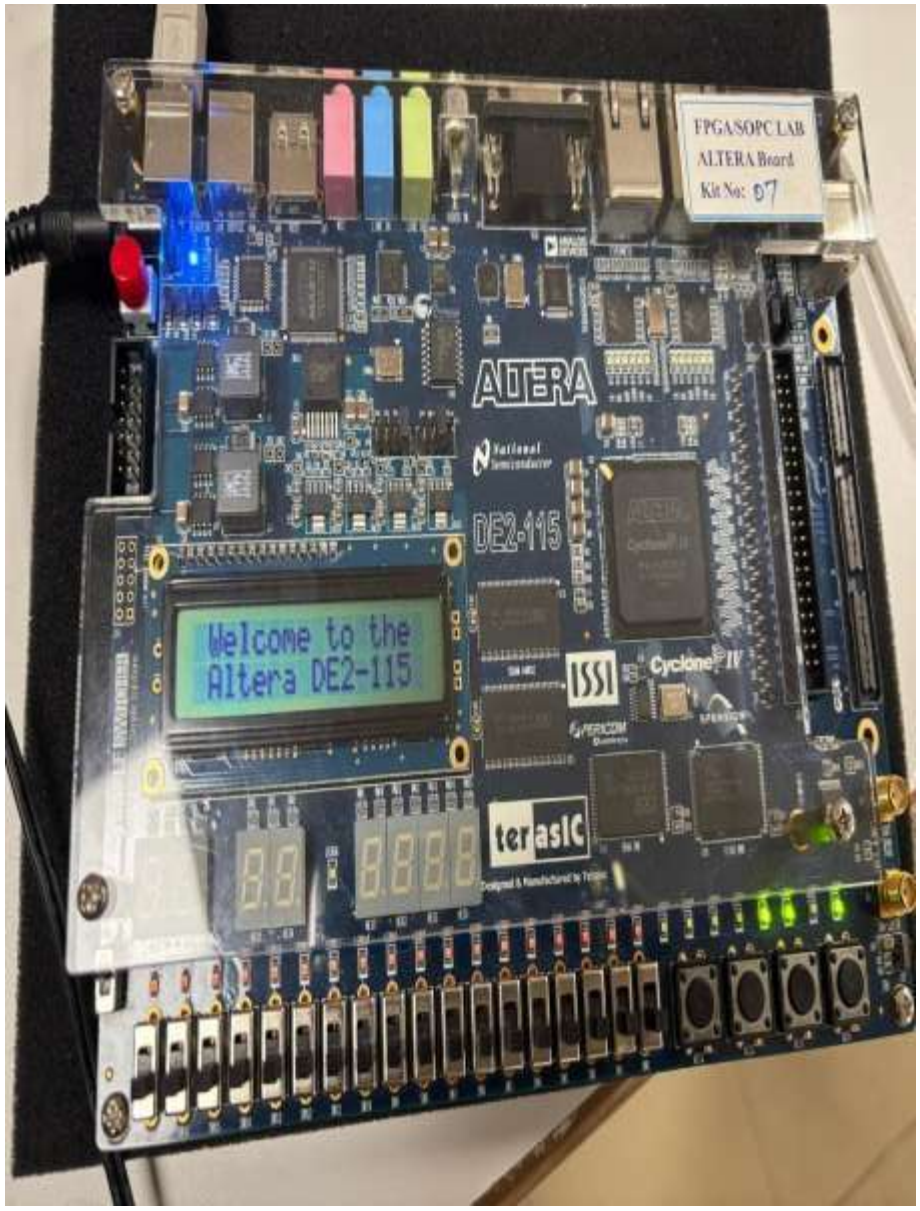
OUTPUT FOR DOWN COUNTER:



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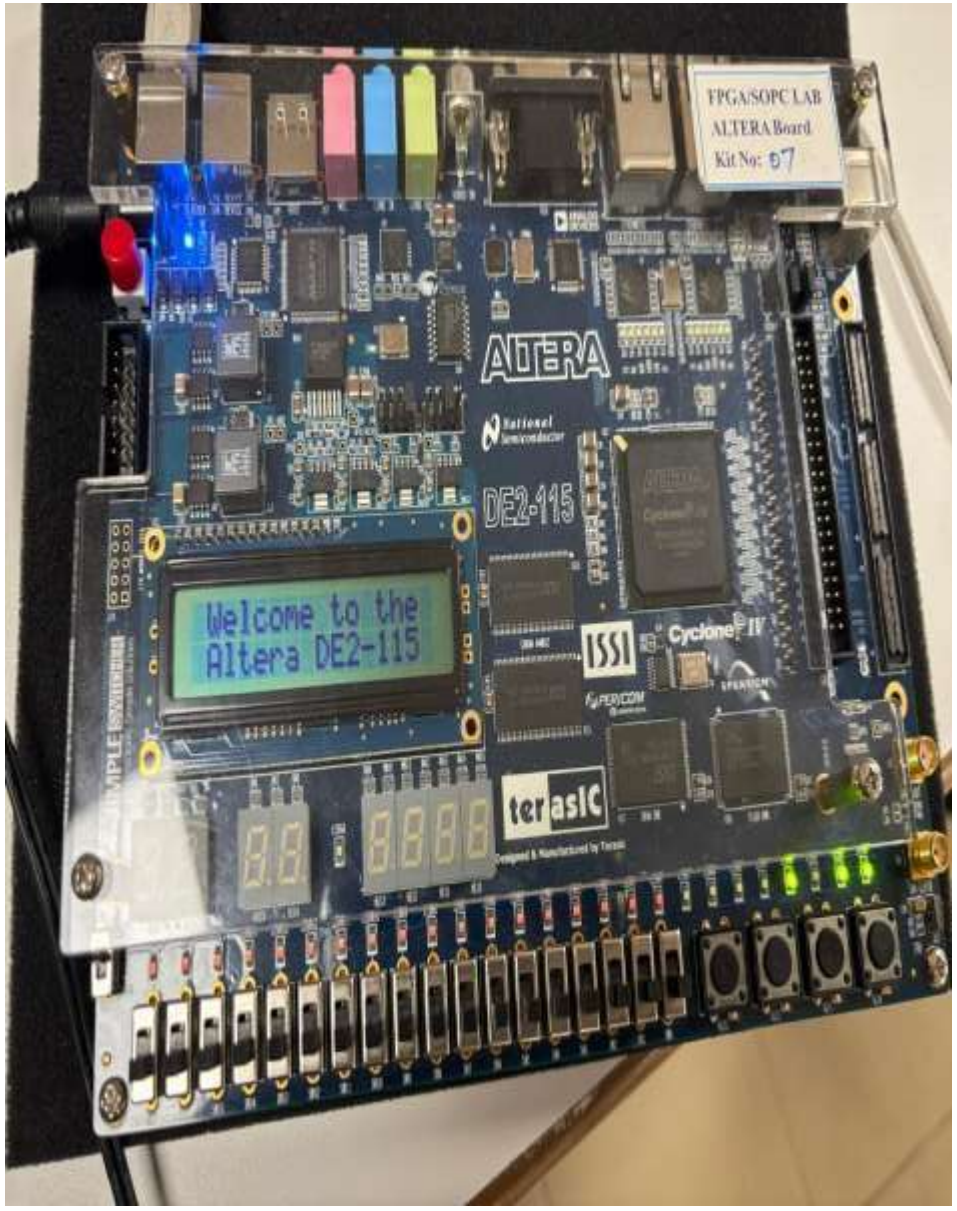
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INFERENCE:

From the simulation and hardware implementation, it is observed that both the shift register and the up/down counter function as expected on the FPGA. The shift register correctly stores and shifts data in the specified direction with each clock pulse, and its outputs match the simulated waveforms. The up/down counter increments or decrements accurately based on the control input, with proper wrap-around and reset behavior. The results confirm that the designed circuits meet the intended specifications and can be reliably implemented in digital systems for data storage, transfer, and counting applications.