AIM: To write the Verilog code for the following multiplier's and verify using FPGA

1) Shift multiplier
2) Booth multiplier
3) Array multiplier

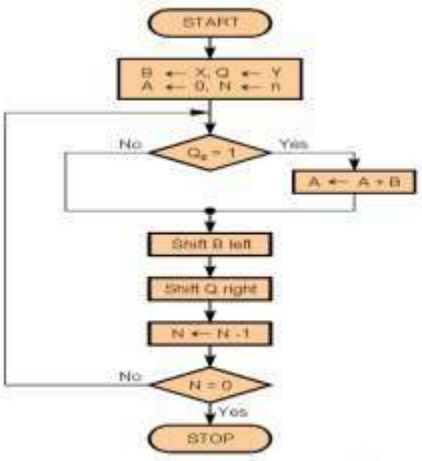
Software used: intel quartus prime

THEORY: Multiplication is a key operation in digital systems, used in areas like signal processing and embedded applications. Common hardware-based multipliers include the Shift Multiplier, Booth Multiplier, and Array Multiplier. The **Shift Multiplier** uses repeated addition and shifting, making it simple but slower. The **Booth Multiplier** improves speed by reducing the number of additions and efficiently handling signed numbers. The **Array Multiplier** performs fast, parallel computation using a grid of adders but uses more hardware. These multipliers are implemented in Verilog and tested using Intel Quartus Prime on FPGA.

CODE:

Shift multiplier:

Block diagram:



The first version of the multiplication algorithm.

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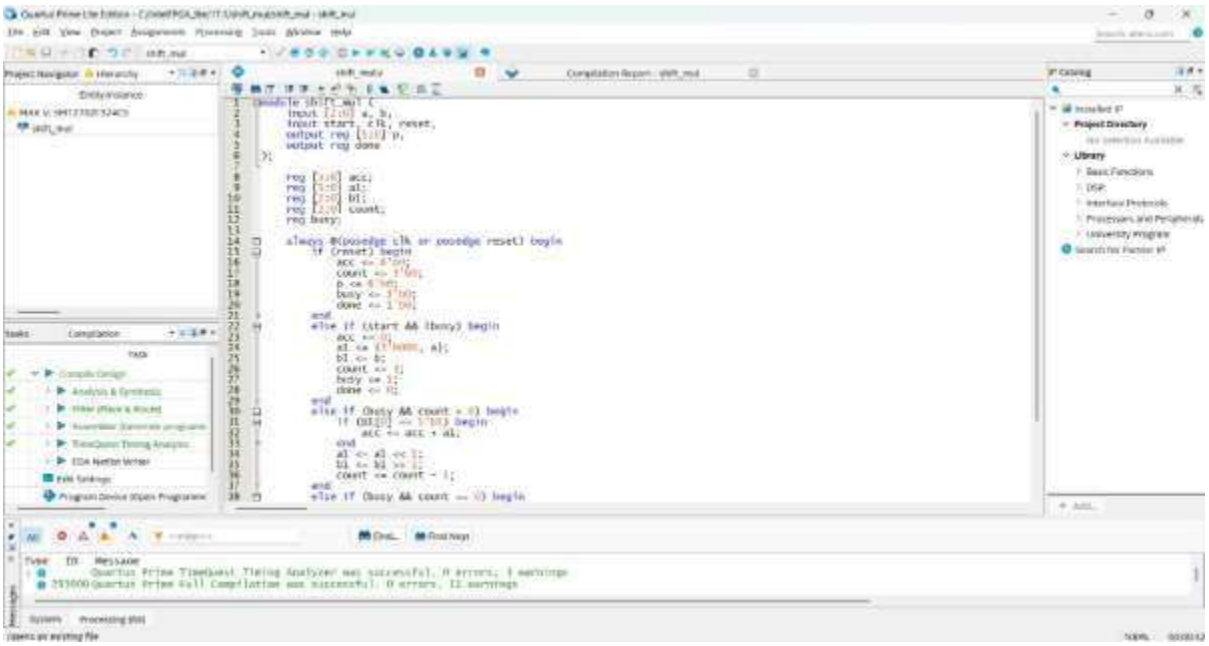
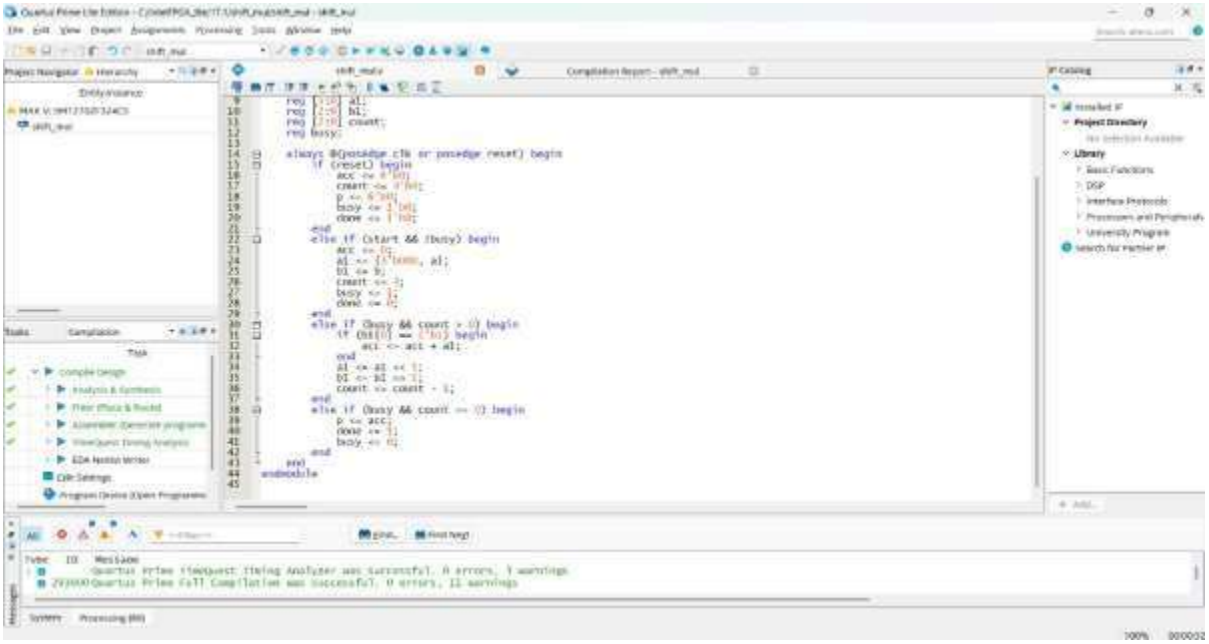


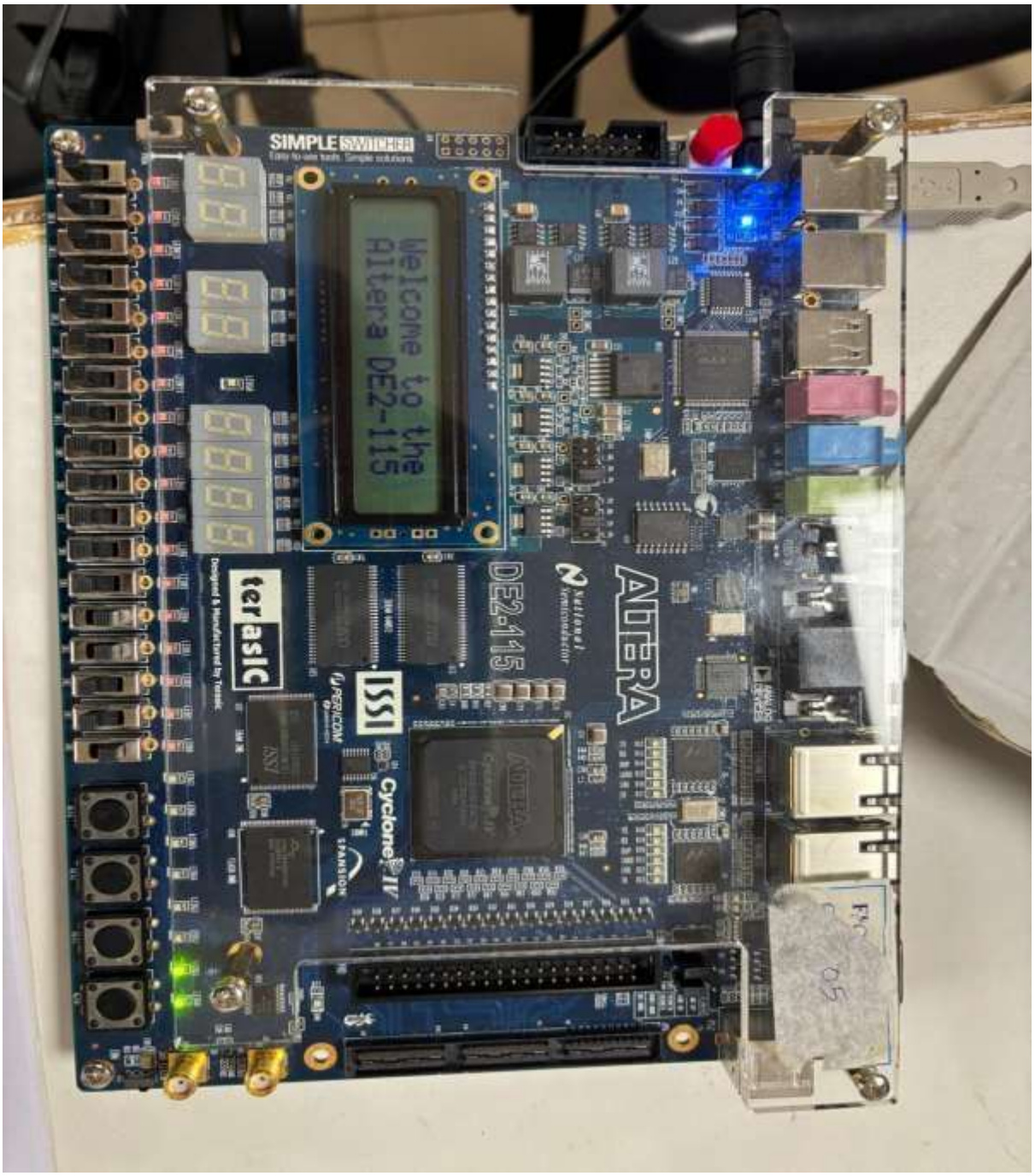


INPUT GIVE:

A=1,B=3

OUTPUT:

P=3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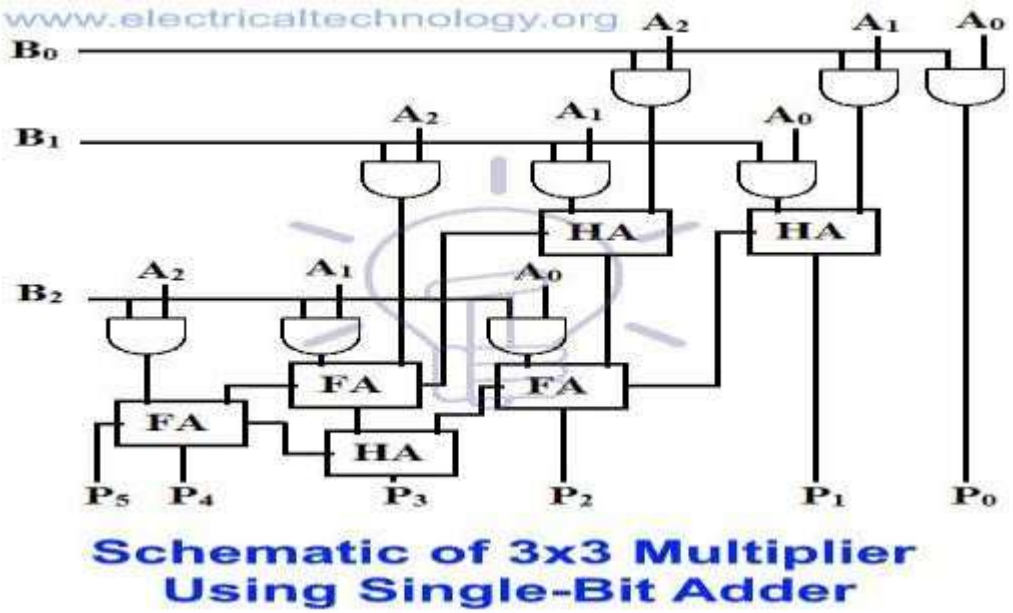
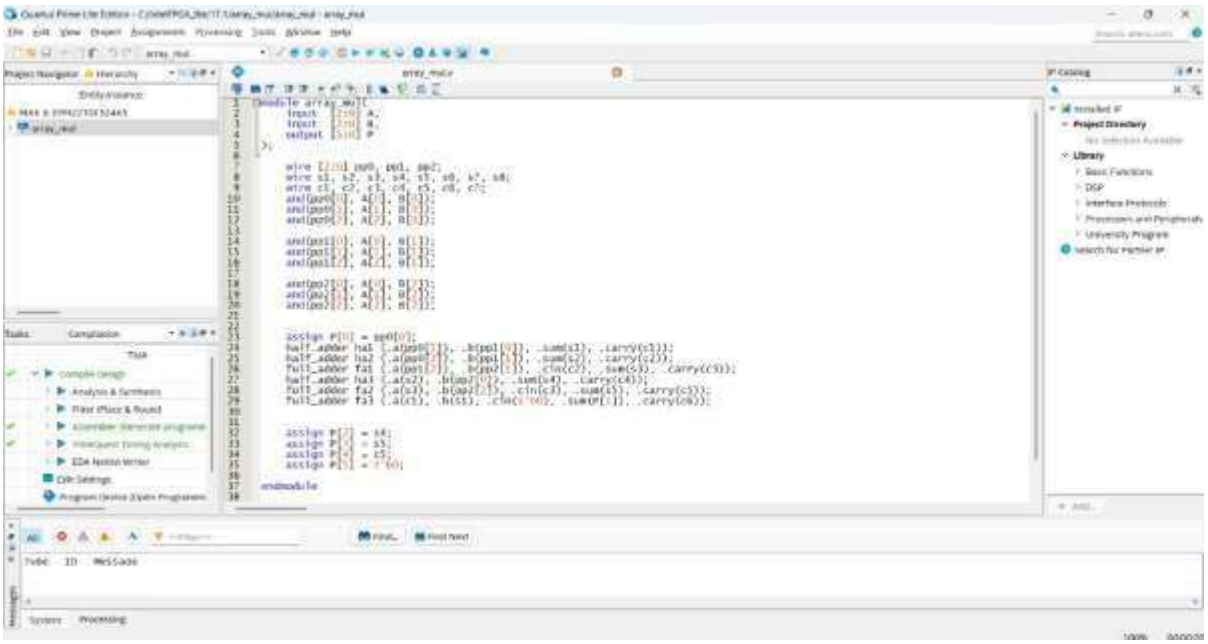
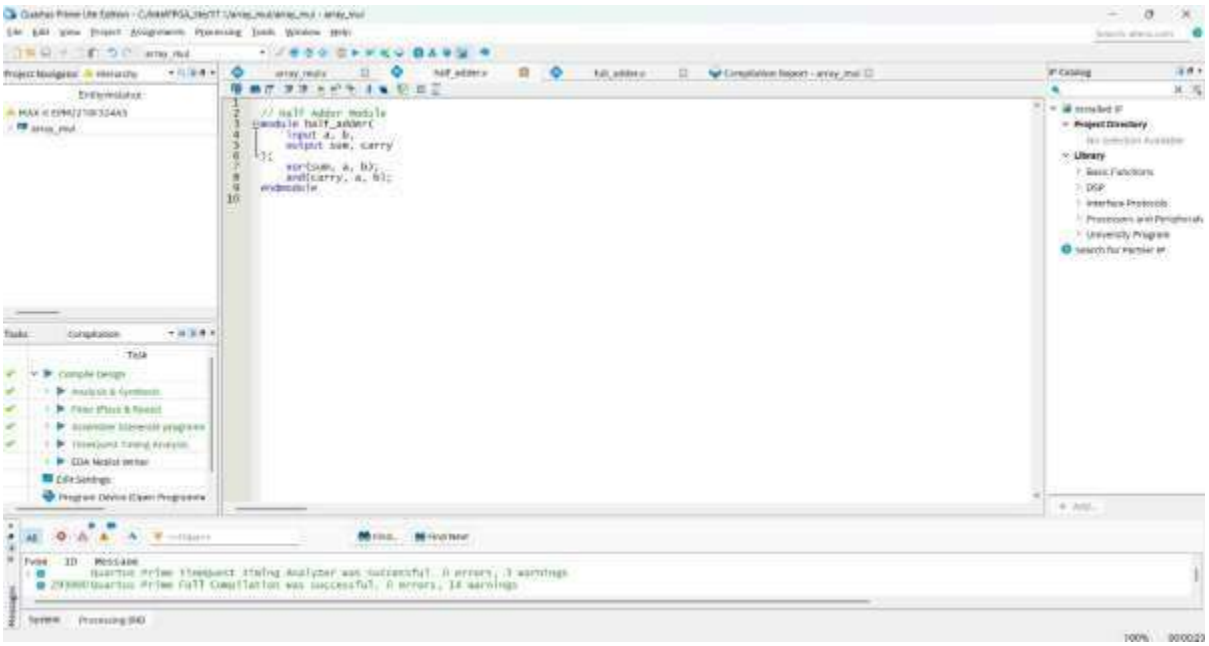
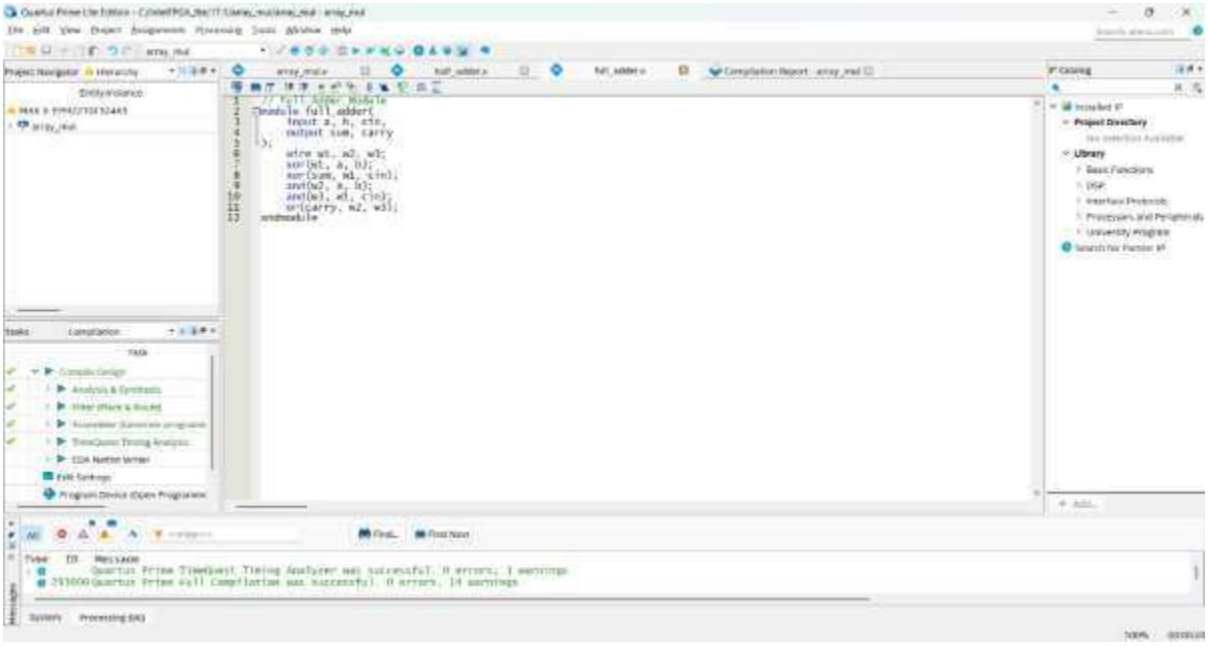
Cyclone IV

Array multiplier:







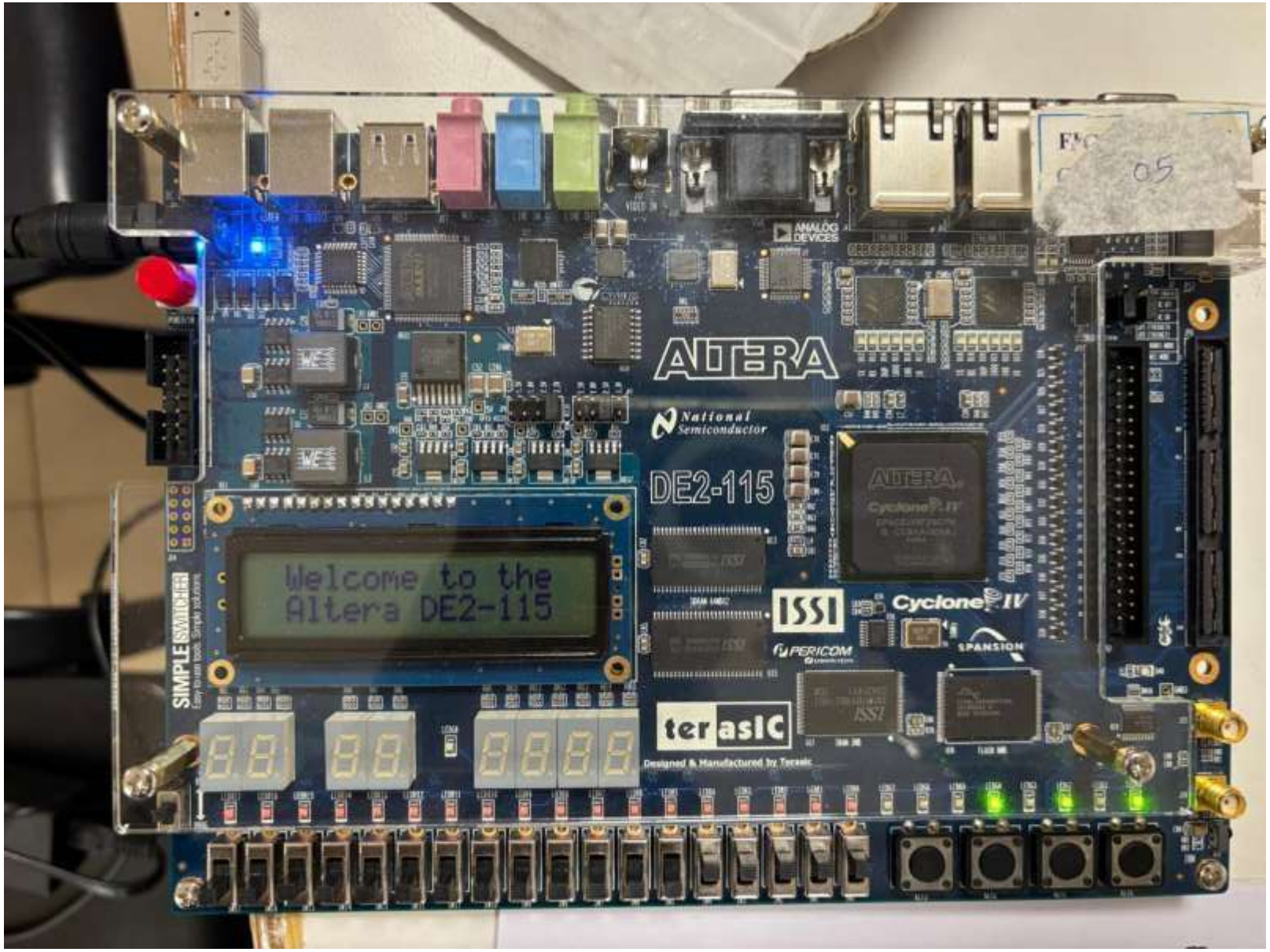


INPUT:

A=7,B=3

OUTPUT:

P=21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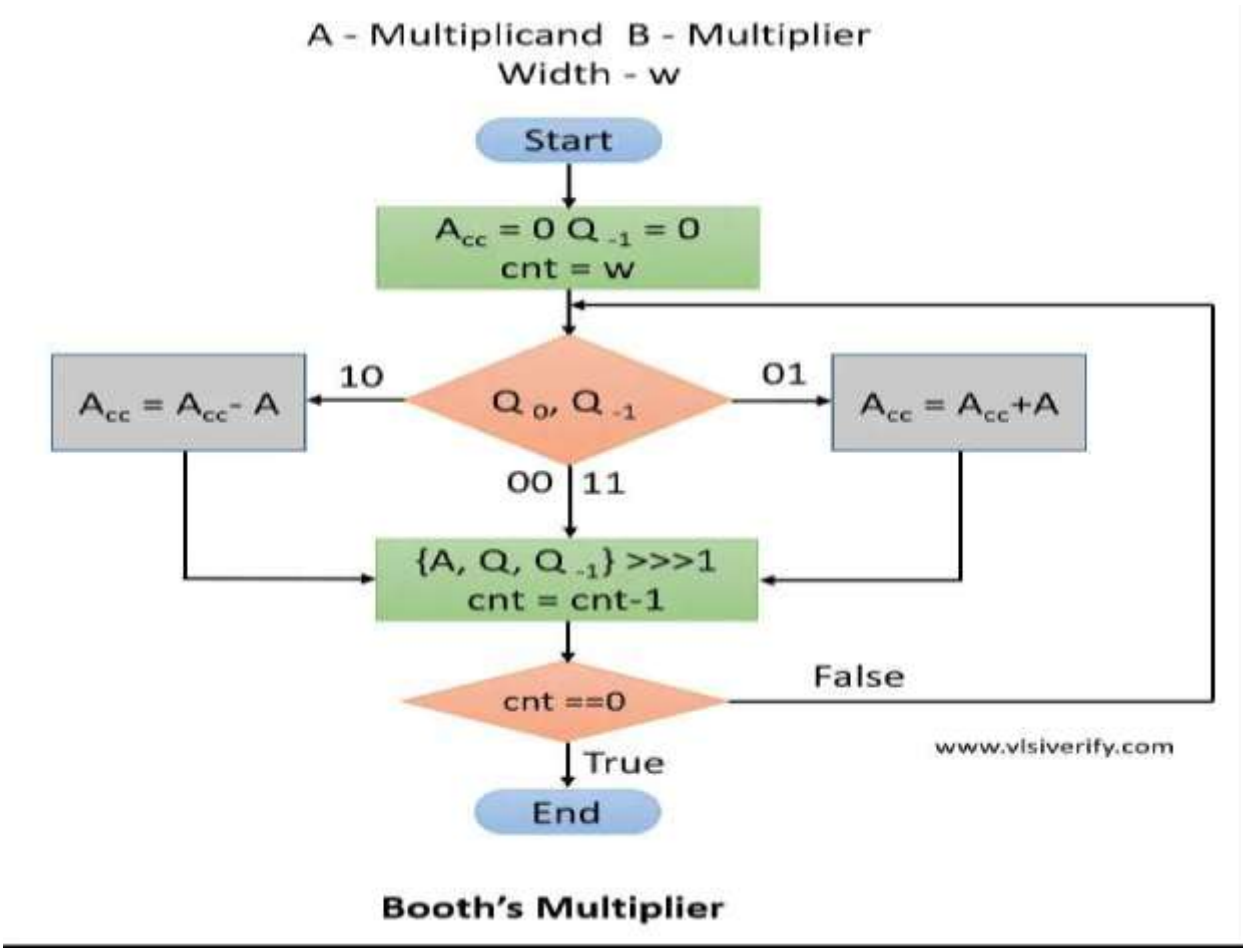
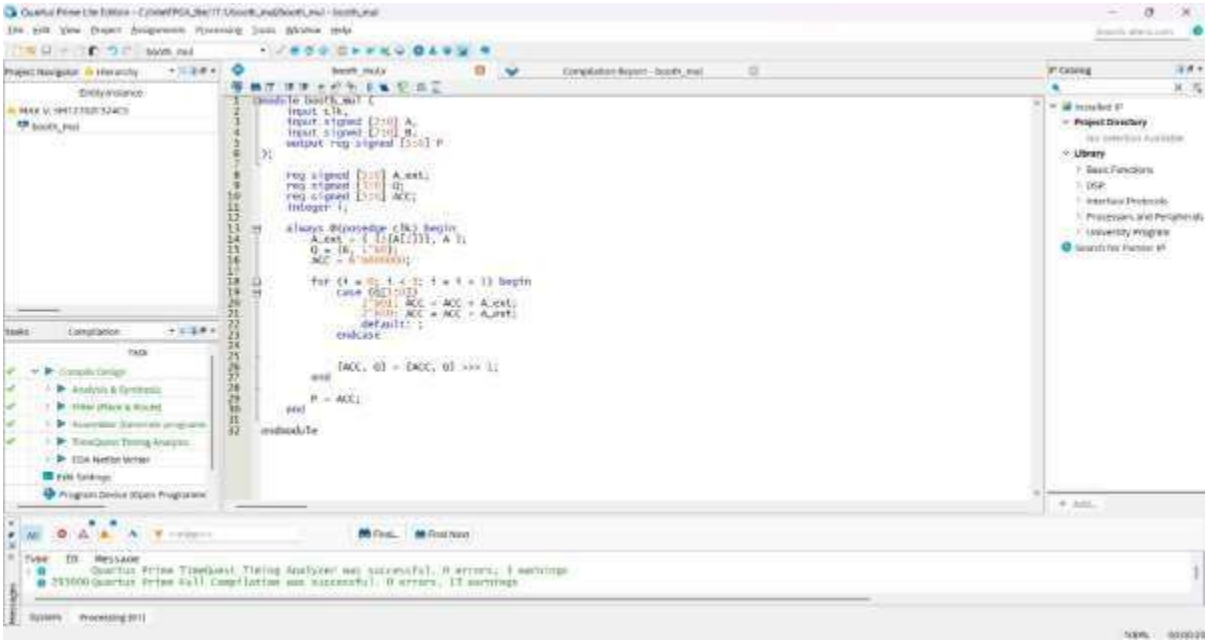
Designed & Manufactured by Terasic
Cyclone IV
ISSI
PERICOM
SPANSION
ANALOG DEVICES
National Semiconductor

Booth multiplier:



Booth's Multiplier

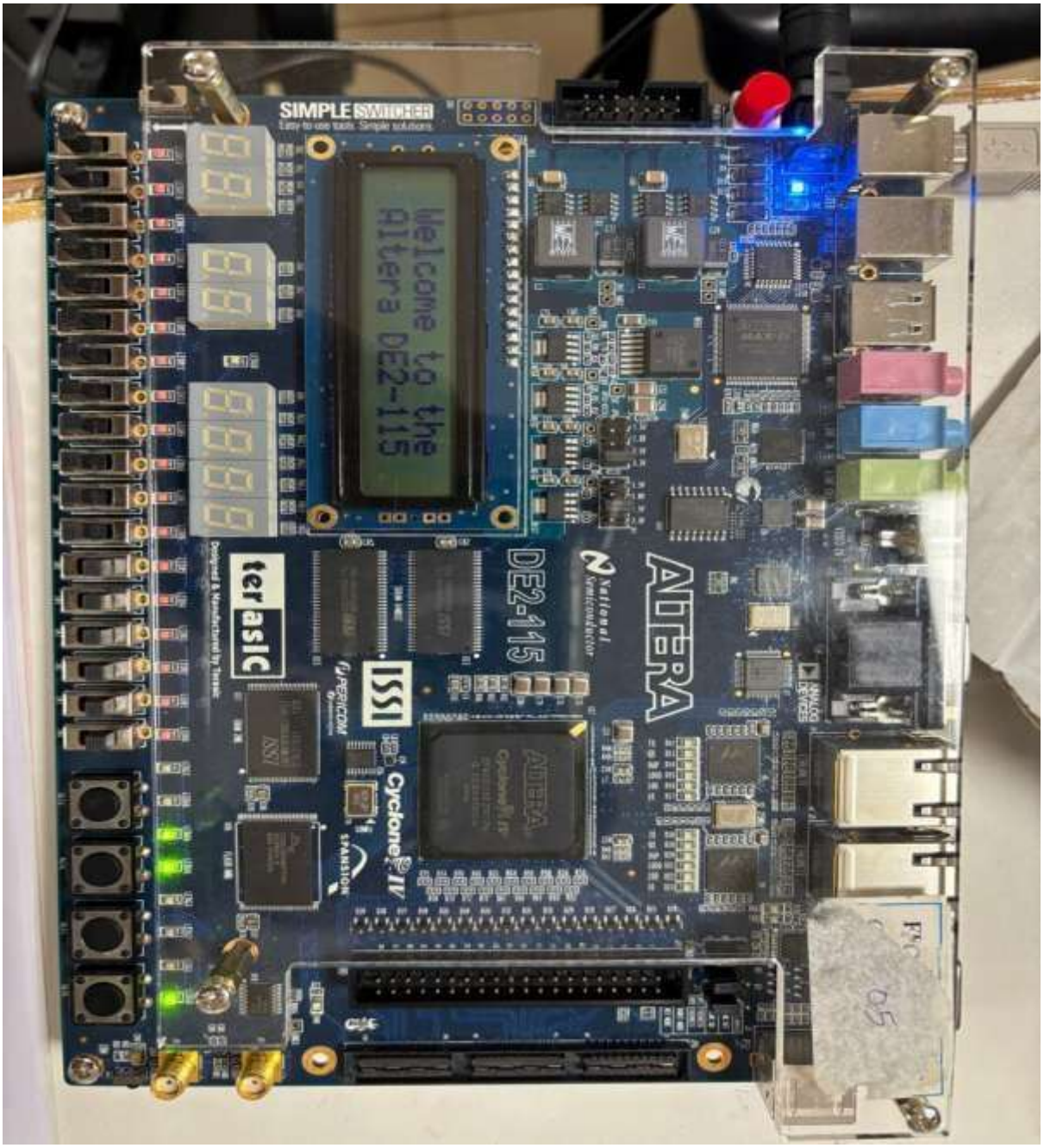


Input:

A=7,B=7

Output:

P=49



RESULT:

The Verilog code for Shift Multiplier, Booth Multiplier, and Array Multiplier was successfully written, compiled, and simulated using Intel Quartus Prime software. All three multipliers were verified on FPGA, and their outputs were found to be correct, confirming the proper functionality of each design.