AIM: To implement the following on FPGA

1) Single port rom
2) Dual port rom
3) Single port ram
4) 11 sequence detector

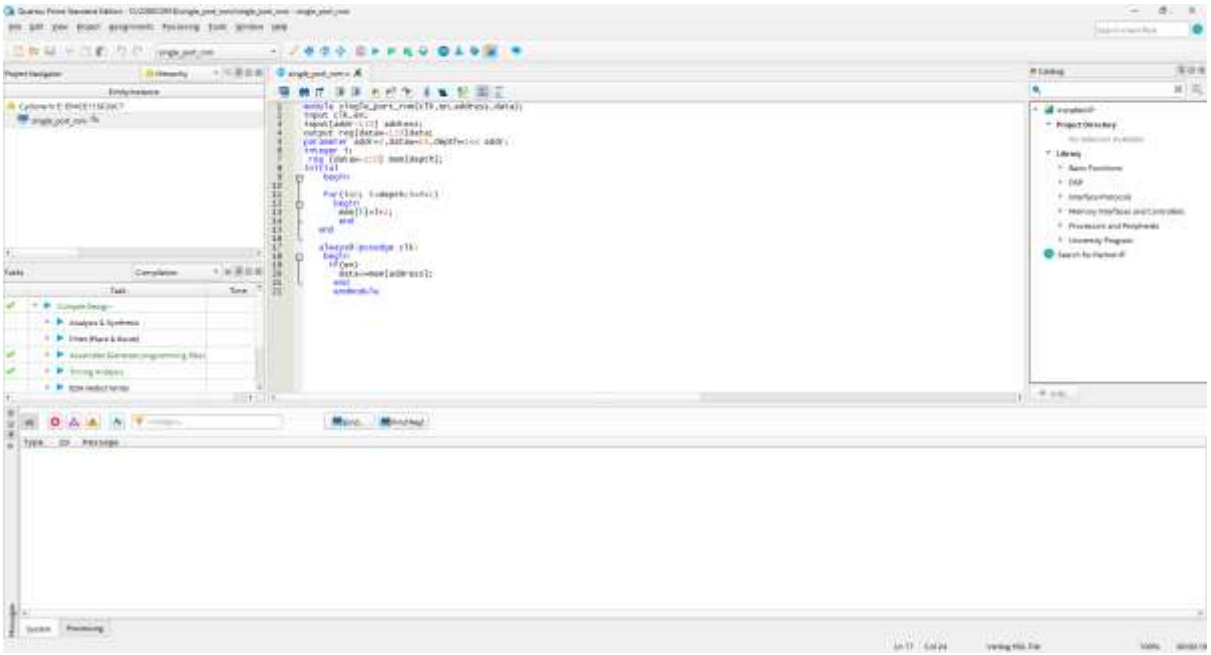
SOFTWARE USED: intel quartus prime

THEORY :

In digital system design, memories and sequence detectors are key components that can be implemented on FPGAs using Intel Quartus Prime. A **Single Port ROM** stores fixed data and allows reading through one address port, while a **Dual Port ROM** supports two ports for parallel access. A **Single Port RAM** enables both read and write operations through a single port for temporary data storage. On the other hand, a **Sequence Detector** is a finite state machine that identifies a specific bit pattern, such as an **11-sequence detector**, which outputs high whenever "11" occurs in the input stream. Implementing these on FPGA helps understand memory design, FSMs, and practical hardware realization using Quartus Prime.

VERILOG CODES:

1) SINGLE PORT ROM

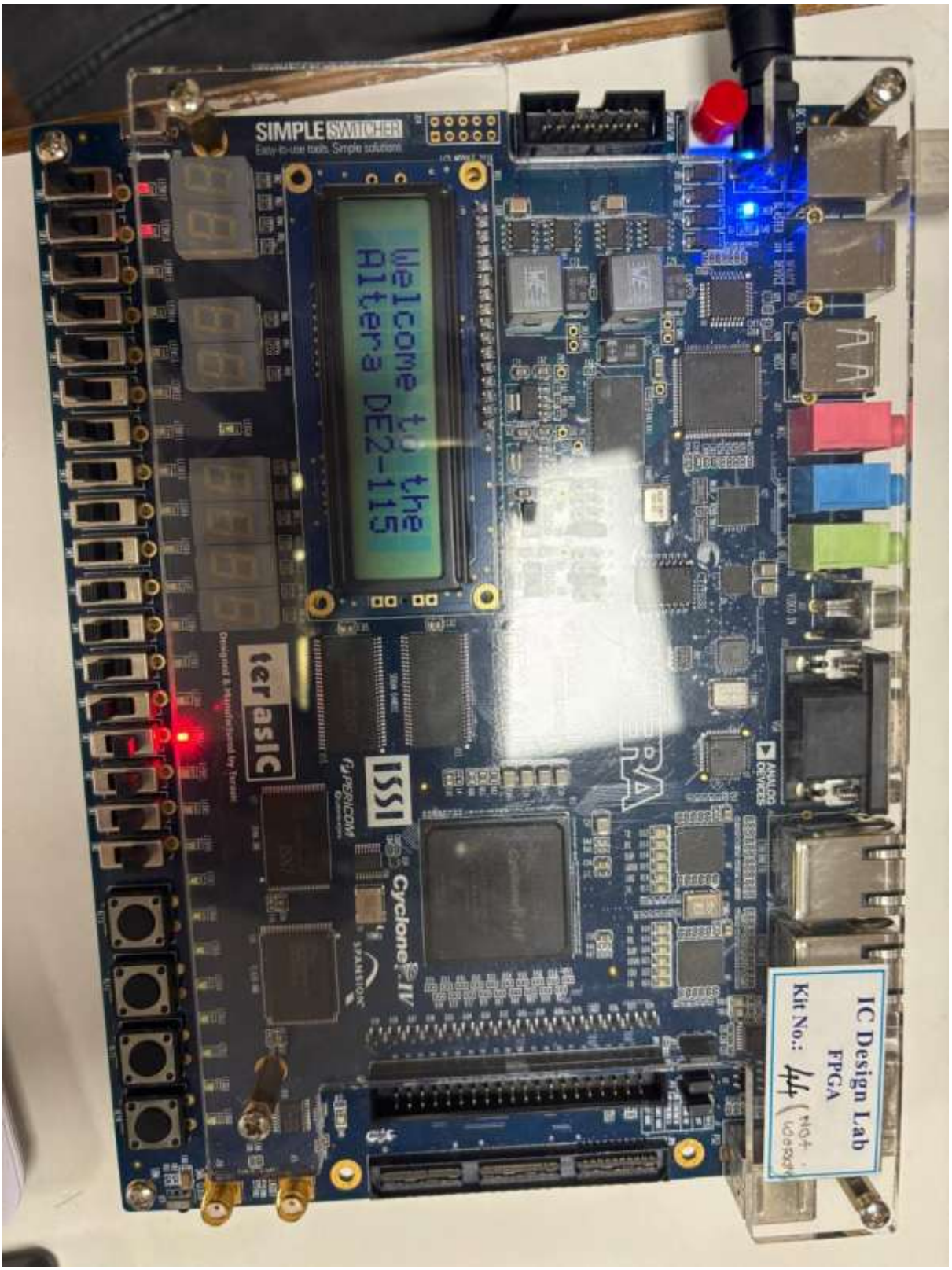


OUTPUT:

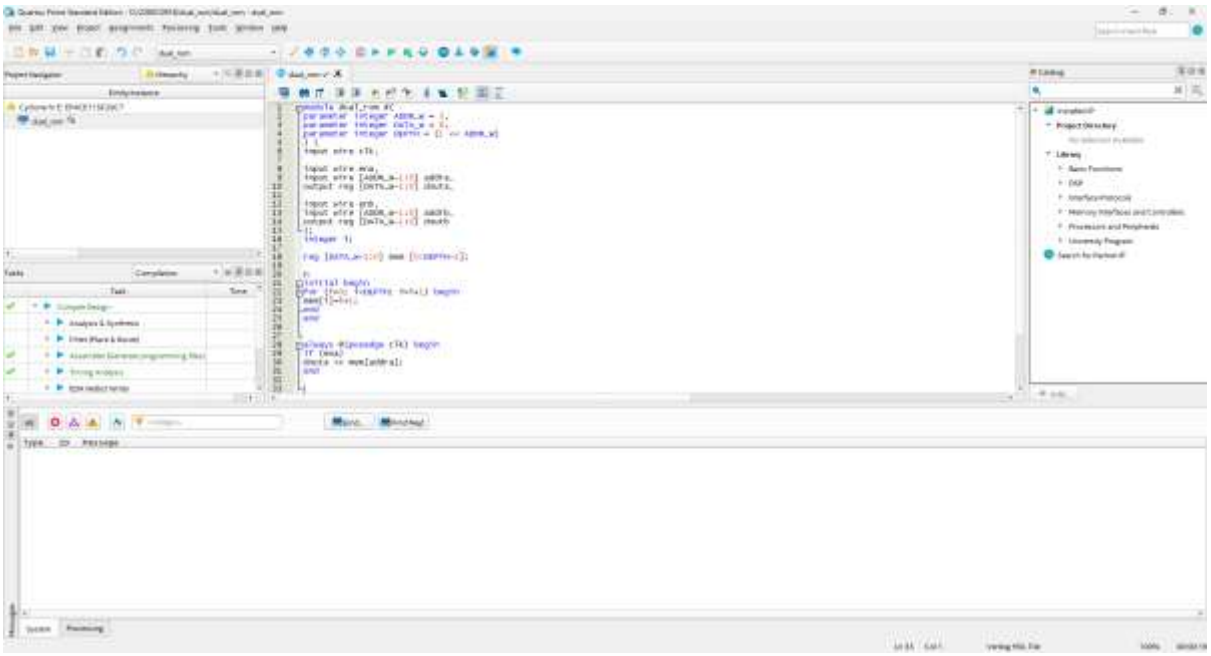
Input given:101 , Output :110

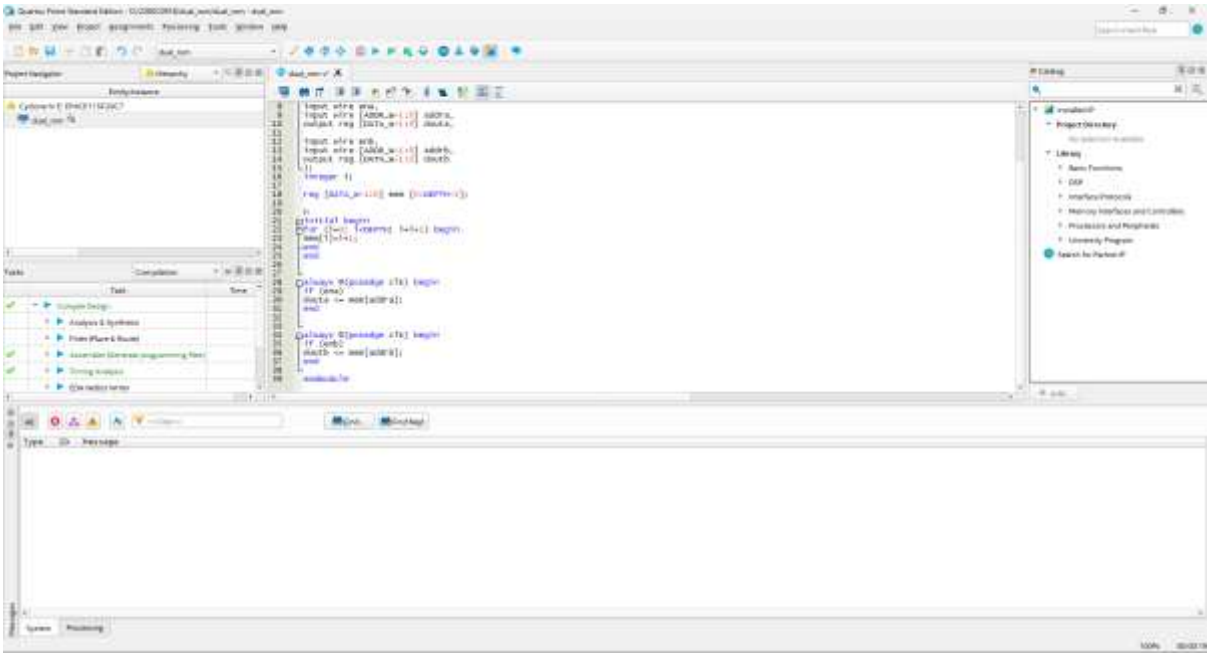
Input give : 100, output: 101

Input given : 111 output:1000



2) DUAL PORT ROM :

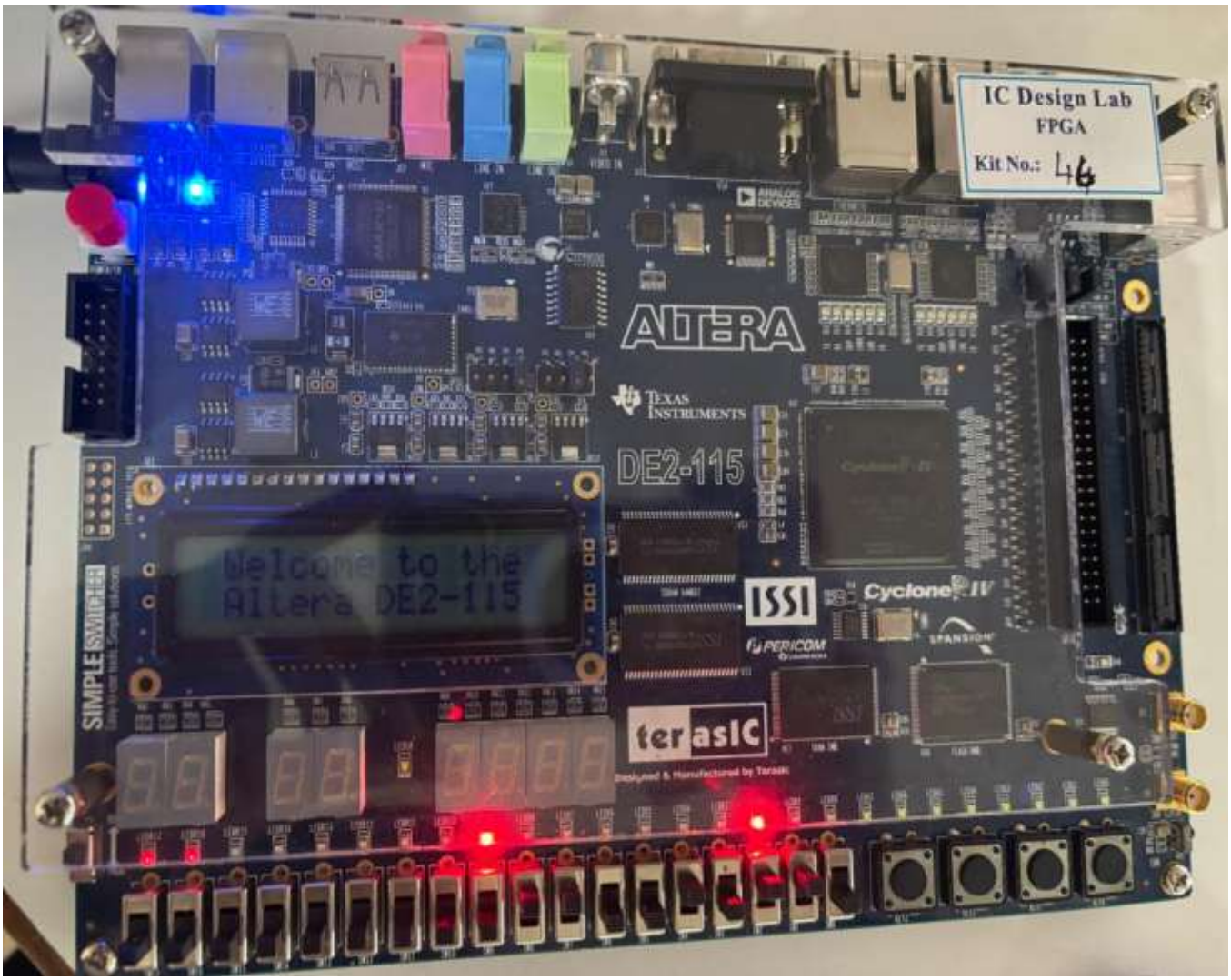




OUTPUT:

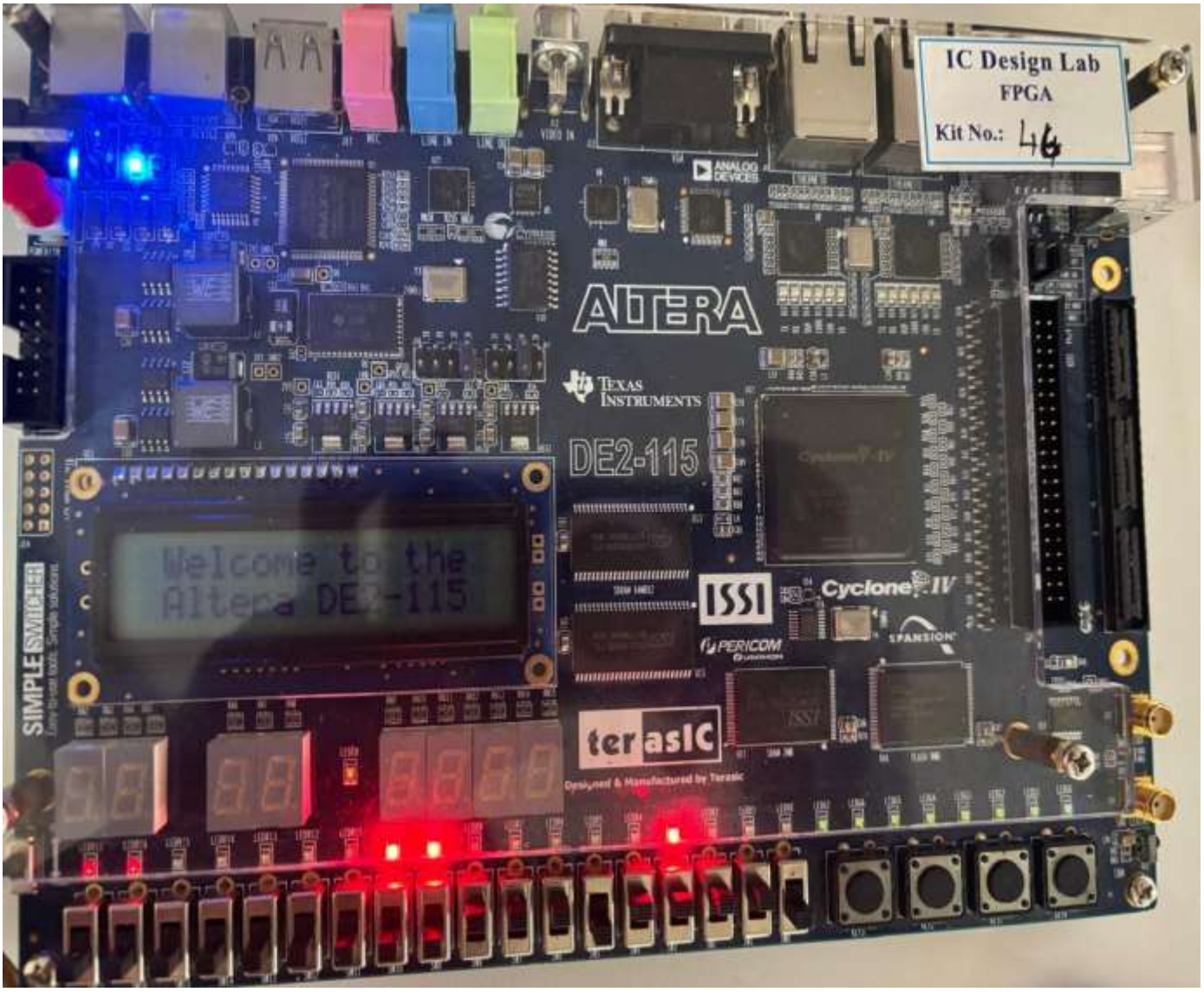
Input address a: 011 , Input address b: 001

Output for a: 100, Ouput for b: 010



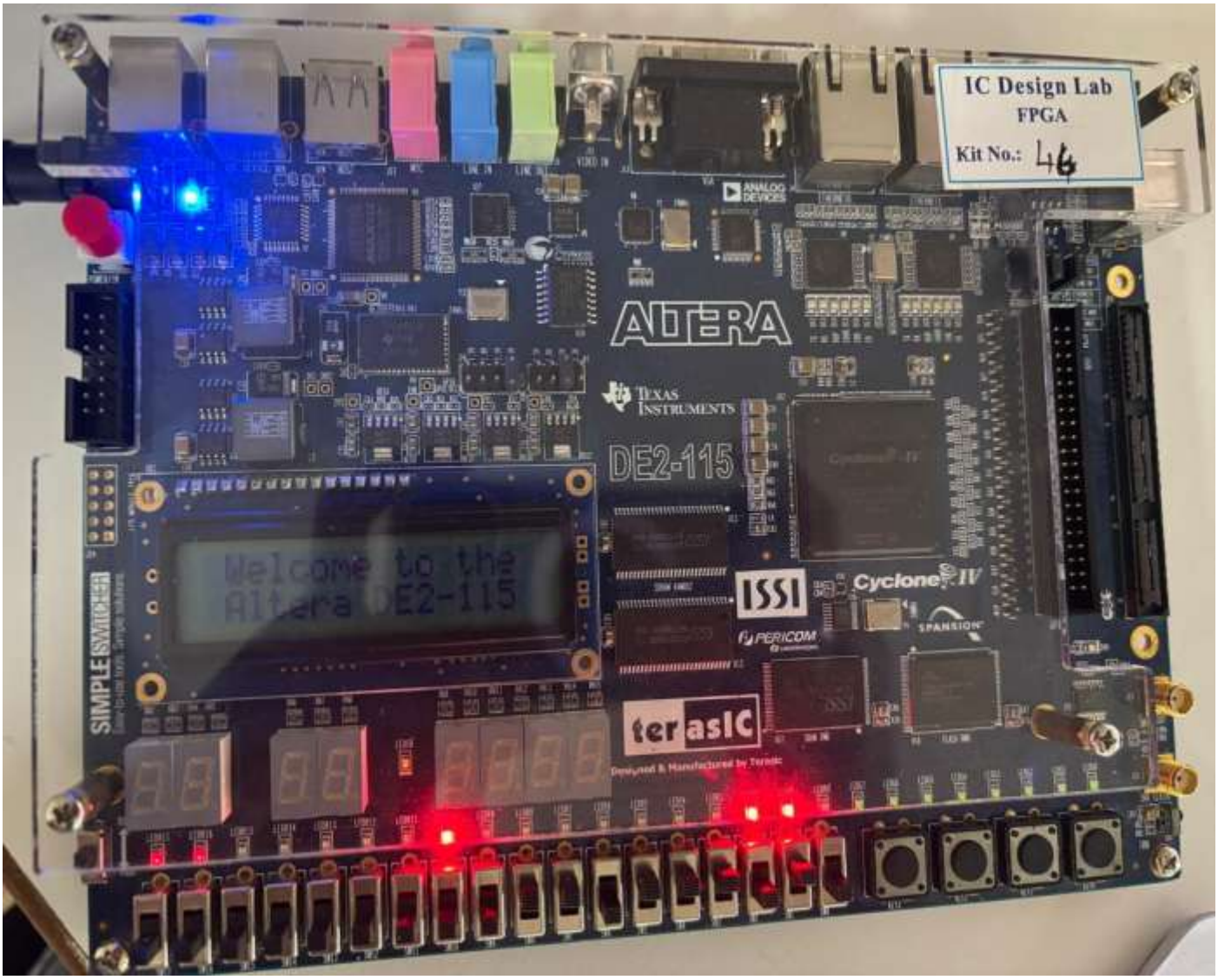
Input address a: 111, Input address b: 101

Output for a: 1000, Ouput for b: 110

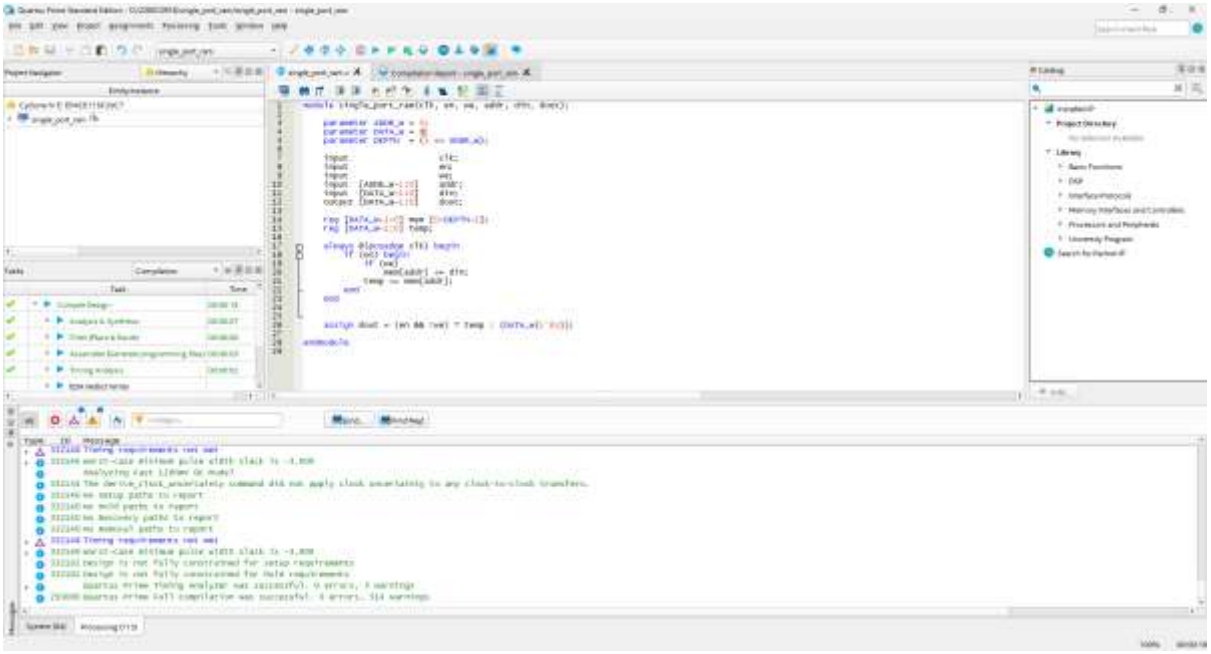


Input address a: 101, Input address b: 011

Output for a: 110, Ouput for b: 100



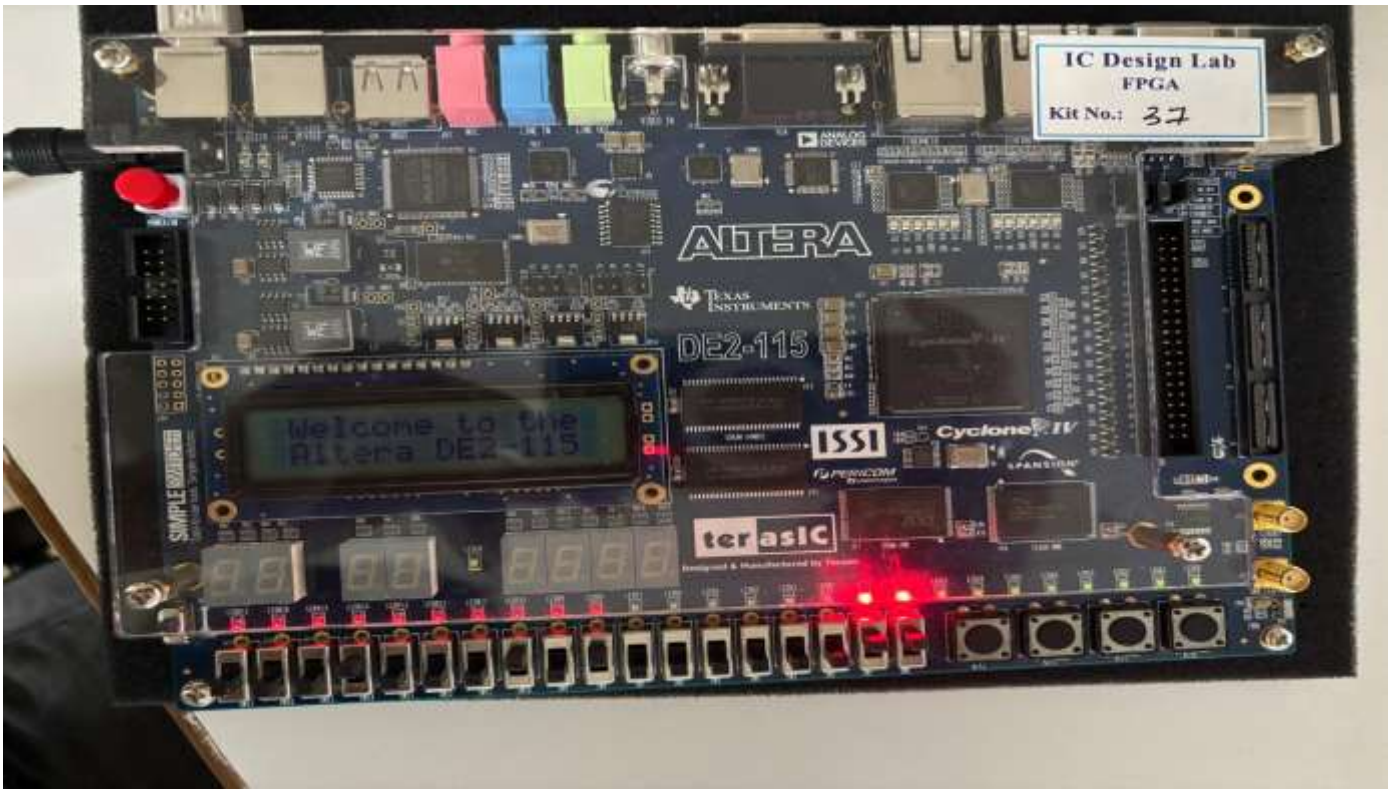
3) Single port ram:



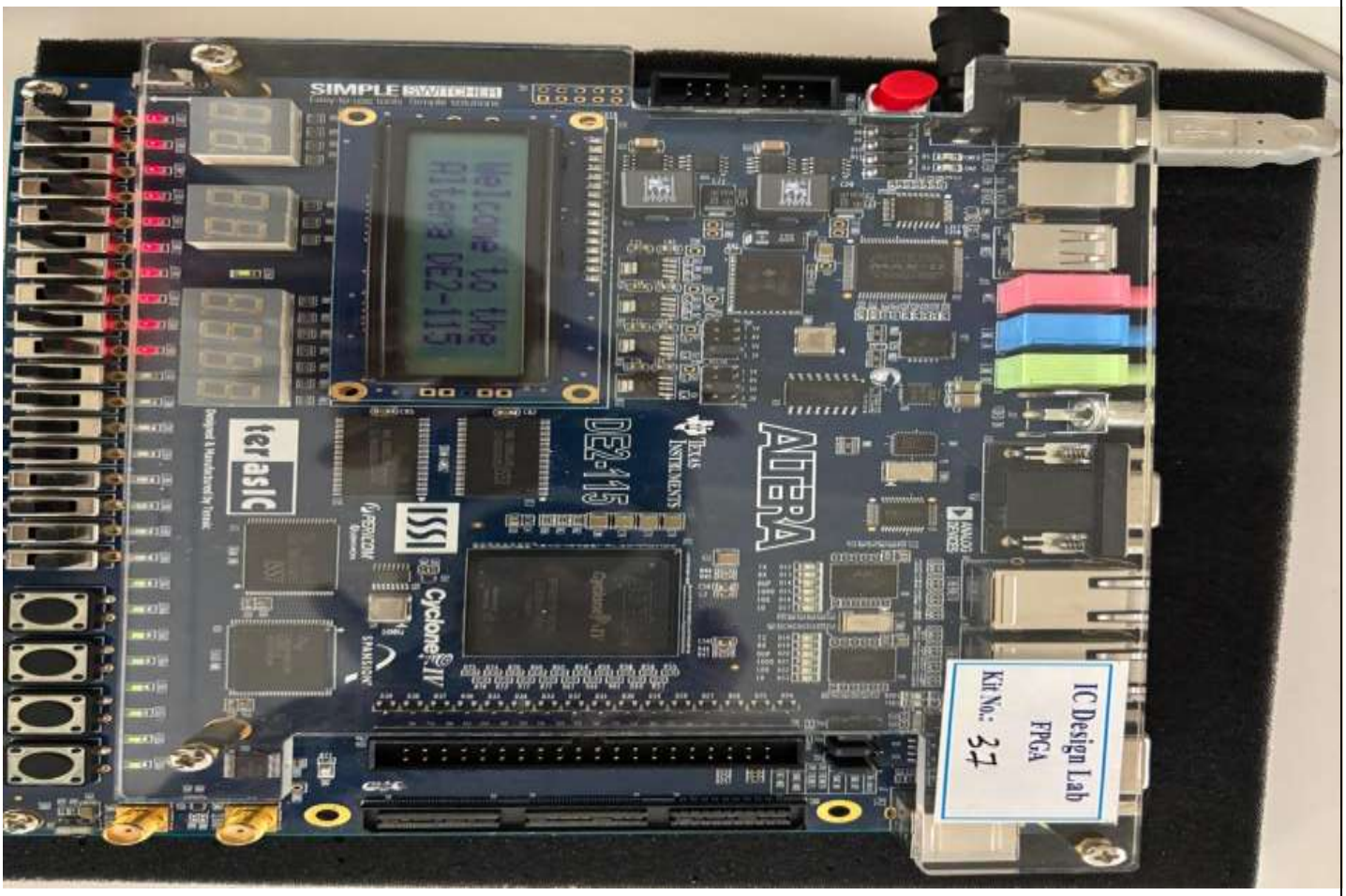
OUTPUT:

Input: Address: 101 , data: 011 ,wr=1

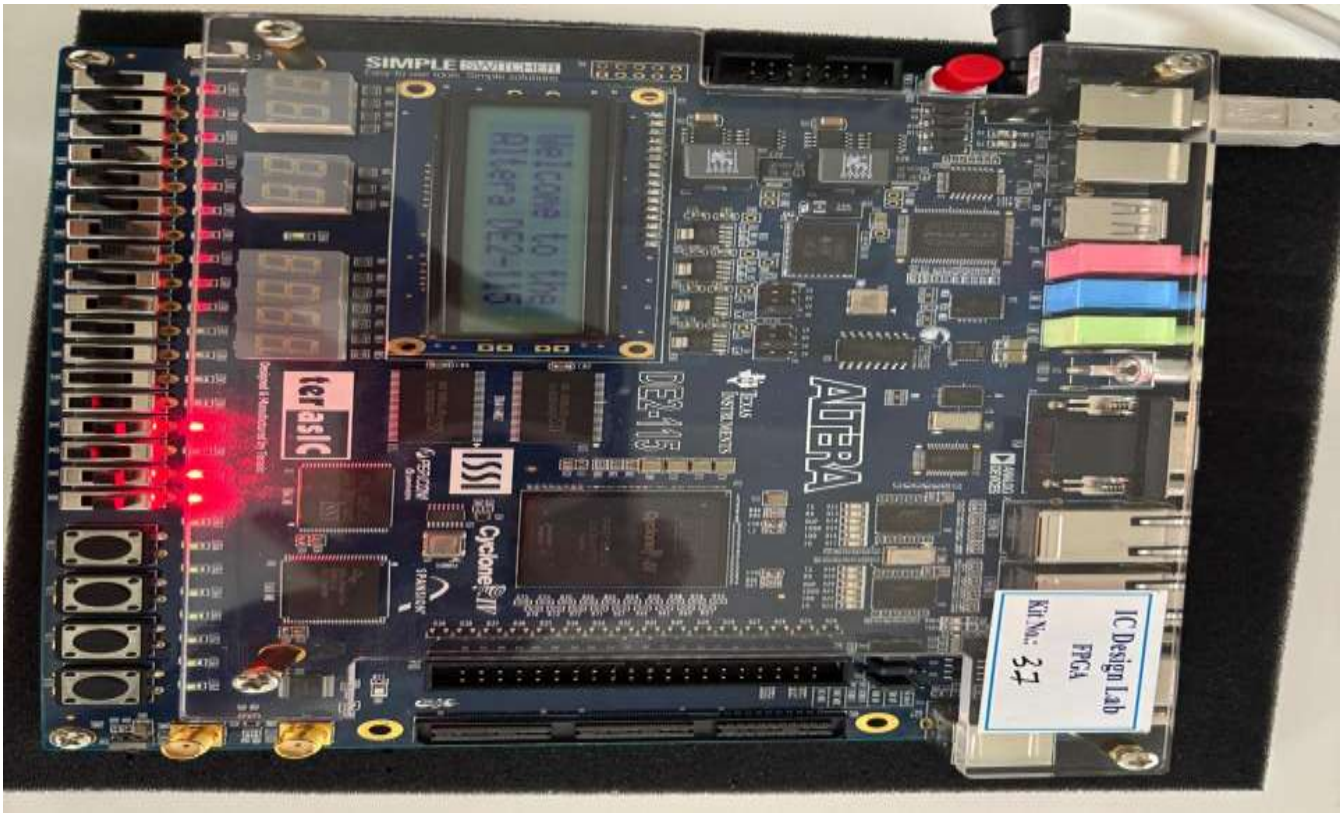
Output: wr=0



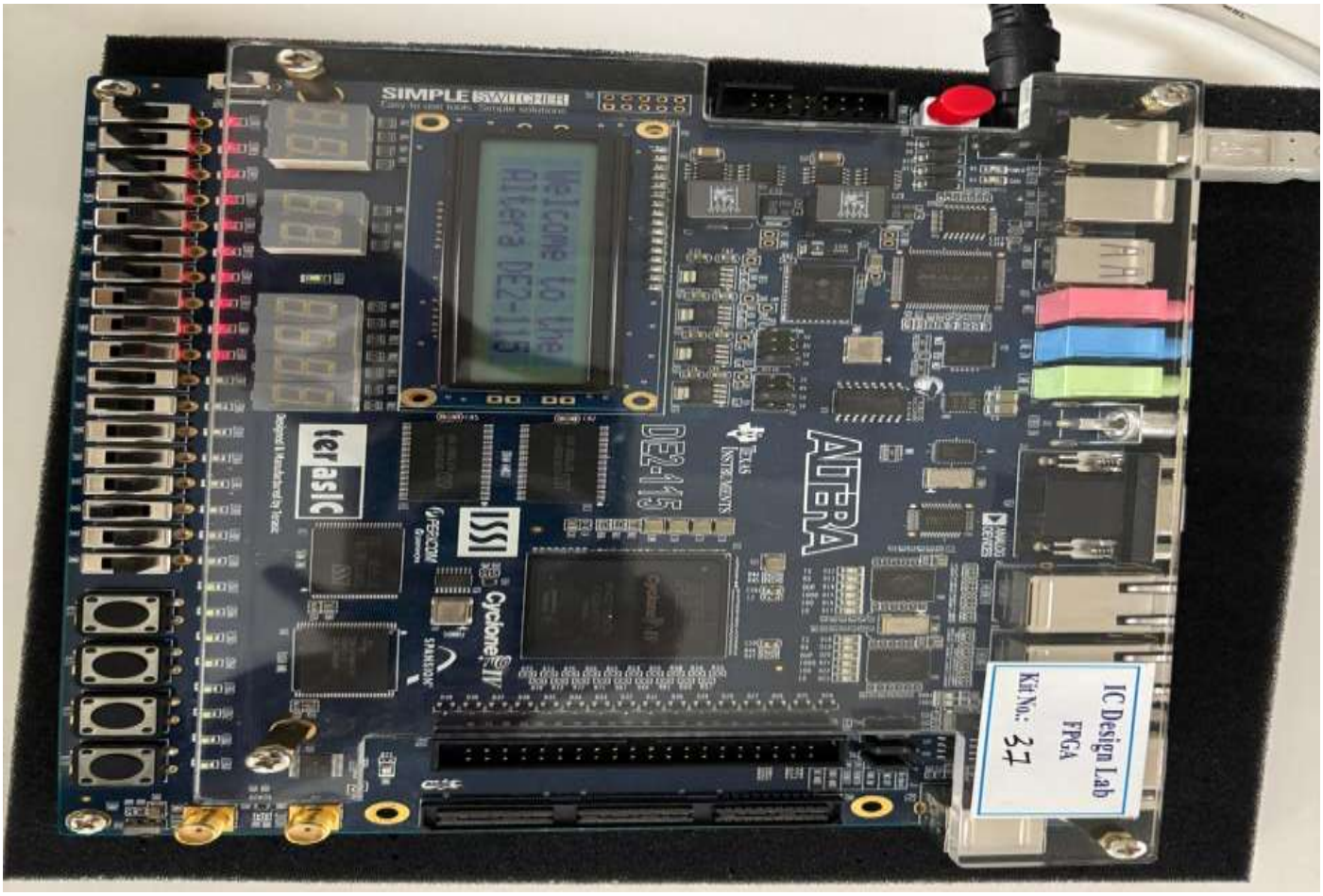
Input : Address: 1101 , data: 1011, wr=1



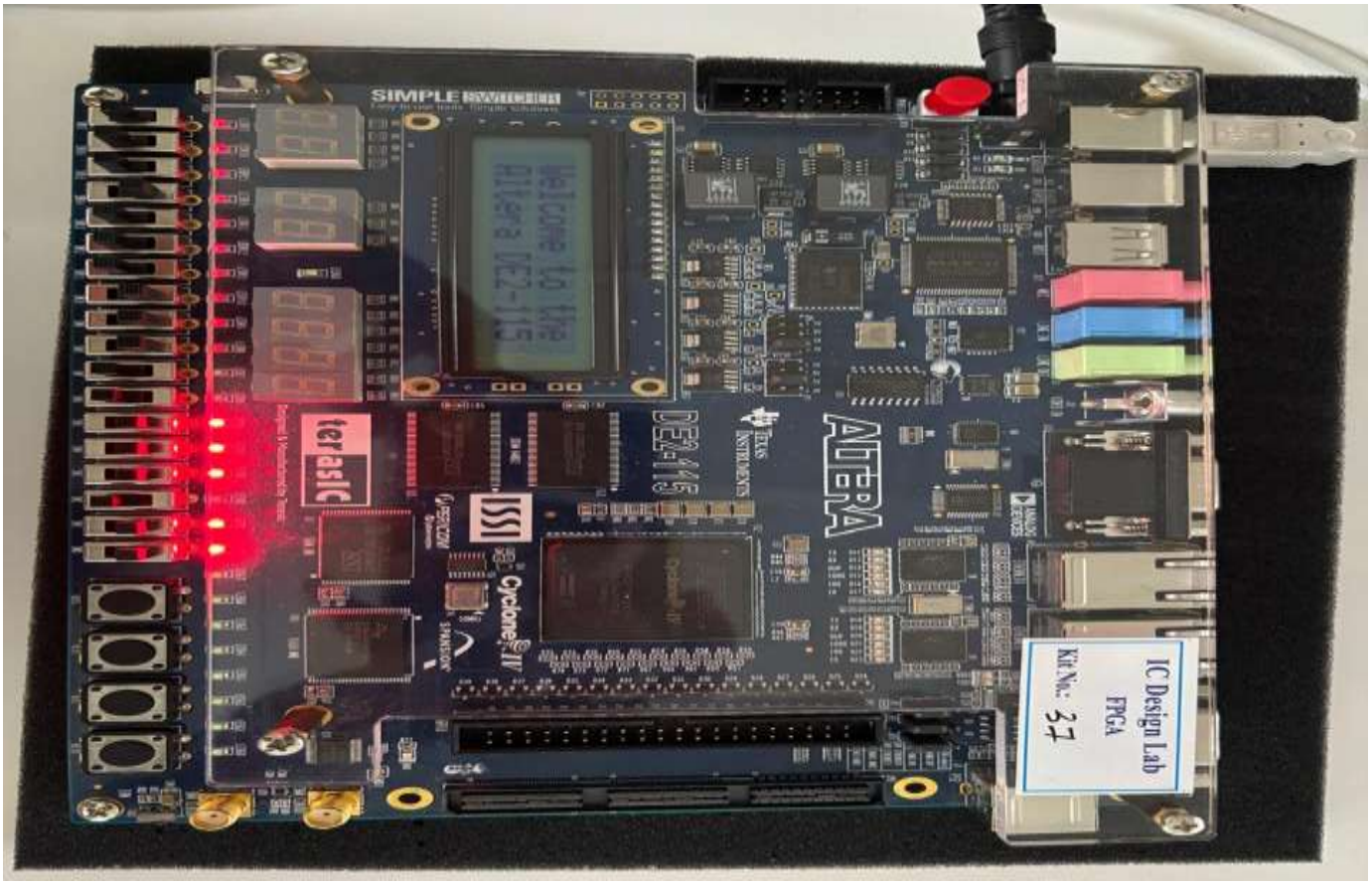
Output: wr=0



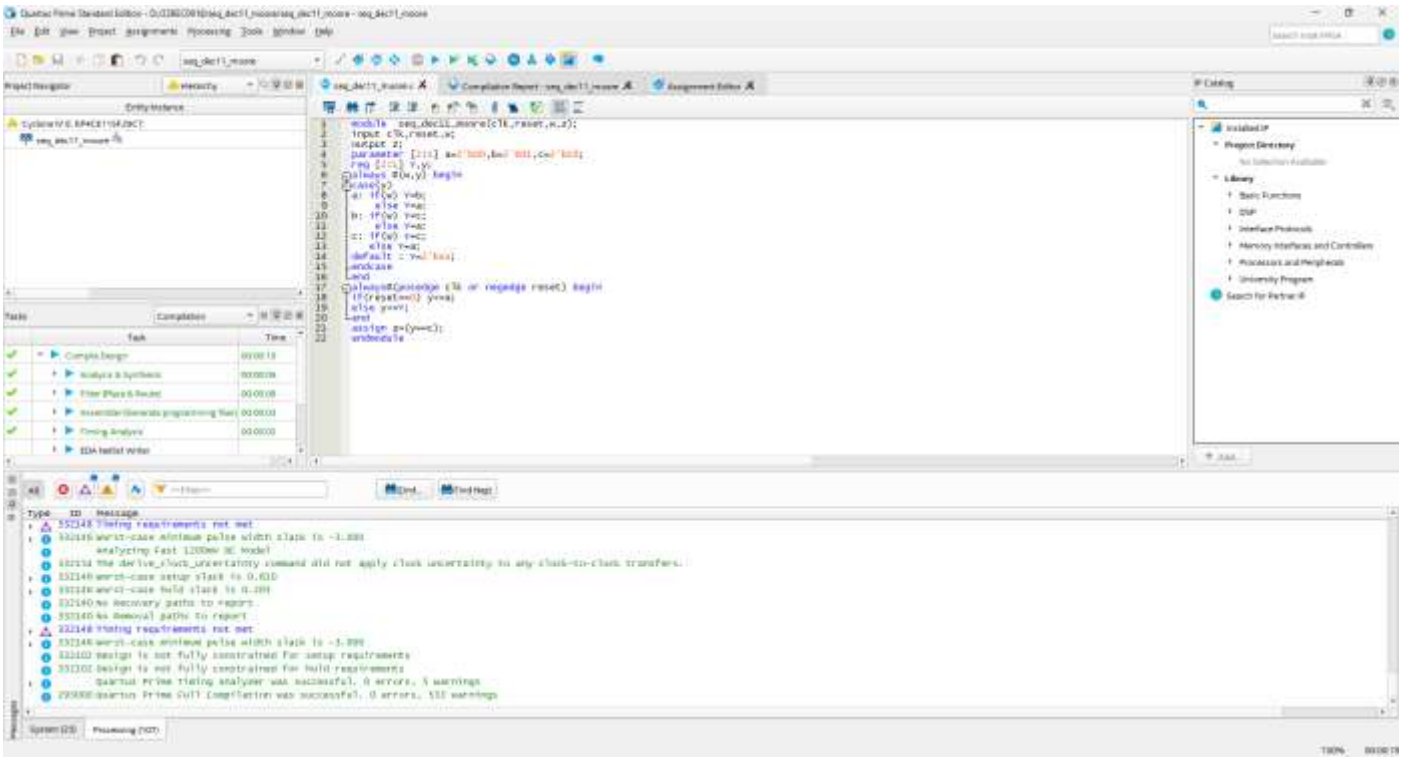
Input: Address:111, data: 111011, wr=1;



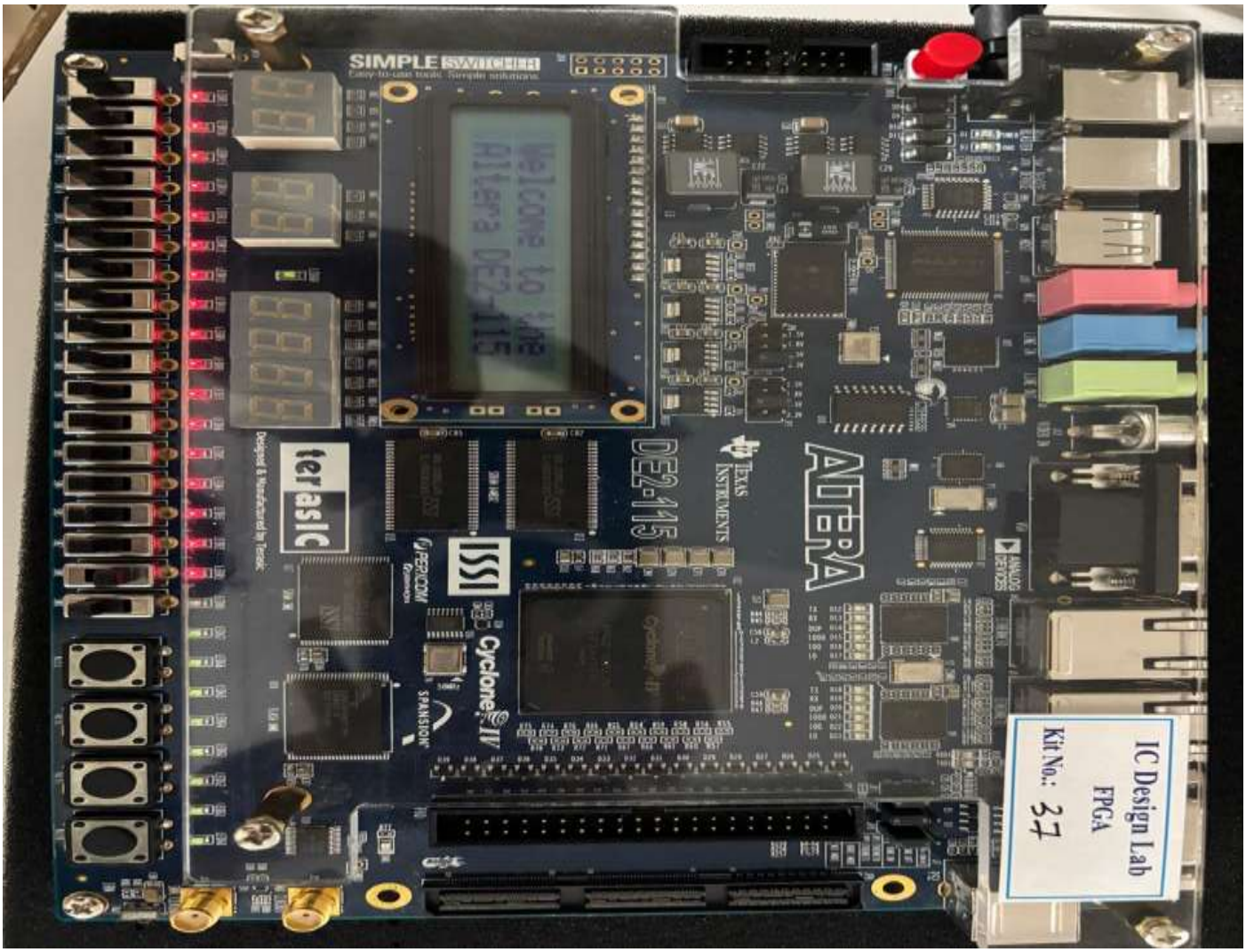
Output: wr=0;



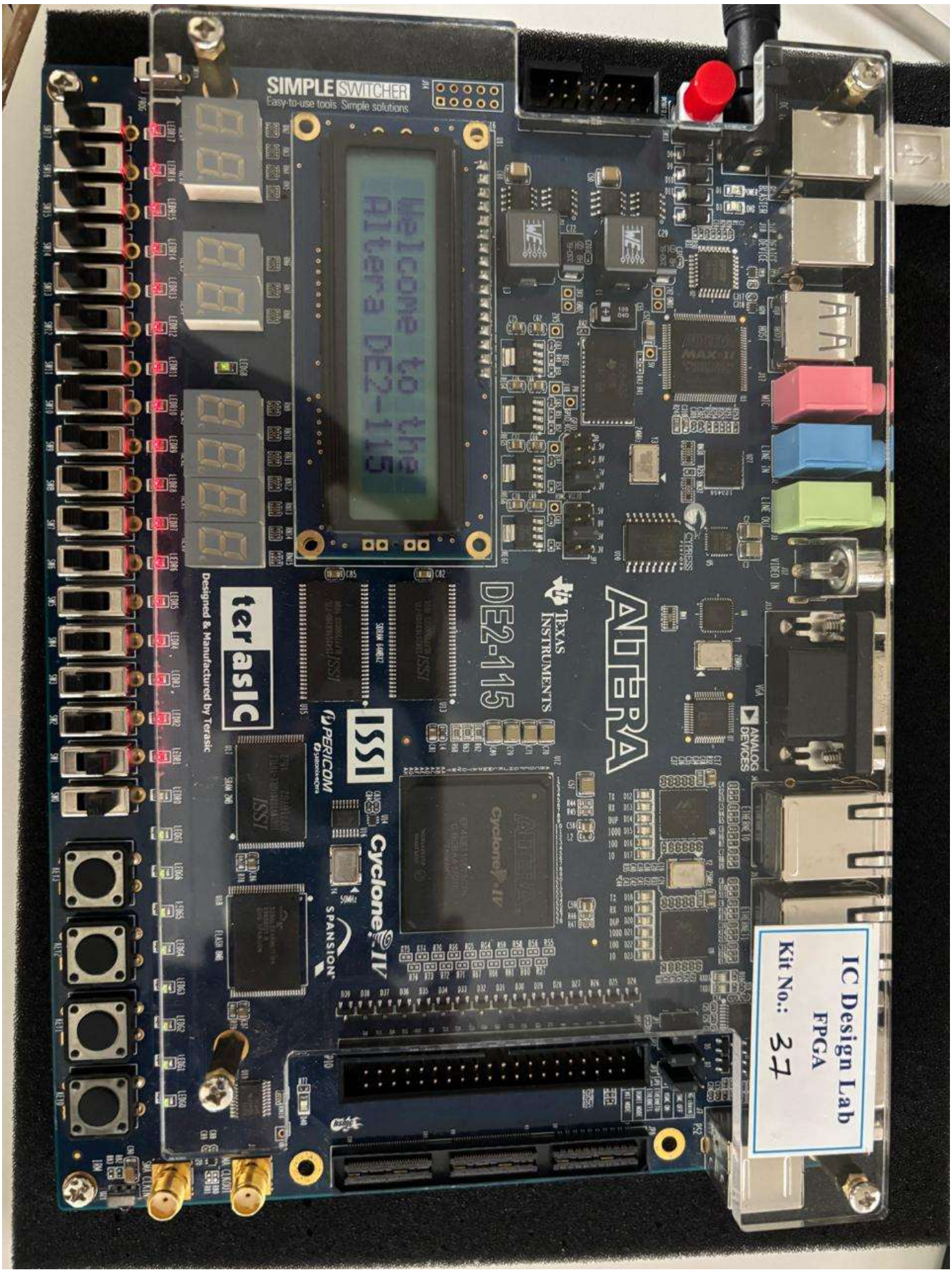
4) 11 sequence detector



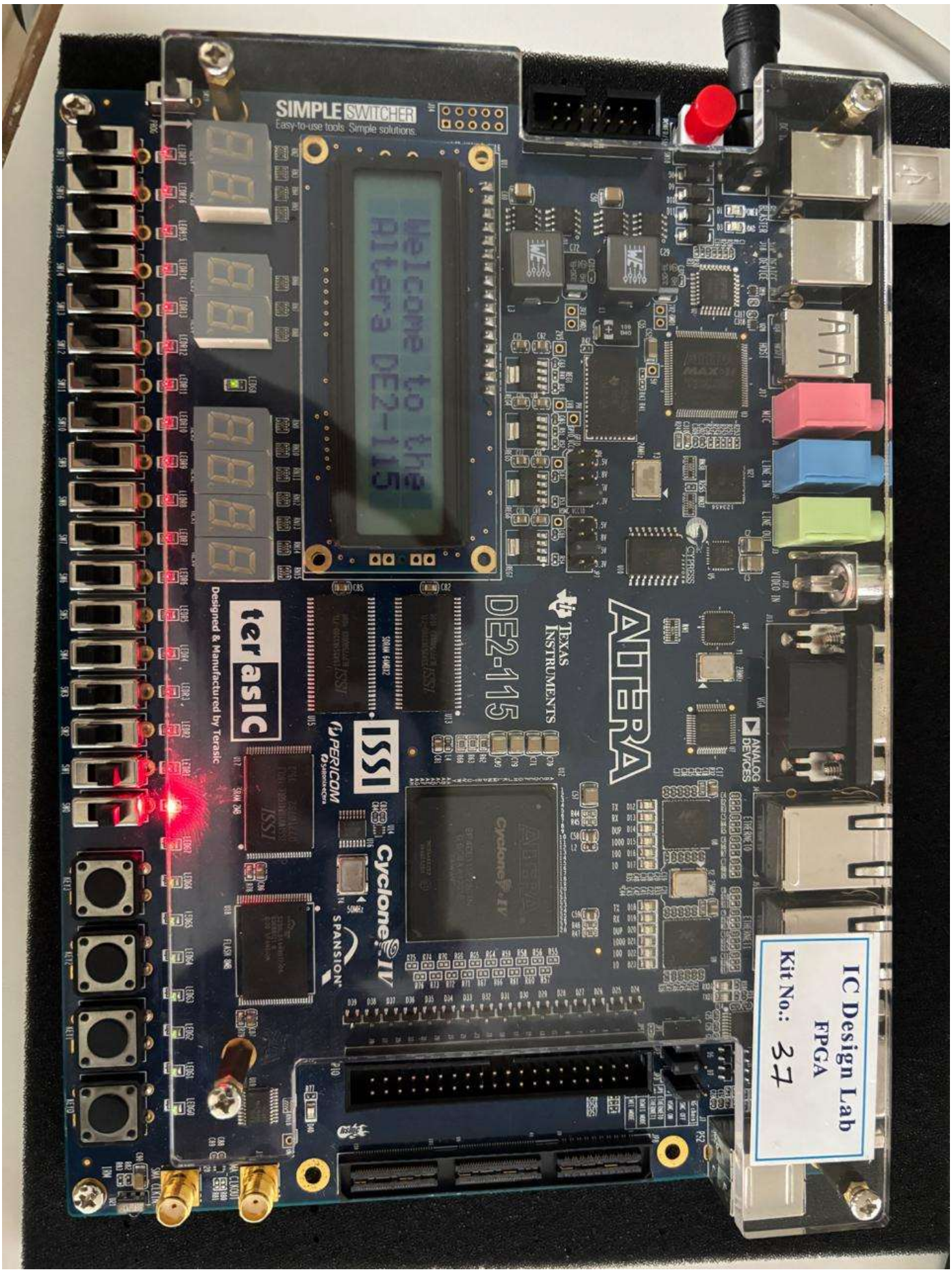
Output: seq_bit given=0, reset=1;



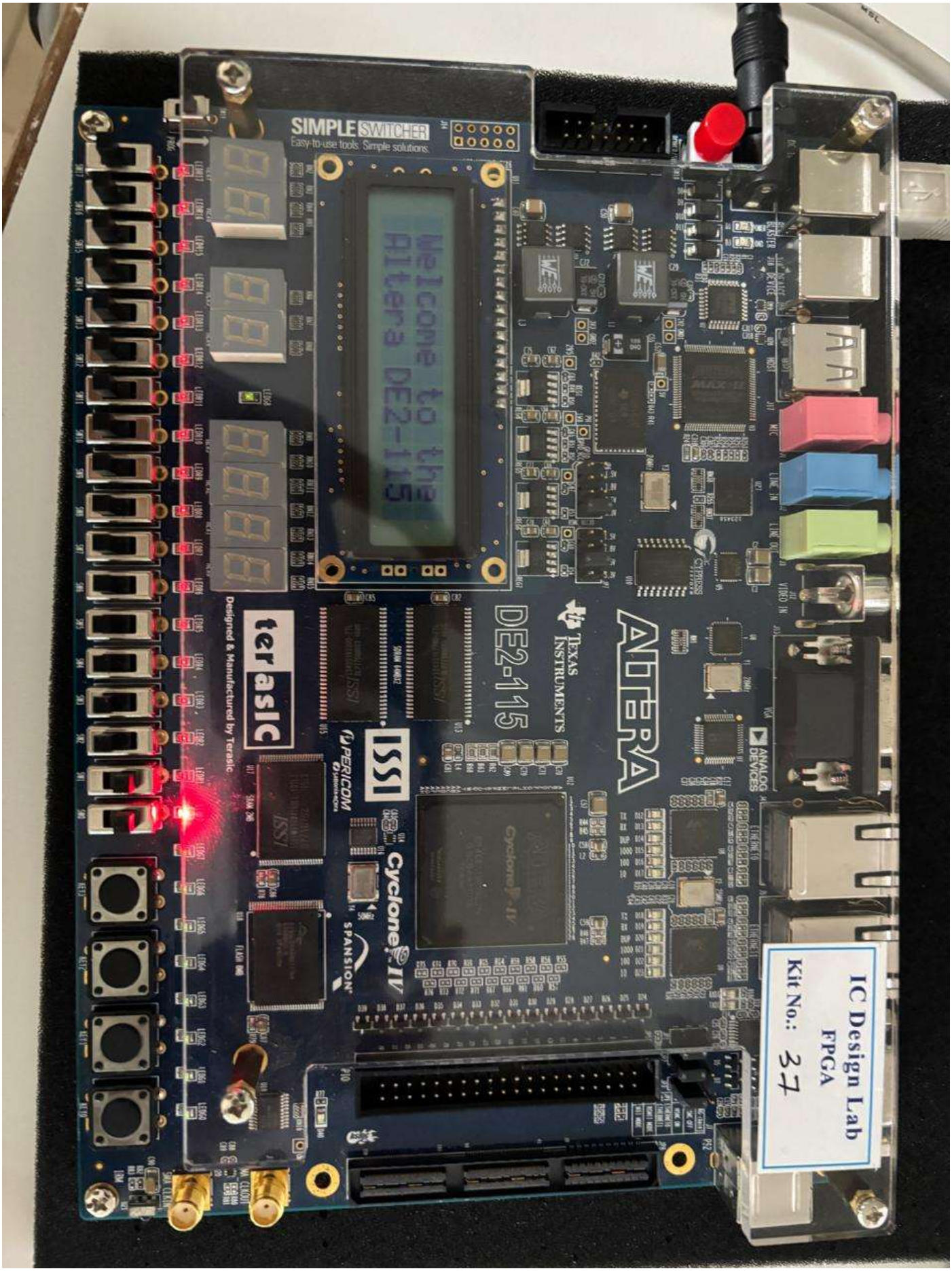
Seq bit give: 1, reset=1;



Seq bit given =1, reset=1;



Seq bit given =1 , reset=1;



Seq bit given =0 , reset=1;